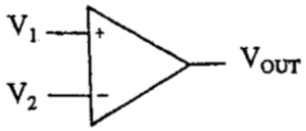
Introduction to operational amplifiers (OP-AMP)

OP-AMP is a very high gain differential amplifier:



Where:
+ Means non-inverting input
− Means inverting input

The output voltage of OP-AMP is described by:

$$V_{OUT} = A_V(V_1 - V_2)$$

The output goes positive when non-inverting input is more positive than the inverting input, and vice versa.
The open loop gain for an OP-AMP A_V is about 10^5 to 10^6.
V_{OUT} is limited by the supply voltage.

Example
If $V_1 = 1.305V$, $V_2 = 1.304V$, then:

$$\begin{aligned} V_{OUT} &= 10^5(1.305 - 1.304) \\ &= 100V \end{aligned}$$

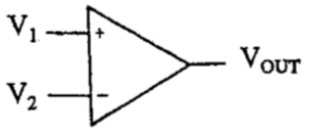
However, since V_{OUT} cannot exceed the supply voltage, the amplifier is saturated at the maximum positive supply voltage. This illustrates that OP-AMPs cannot be used on their own, feedback is therefore required.

Eternal feedback

Negative feedback is the process of coupling the output back in such way as to cancel some of the input.
In lowering the gain of the amplifier, other characteristics are improved.
The resultant amplifier gain is made less dependent on the characteristics of the open loop gain of the OP-AMP but depends on the feedback network.

Applications

2 rules for analysis:



$I_{OUT} > 0$

R1:
Since a very **small difference between V_1 and V_2** will cause the **V_{OUT}** of OP-AMP goes into **saturation**, the **difference can be ignored**. Therefore:

$$\boldsymbol{V_1 = V_2}$$

R2:
Since OP-AMPs draw very little input current, we **assume** there is **no the input current**:

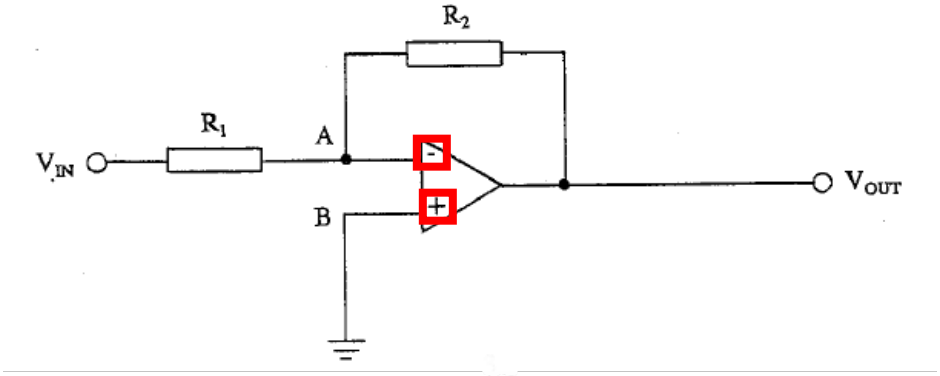
$$\boldsymbol{I_1 = I_2 = 0}$$

**Basic cautions in applying Rule 1, 2

- **Feedback must be negative**. (inverting and non-inverting inputs must not be mixed up)
- **R1 and R2 applies only when**:
  - **Neither the inputs nor output is saturated at one of the supply voltages**.

  The output cannot swing beyond the supply voltages.

- Inverting amplifier



Analysis:
By R1:

$$V_A = V_B = 0$$

Since B is connected to ground, A is known as virtual ground.

By R2:

$$I_A = I_B = 0$$

KCL:

$$I_1 = I_A + I_2$$
$$I_1 = I_2$$

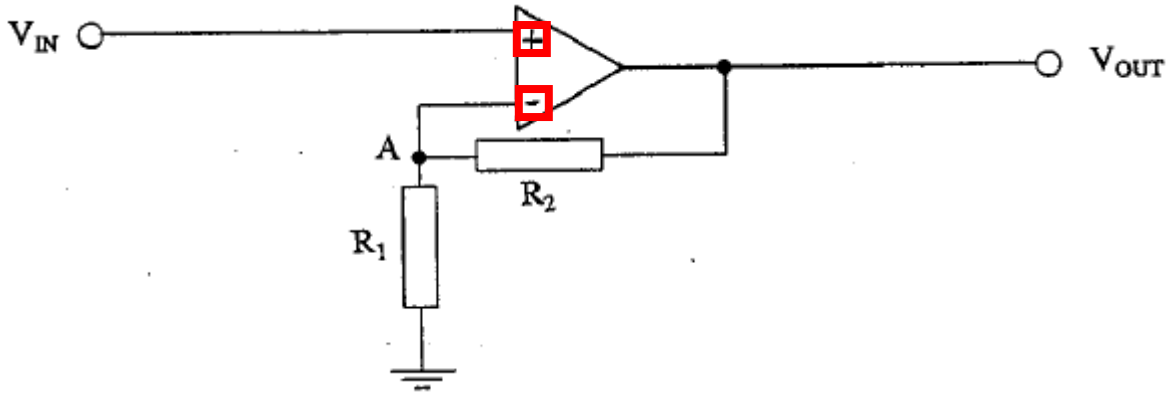
KVL:

$$V_{IN} - I_1 R_1 = 0$$
$$0 - I_2 R_2 = V_{OUT}$$

Gives:

$$\frac{V_{IN}}{R_1} = -\left(\frac{V_{OUT}}{R_2}\right)$$
$$\boldsymbol{\frac{V_{OUT}}{V_{IN}} = -\left(\frac{R_2}{R_1}\right)}$$

- Non-Inverting Amplifier



Analysis:
By R1:

$$V_{IN} = V_A$$

Point A is a voltage divider:

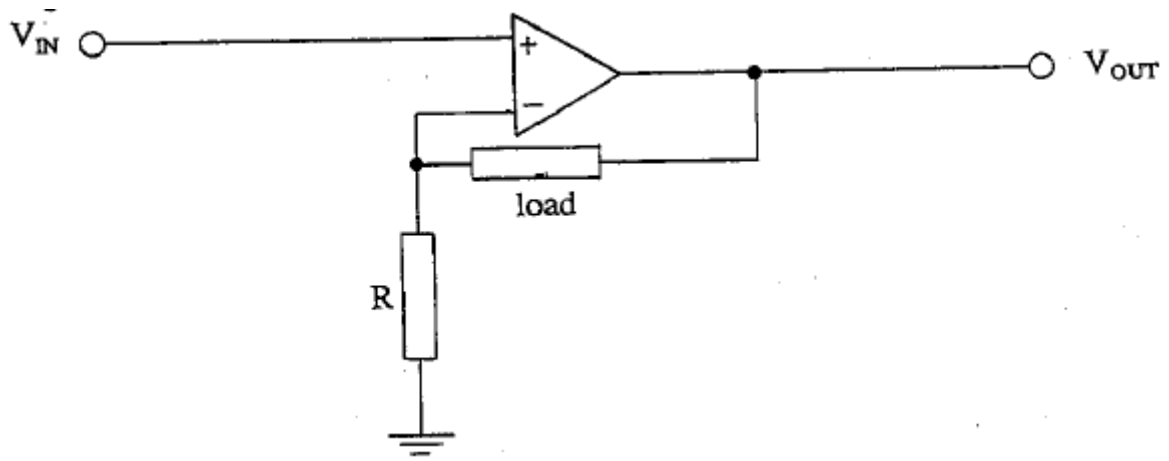
$$\frac{V_A}{R_1} = \frac{V_{OUT}}{R_2 + R_1}$$

$$\frac{V_{IN}}{R_1} = \frac{V_{OUT}}{R_2 + R_1}$$

$$\boldsymbol{\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_2}{R_1}}$$

- Current source

The non-inverting amplifier can be used to simulate a current source:

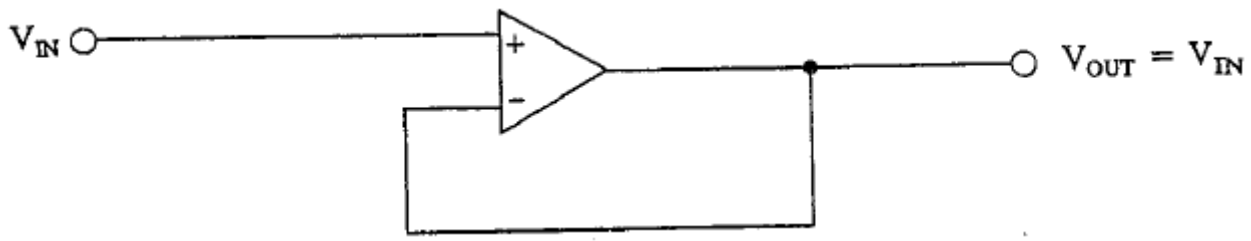


At the junction of the load and R, the voltage is V_{IN} (by R1) and a current:

$$I = \frac{V_{IN}}{R}$$

always flows through the load, irrespective of the magnitude of the load.

- Follower

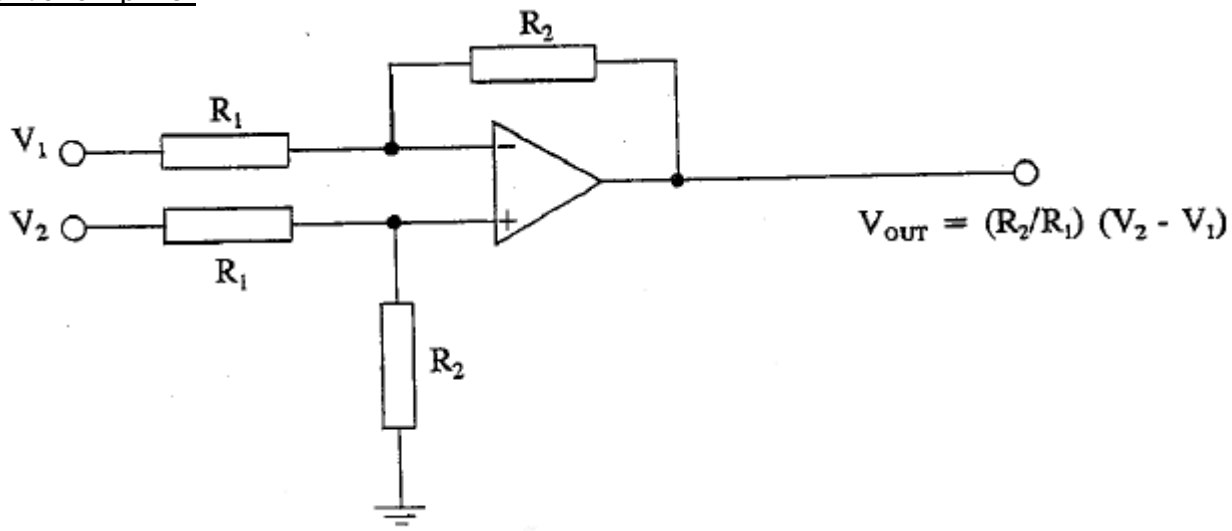


Analysis:
By R1:

$$\boldsymbol{V_{IN} = V_{OUT}}$$

Therefore, the Gain here is 1.
Follower also known as buffer because of its isolating properties. (High input impedance, low output impedance)

- Differential amplifier



Analysis:
By R1:

$$V^- = V^+$$

At the voltage dividing junction between R_1 and R_2 at the non-inverting terminal:

$$\frac{V^+}{R_2} = \frac{V_2}{R_1 + R_2}$$
$$V^+ = V^- = \frac{V_2 R_2}{R_1 + R_2}$$

Apply KCL (with R2) and KVL from V1 to V_{OUT}:

$$I_1 = I_2 + I^-$$
$$I_1 = I_2$$

$$V_1 - I_1 R_1 = V^-$$
$$V^- - I_2 R_2 = V_{OUT}$$

$$\frac{V_1 - V^-}{R_1} = I_1$$
$$\frac{V^- - V_{OUT}}{R_2} = I_2$$

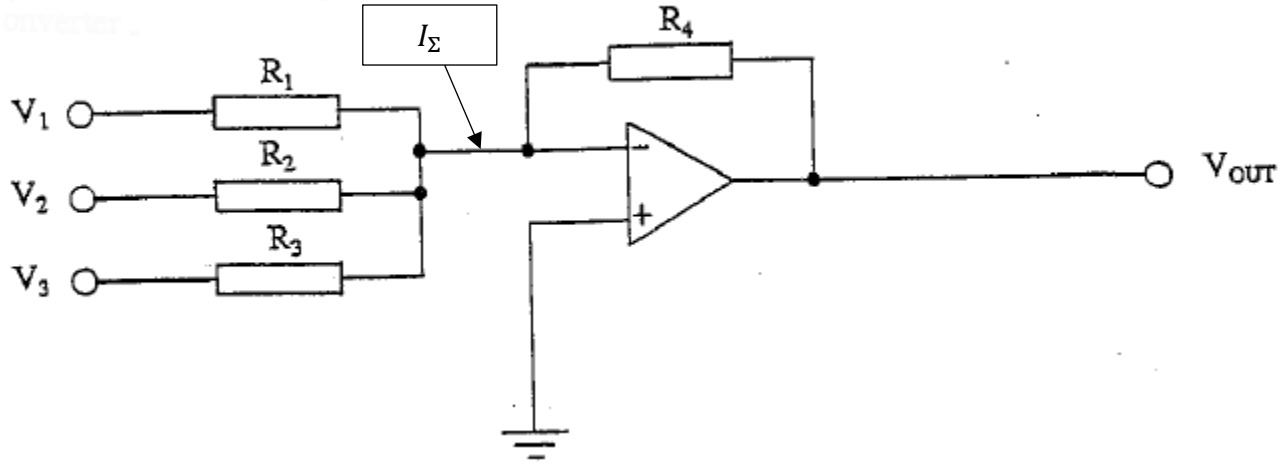
$I_1 = I_2$

$$\frac{V_1 - V^-}{R_1} = \frac{V^- - V_{OUT}}{R_2}$$
$$V_{OUT} + \frac{R_2}{R_1}(V_1 - V^-) = V^-$$
$$V_{OUT} = V^- - \frac{R_2}{R_1}(V_1 - V^-)$$

$V^- = \frac{V_2 R_2}{R_1 + R_2}$

$$V_{OUT} = V^-\left(1 + \frac{R_2}{R_1}\right) - \frac{R_2}{R_1}V_1$$
$$V_{OUT} = \frac{V_2 R_2}{R_1 + R_2}\left(\frac{R_1 + R_2}{R_1}\right) - \frac{R_2}{R_1}V_1$$
$$\boldsymbol{V_{OUT} = \frac{R_2}{R_1}(V_2 - V_1)}$$

- Summing amplifier



Analysis:
BY R1:

$$V^- = V^+ = 0$$

At the input side:
For each branch:

$$V_k - I_k R_k = 0$$
$$I_k = \frac{V_k}{R_k}$$

By KCL:

$$I_\Sigma = \sum_{IN} \frac{V_k}{R_k}$$

Then at the junction between the inputs and R_4, with R2:

$$I_\Sigma = I_4 + I^-$$
$$I_\Sigma = I_4$$

$$V^- - I_4 R_4 = V_{OUT}$$
$$\boldsymbol{V_{OUT} = -\left(R_4 \sum_{IN} \frac{V_k}{R_k}\right)}$$

Deviations from ideal characteristics

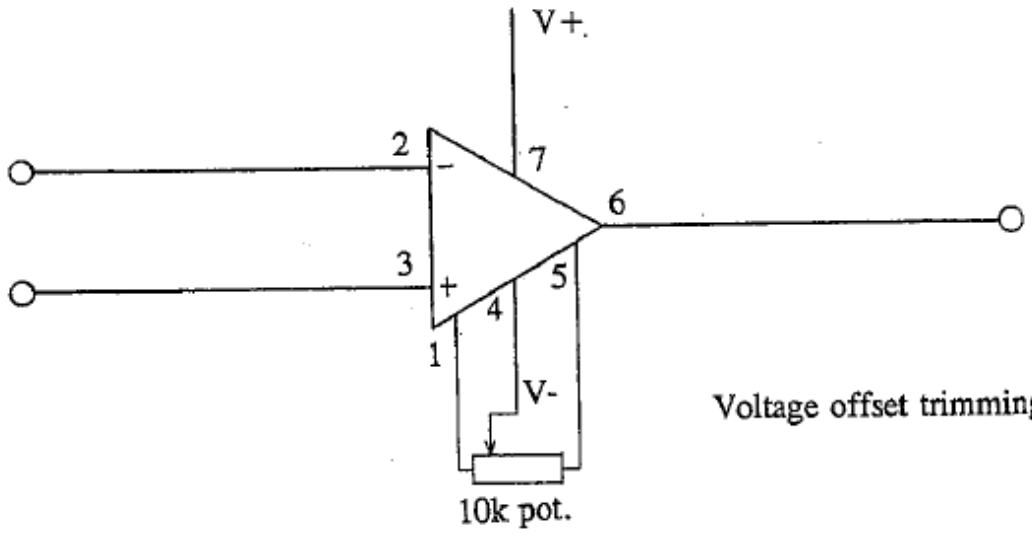
- **Ideal characteristics**
  An ideal OP-AMP would have the following characteristics:
  - V_{OUT} = 0 when both inputs are at the same voltage (offset voltage = 0)
  - I_{IN} = 0 (input impedance → ∞)
  - Output can change instantaneously (slew rate → ∞)
  - Open loop gain → ∞

- **Deviations and their effects on circuit design**
  - Input offset voltage (V_{OS})
    Due to manufacturing variations, OP-AMPs do not have perfectly balanced input stages, if both inputs are connected together, the output will saturate at either V^+ or V^- but not 0.

    The difference in input voltages required to bring the output to 0 is called the input offset voltage (V_{OS}).

    Example:
    A 741 OP-AMP IC circuit has a typical VOS of 2 ~ 6mV. Therefore, for an inverting amplifier built with 741 having a close loop gain of 100 will give an output of $6mV \times 100 = \pm 0.6V$ with a zero input.

    Usually OP-AMPs have provisions for trimming the input offset voltage to 0.
    For 741, a 10k potentiometer is connected across terminals 1 and 5 with the wiper connected to V^- as shown:

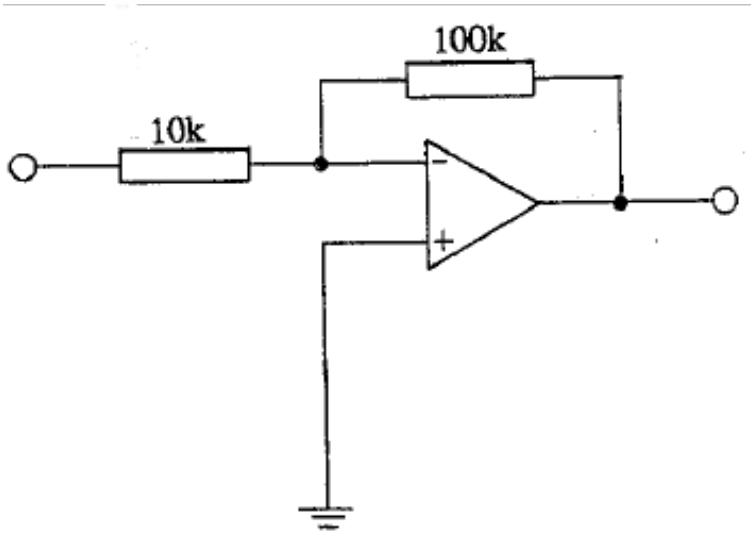


Voltage offset trimming circuit for 741

- Input bias current (I_B)
  The input terminals always draw / supply a small current called the input bias current (I_B), which is defined as ½ the sum of the input currents with the inputs tied together. In fact, the input current are the base currents of the input transistors. For a 741 IC circuit, the input bias current is typically 80 ~ 500nA.

  Even after the input offset voltage has been trimmed to 0, the output voltage still ≠ 0.

  The effect if input bias current can be visualized easily by analyzing an inverting amplifier:



  Where R_1 = 10k, R_2 = 100k.

  For the above circuit, the junction between 10k and 100k have an impedance of:

$$Z = R_1||R_2$$

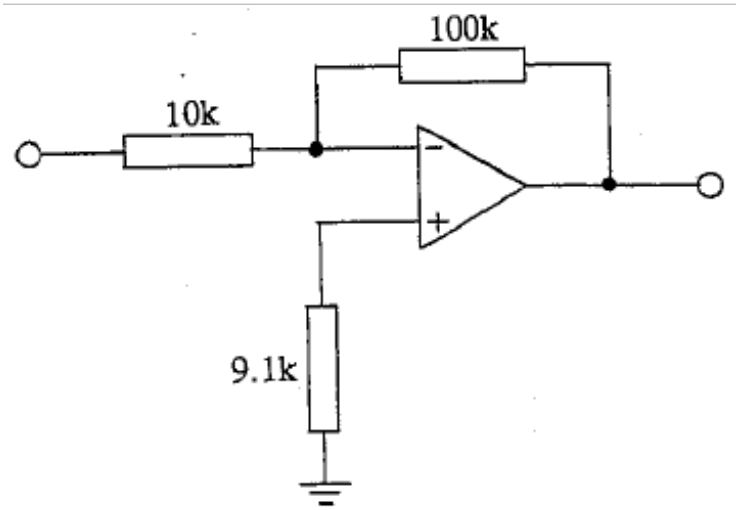
  Therefore, the input bias current produce a voltage V_{IN}:

$$V_{IN} = I_B(R_1||R_2)$$

  Therefore, the output voltage V_{OUT} for ground inputs will be:

$$\begin{aligned} V_{OUT} &= -\frac{R_2}{R_1}V_{IN} \\ V_{OUT} &= -\frac{R_2}{R_1}I_B(R_1||R_2) \\ &= -\frac{100}{10} \times 500 \times 10^{-9} \times 9100 \\ &= -0.045V \end{aligned}$$

This input bias current (IB) cannot be trimmed off because the base of the input transistor always requires a certain amount of current. To minimize the IB effect, we can ensure both inputs see the same impedance:



For this case, a 9.1kΩ resistor is connected to the non-inverting terminal so that both terminals see 9.1kΩ impedance. This cure works only if both inputs draw the same amount of bias current.

If the resistance of the feedback network is kept small, the input bias current will not produce a large voltage offset. Typically, the resistance seen from the OP-AMP inputs are 1 ~ 100kΩ.

Another way to minimize the IB effect is to use OP-AMPs with lower bias currents.

- Input offset current (I_{OS})

  The input offset current I_{OS} is the difference in input bias currents IB between the two inputs. The offset current is a result of manufacturing variations. Typically the offset current is about:

$$I_{OS} = \frac{1}{10} I_B$$

  Even when the impedance are balanced by the above method, the output will still suffer from some offset. However, this small current is usually tolerable.

  If the application requires a smaller offset, we can:
  - Lower the feedback resistance
  - Use an OP-AMP with lower input current

- Slew rate (S)

  The rate of change of output is limited by the internal capacitances and drive currents. This limiting speed is specified as the slew rate (S). A 741 IC circuit have an S = 0.5V/μs. A high speed OP-AMP might have an S = 100V/μs.

  A sine wave of amplitude A volts and frequency fHz requires a minimum slew rate of:

  $$S = 2\pi Af$$

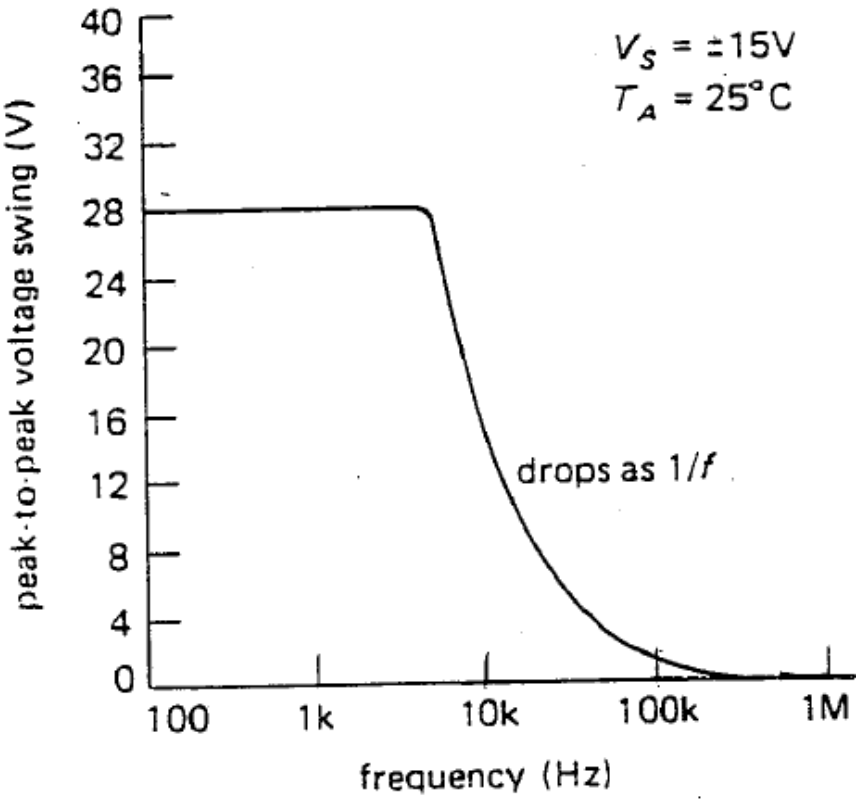
  Alternatively, for a given slew rate S, the output amplitude A is limited to:

  $$A = \frac{S}{2\pi f}$$

  The following curve shows the output swing versus frequency for a 741 with $\pm$15V supply. The maximum swing is 28V (-14V to +14V). the output swing starts to drop at:

  $$f = \frac{S}{2\pi A} = \frac{5 \times 10^5}{28\pi} = 5.7kHz$$

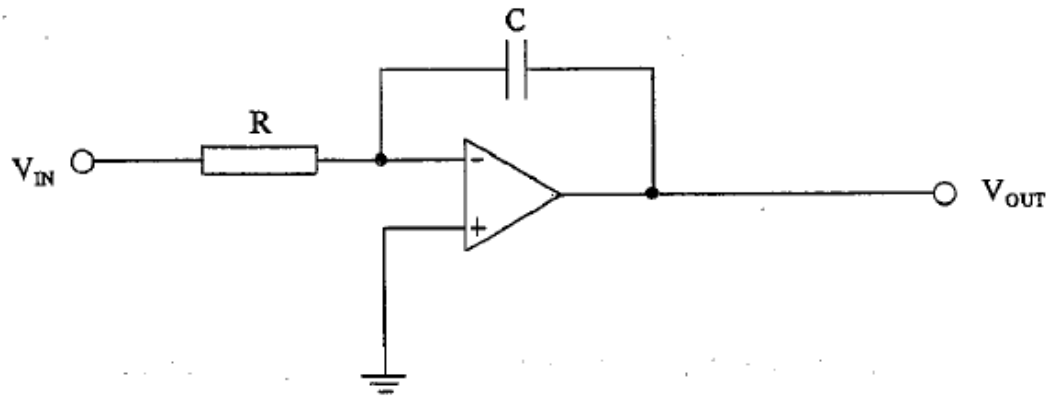
  Then the output swing drops as 1/f:



Further applications

There are application circuits where non-ideal characteristics of OP-AMP have significant influence on the circuit design.

- Integrator



Analysis:
By R1, at the junction between R and C:

$$V^- = V^+ = 0$$

And:

$$I_{IN} = I^- + I_C$$
$$I_{IN} = I_C$$

From V_{IN} to junction:
By KVL:

$$V_{IN} - I_{IN}R = V^- = 0$$

$$\mathrm{I_c} = \mathrm{C}\frac{\mathrm{dV_c}}{\mathrm{dt}}$$
$$0 - V_c = V_{OUT}$$
$$\mathrm{I_c} = -\mathrm{C}\frac{\mathrm{dV_{OUT}}}{\mathrm{dt}}$$

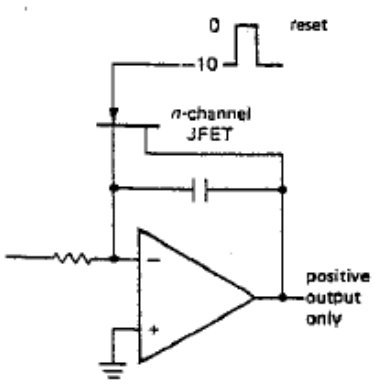
$$\frac{V_{IN}}{R} = I_{IN} = I_C = -C\left(\frac{dV_{OUT}}{dt}\right)$$
$$\boldsymbol{V_{IN} = -RC\frac{dV_{OUT}}{dt}}$$

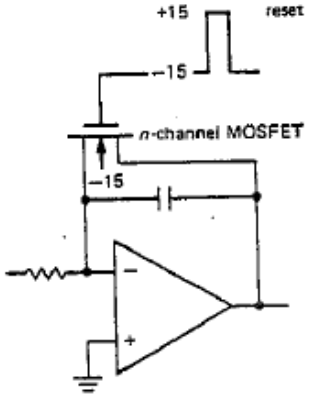
The problem of this design is that the output will wander off even when the input is grounded.
The reason is due to the OP-AMP offsets and bias current. There are several ways to minimise this problem:

- Use FET OP-AMPs for low input current and offset
- Trim the OP-AMP input offset voltage carefully
- Use large R and C values

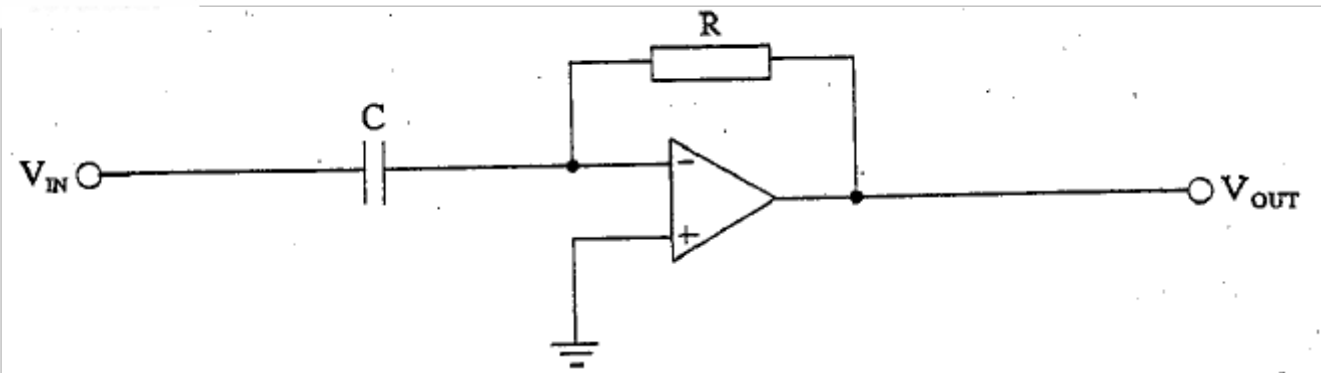
Example:
An OP-AMP with bias current of about 30pA trimmed to a voltage offset of 0.2mV and used with R = 10MΩ and C = 10μF will produce an output drift of < 0.003V in 1000 seconds.

It is possible to close a switch placed across the capacitor periodically to zero the integrator before each integration. The output will then drift only over short time scales.





- Differentiator



Analysis:
By R1, at the junction between C and R:

$$V^- = V^+ = 0$$

And:

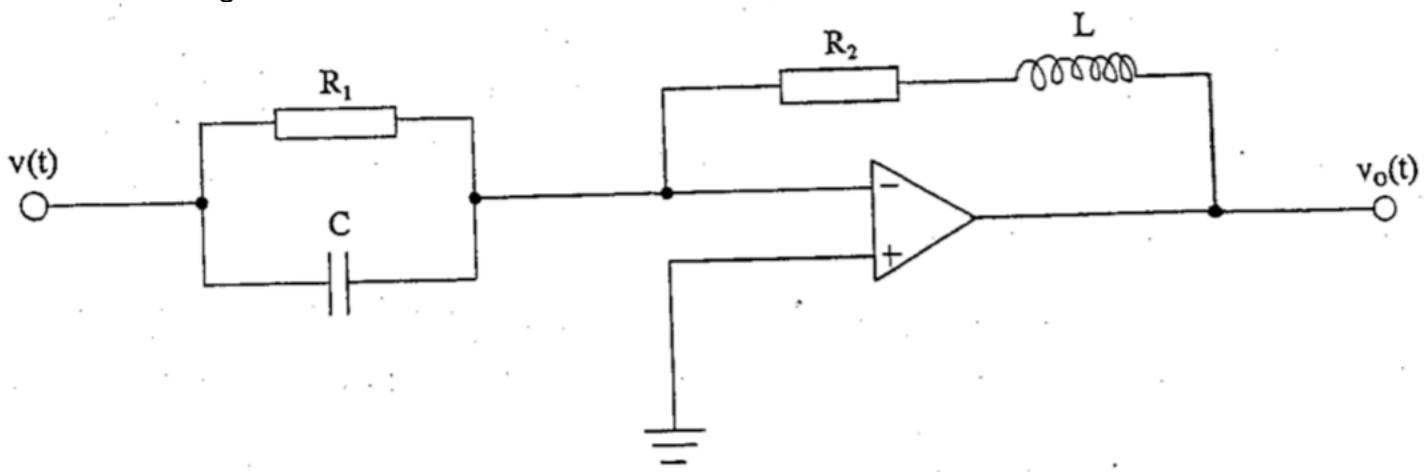
$$I_{IN} = I^- + I_R$$
$$I_{IN} = I_R$$
$$I_R = C\frac{dV_{IN}}{dt}$$

From the junction to V_{OUT}:

$$V^- - I_R R = V_{OUT}$$
$$V_{OUT} = -\left(RC\frac{dV_{IN}}{dt}\right)$$

Tutorial Questions

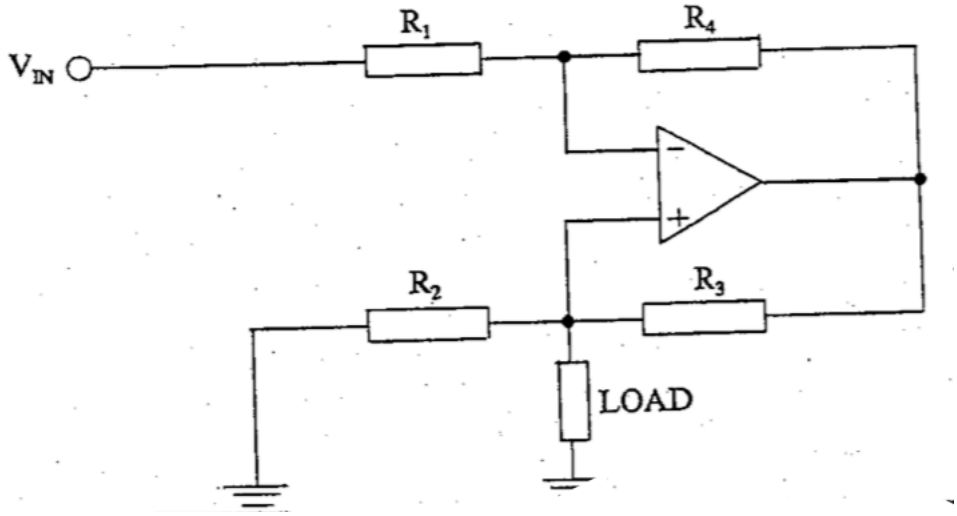
1. For the following circuit:



show that $V_o(t)$ in terms of $V(t)$ can be express by:

$$V_o(t) = -\frac{R_2}{R_1}V(t) - \left(R_2C + \frac{L}{R_1}\right)\frac{dv(t)}{dt} - LC\frac{d^2V(t)}{dt^2}$$

2. The circuit below shows a current source:



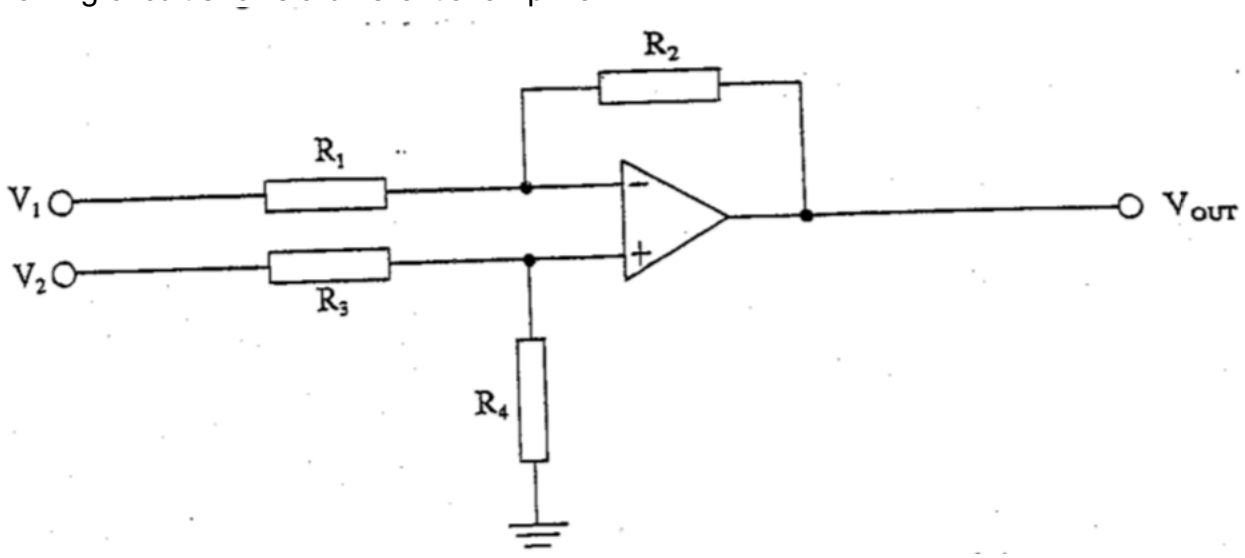
Given that:

$$\frac{R_3}{R_2} = \frac{R_4}{R_1}$$

Find the current through the load.

Note:
This current source has several limitations:
- The resistors must match exactly.
- If I_{LOAD} is large, the resistors must be small and the range of output voltages is limited $[-\frac{V_{IN}}{R_2}]$

3. The following circuit shows a differential amplifier:



a) If VOUT is represented as:

$$V_{OUT} = A_1V_1 + A_2V_2$$

Find A_1 and A_2.

$$[A_1 = -\left(\frac{R_2}{R_1}\right), A_2 = \frac{R_4(R_1+R_2)}{R_1(R_3+R_4)}]$$

b) If:

$$\frac{R_2}{R_1} = \frac{R_4}{R_3}$$

Find V_{OUT}.

$$[V_{OUT} = \frac{R_2}{R_1}(V_2 - V_1)]$$

c) Denoting:

$$\begin{cases} V_D = V_2 - V_1 \\ V_C = \frac{1}{2}(V_1 + V_2) \end{cases}$$

V_{OUT} can be expressed in the form:

$$V_{OUT} = A_DV_D + A_CV_C$$

Find A_D and A_C in terms of A_1 and A_2.

$$[A_D = \frac{1}{2}(A_2 - A_1), A_C = A_1 + A_2]$$

4. Show that the gain of the following inverting amplifier is 102: