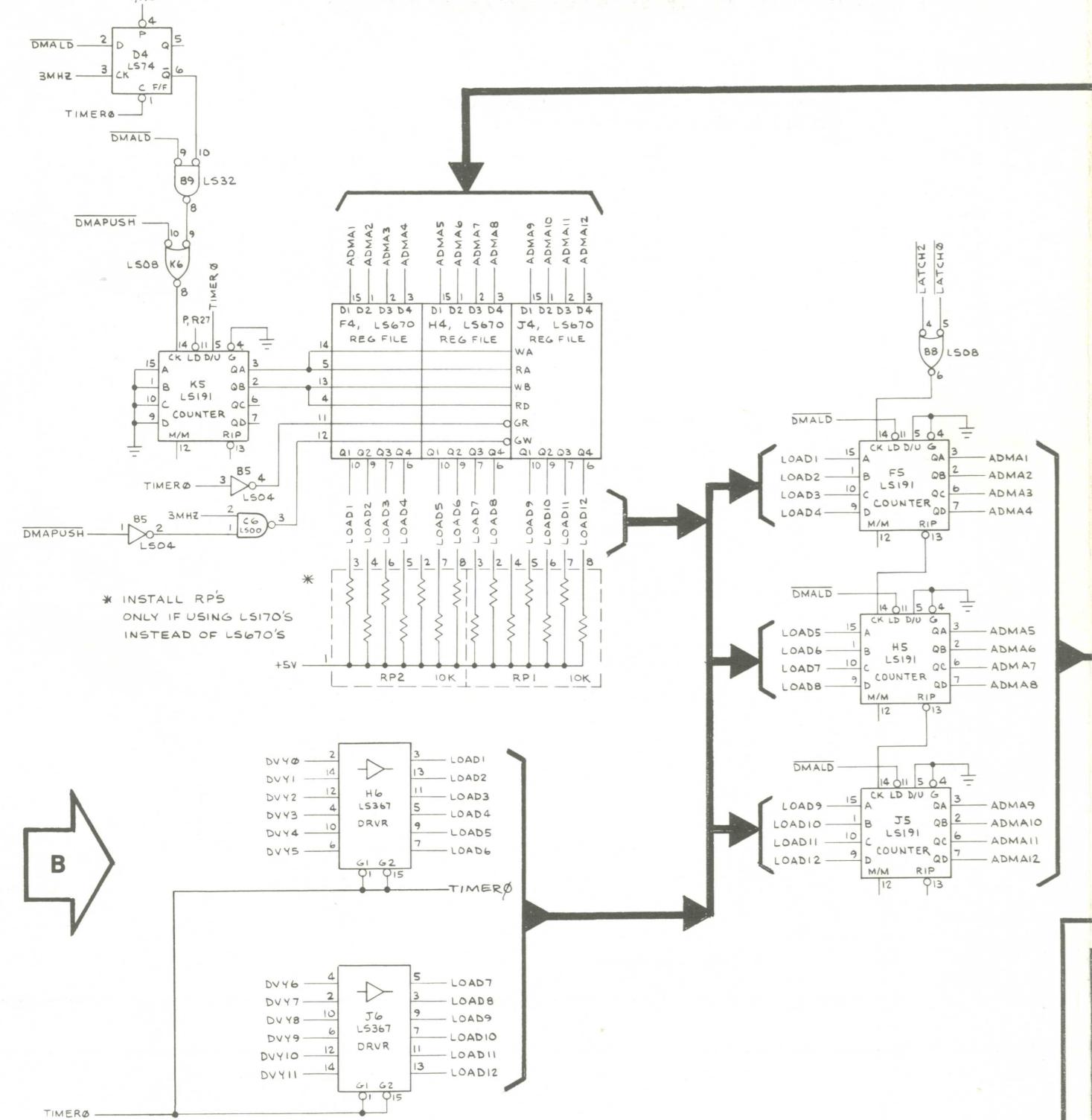


VECTOR GENERATOR PROGRAM COUNTER



Counters F5, H5 and J5 contain the address of the next data byte (instruction) to be fetched from the Vector Generator memory. Because these counters point to the next instruction in memory to be refetched and performed, they are called the program counter. This program counter is incremented one count (to the next sequential address) each time the information at its current address is loaded into data latch 0 or data latch 2.

The program counter may also be preset to "jump" to a previous address. This new address can be loaded into the program counter from the vector generator memory via

data latches F7 and H7 and buffers H6 and J6.

The program counter may also be preset to "return" to a previous address which it had stored in its "stack". The stack consists of register files F4, H4, J4, and down/up counter K5. The stack is a 4-word 12-bit memory, used to save the contents of the program counter for future reference. It is loaded when DMA PUSH is low. Immediately after information is written into the stack, counter K5 increments one count. Immediately before loading the program counter from the stack, counter K5 decrements one count.

The address selector consists of multiplexers F3, H3, J3 and K3. When VMEM is low, the MPU of the microcomputer gains access to the address inputs of the vector generator memory. In this state, BUFFEN is from $\bar{Q}2$ and VW (vector generator write) is low when $\bar{Q}2$ and RWB are both low. When VMEM is high, the address input to the vector generator memory is from the vector generator program counter and state machine. In this state, BUFFEN and VW are both held high by the pullup resistors connected to the $\bar{Q}2$ and $\bar{Q}3$ inputs of multiplexer K3.

Address decoder L3 decodes address bits A11 and A12, and selects the RAM or one of three ROMs of the vector generator memory.

This address-selecting arrangement allows the game MPU to access the vector generator memory, i.e., write data into the vector generator RAM to instruct the vector generator what it should do next. The address selector can then allow the vector generator program counter and state machine to access this same area of RAM also, and read what instructions were sent to it by the game MPU.

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The purpose of the vector timer is to time out the length of time it takes to "draw" an actual vector on the monitor display. During the interval when the X and Y position counters are actually drawing the vector, STOP is high. This prevents the vector generator state machine from advancing to its next state until the vector currently being drawn is completed. As soon as the vector has been drawn, STOP goes low, allowing the state machine to advance to the next state in its intended sequence.

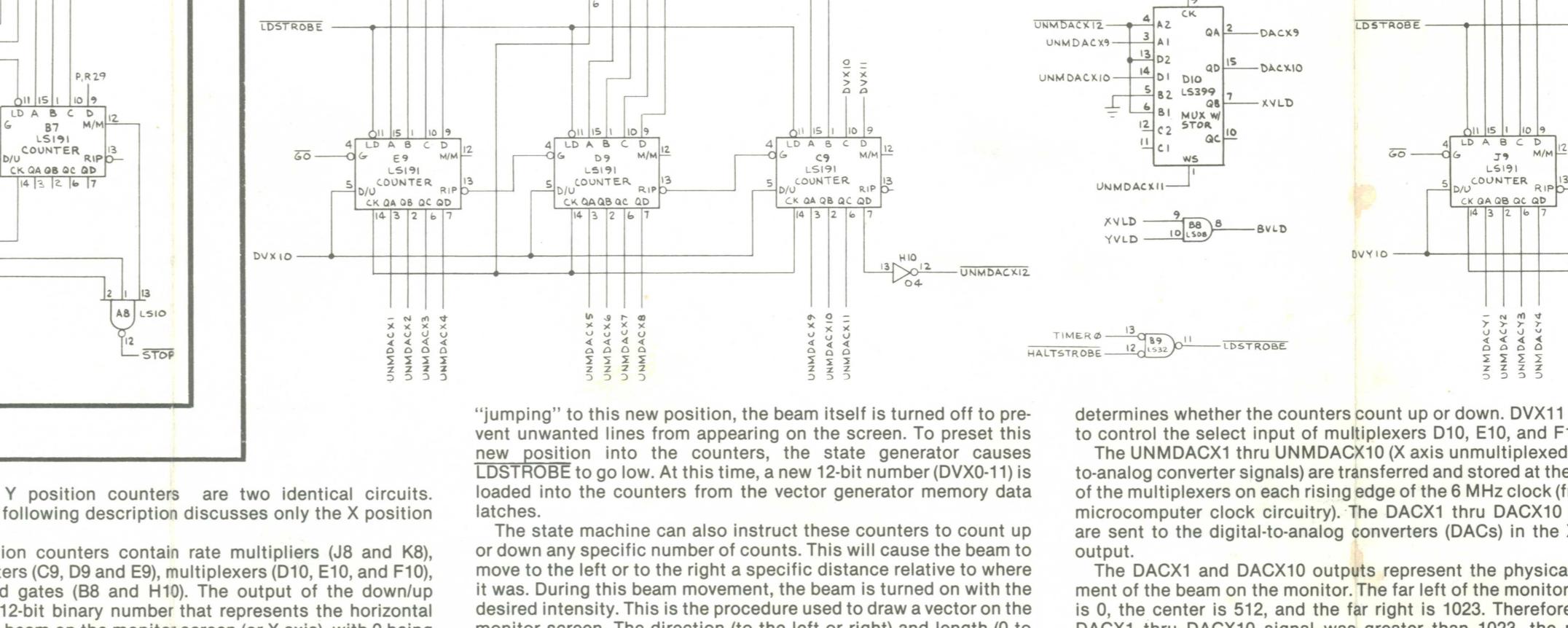
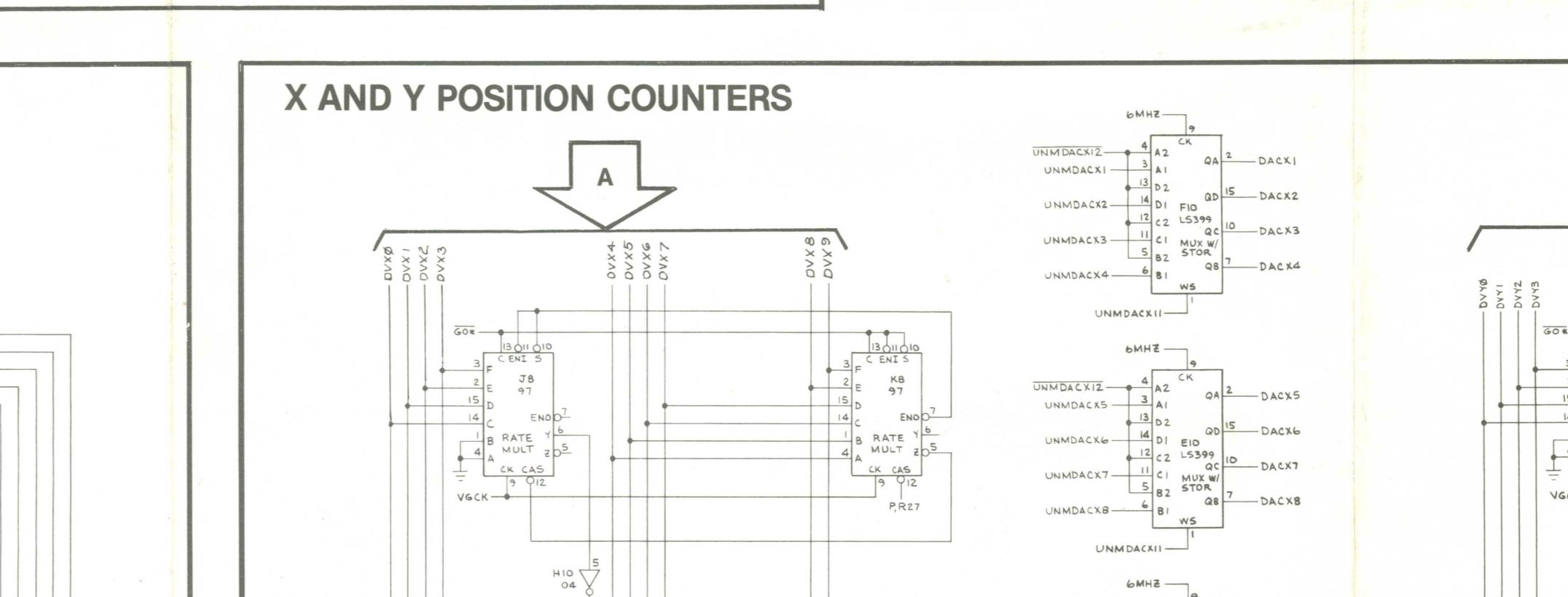
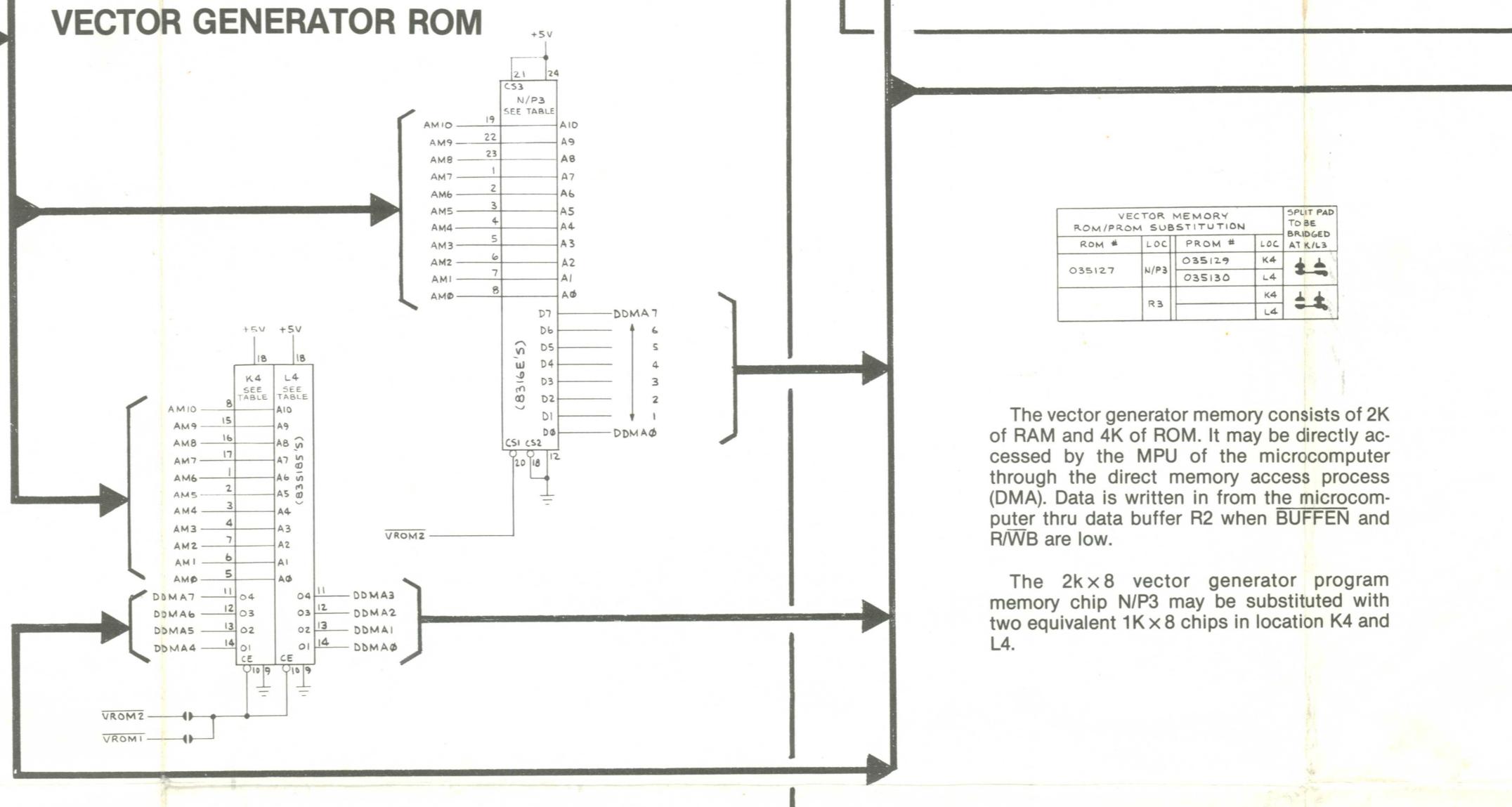
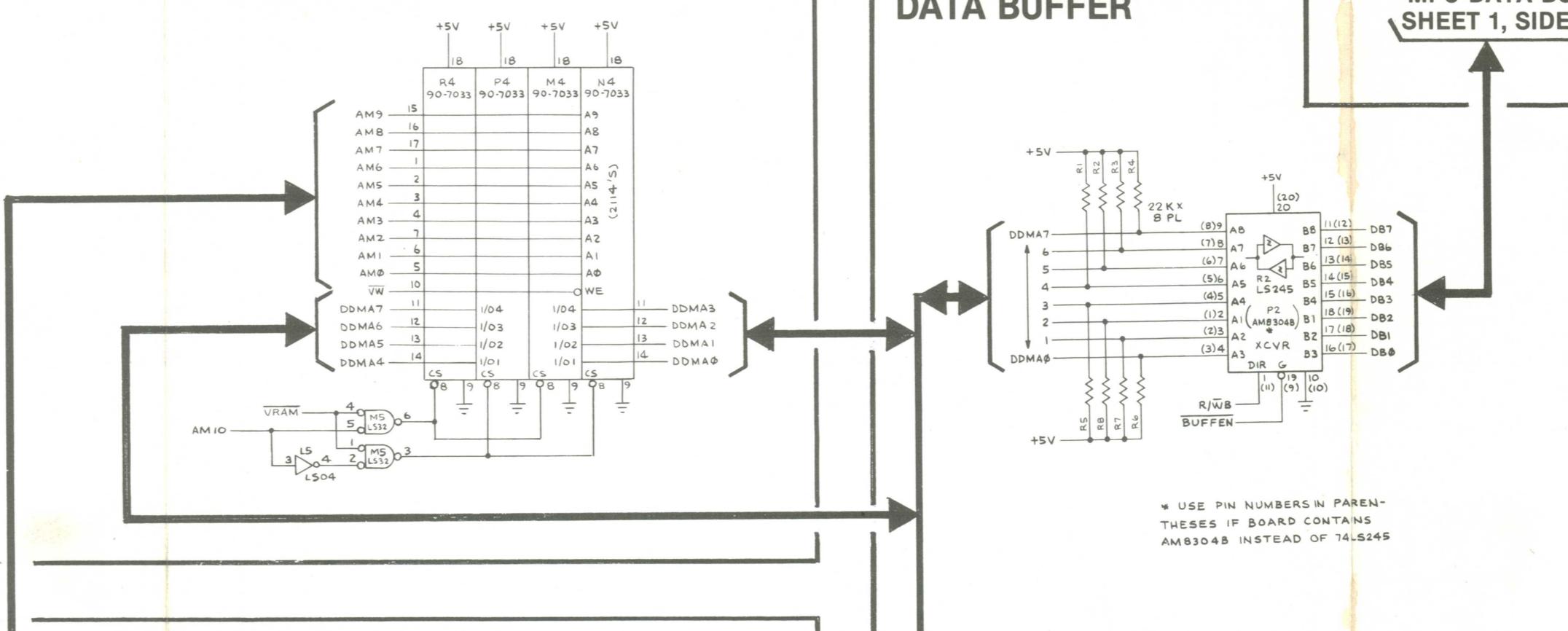
The vector timer consists of multiplexer F6, decoder E7, LATCH M7, ADDER M6, and counters B7, C7, and D7. M7 contains a scale factor which is added in M6 to the four timer signals. If TIMER0 thru TIMER3 inputs are any state but all high, decoder E7 directly decodes the sum and loads the decoded low into one of the counters. When GO goes low, the counters count from the loaded count until the counters all reach their maximum count. This count is a maximum length of 1024. At this time STOP goes low and clears the GO flip-flop of the state machine.

The VGCK input to the clock circuitry is a buffered 1.5 MHz

clock signal from the microcomputer. This is the same frequency used to clock the MPU of the microcomputer. The signal clocks latch D8 unless the microcomputer is addressing the vector RAM or ROM memories (when VMEM goes low). Then the clock input to latch D8 goes high and stays high until VMEM goes high.

If the TIMER signals are all high, ALPHANUM goes low and data signals DVX11 and DVY11 are decoded by decoder E7. This is added to the scale factor and loaded into the counters.

VECTOR GENERATOR RAM



The X and Y position counters are two identical circuits. Therefore, the following description discusses only the X position counters.

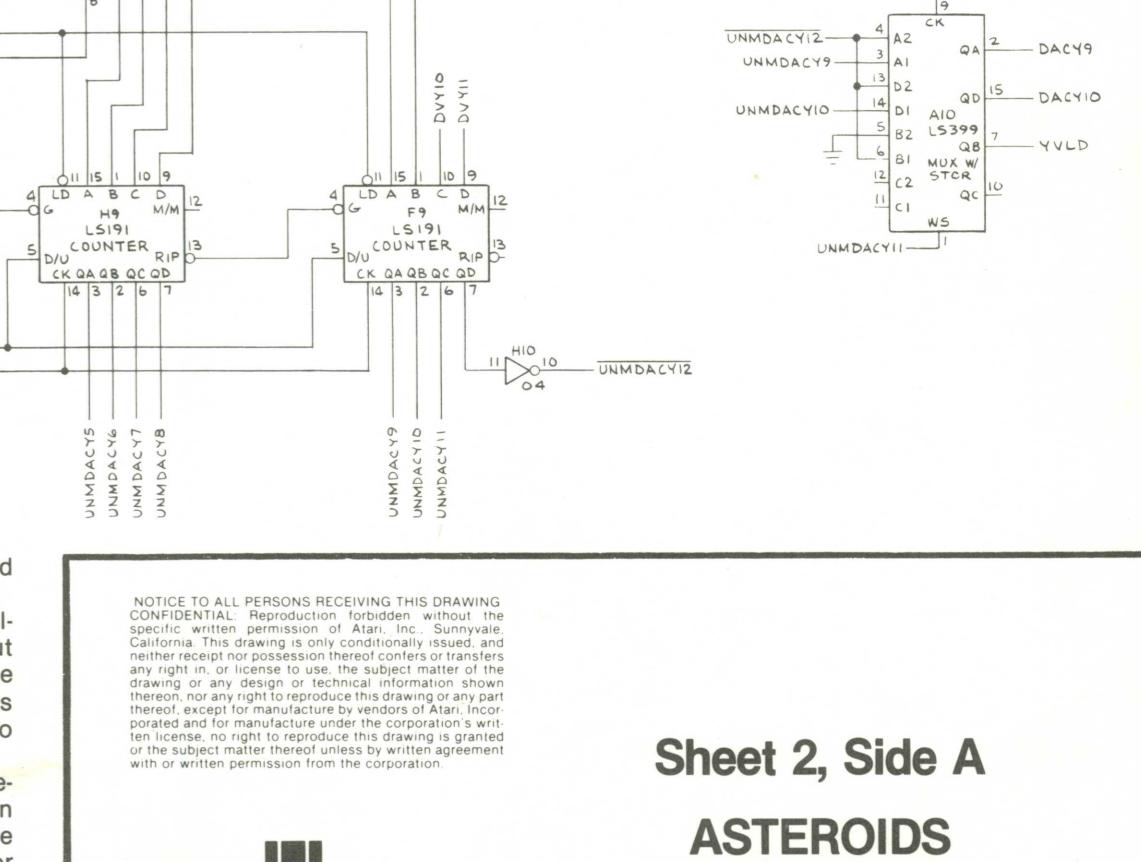
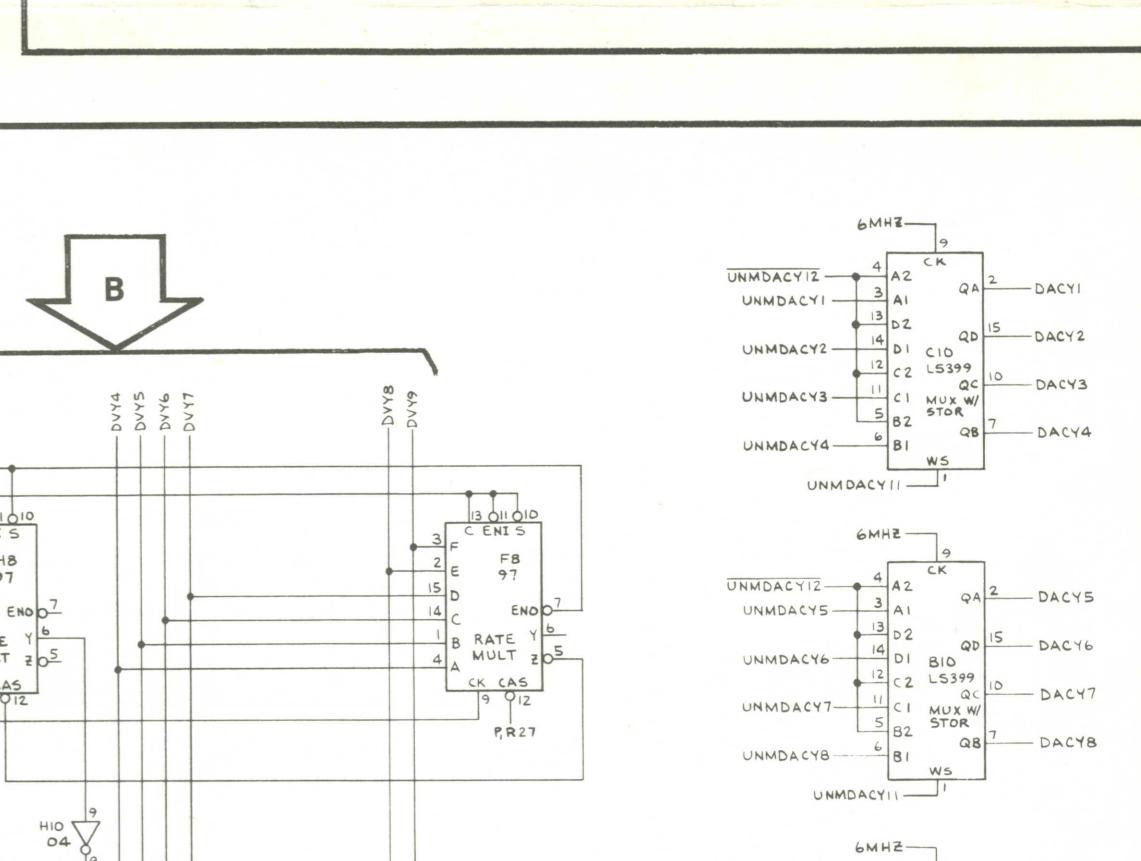
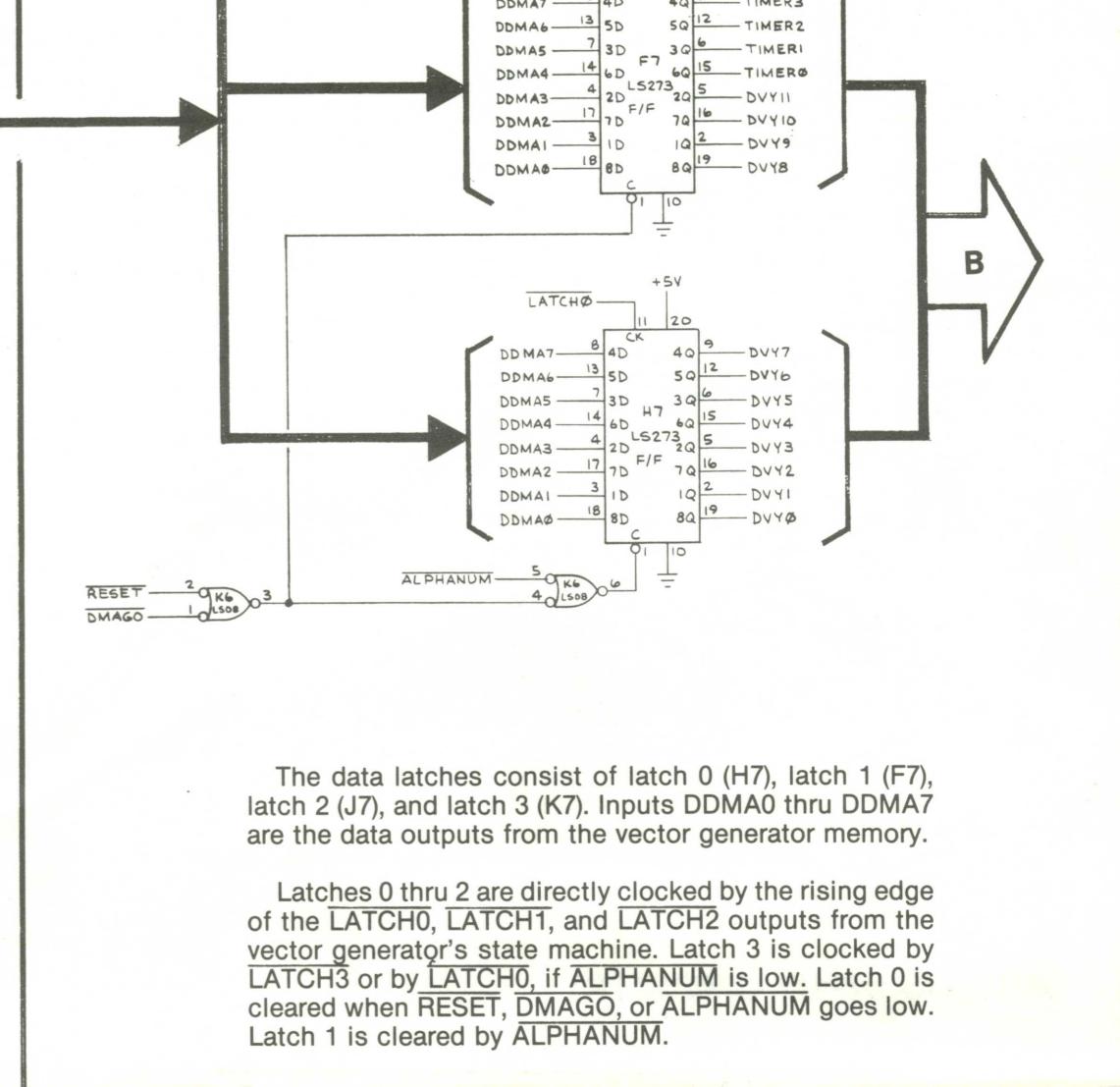
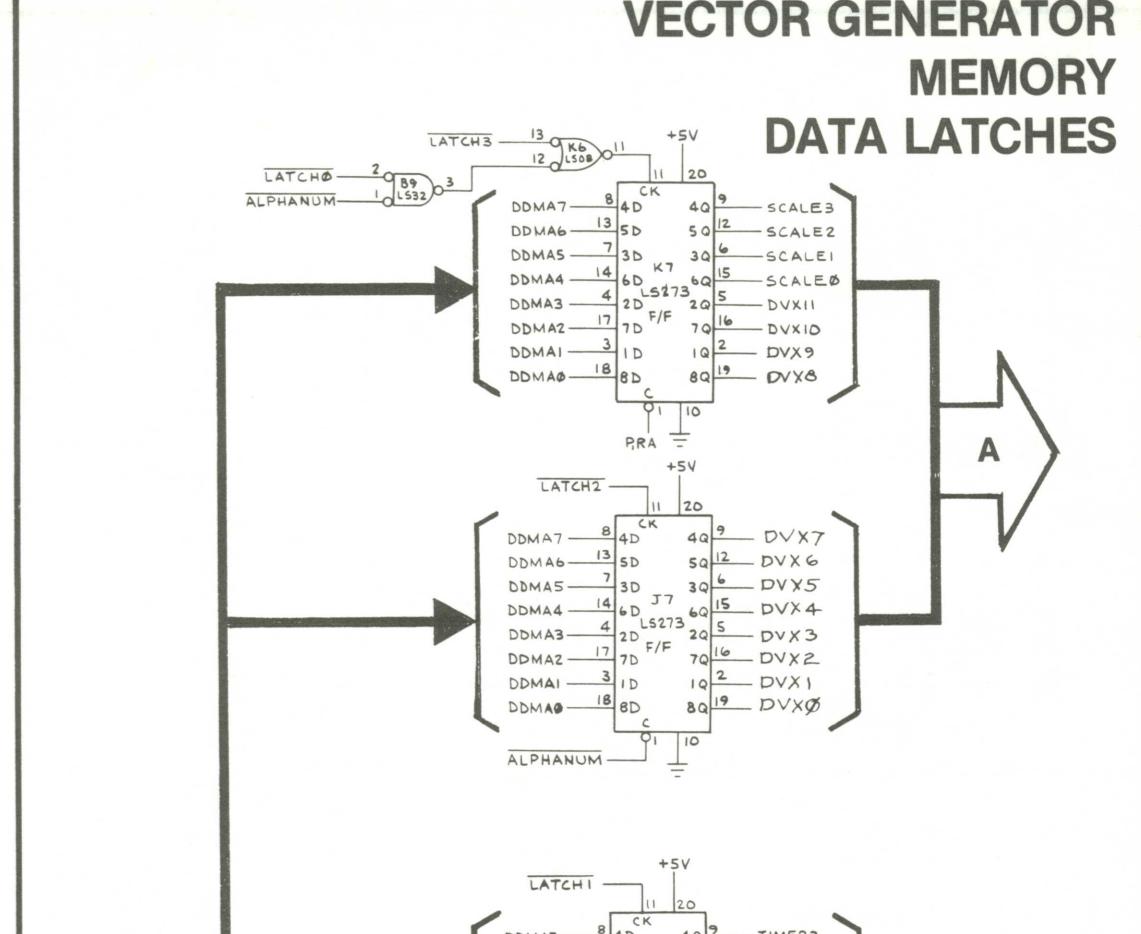
The X position counters contain rate multipliers J8 and K8, down/up counters C9, D9 and E9, multiplexers D10, E10, and F10, and associated gates (B8 and H10). The output of the down/up counter is a 12-bit binary number that represents the horizontal location of the beam on the monitor screen (or X axis), with the most significant bit (MSB) at the top of the screen and the least significant bit (LSB) at the bottom. Increasing or decreasing this binary number output will cause the beam to move to the right or left, respectively. The vector generator state machine decides instructions from its memory, and then is capable of using that data to alter the binary count of these counters in one of two ways.

The DACX1 thru DACX10 outputs represent the physical placement of the beam on the monitor. The far left of the monitor screen is 0, the center is 512, and the far right is 1023. Therefore, if the beam is positioned at address 1023, the beam would go to the right side of the screen and start again on the left side of the screen, a "wraparound" condition. To prevent a wraparound, the multiplexers' select input from UNMDACX1 goes high when the count is greater than 1023 or less than 0. This selects UNMDACX12 to be output from the multiplexers to the DACs, forcing all zeros or all ones, and thus keeping the beam on the appropriate side on the screen, instead of allowing it to wraparound.

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Sheet 2, Side A

ASTEROIDS Video Generator

