

# ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit $\mu$ P Compatible A/D Converters

## General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder — similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

## Features

- Compatible with 8080  $\mu$ P derivatives — no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"

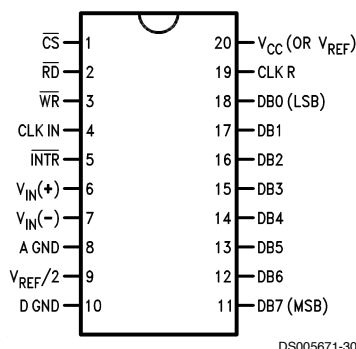
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5  $V_{DC}$ , 2.5  $V_{DC}$ , or analog span adjusted voltage reference

## Key Specifications

- Resolution 8 bits
- Total error  $\pm 1/4$  LSB,  $\pm 1/2$  LSB and  $\pm 1$  LSB
- Conversion time 100  $\mu$ s

## Connection Diagram

**ADC080X**  
Dual-In-Line and Small Outline (SO) Packages



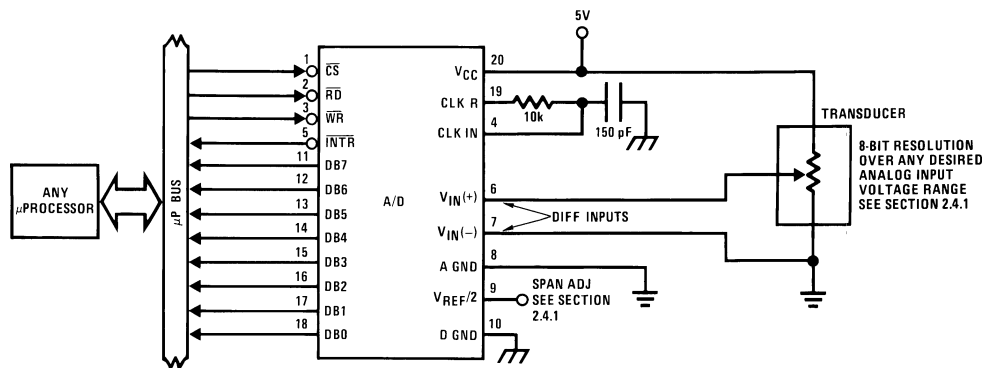
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See Ordering Information

## Ordering Information

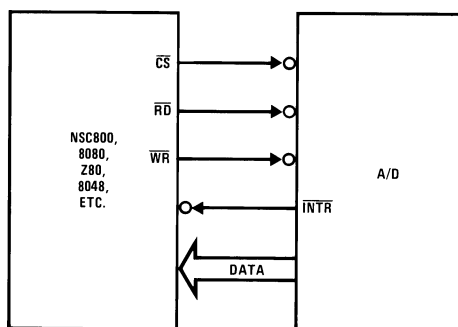
TEMP RANGE		0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted	ADC0802LCWM		ADC0801LCN
	±½ Bit Unadjusted			ADC0802LCN
	±½ Bit Adjusted	ADC0803LCN		
	±1Bit Unadjusted	ADC0805LCN/ADC0804LCJ		
PACKAGE OUTLINE		M20B — Small Outline	N20A — Molded DIP	

## Typical Applications



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### 8080 Interface



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Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2=2.500 V_{DC}$ (No Adjustments)	$V_{REF}/2=\text{No Connection}$ (No Adjustments)
ADC0801	$\pm 1/4$ LSB		
ADC0802		$\pm 1/2$ LSB	
ADC0803	$\pm 1/2$ LSB		
ADC0804		$\pm 1$ LSB	
ADC0805			$\pm 1$ LSB

## Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ ) (Note 3)	6.5V
Voltage	
Logic Control Inputs	-0.3V to +18V
At Other Input and Outputs	-0.3V to ( $V_{CC}+0.3V$ )
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C

Infrared (15 seconds)	220°C
Storage Temperature Range	-65°C to +150°C
Package Dissipation at $T_A=25^\circ\text{C}$	875 mW
ESD Susceptibility (Note 10)	800V

## Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0804LCJ	-40°C $\leq T_A \leq$ +85°C
ADC0801/02/03/05LCN	-40°C $\leq T_A \leq$ +85°C
ADC0804LCN	0°C $\leq T_A \leq$ +70°C
ADC0802/04LCWM	0°C $\leq T_A \leq$ +70°C
Range of $V_{CC}$	4.5 $V_{DC}$ to 6.3 $V_{DC}$

## Electrical Characteristics

The following specifications apply for  $V_{CC}=5 V_{DC}$ ,  $T_{MIN} \leq T_A \leq T_{MAX}$  and  $f_{CLK}=640$  kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			$\pm 1/4$	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2=2.500 V_{DC}$			$\pm 1/2$	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			$\pm 1/2$	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2=2.500 V_{DC}$			$\pm 1$	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$ -No Connection			$\pm 1$	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05	2.5	8.0		k $\Omega$
	ADC0804 (Note 9)	0.75	1.1		k $\Omega$
Analog Input Voltage Range	(Note 4) $V(+)$ or $V(-)$	Gnd-0.05		$V_{CC}+0.05$	$V_{DC}$
DC Common-Mode Error	Over Analog Input Voltage Range		$\pm 1/16$	$\pm 1/8$	LSB
Power Supply Sensitivity	$V_{CC}=5 V_{DC} \pm 10\%$ Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		$\pm 1/16$	$\pm 1/8$	LSB

## AC Electrical Characteristics

The following specifications apply for  $V_{CC}=5 V_{DC}$  and  $T_{MIN} \leq T_A \leq T_{MAX}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_C$	Conversion Time	$f_{CLK}=640$ kHz (Note 6)	103		114	$\mu\text{s}$
$T_C$	Conversion Time	(Notes 5, 6)	66		73	$1/f_{CLK}$
$f_{CLK}$	Clock Frequency	$V_{CC}=5V$ , (Note 5)	100	640	1460	kHz
	Clock Duty Cycle		40		60	%
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}=0 V_{DC}$ , $f_{CLK}=640$ kHz	8770		9708	conv/s
$t_{W(WR)L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}=0 V_{DC}$ (Note 7)	100			ns
$t_{ACC}$	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L=100$ pF		135	200	ns
$t_{1H}$ , $t_{0H}$	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$C_L=10$ pF, $R_L=10k$ (See TRI-STATE Test Circuits)		125	200	ns
$t_{WI}$ , $t_{RI}$	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
$C_{IN}$	Input Capacitance of Logic Control Inputs			5	7.5	pF

## AC Electrical Characteristics (Continued)

The following specifications apply for  $V_{CC}=5\text{ V}_{DC}$  and  $T_{MIN}\leq T_A\leq T_{MAX}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$C_{OUT}$	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
<b>CONTROL INPUTS</b> [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
$V_{IN}(1)$	Logical "1" Input Voltage (Except Pin 4 CLK IN)	$V_{CC}=5.25\text{ V}_{DC}$	2.0		15	$V_{DC}$
$V_{IN}(0)$	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V_{CC}=4.75\text{ V}_{DC}$			0.8	$V_{DC}$
$I_{IN}(1)$	Logical "1" Input Current (All Inputs)	$V_{IN}=5\text{ V}_{DC}$		0.005	1	$\mu A_{DC}$
$I_{IN}(0)$	Logical "0" Input Current (All Inputs)	$V_{IN}=0\text{ V}_{DC}$	-1	-0.005		$\mu A_{DC}$
<b>CLOCK IN AND CLOCK R</b>						
$V_{T+}$	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	$V_{DC}$
$V_{T-}$	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	$V_{DC}$
$V_H$	CLK IN (Pin 4) Hysteresis ( $V_{T+}$ ) - ( $V_{T-}$ )		0.6	1.3	2.0	$V_{DC}$
$V_{OUT}(0)$	Logical "0" CLK R Output Voltage	$I_O=360\text{ }\mu A$ $V_{CC}=4.75\text{ V}_{DC}$			0.4	$V_{DC}$
$V_{OUT}(1)$	Logical "1" CLK R Output Voltage	$I_O=-360\text{ }\mu A$ $V_{CC}=4.75\text{ V}_{DC}$	2.4			$V_{DC}$
<b>DATA OUTPUTS AND INTR</b>						
$V_{OUT}(0)$	Logical "0" Output Voltage Data Outputs INTR Output	$I_{OUT}=1.6\text{ mA}$ , $V_{CC}=4.75\text{ V}_{DC}$ $I_{OUT}=1.0\text{ mA}$ , $V_{CC}=4.75\text{ V}_{DC}$			0.4 0.4	$V_{DC}$ $V_{DC}$
$V_{OUT}(1)$	Logical "1" Output Voltage	$I_O=-360\text{ }\mu A$ , $V_{CC}=4.75\text{ V}_{DC}$	2.4			$V_{DC}$
$V_{OUT}(1)$	Logical "1" Output Voltage	$I_O=-10\text{ }\mu A$ , $V_{CC}=4.75\text{ V}_{DC}$	4.5			$V_{DC}$
$I_{OUT}$	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT}=0\text{ V}_{DC}$ $V_{OUT}=5\text{ V}_{DC}$	-3		3	$\mu A_{DC}$ $\mu A_{DC}$
$I_{SOURCE}$		$V_{OUT}$ Short to Gnd, $T_A=25^\circ C$	4.5	6		$mA_{DC}$
$I_{SINK}$		$V_{OUT}$ Short to $V_{CC}$ , $T_A=25^\circ C$	9.0	16		$mA_{DC}$
<b>POWER SUPPLY</b>						
$I_{CC}$	Supply Current (Includes Ladder Current)  ADC0801/02/03/04LCJ/05 ADC0804LCN/LCWM	$f_{CLK}=640\text{ kHz}$ , $V_{REF}/2=NC$ , $T_A=25^\circ C$ and $CS=5V$		1.1 1.9	1.8 2.5	mA mA

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 2:** All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

**Note 3:** A zener diode exists, internally, from  $V_{CC}$  to Gnd and has a typical breakdown voltage of  $7\text{ V}_{DC}$ .

**Note 4:** For  $V_{IN}(-)\geq V_{IN}(+)$  the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the  $V_{CC}$  supply. Be careful, during testing at low  $V_{CC}$  levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog  $V_{IN}$  does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute  $0\text{ V}_{DC}$  to  $5\text{ V}_{DC}$  input voltage range will therefore require a minimum supply voltage of  $4.950\text{ V}_{DC}$  over temperature variations, initial tolerance and loading.

**Note 5:** Accuracy is guaranteed at  $f_{CLK} = 640\text{ kHz}$ . At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

**Note 6:** With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see Figure 4 and section 2.0.

## AC Electrical Characteristics (Continued)

**Note 7:** The  $\overline{CS}$  input is assumed to bracket the  $\overline{WR}$  strobe input and therefore timing is dependent on the  $\overline{WR}$  pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the  $\overline{WR}$  pulse (see timing diagrams).

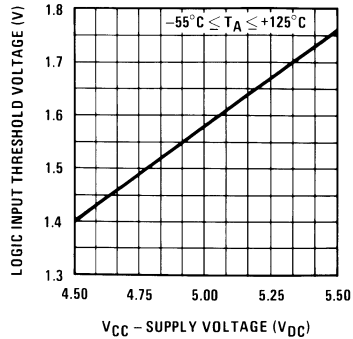
**Note 8:** None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and Figure 7.

**Note 9:** The  $V_{REF}/2$  pin is the center point of a two-resistor divider connected from  $V_{CC}$  to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 k $\Omega$ . In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 k $\Omega$ .

**Note 10:** Human body model, 100 pF discharged through a 1.5 k $\Omega$  resistor.

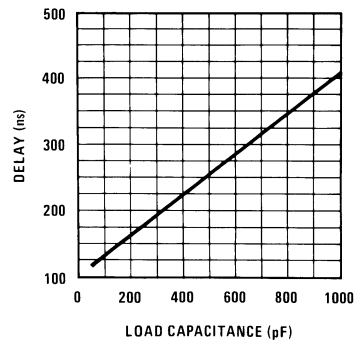
## Typical Performance Characteristics

**Logic Input Threshold Voltage vs. Supply Voltage**



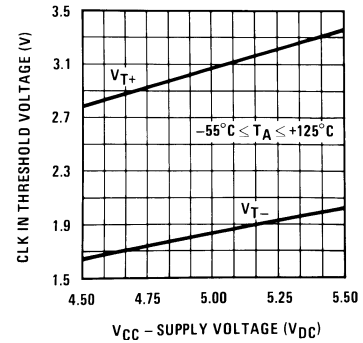
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**Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance**



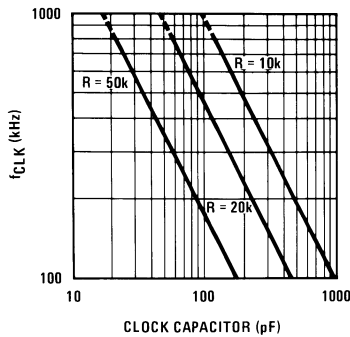
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**CLK IN Schmitt Trip Levels vs. Supply Voltage**



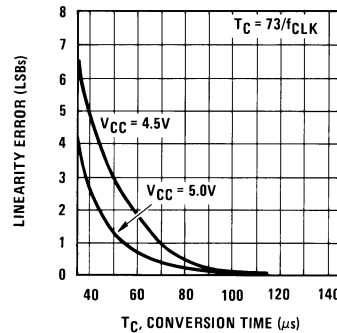
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**fCLK vs. Clock Capacitor**



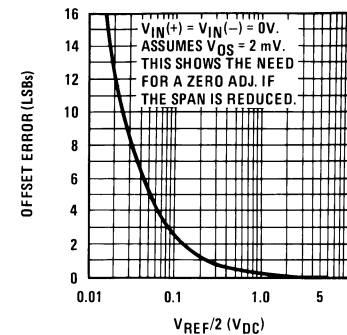
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**Full-Scale Error vs Conversion Time**



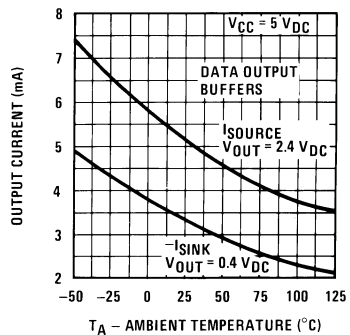
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**Effect of Unadjusted Offset Error vs. VREF/2 Voltage**



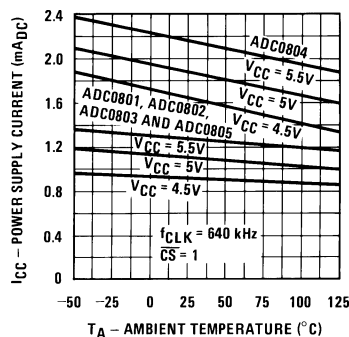
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**Output Current vs Temperature**



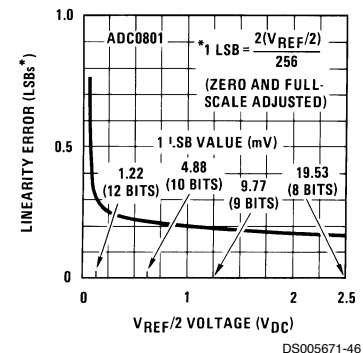
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**Power Supply Current vs Temperature (Note 9)**



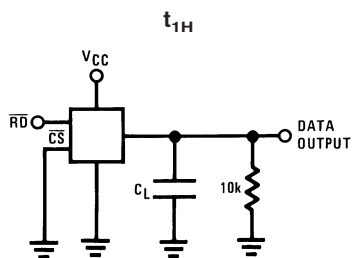
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**Linearity Error at Low VREF/2 Voltages**



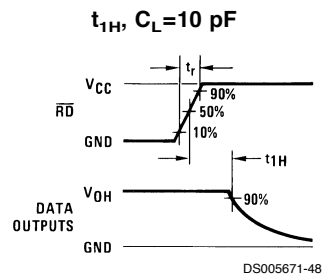
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## TRI-STATE Test Circuits and Waveforms

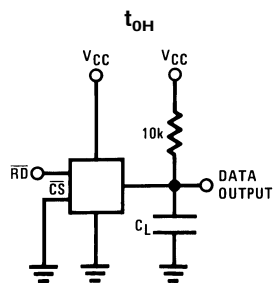


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$t_r = 20 \text{ ns}$

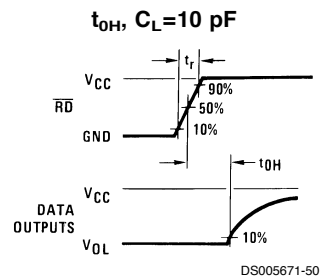


DS005671-48



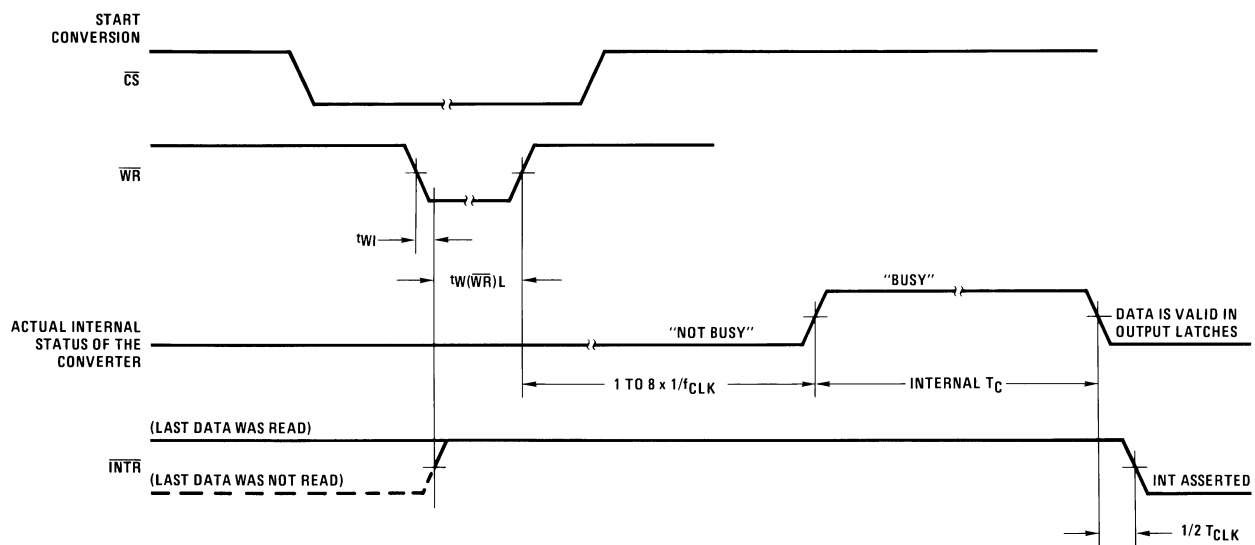
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$t_r = 20 \text{ ns}$



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## Timing Diagrams (All timing is measured from the 50% voltage points)



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The diagram shows the timing relationship between the **INTR** (Interrupt Request), **CS** (Chip Select), **RD** (Read Strobe), and **DATA OUTPUTS** signals. The **INTR** signal is active-low. The **CS** signal is active-low. The **RD** signal is active-low. The **DATA OUTPUTS** signal is shown as a dashed line, indicating it is in a high-impedance state when not selected. The timing parameters are defined as follows:

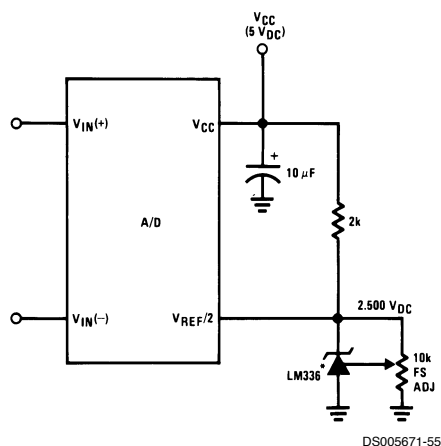
- $t_{RL}$** : Read Latency, the time from the falling edge of **CS** to the data becoming valid.
- $t_{ACC}$** : Access Time, the time from the falling edge of **RD** to the data becoming valid.
- $t_{1H}, t_{0H}$** : Hold Time, the time from the rising edge of **RD** to the data becoming invalid.
- TRI-STATE<sup>®</sup>**: The state of the **DATA OUTPUTS** when not selected.
- NOTE**: A period between the falling edge of **CS** and the falling edge of **RD**.

## Typical Applications

[illegible]

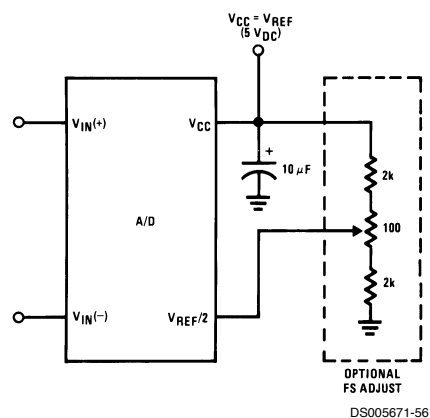
Note: before using caps at  $V_{IN}$  or  $V_{REF}/2$ , see section 2.3.2 Input Bypass Capacitors.

### Absolute with a 2.500V Reference

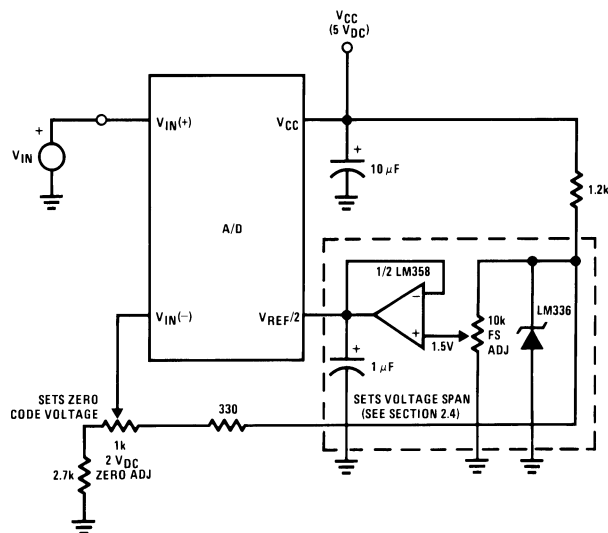


\*For low power, see also LM385–2.5

### Absolute with a 5V Reference

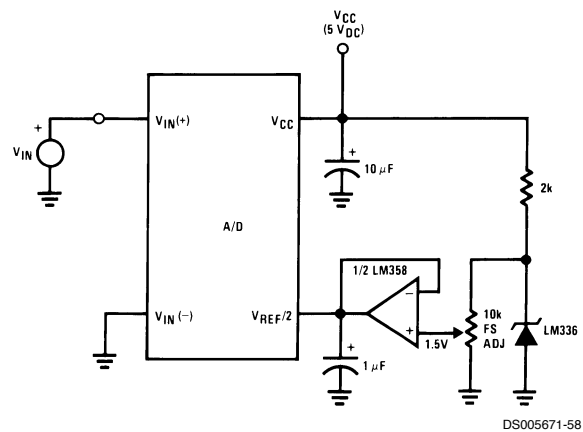


### Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



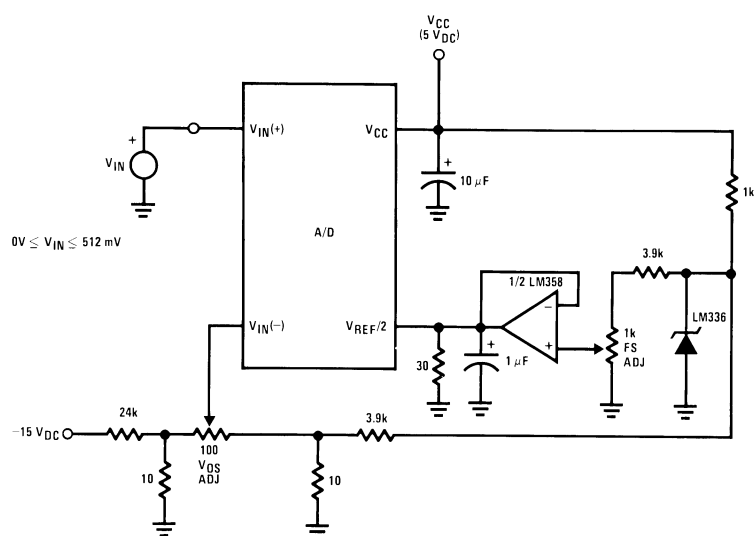
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**Span Adjust:**  $0V \leq V_{IN} \leq 3V$



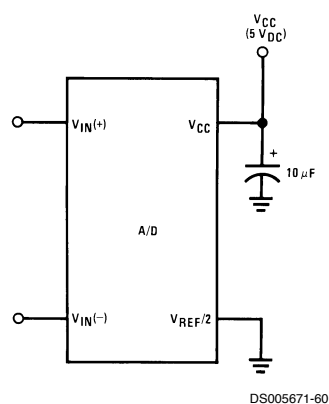


## Directly Converting a Low-Level Signal


$$V_{REF}/2=256 \text{ mV}$$

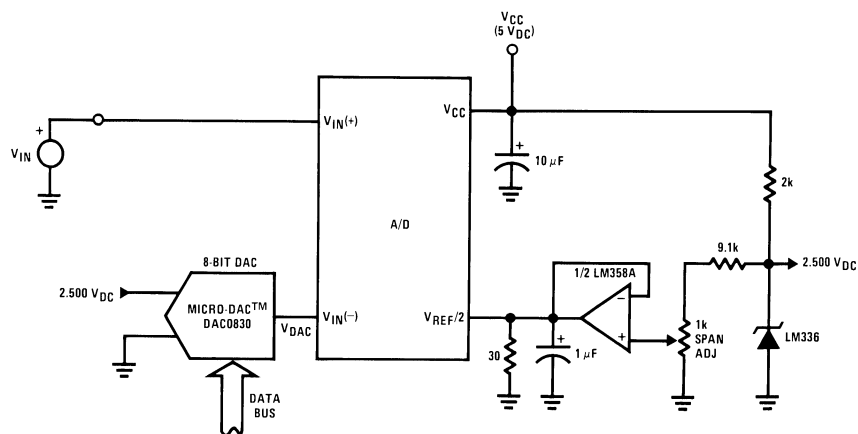
DS005671-59

### A $\mu$ P Interfaced Comparator



For:  
 $V_{IN(+)} > V_{IN(-)}$   
 Output = FF<sub>HEX</sub>  
 For:  
 $V_{IN(+)} < V_{IN(-)}$   
 Output = 00<sub>HEX</sub>

### 1 mV Resolution with $\mu$ P Controlled Range

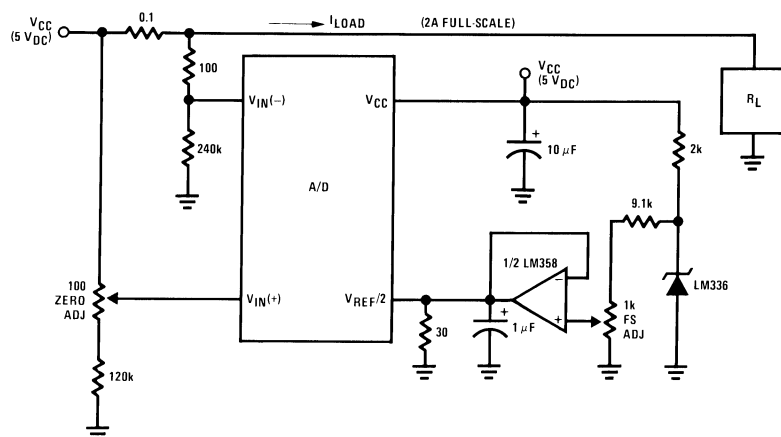


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$V_{REF}/2=128\text{ mV}$   
 $1\text{ LSB}=1\text{ mV}$   
 $V_{DAC}\leq V_{IN}\leq(V_{DAC}+256\text{ mV})$   
 $0\leq V_{DAC}<2.5\text{V}$

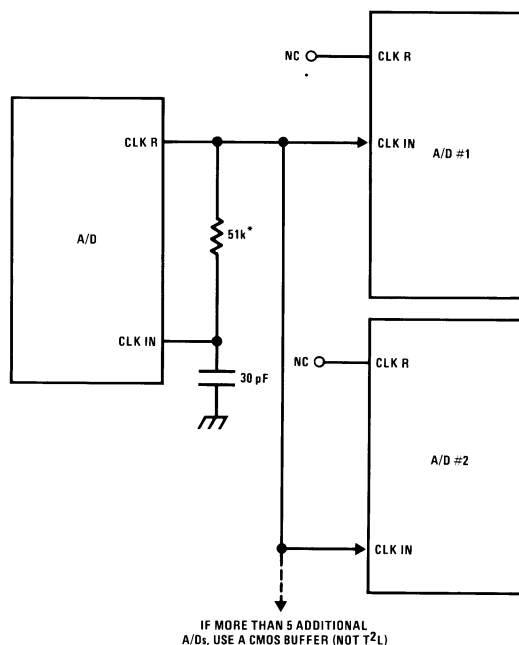
## Typical Applications (Continued)

### Digitizing a Current Flow



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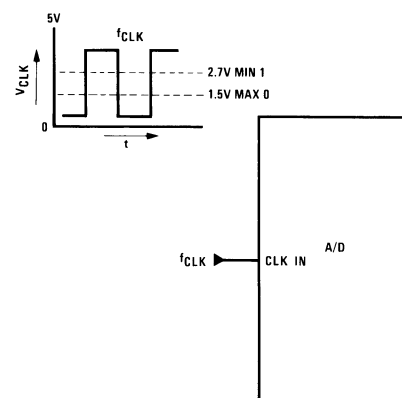
### Self-Clocking Multiple A/Ds



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\* Use a large R value to reduce loading at CLK R output.

### External Clocking

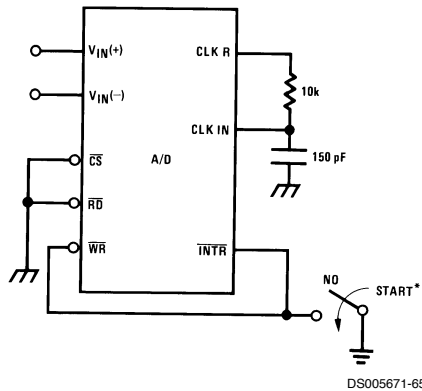


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100 kHz ≤ f<sub>CLK</sub> ≤ 1460 kHz

## Typical Applications (Continued)

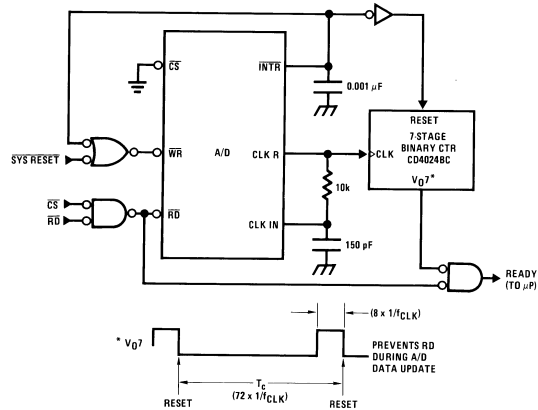
## Self-Clocking in Free-Running Mode



DS005671-65

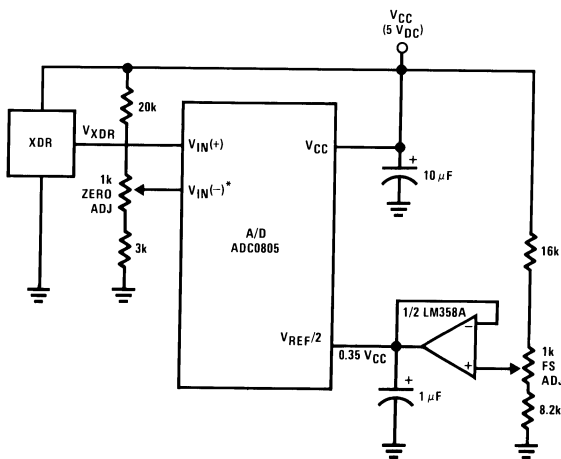
\*After power-up, a momentary grounding of the  $\overline{\text{WR}}$  input is needed to guarantee operation.

## $\mu$ P Interface for Free-Running A/D



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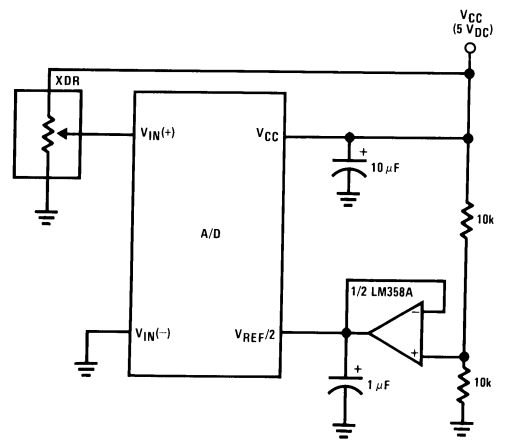
## Operating with “Automotive” Ratiometric Transducers



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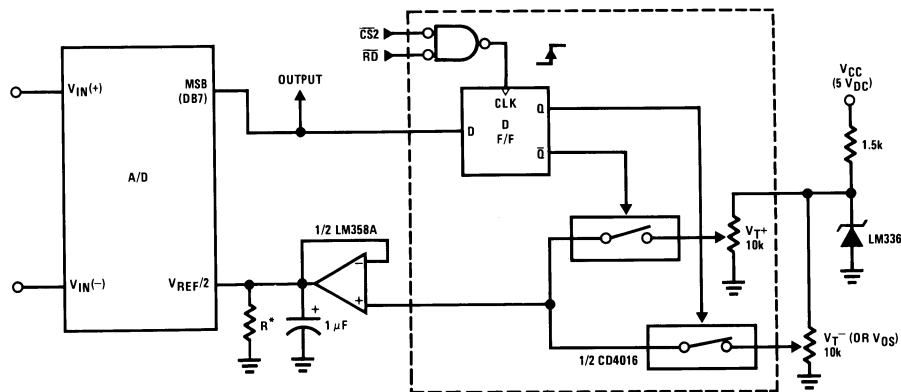
\* $V_{IN(-)} = 0.15 V_{CC}$   
 $15\% \text{ of } V_{CC} \leq V_{XDR} \leq 85\% \text{ of } V_{CC}$

### Ratiometric with $V_{REF}/2$ Forced



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### **$\mu$ P Compatible Differential-Input Comparator with Pre-Set $V_{OS}$ (with or without Hysteresis)**



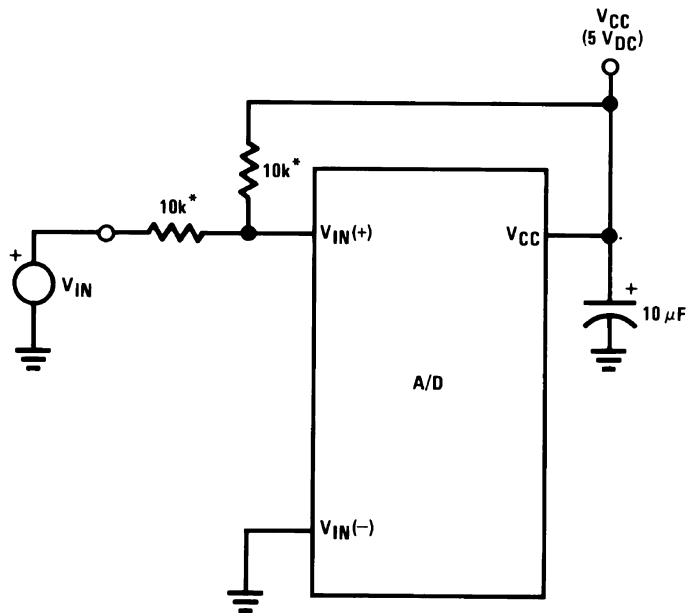
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\*See Figure 5 to select R value  
DB7="1" for  $V_{IN(+)} > V_{IN(-)} + (V_{REF}/2)$   
Omit circuitry within the dotted area if  
hysteresis is not needed



## Typical Applications (Continued)

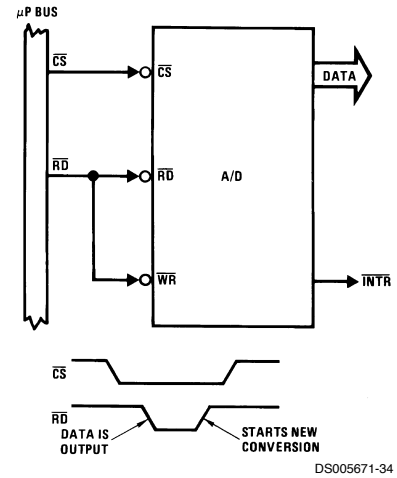
### Handling $\pm 5V$ Analog Inputs



DS005671-33

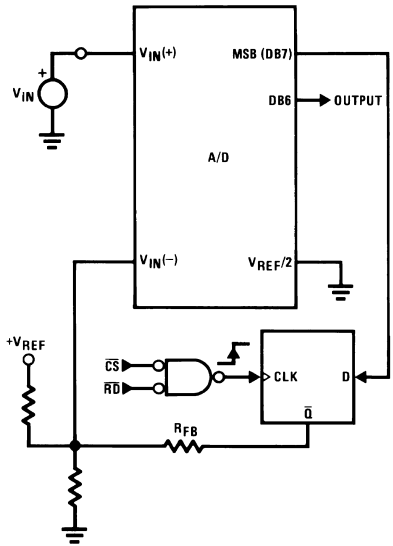
\*Beckman Instruments #694-3-R10K resistor array

### Read-Only Interface



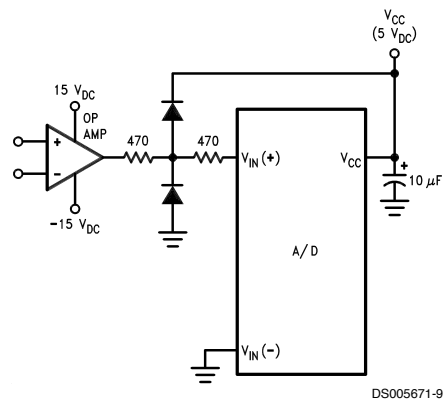
DS005671-34

### $\mu P$ Interfaced Comparator with Hysteresis



DS005671-35

### Protecting the Input

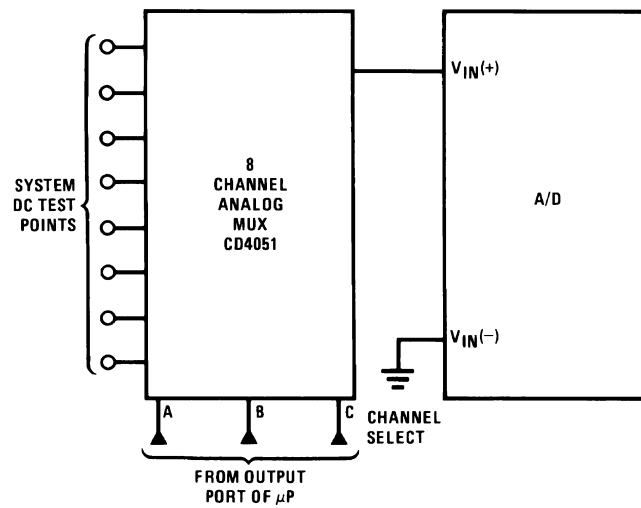


DS005671-9

Diodes are 1N914

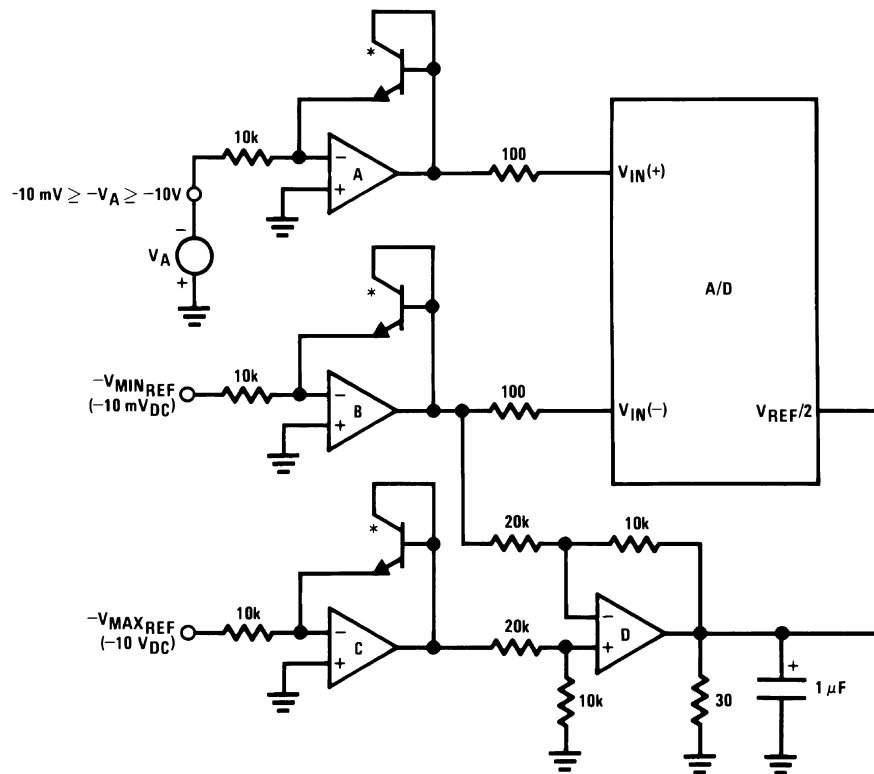
## Typical Applications (Continued)

### Analog Self-Test for a System



DS005671-36

### A Low-Cost, 3-Decade Logarithmic Converter



DS005671-37

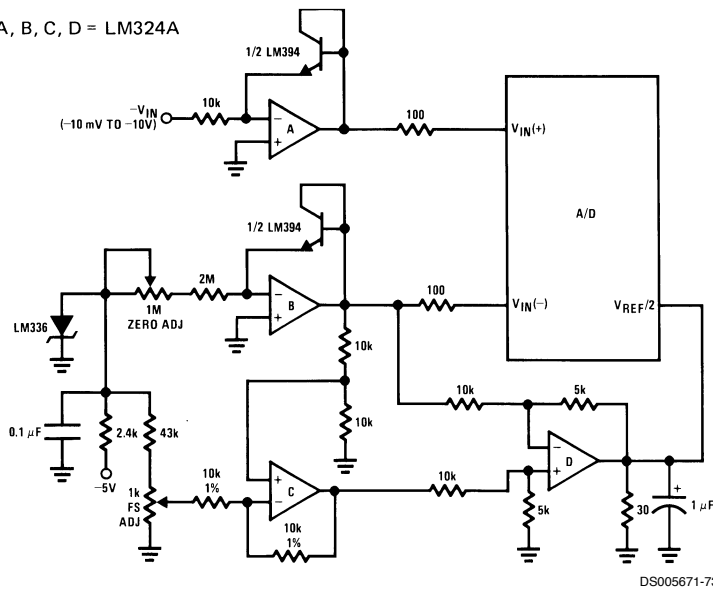
\*LM389 transistors

A, B, C, D = LM324A quad op amp

## Typical Applications (Continued)

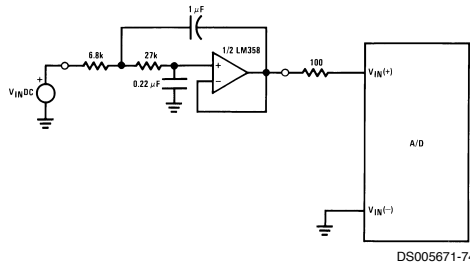
### 3-Decade Logarithmic A/D Converter

A, B, C, D = LM324A



DS005671-73

### Noise Filtering the Analog Input



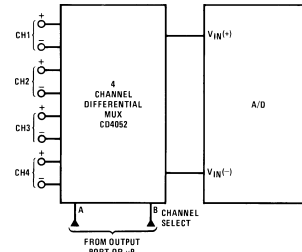
DS005671-74

$f_c = 20$  Hz

Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter

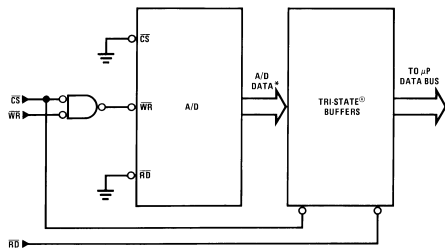
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

### Multiplexing Differential Inputs



DS005671-75

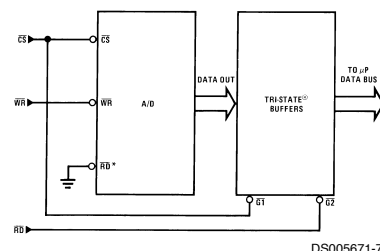
### Output Buffers with A/D Data Enabled



DS005671-76

\*A/D output data is updated 1 CLK period prior to assertion of  $\overline{\text{INT}}$

### Increasing Bus Drive and/or Reducing Time on Bus

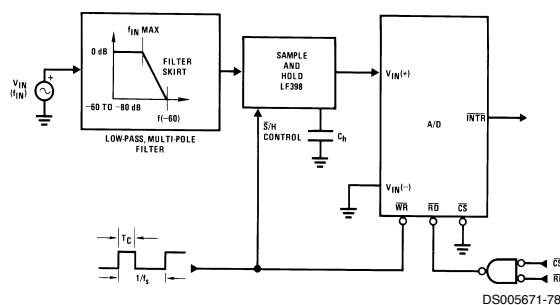


DS005671-77

\*Allows output data to set-up at falling edge of  $\overline{\text{CS}}$

## Typical Applications (Continued)

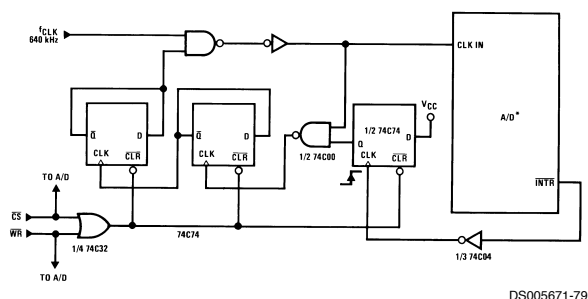
### Sampling an AC Input Signal



**Note 11:** Oversample whenever possible [keep  $f_s > 2f(-60)$ ] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

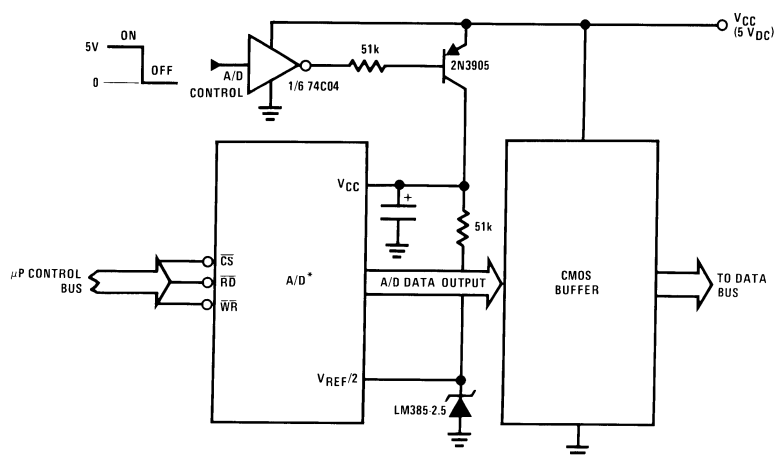
**Note 12:** Consider the amplitude errors which are introduced within the passband of the filter.

### 70% Power Savings by Clock Gating



(Complete shutdown takes  $\approx 30$  seconds.)

### Power Savings by A/D and $V_{REF}$ Shutdown



\*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to  $V_{CC}$  with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

DS005671-80

## Functional Description

### 1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the  $V_{REF}/2$  pin). The digital output codes that correspond to these inputs are shown as

D-1, D, and D+1. For the perfect A/D, not only will center-value (A-1, A, A+1, . . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located  $\pm 1/2$  LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend



## Functional Description (Continued)

$\pm 1/2$  LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Figure 2 shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than  $\pm 1/4$  LSB. In other words, if we apply an analog input equal to the center-value  $\pm 1/4$  LSB, we guarantee that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than  $1/2$  LSB.

The error curve of Figure 3 shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of Figure 1 is  $+1/2$  LSB because the digital code appeared  $1/2$  LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt up-side steps are always 1 LSB in magnitude.

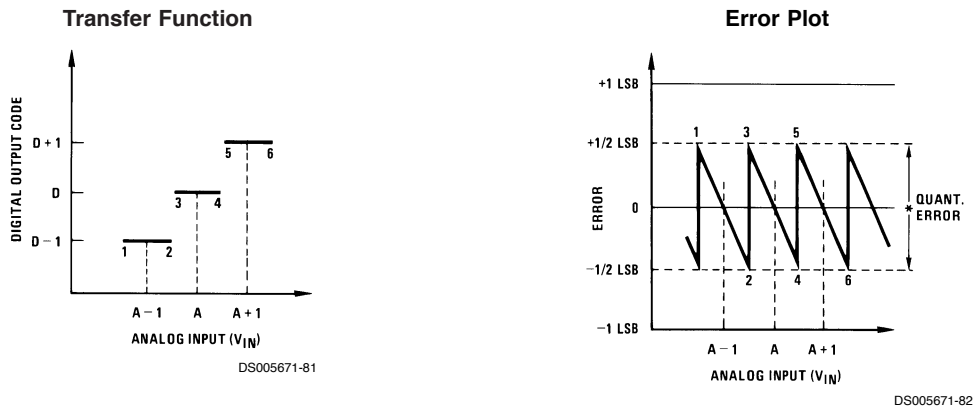


FIGURE 1. Clarifying the Error Specs of an A/D Converter  
Accuracy= $\pm 0$  LSB: A Perfect A/D

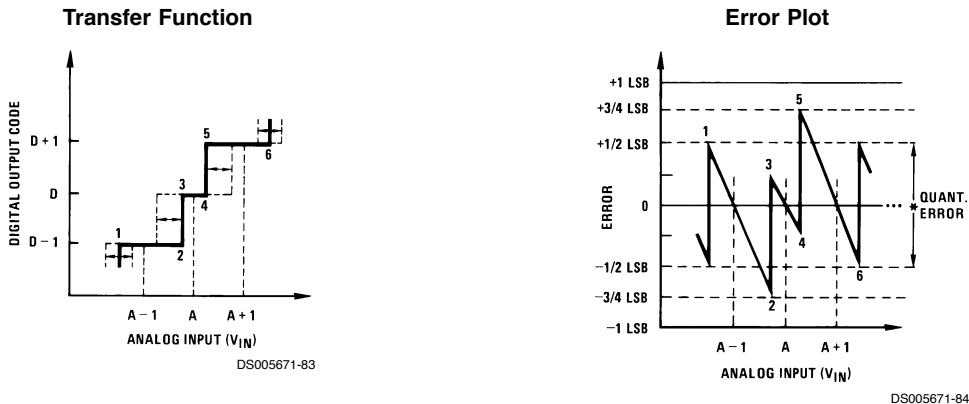
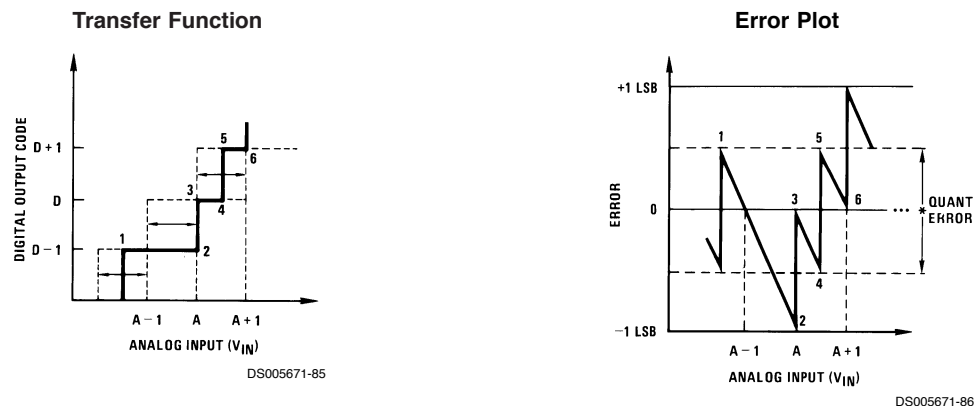


FIGURE 2. Clarifying the Error Specs of an A/D Converter  
Accuracy= $\pm 1/4$  LSB

## Functional Description (Continued)



**FIGURE 3. Clarifying the Error Specs of an A/D Converter**  
Accuracy =  $\pm \frac{1}{2}$  LSB

### 2.0 FUNCTIONAL DESCRIPTION

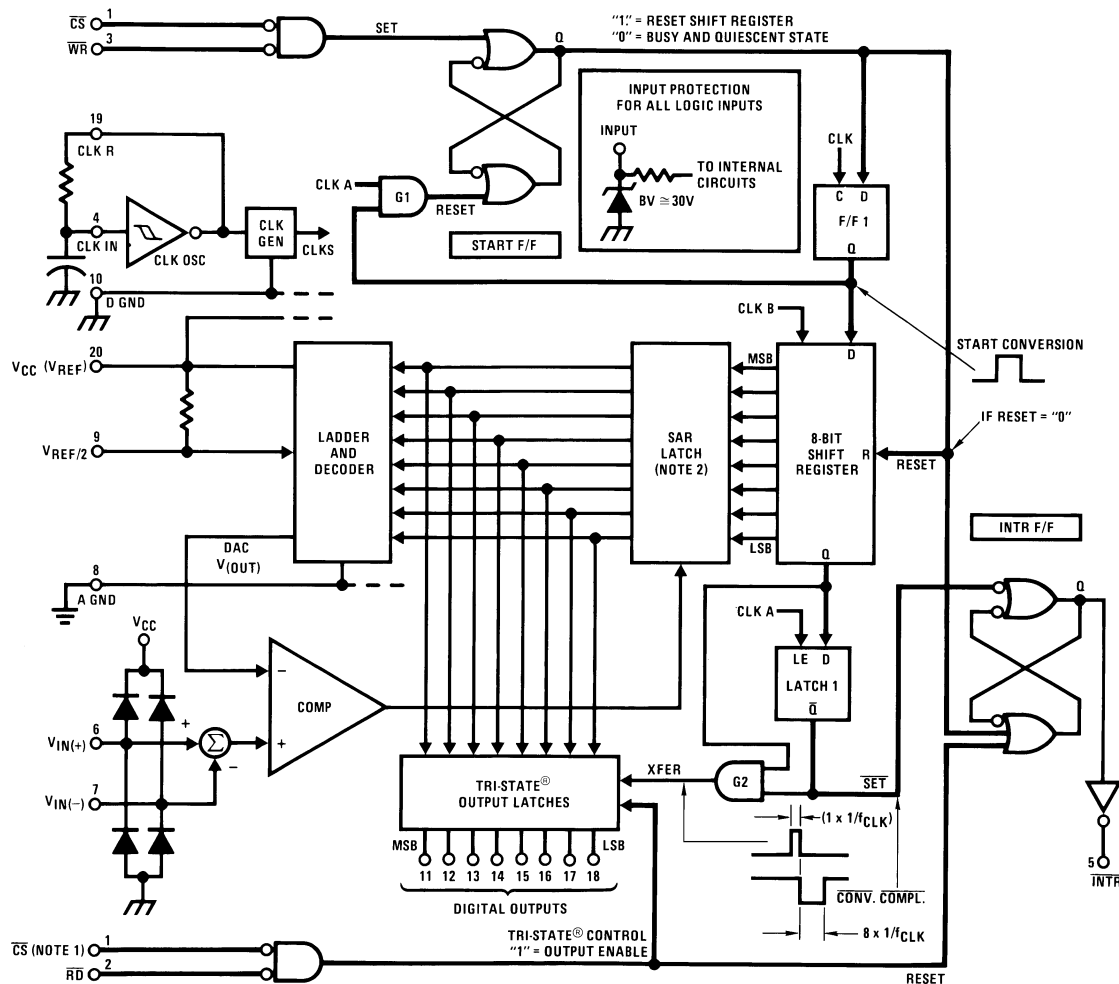
The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage  $[V_{IN(+)} - V_{IN(-)}]$  to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ( $\overline{INTR}$  makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting  $\overline{INTR}$  to the  $\overline{WR}$  input with  $\overline{CS} = 0$ . To ensure start-up under all possible conditions, an external  $\overline{WR}$  pulse is required during the first power-up cycle.

On the high-to-low transition of the  $\overline{WR}$  input the internal SAR latches and the shift register stages are reset. As long as the  $\overline{CS}$  input and  $\overline{WR}$  input remain low, the A/D will remain in a reset state. Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.

A functional diagram of the A/D converter is shown in Figure 4. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having  $\overline{CS}$  and  $\overline{WR}$  simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt ( $\overline{INTR}$ ) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either  $\overline{WR}$  or  $\overline{CS}$  is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide  $\overline{CS}$  and  $\overline{WR}$  signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

## Functional Description (Continued)



DS005671-13

**Note 13:**  $\overline{CS}$  shown twice for clarity.

**Note 14:** SAR = Successive Approximation Register.

**FIGURE 4. Block Diagram**

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the  $\overline{INTR}$  input signal.

Note that this  $\overline{SET}$  control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at  $\frac{1}{8}$  of the frequency of the external clock). If the data output is continuously enabled ( $\overline{CS}$  and  $\overline{RD}$  both held low), the INTR output will still signal the end of conversion (by a high-to-low transition), because the  $\overline{SET}$  input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This  $\overline{INTR}$  output will therefore stay low for the duration of the  $\overline{SET}$  signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ( $\overline{INTR}$  pin tied to  $\overline{WR}$  and  $\overline{CS}$  wired low — see also section 2.8), the START F/F is SET by the high-to-low transition of the INTR signal. This resets the SHIFT REGISTER

which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the  $\overline{Q}$  output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting INTR output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both  $\overline{CS}$  and  $\overline{RD}$  being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

### 2.1 Digital Control Inputs

The digital control inputs ( $\overline{CS}$ ,  $\overline{RD}$ , and  $\overline{WR}$ ) meet standard T<sup>2</sup>L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the  $\overline{CS}$  input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the  $\overline{WR}$  input (pin 3) and the Output Enable function is caused by an active low pulse at the  $\overline{RD}$  input (pin 2).

## Functional Description (Continued)

### 2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The  $V_{IN(-)}$  input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling  $V_{IN(+)}$  and  $V_{IN(-)}$  is 4-1/2 clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(\text{MAX}) = (V_P) (2\pi f_{cm}) \left( \frac{4.5}{f_{CLK}} \right)$$

where:

$\Delta V_e$  is the error voltage due to sampling delay

$V_P$  is the peak value of the common-mode voltage

$f_{cm}$  is the common-mode frequency

As an example, to keep this error to 1/4 LSB (~5 mV) when operating with a 60 Hz common-mode frequency,  $f_{cm}$ , and using a 640 kHz A/D clock,  $f_{CLK}$ , would allow a peak value of the common-mode voltage,  $V_P$ , which is given by:

$$V_P = \frac{[\Delta V_e(\text{MAX}) (f_{CLK})]}{(2\pi f_{cm}) (4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3}) (640 \times 10^3)}{(6.28) (60) (4.5)}$$

which gives

$$V_P = 1.9V.$$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

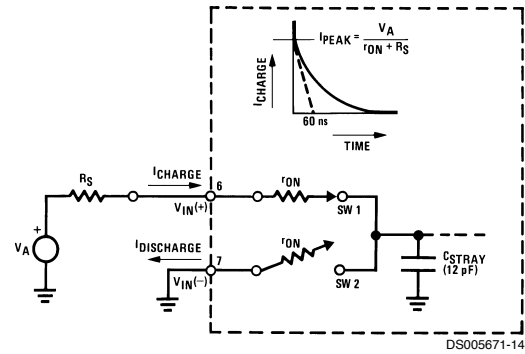
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

### 2.3 Analog Inputs

#### 2.3.1 Input Current

##### Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in Figure 5.



$r_{ON}$  of SW 1 and SW 2  $\approx 5 \text{ k}\Omega$

$t = r_{ON} C_{STRAY} \approx 5 \text{ k}\Omega \times 12 \text{ pF} = 60 \text{ ns}$

FIGURE 5. Analog Input Impedance

The voltage on this capacitance is switched and will result in currents entering the  $V_{IN(+)}$  input pin and leaving the  $V_{IN(-)}$  input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

##### Fault Mode

If the voltage source applied to the  $V_{IN(+)}$  or  $V_{IN(-)}$  pin exceeds the allowed operating range of  $V_{CC} + 50 \text{ mV}$ , large input currents can flow through a parasitic diode to the  $V_{CC}$  pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the  $V_{CC}$  pin (with the current bypassed with this diode, the voltage at the  $V_{IN(+)}$  pin can exceed the  $V_{CC}$  voltage by the forward voltage of this diode).

#### 2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the  $V_{IN(+)}$  input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the  $V_{IN(+)}$  input at 5V, this DC current is at a maximum of approximately  $5 \mu\text{A}$ . Therefore, *bypass capacitors should not be used at the analog inputs or the  $V_{REF/2}$  pin for high resistance sources ( $> 1 \text{ k}\Omega$ )*. If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

#### 2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor ( $\leq 1 \text{ k}\Omega$ ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, ( $\leq 1 \text{ k}\Omega$ ), a  $0.1 \mu\text{F}$  bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long

## Functional Description (Continued)

wire. A 100Ω series resistor can be used to isolate this capacitor — both the R and C are placed outside the feedback loop — from the output of an op amp, if used.

### 2.3.4 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust  $V_{REF}/2$  for a proper full-scale reading — see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

## 2.4 Reference Voltage

### 2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5  $V_{DC}$ , 2.5  $V_{DC}$  or an adjusted voltage reference. This has been achieved in the design of the IC as shown in Figure 6.

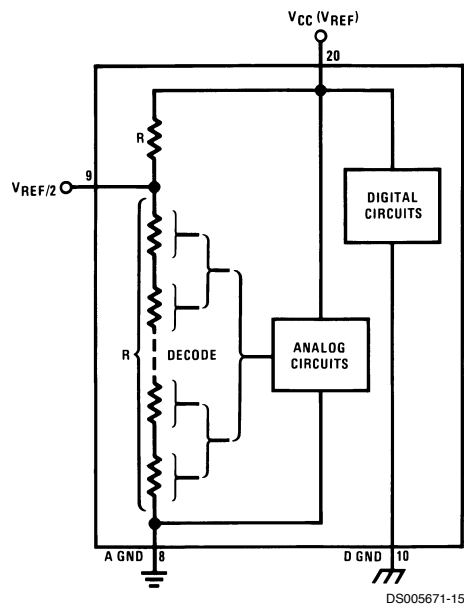


FIGURE 6. The  $V_{REFERENCE}$  Design on the IC

Notice that the reference voltage for the IC is either  $\frac{1}{2}$  of the voltage applied to the  $V_{CC}$  supply pin, or is equal to the voltage that is externally forced at the  $V_{REF}/2$  pin. This allows for a ratiometric voltage reference using the  $V_{CC}$  supply, a 5  $V_{DC}$  reference voltage can be used for the  $V_{CC}$  supply or a voltage less than 2.5  $V_{DC}$  can be applied to the  $V_{REF}/2$  input for increased application flexibility. The internal gain to the  $V_{REF}/2$  input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span — or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5  $V_{DC}$  to 3.5  $V_{DC}$ , instead of 0V to 5  $V_{DC}$ , the span would be 3V as shown in Figure 7. With 0.5  $V_{DC}$  applied to the  $V_{IN}(-)$  pin to absorb the offset, the reference voltage can be made equal to  $\frac{1}{2}$  of the 3V span or 1.5  $V_{DC}$ . The A/D now will encode the  $V_{IN}(+)$  signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5  $V_{DC}$  input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

### 2.4.2 Reference Accuracy Requirements

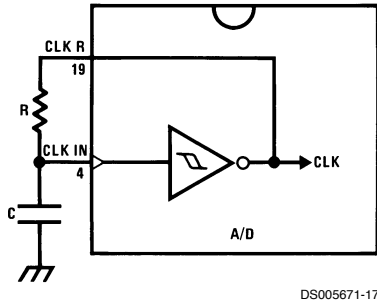
The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratio-metric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For  $V_{REF}/2$  voltages of 2.4  $V_{DC}$  nominal value, initial errors of  $\pm 10$  mV  $V_{DC}$  will cause conversion errors of  $\pm 1$  LSB due to the gain of 2 of the  $V_{REF}/2$  input. In reduced span applications, the initial value and the stability of the  $V_{REF}/2$  input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the  $V_{REF}/2$  input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ . Other temperature range parts are also available.





## Functional Description (Continued)



$$f_{CLK} \cong \frac{1}{1.1 RC}$$

$$R \cong 10 \text{ k}\Omega$$

**FIGURE 8. Self-Clocking the A/D**

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

### 2.7 Restart During a Conversion

If the A/D is restarted ( $\overline{CS}$  and  $\overline{WR}$  go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The  $\overline{INTR}$  output simply remains at the "1" level.

### 2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the  $\overline{CS}$  input is grounded and the  $\overline{WR}$  input is tied to the  $\overline{INTR}$  output. This  $\overline{WR}$  and  $\overline{INTR}$  node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

### 2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers

(low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

### 2.10 Power Supplies

Noise spikes on the  $V_{CC}$  supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter  $V_{CC}$  pin and values of 1  $\mu$ F or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the  $V_{CC}$  supply.

### 2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

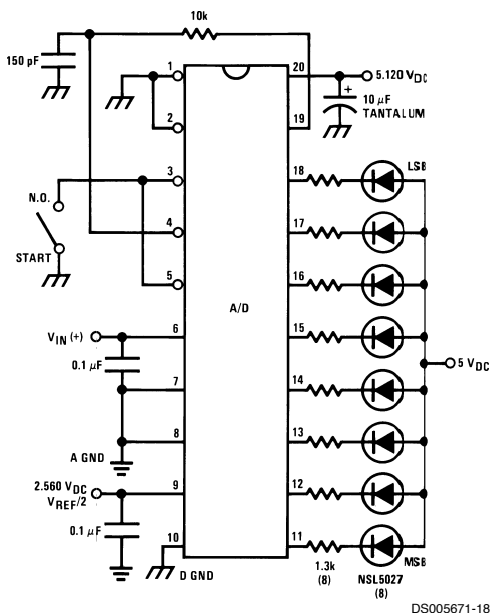
A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any  $V_{REF}/2$  bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of  $1/4$  LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

### 3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 9. For ease of testing, the  $V_{REF}/2$  (pin 9) should be supplied with 2.560  $V_{DC}$  and a  $V_{CC}$  supply voltage of 5.12  $V_{DC}$  should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090  $V_{DC}$  (5.120– $1\frac{1}{2}$  LSB) should be applied to the  $V_{IN}(+)$  pin with the  $V_{IN}(-)$  pin grounded. The value of the  $V_{REF}/2$  input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of  $V_{REF}/2$  should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table 1 shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in Table 1, the nominal value of the digital display (when  $V_{REF}/2 = 2.560V$ ) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are  $3.520 + 0.120$  or 3.640  $V_{DC}$ . These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.



For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, “A–C”, directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 11*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides  $\frac{1}{4}$  LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

#### 4.0 MICROPROCESSOR INTERFACING

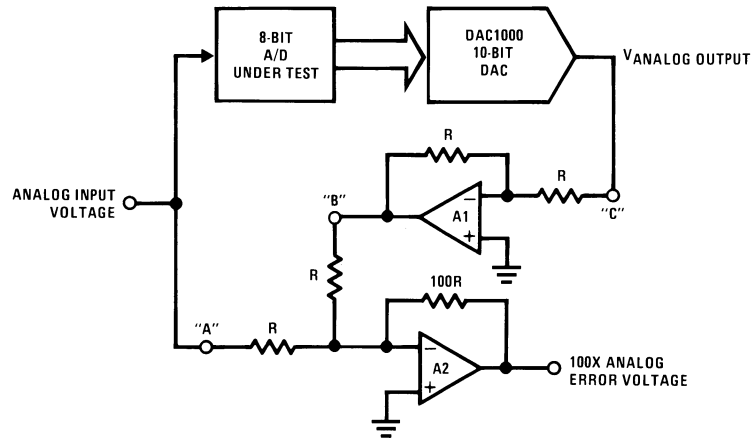
To discuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

#### 4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for  $\overline{CS}$  and the  $\overline{MEMR}$  and  $\overline{MEMW}$  strobes) or it can be controlled as an I/O device by using the  $\overline{I/O R}$  and  $\overline{I/O W}$  strobes and decoding the address bits A0  $\rightarrow$  A7 (or address bits A8  $\rightarrow$  A15 as they will contain the same 8-bit address information) to obtain the  $\overline{CS}$  input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 12*.

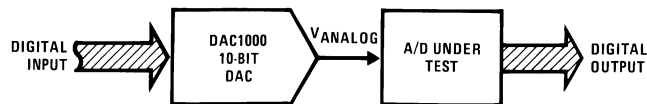


## Functional Description (Continued)



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FIGURE 10. A/D Tester with Analog Error Output



DS005671-90

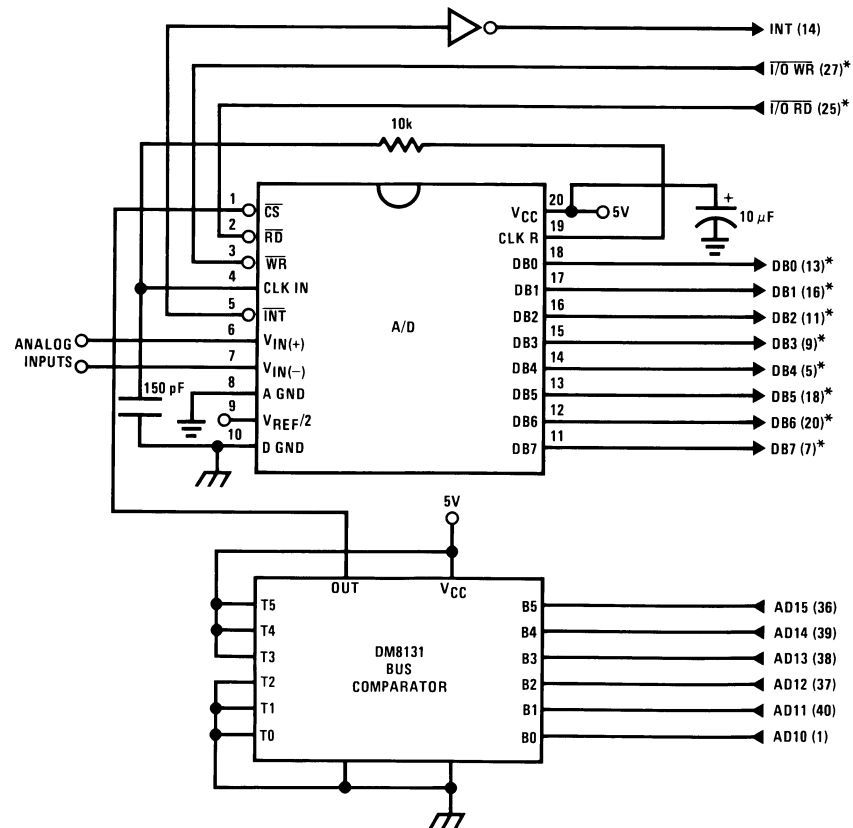
FIGURE 11. Basic "Digital" A/D Tester

TABLE 1. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560 V_{DC}$	
		MS GROUP	LS GROUP	VMS GROUP (Note 15)	VLS GROUP (Note 15)
F	1 1 1 1	15/16	15/256	4.800	0.300
E	1 1 1 0	7/8	7/128	4.480	0.280
D	1 1 0 1	13/16	13/256	4.160	0.260
C	1 1 0 0	3/4	3/64	3.840	0.240
B	1 0 1 1	11/16	11/256	3.520	0.220
A	1 0 1 0	5/8	5/128	3.200	0.200
9	1 0 0 1	9/16	9/256	2.880	0.180
8	1 0 0 0	1/2	1/32	2.560	0.160
7	0 1 1 1	7/16	7/256	2.240	0.140
6	0 1 1 0	3/8	3/128	1.920	0.120
5	0 1 0 1	5/16	2/256	1.600	0.100
4	0 1 0 0	1/4	1/64	1.280	0.080
3	0 0 1 1	3/16	3/256	0.960	0.060
2	0 0 1 0	1/8	1/128	0.640	0.040
1	0 0 0 1	1/16	1/256	0.320	0.020
0	0 0 0 0			0	0

Note 15: Display Output = VMS Group + VLS Group

## Functional Description (Continued)



DS005671-20

**Note 16:** \*Pin numbers for the DP8228 system controller, others are INS8080A.

**Note 17:** Pin 23 of the INS8228 must be tied to +12V through a 1 k $\Omega$  resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

**FIGURE 12. ADC0801\_INS8080A CPU Interface**

## Functional Description (Continued)

### SAMPLE PROGRAM FOR *Figure 12* ADC0801-INS8080A CPU INTERFACE

0038	C3 00 03	RST 7:	JMP	LD DATA	
.	.	.			
.	.	.			
0100	21 00 02	START:	LXI H 0200H		; HL pair will point to
					; data storage locations
0103	31 00 04	RETURN:	LXI SP 0400H		; Initialize stack pointer (Note 1)
0106	7D		MOV A, L		; Test # of bytes entered
0107	FE 0F		CPI 0FH		; If # = 16. JMP to
0109	CA 13 01		JZ CONT		; user program
010C	D3 E0		OUT E0 H		; Start A/D
010E	FB		EI		; Enable interrupt
010F	00	LOOP:	NOP		; Loop until end of
0110	C3 0F 01		JMP LOOP		; conversion
0113	.	CONT:	.		
.	.	.	.		
.	.	(User program to	.		
.	.	process data)	.		
.	.	.	.		
.	.	.	.		
0300	DB E0	LD DATA:	IN E0 H		; Load data into accumulator
0302	77		MOV M, A		; Store data
0303	23		INX H		; Increment storage pointer
0304	C3 03 01		JMP RETURN		

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**Note 18:** The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

**Note 19:** All address used were arbitrarily chosen.

The standard control bus signals of the 8080 ( $\overline{\text{CS}}$ ,  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$ ) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

#### 4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

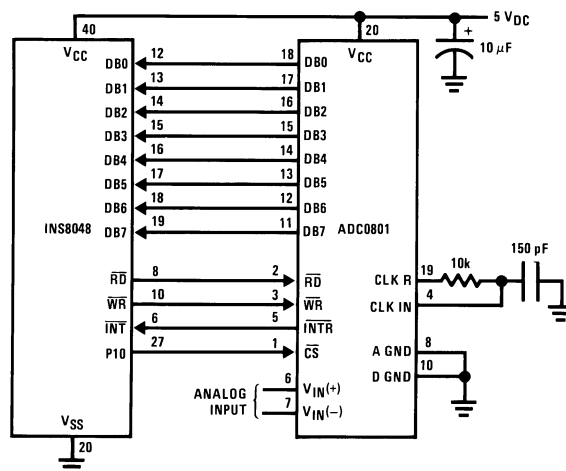
The following sample program and associated hardware shown in *Figure 12* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate  $\overline{\text{CS}}$  for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as  $\overline{\text{CS}}$  inputs — one for each I/O device.

#### 4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 13*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals  $\overline{RD}$ ,  $\overline{WR}$  and  $\overline{INT}$  of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The  $\overline{RD}$  and  $\overline{WR}$  signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

## Functional Description (Continued)



DS005671-21

FIGURE 13. INS8048 Interface

### SAMPLE PROGRAM FOR Figure 13 INS8048 INTERFACE

```

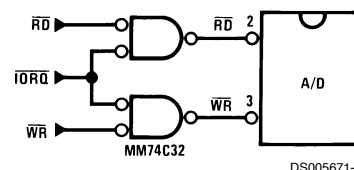
04 10          JMP      10H          : Program starts at addr 10
          ORG      3H
04 50          JMP      50H          ; Interrupt jump vector
          ORG      10H              ; Main program
99 FE          ANL      P1, #0FEH    ; Chip select
81             MOVX     A, @R1       ; Read in the 1st data
          ; to reset the intr
89 01          START:  ORL      P1, #1 ; Set port pin high
B8 20          MOV      RO, #20H     ; Data address
B9 FF          MOV      R1, #0FFH    ; Dummy address
BA 10          MOV      R2, #10H     ; Counter for 16 bytes
23 FF          AGAIN:  MOV      A, #0FFH ; Set ACC for intr loop
99 FE          ANL      P1, #0FEH    ; Send CS (bit 0 of P1)
91             MOVX     @R1, A       ; Send WR out
05             EN      I            ; Enable interrupt
96 21          LOOP:   JNZ      LOOP ; Wait for interrupt
EA 1B          DJNZ     R2, AGAIN     ; If 16 bytes are read
00             NOP
00             NOP
          ORG      50H
81             MOVX     A, @R1       ; Input data, CS still low
A0             MOV      @RO, A       ; Store in memory
18             INC      RO          ; Increment storage counter
89 01          ORL      P1, #1       ; Reset CS signal
27             CLR      A           ; Clear ACC to get out of
93             RETR              ; the interrupt loop

```

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### 4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General  $\overline{RD}$  and  $\overline{WR}$  strobes are provided and separate memory request,  $\overline{MREQ}$ , and I/O request,  $\overline{IORQ}$ , signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the  $\overline{RD}$  and  $\overline{WR}$  strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 14.



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FIGURE 14. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to

## Functional Description (Continued)

A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

### 4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the  $\overline{RD}$  and  $\overline{WR}$  strobe signals. Instead it employs a single  $\overline{R/\overline{W}}$  line and additional timing, if needed, can be derived from the  $\phi 2$  clock. All I/O devices are memory mapped in the 6800 system, and a special signal,  $\overline{VMA}$ , indicates that the current address is valid. *Figure 15* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the  $\overline{CS}$  decoding is shown using  $\frac{1}{2}$  DM8092. Note that in many 6800 systems, an already decoded  $\overline{4/5}$  line is brought out to the common bus at pin 21. This can be tied directly to the  $\overline{CS}$  pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 16* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the  $\overline{\text{CS}}$  pin of the A/D is grounded since the PIA is

already memory mapped in the M6800 system and no  $\overline{CS}$  decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D  $\overline{RD}$  pin can be grounded.

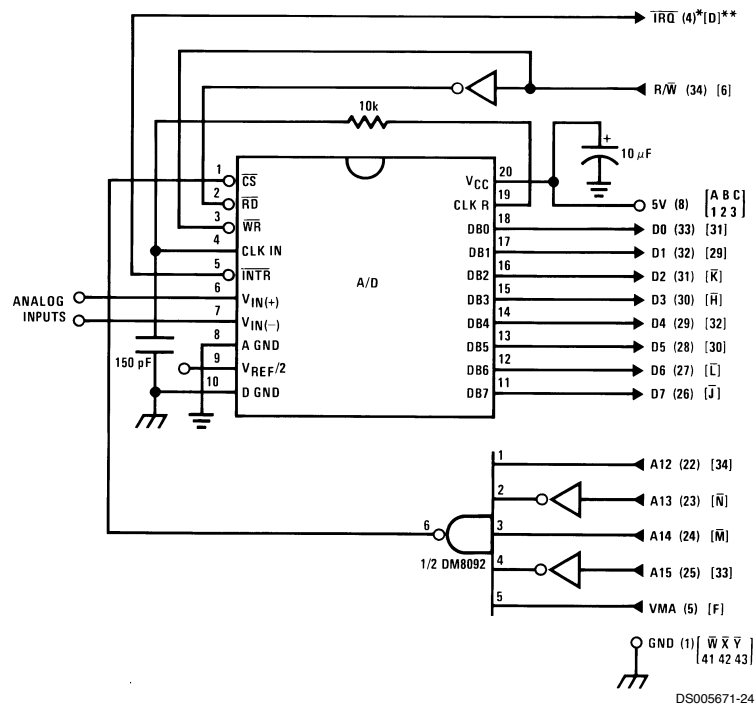
A sample interface program equivalent to the previous one is shown below *Figure 16*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

## 5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

## 5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 17*.



**Note 20:** Numbers in parentheses refer to MC6800 CPU pin out.

**Note 21:** Number or letters in brackets refer to standard M6800 system common bus code.

**FIGURE 15. ADC0801-MC6800 CPU Interface**

## Functional Description (Continued)

### SAMPLE PROGRAM FOR Figure 15 ADC0801-MC6800 CPU INTERFACE

```

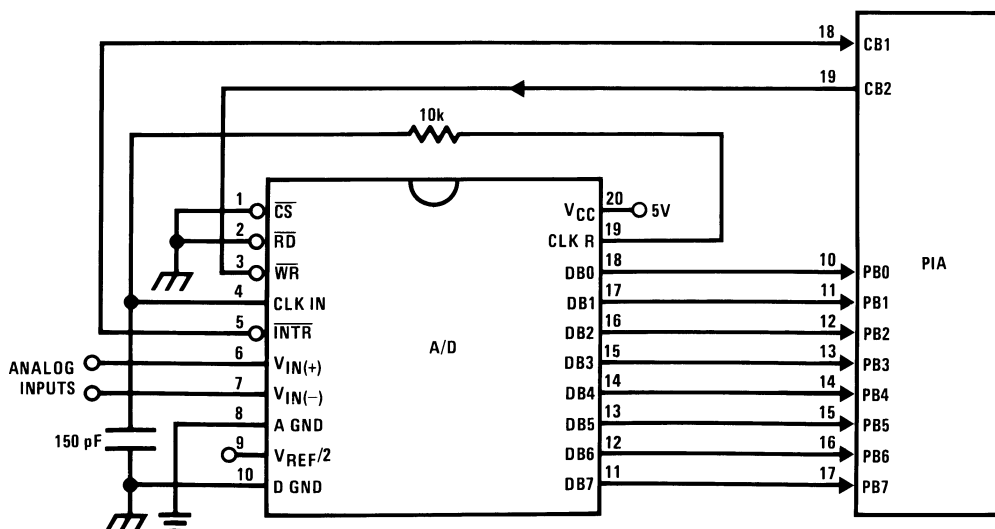
0010    DF 36          DATAIN    STX      TEMP2          ; Save contents of X
0012    CE 00 2C          LDX      #$002C          ; Upon IRQ low CPU
0015    FF FF F8          STX      $FFF8          ; jumps to 002C
0018    B7 50 00          STAA     $5000          ; Start ADC0801
001B    0E              CLI              ;
001C    3E          CONVRT    WAI              ; Wait for interrupt
001D    DE 34          LDX      TEMP1
001F    8C 02 0F          CPX      #$020F          ; Is final data stored?
0022    27 14          BEQ      ENDP
0024    B7 50 00          STAA     $5000          ; Restarts ADC0801
0027    08              INX
0028    DF 34          STX      TEMP1
002A    20 F0          BRA      CONVRT
002C    DE 34          INTRPT    LDX      TEMP1
002E    B6 50 00          LDAA     $5000          ; Read data
0031    A7 00          STAA     X              ; Store it at X
0033    3B              RTI
0034    02 00          TEMP1    FDB      $0200          ; Starting address for
                                          ; data storage

0036    00 00          TEMP2    FDB      $0000
0038    CE 02 00          ENDP    LDX      #$0200          ; Reinitialize TEMP1
003B    DF 34          STX      TEMP1
003D    DE 36          LDX      TEMP2
003F    39              RTS              ; Return from subroutine
                                          ; To user's program

```

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**Note 22:** In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.



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FIGURE 16. ADC0801-MC6820 PIA Interface

## Functional Description (Continued)

### SAMPLE PROGRAM FOR Figure 16 ADC0801–MC6820 PIA INTERFACE

```

0010    CE 00 38      DATAIN    LDX      #$0038      ; Upon  $\overline{\text{IRQ}}$  low CPU
0013    FF FF F8      STX        $FFF8      ; jumps to 0038
0016    B6 80 06      LDAA       PIAORB      ; Clear possible  $\overline{\text{IRQ}}$  flags
0019    4F            CLRA
001A    B7 80 07      STAA       PIACRB
001D    B7 80 06      STAA       PIAORB      ; Set Port B as input
0020    0E            CLI
0021    C6 34          LDAB       #$34
0023    86 3D          LDAA       #$3D
0025    F7 80 07      CONVRT     STAB       PIACRB      ; Starts ADC0801
0028    B7 80 07      STAA       PIACRB
002B    3E            WAI          ; Wait for interrupt
002C    DE 40          LDX        TEMP1
002E    8C 02 0F      CPX        #$020F      ; Is final data stored?
0031    27 0F          BEQ        ENDP
0033    08            INX
0034    DF 40          STX        TEMP1
0036    20 ED          BRA        CONVRT
0038    DE 40          INTRPT     LDX        TEMP1
003A    B6 80 06      LDAA       PIAORB      ; Read data in
003D    A7 00          STAA       X          ; Store it at X
003F    3B            RTI
0040    02 00          TEMP1     FDB       $0200      ; Starting address for
                                           ; data storage
0042    CE 02 00      ENDP        LDX        #$0200      ; Reinitialize TEMP1
0045    DF 40          STX        TEMP1
0047    39            RTS          ; Return from subroutine
                                           ; To user's program
           PIAORB      EQU        $8006
           PIACRB      EQU        $8007

```

DS005671-A2

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the  $\overline{\text{CS}}$  inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the

CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

### 5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.





## Functional Description (Continued)

### SAMPLE PROGRAM FOR Figure 17 INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#\$002A	; Upon IRQ LOW CPU
0015	FF FF F8		STX	\$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	\$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#\$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#\$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

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### SAMPLE PROGRAM FOR Figure 17 INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#\$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	\$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	\$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	\$0000	

DS005671-A4

**Note 25:** In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. Figure 18 is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50  $\mu$ V for  $\frac{1}{4}$  LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN(+)} - V_{IN(-)}]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R_2}{R_1}\right]}_{\text{GAIN}} + \underbrace{(V_{OS2} - V_{OS1} - V_{OS3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R_2}{R_1}\right)}_{\text{GAIN}}$$

where  $I_X$  is the current through resistor  $R_X$ . All of the offset error terms can be cancelled by making  $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$ . This is the principle of this auto-zeroing scheme.

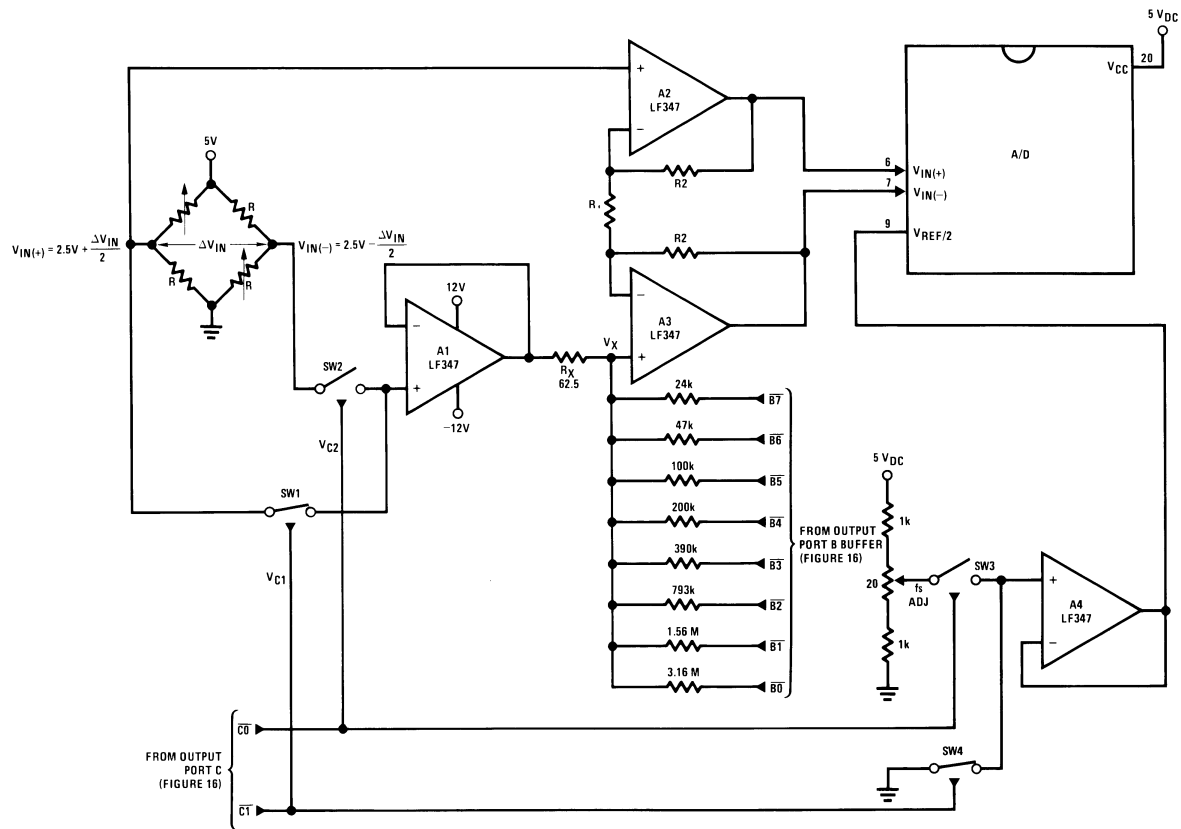
The INS8080A uses the 3 I/O ports of an INS8255 Programmable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in Figure 19. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at  $V_X$  increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on

## Functional Description (Continued)

any output of Port B will source current into node  $V_X$  thus raising the voltage at  $V_X$  and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node  $V_X$  and decrease the voltage, causing the differential output to become more positive. For the resistor values shown,  $V_X$  can move  $\pm 12$  mV with a resolution of  $50 \mu\text{V}$ , which will null the offset error term to  $1/4$  LSB of full-scale for

the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



**Note 26:**  $R2 = 49.5 R1$

**Note 27:** Switches are LMC13334 CMOS analog switches.

**Note 28:** The 9 resistors used in the auto-zero section can be  $\pm 5\%$  tolerance.

**FIGURE 18. Gain of 100 Differential Transducer Preamp**

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## Functional Description (Continued)

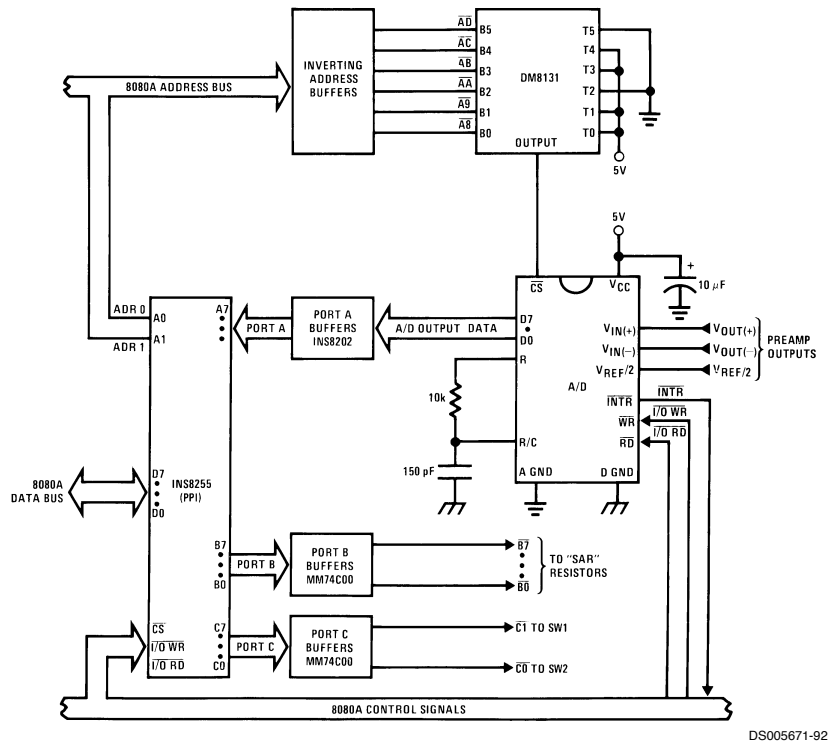


FIGURE 19. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 20*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [ $V_{IN(-)} \geq V_{IN(+)}$ ]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull  $V_X$  more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make  $V_X$  more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 21*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

- Port A and the ADC0801 are at port address E4
- Port B is at port address E5
- Port C is at port address E6
- PPI control word port is at port address E7
- Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

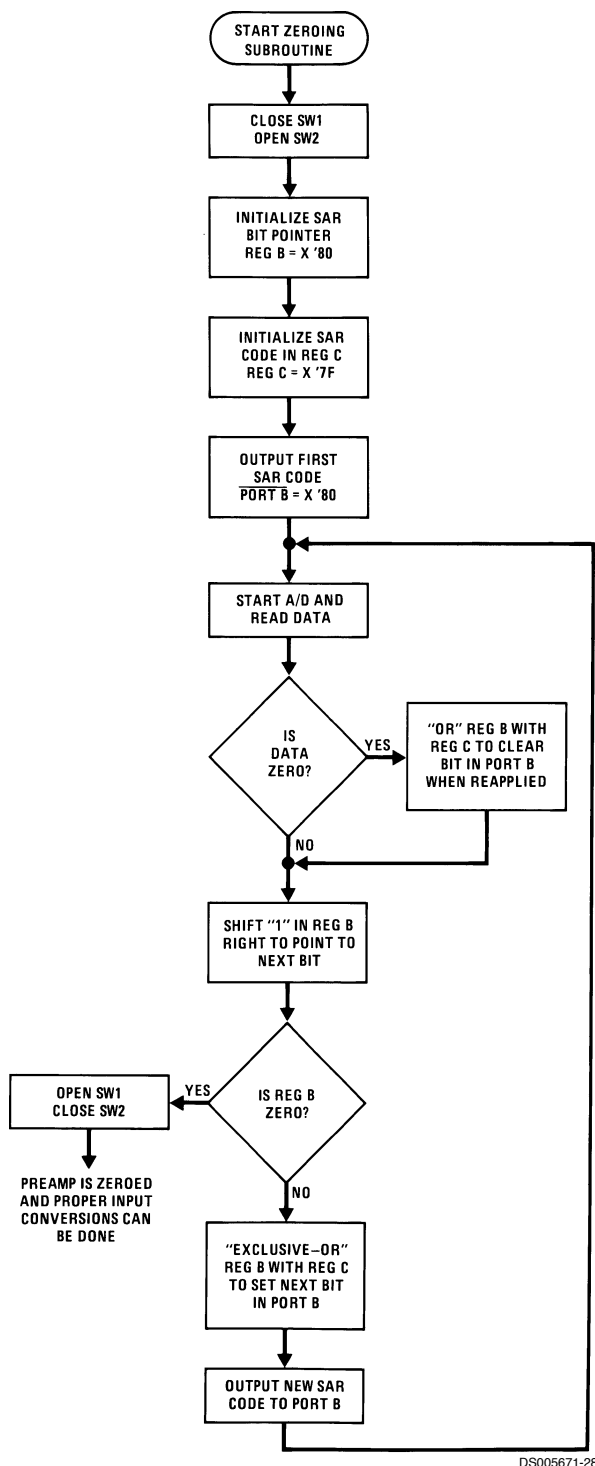
### 5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a

need for the CPU to determine which device requires servicing. *Figure 22* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ( $\overline{INTR}$  asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the  $\overline{INTR}$  outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

# Functional Description (Continued)



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FIGURE 20. Flow Chart for Auto-Zero Routine

## Functional Description (Continued)

3D00	3E90	MVI 90		
3D02	D3E7	Out Control Port		; Program PPI
3D04	2601	MVI H 01	Auto-Zero Subroutine	
3D06	7C	MOV A,H		
3D07	D3E6	OUT C		; Close SW1 open SW2
3D09	0680	MVI B 80		; Initialize SAR bit pointer
3D0B	3E7F	MVI A 7F		; Initialize SAR code
3D0D	4F	MOV C,A	Return	
3D0E	D3E5	OUT B		; Port B = SAR code
3D10	31AA3D	LXI SP 3DAA	Start	; Dimension stack pointer
3D13	D3E4	OUT A		; Start A/D
3D15	FB	IE		
3D16	00	NOP	Loop	; Loop until $\overline{\text{INT}}$ asserted
3D17	C3163D	JMP Loop		
3D1A	7A	MOV A,D	Auto-Zero	
3D1B	C600	ADI 00		
3D1D	CA2D3D	JZ Set C		; Test A/D output data for zero
3D20	78	MOV A,B	Shift B	
3D21	F600	ORI 00		; Clear carry
3D23	1F	RAR		; Shift "1" in B right one place
3D24	FE00	CPI 00		; Is B zero? If yes last
3D26	CA373D	JZ Done		; approximation has been made
3D29	47	MOV B,A		
3D2A	C3333D	JMP New C		
3D2D	79	MOV A,C	Set C	
3D2E	B0	ORA B		; Set bit in C that is in same
3D2F	4F	MOV C,A		; position as "1" in B
3D30	C3203D	JMP Shift B		
3D33	A9	XRA C	New C	; Clear bit in C that is in
3D34	C30D3D	JMP Return		; same position as "1" in B
3D37	47	MOV B,A	Done	; then output new SAR code.
3D38	7C	MOV A,H		; Open SW1, close SW2 then
3D39	EE03	XRI 03		; proceed with program. Preamp
3D3B	D3E6	OUT C		; is now zeroed.
3D3D		•	Normal	
		•		
		•		
		Program for processing proper data values		
3C3D	DBE4	IN A	Read A/D Subroutine	; Read A/D data
3C3F	EEFF	XRI FF		; Invert data
3C41	57	MOV D,A		
3C42	78	MOV A,B		; Is B Reg = 0? If not stay
3C43	E6FF	ANI FF		; in auto zero subroutine
3C45	C21A3D	JNZ Auto-Zero		
3C48	C33D3D	JMP Normal		

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**Note 29:** All numerical values are hexadecimal representations.

**FIGURE 21. Software for Auto-Zeroed Differential A/D**

### 5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode (Continued)

The following notes apply:

- It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.
- The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.
- A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.

- The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.
- The peripherals of concern are mapped into I/O space with the following port assignments:



## Functional Description (Continued)

### INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE	SOURCE STATEMENT	COMMENT
0038	E5	PUSH HL	; Save contents of all registers affected by
0039	C5	PUSH BC	; this subroutine.
003A	F5	PUSH AF	; Assumed INT mode 1 earlier set.
003B	21 00 3E	LD (HL), X3E00	; Initialize memory pointer where data will be stored.
003E	0E 01	LD C, X01	; C register will be port ADDR of A/D converters.
0040	D300	OUT X00, A	; Load peripheral status word into 8-bit latch.
0042	DB00	IN A, X00	; Load status word into accumulator.
0044	47	LD B, A	; Save the status word.
0045	79	TEST LD A, C	; Test to see if the status of all A/D's have
0046	FE 08	CP, X08	; been checked. If so, exit subroutine
0048	CA 60 00	JPZ, DONE	
004B	78	LD A, B	; Test a single bit in status word by looking for
004C	1F	RRA	; a "1" to be rotated into the CARRY (an INT
004D	47	LD B, A	; is loaded as a "1"). If CARRY is set then load
004E	DA 5500	JPC, LOAD	; contents of A/D at port ADDR in C register.
0051	0C	NEXT INC C	; If CARRY is not set, increment C register to point
0052	C3 4500	JP, TEST	; to next A/D, then test next bit in status word.
0055	ED 78	LOAD IN A, (C)	; Read data from interrupting A/D and invert
0057	EE FF	XOR FF	; the data.
0059	77	LD (HL), A	; Store the data
005A	2C	INC L	
005B	71	LD (HL), C	; Store A/D identifier (A/D port ADDR).
005C	2C	INC L	
005D	C3 51 00	JP, NEXT	; Test next bit in status word.
0060	F1	DONE POP AF	; Re-establish all registers as they were
0061	C1	POP BC	; before the interrupt.
0062	E1	POP HL	
0063	C9	RET	; Return to original program

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## Notes

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