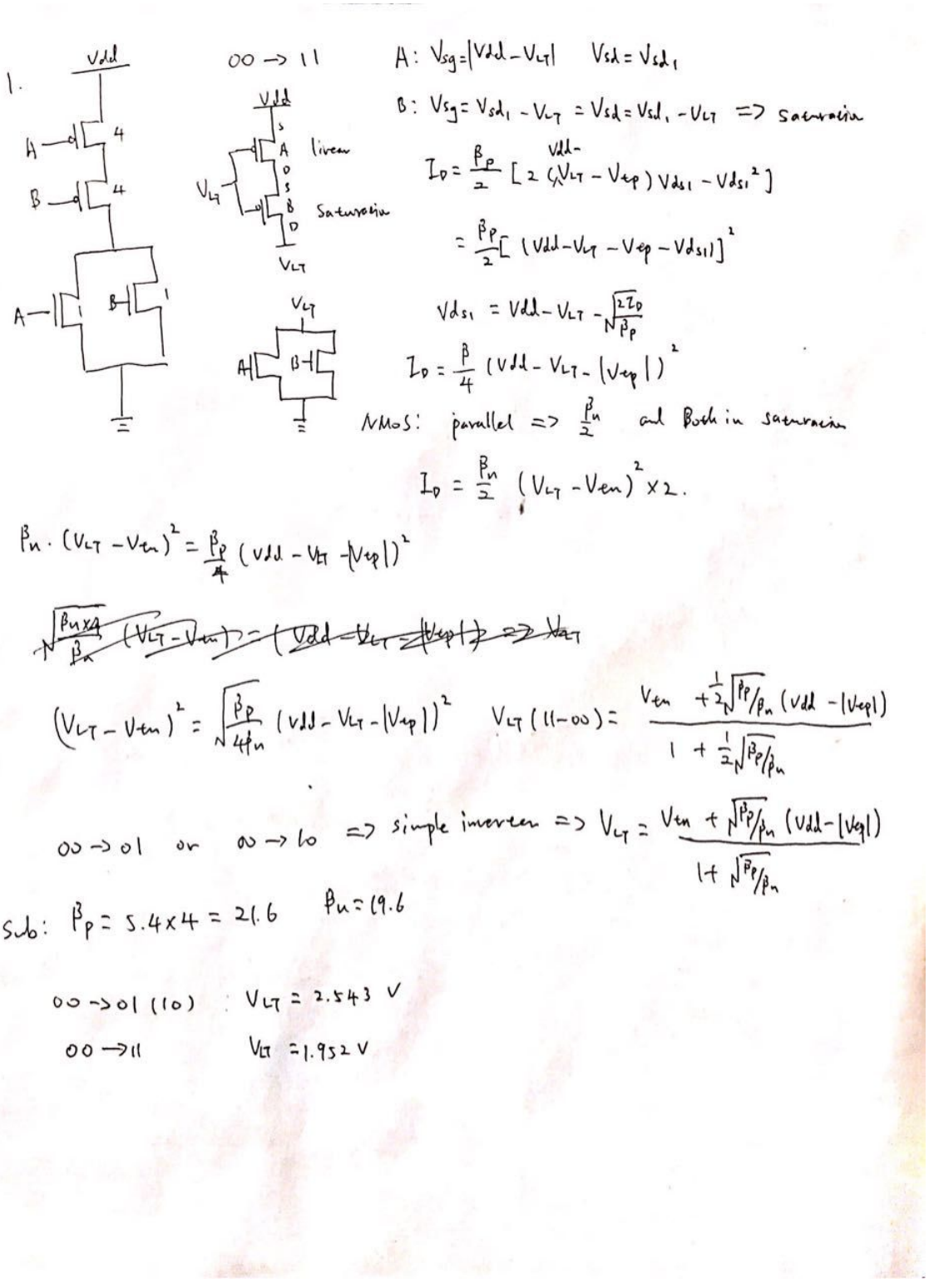
HW5
Youzhe Dou

1.



$$t_r = \frac{C_L}{\beta_p (V_H - |V_{tp}|)} \left\{ \frac{2|V_{tp}|}{V_H - |V_{tp}|} + \ln\left[\frac{2(V_H - |V_{tp}|)}{V_L} - 1 \right] \right\} = 0.0374\ \mu s$$

$\begin{matrix} 01 \\ 10 \end{matrix} \rightarrow 00 \quad t_r' = t_r = 0.0374\ \mu s$

$11 \rightarrow 00 \quad t_r' = 2t_r = 0.0748\ \mu s$

$$t_f = \frac{C_L}{\beta_n (V_H - V_{tn})} \left\{ \frac{2V_{tn}}{V_H - V_{tn}} + \ln\left[\frac{2[V_H - V_{tn}]}{V_L} - 1 \right] \right\} = 0.0412\ \mu s$$

$00 \rightarrow 01$ or $10 \quad t_f' = t_f = 0.0412\ \mu s$

$00 \rightarrow 11 \quad t_f' = \frac{1}{2} t_f = 0.0206\ \mu s$

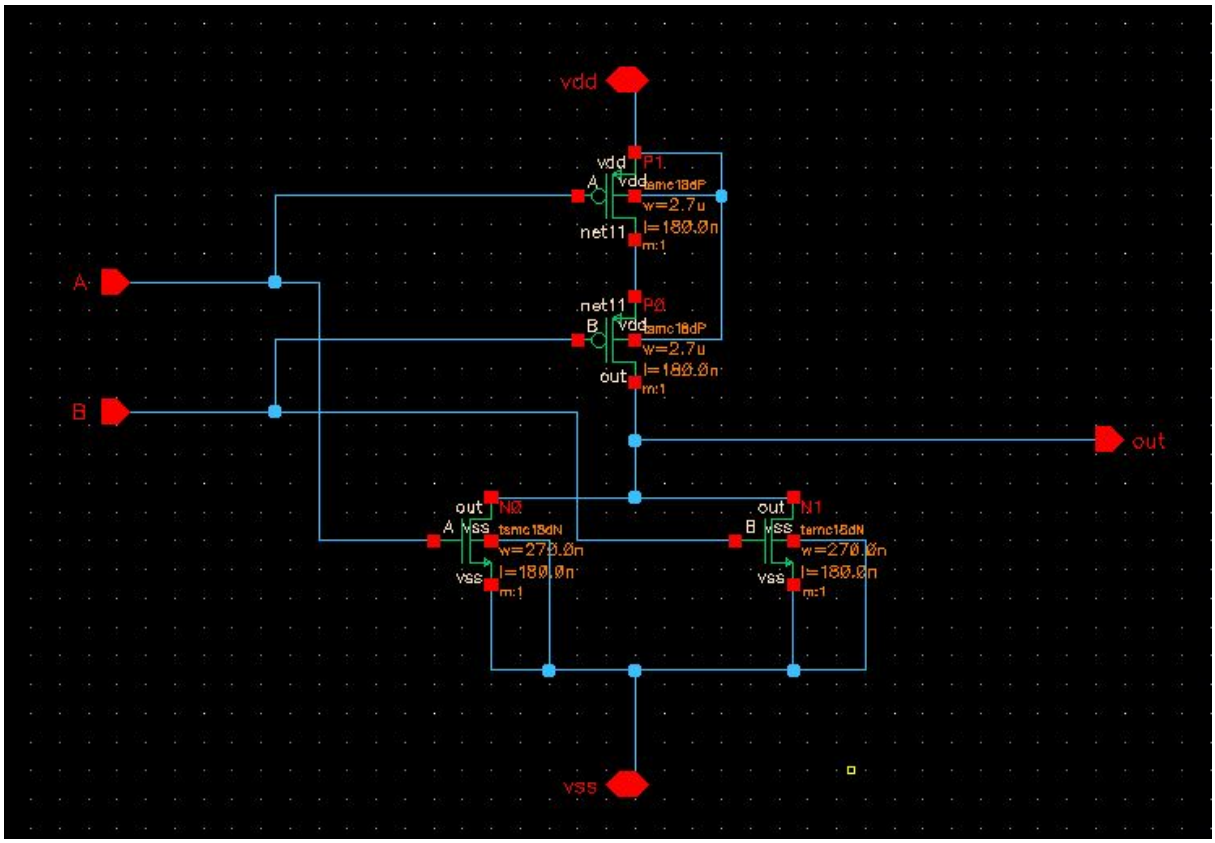
2.

(a)

For a 2-inputs NOR gate, the worst case rising time should be the transition (11-00) and the worst case falling time should be the transition (00-01). After some adjustment to equalize the worst rise and fall time, I came to the following W/L ratio for each gate:

PMOS: 30/2 (2700 nm / 180 nm)

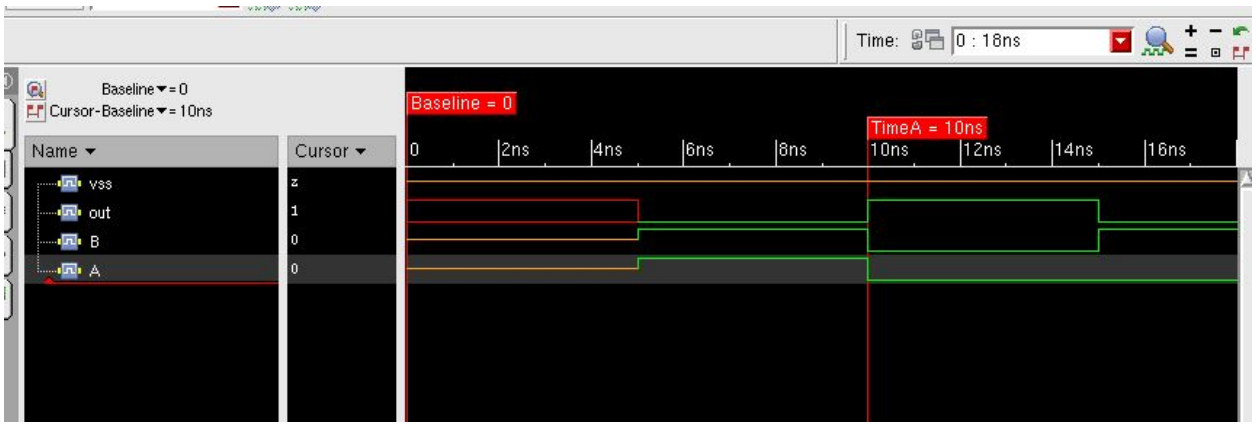
NMOS: 3/2 (270 nm / 180 nm)



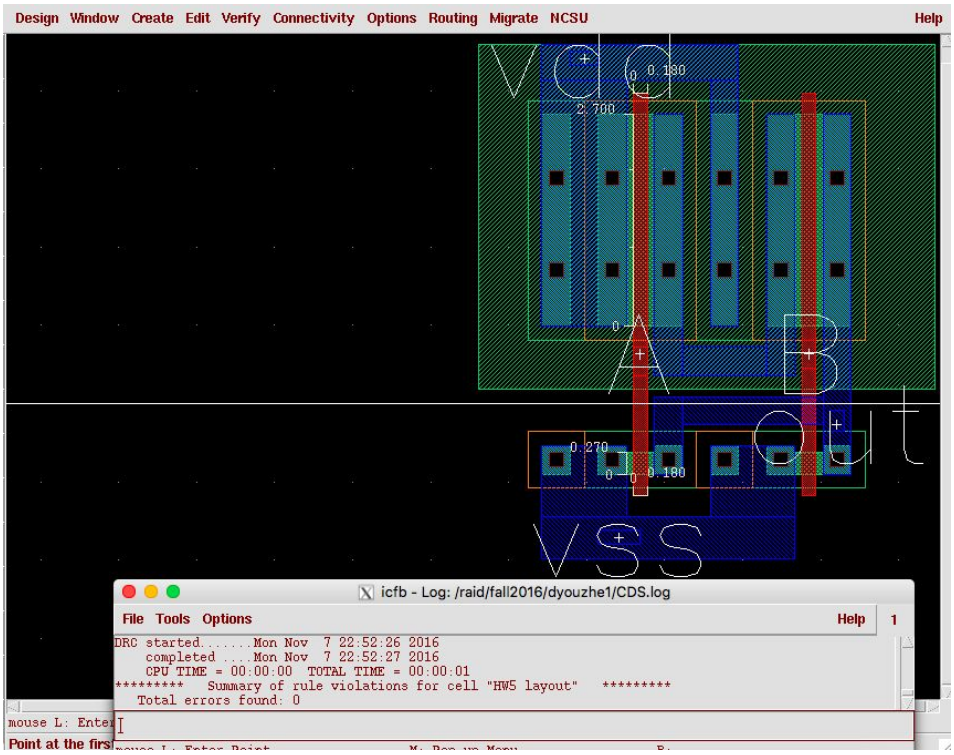
(b)

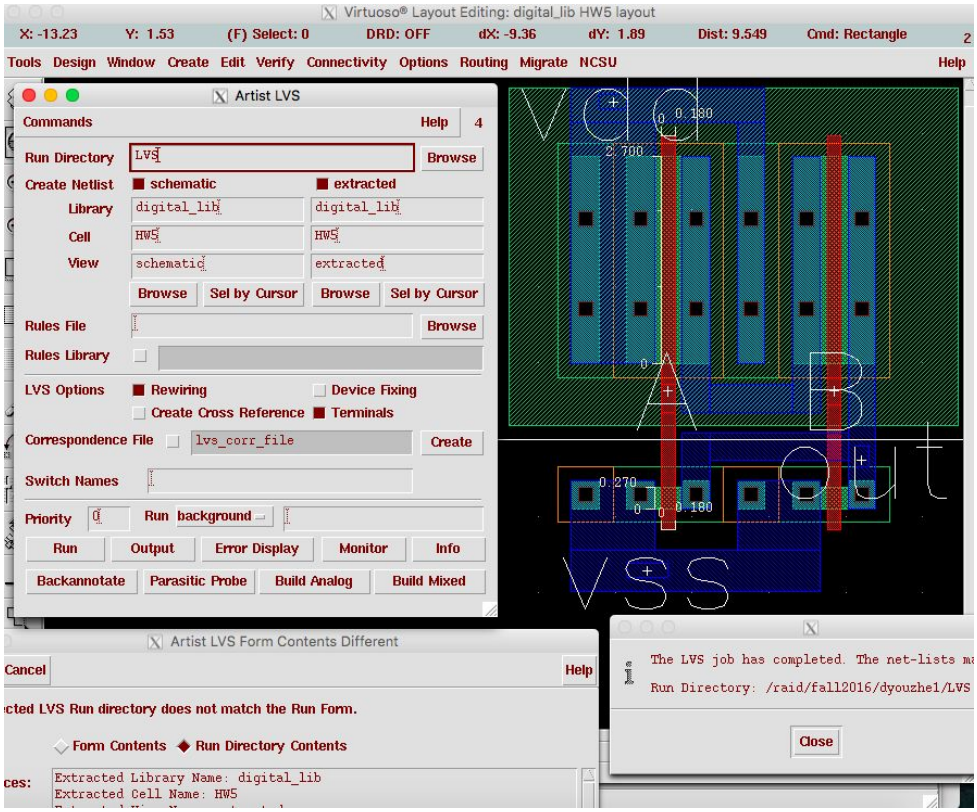
```
module HW5 (A, B, out, vdd, vss );
inout vdd,vss,A,B,out;
nor #0.03 net1(out,A,B);
endmodule


// Verilog stimulus file.
// Please do not create a module in this file.
// Default verilog stimulus.
```

```
initial
begin
   io_A = 1'bz;
   io_B = 1'bz;
   io_out = 1'bz;
   io_vdd = 1'bz;
   io_vss = 1'bz;
#5
   io_A = 1'b1;
   io_B = 1'b1;
#5
   io_A = 1'b0;
   io_B = 1'b0;
#5
   io_A = 1'b0;
   io_B = 1'b1;
#20 $finish;
end
```



(c)


Design Window Create Edit Verify Connectivity Options Routing Migrate NCSU Help
VDD
0.130
2.700
A
B
out
0.270
0.180
VSS
icfb - Log: /raid/fall2016/dyouzhe1/CDS.log
File Tools Options Help 1
DRC started.....Mon Nov 7 22:52:26 2016
completed ....Mon Nov 7 22:52:27 2016
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
********* Summary of rule violations for cell "HW5 layout" *********
Total errors found: 0
mouse L: Ente
Point at the firs


Virtuoso® Layout Editing: digital_lib HW5 layout
X: -13.23 Y: 1.53 (F) Select: 0 DRD: OFF dX: -9.36 dY: 1.89 Dist: 9.549 Cmd: Rectangle
Tools Design Window Create Edit Verify Connectivity Options Routing Migrate NCSU Help
Artist LVS
Commands Help 4
Run Directory LVS Browse
Create Netlist schematic extracted
Library digital_lib digital_lib
Cell HW5 HW5
View schematic extracted
Browse Sel by Cursor Browse Sel by Cursor
Rules File Browse
Rules Library
LVS Options Rewiring Device Fixing
Create Cross Reference Terminals
Correspondence File lvs_corr_file Create
Switch Names
Priority 0 Run background
Run Output Error Display Monitor Info
Backannotate Parasitic Probe Build Analog Build Mixed
VCC
A
B
Out
VSS
Artist LVS Form Contents Different
Cancel Help
cted LVS Run directory does not match the Run Form.
Form Contents Run Directory Contents
ces:
Extracted Library Name: digital_lib
Extracted Cell Name: HW5
The LVS job has completed. The net-lists ma
Run Directory: /raid/fall2016/dyouzhe1/LVS
Close

/raid/fall2016/dyouzhe1/LVS/si.out

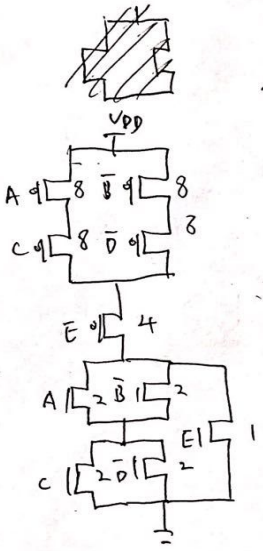
File Help 5

```
@(#)$CDS: LVS.exe version 5.1.0 11/22/2011 01:35 (cicln04) $

Command line: /cadence/installs/IC5141/tools.lnx86/dfII/bin/32bit/LVS.exe -dir /raid/fall2016/dyouzhe1/LVS -l -s -t /raid/fal
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

    Net-list summary for /raid/fall2016/dyouzhe1/LVS/layout/netlist
       count
           6               nets
           5               terminals
           2               pmos
           2               nmos

    Net-list summary for /raid/fall2016/dyouzhe1/LVS/schematic/netlist
       count
           6               nets
           5               terminals
           2               pmos
           2               nmos


    Terminal correspondence points
    N1          N1          A
    N3          N3          B
    N5          N4          out
    N2          N2          vdd
    N0          N0          vss

Devices in the netlist but not in the rules:
       pmos nmos

The net-lists match.

                               layout  schematic
                                  instances
       un-matched                  0       0
       rewired                     0       0
       size errors                 0       0
       pruned                      0       0
       active                      4       4
       total                       4       4

                                    nets
```

(d)

2(d)

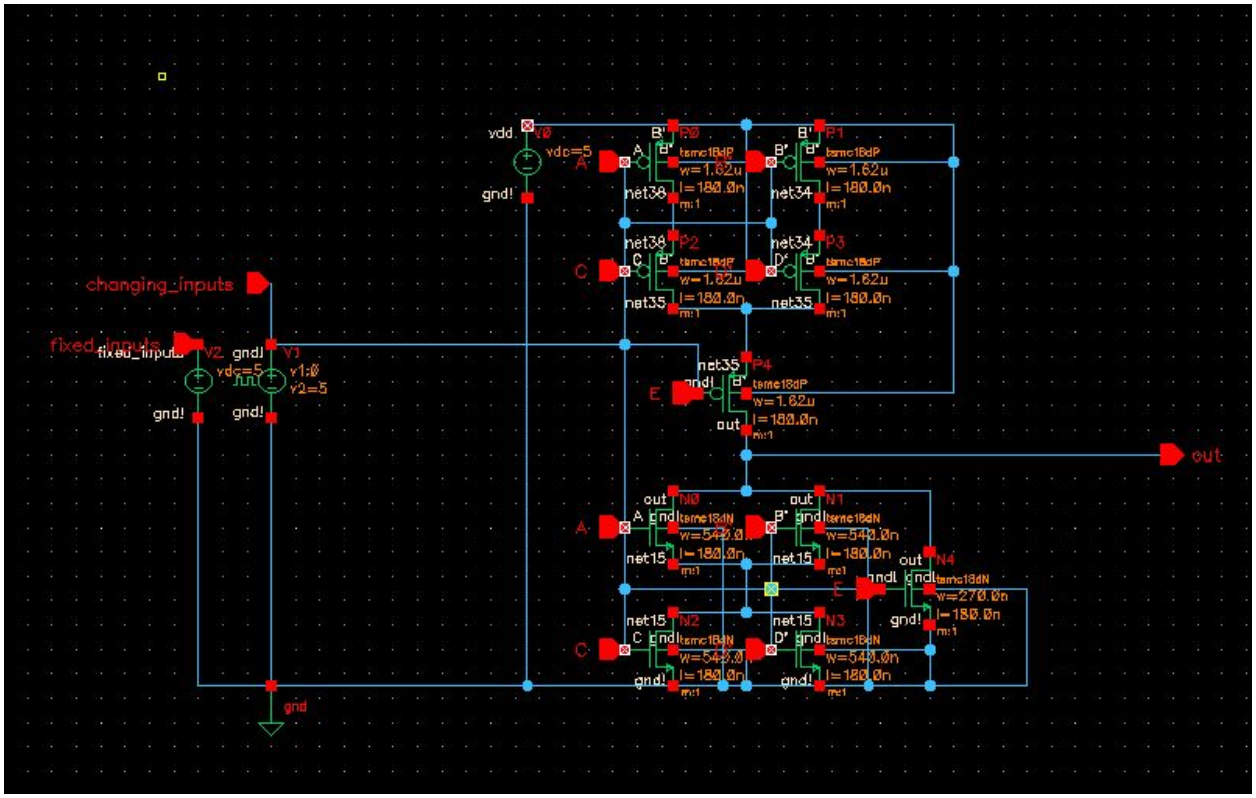
$$F = (\bar{A}B + \bar{C}D)\bar{E} = \overline{\overline{(\bar{A}B + \bar{C}D)\bar{E}}} = \overline{(A+\bar{B})\cdot(C+\bar{D}) + E}$$

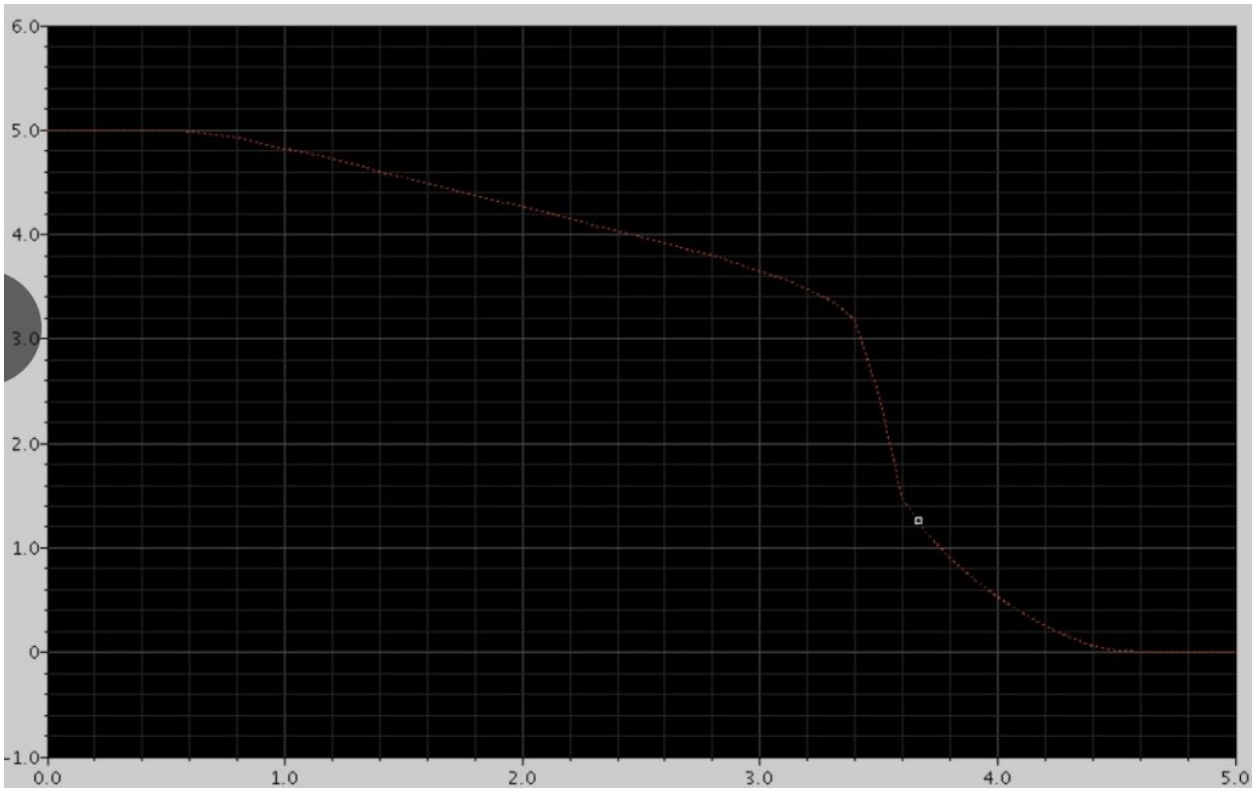


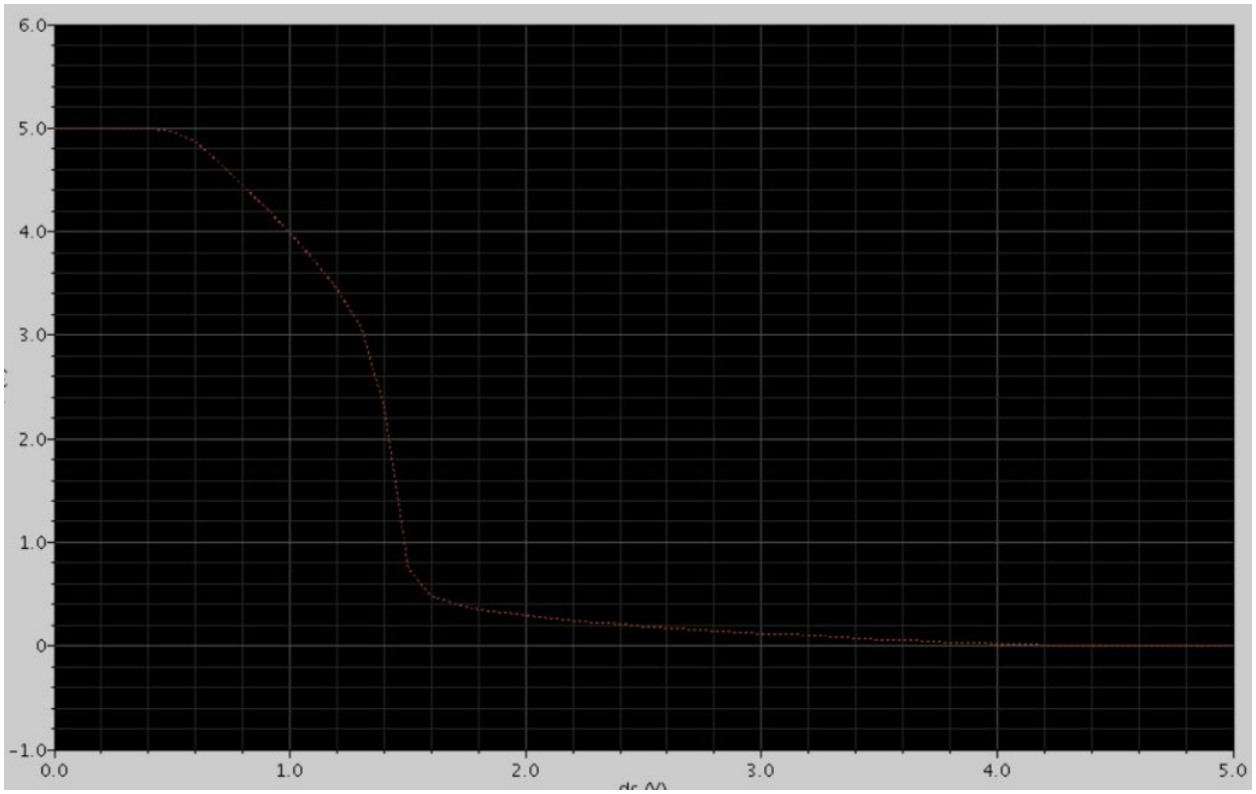
~~Best~~ worst tn : $A = C = E = 0$

worst tf : $\bar{B} = \bar{D} = 0 \quad B = D = 1$

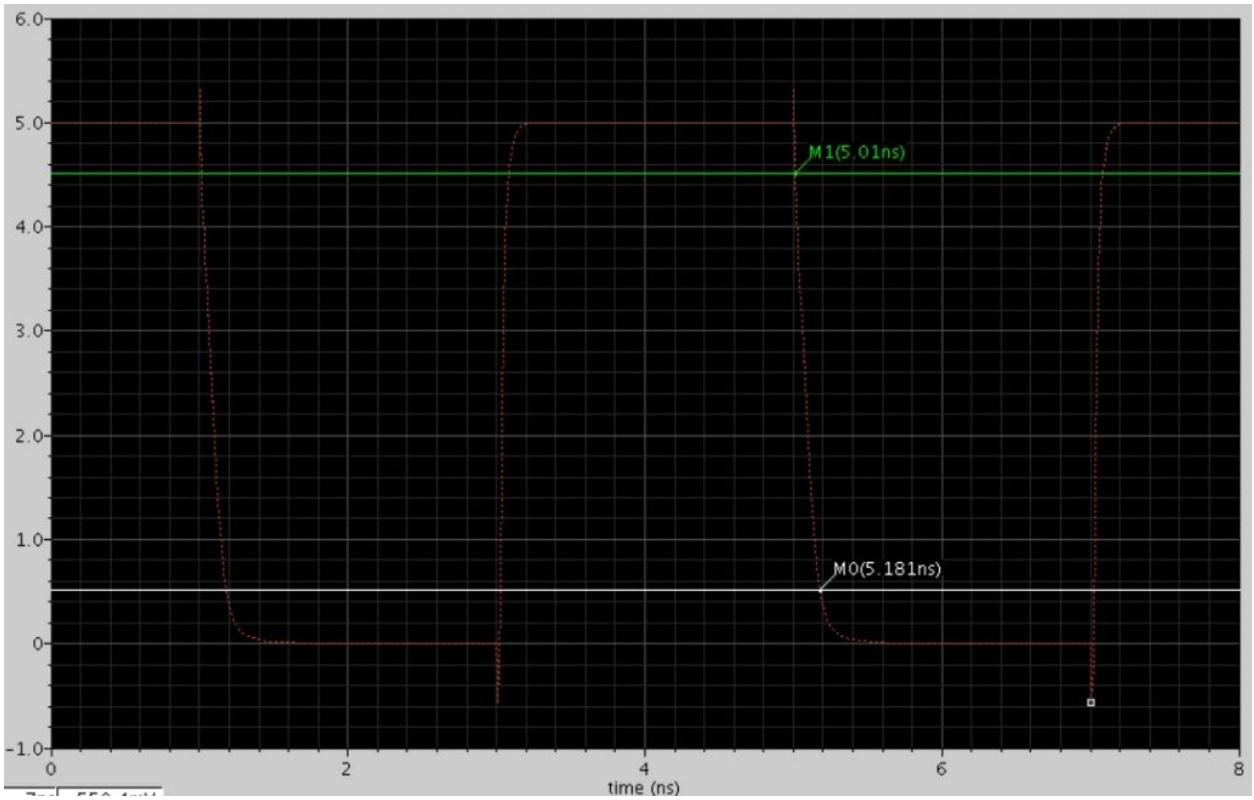
sizing shown in diagram.



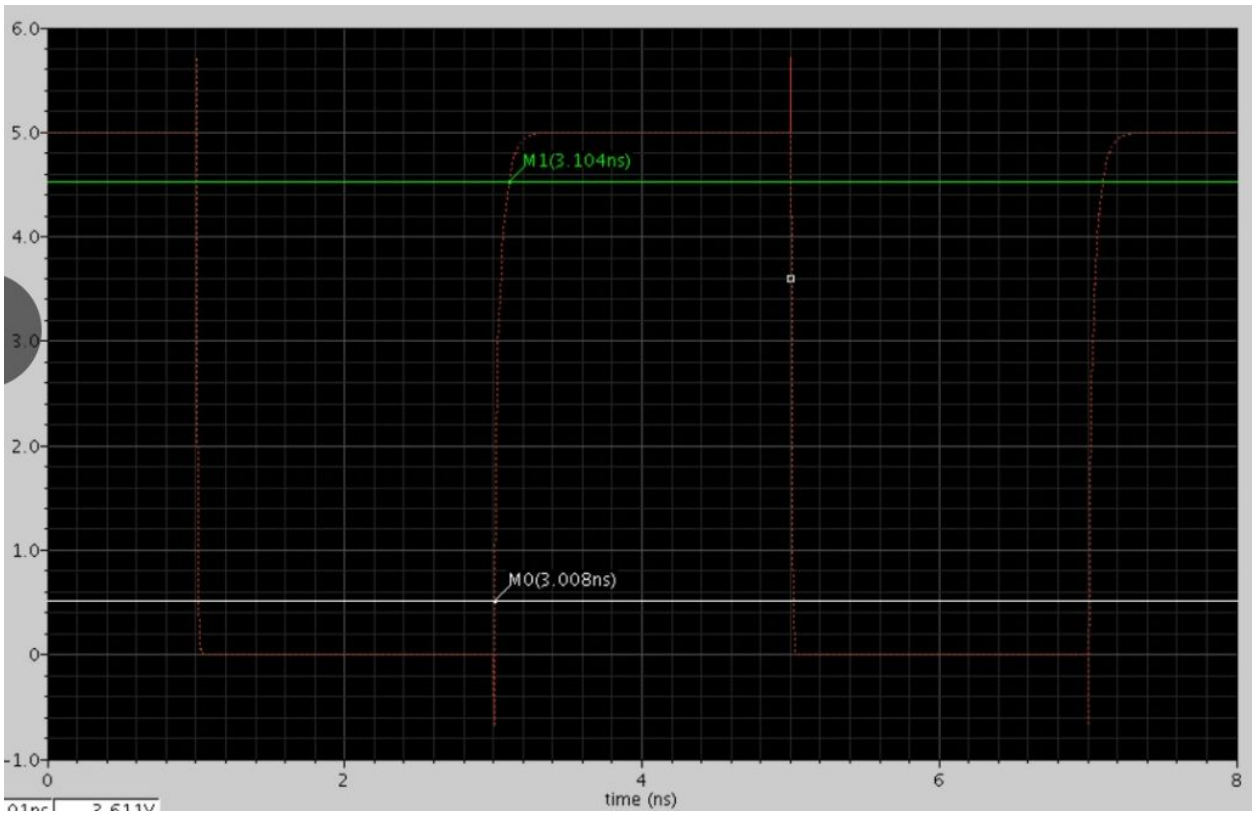




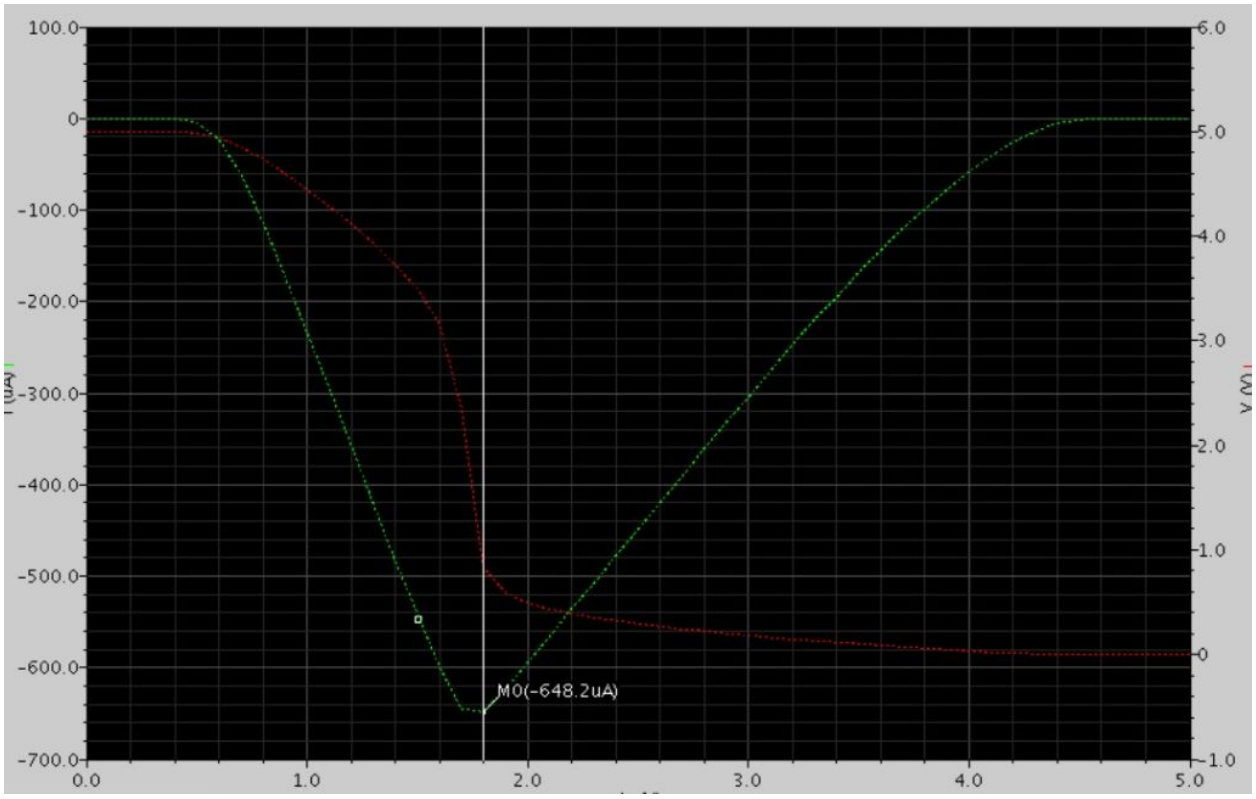
DC analysis for worst case rise and fall time.



Worst fall time=0.17 ns



Worst rise time =0.096 ns



peak power = peak current $*$ *voltage supply* $= 648.2 * 10^{-6} * 5 = 3.241 * 10^{-3} w$