CAD of Digital VLSI Systems Homework 4 Youzhe Dou

| NIH: PMOS (Sue) NMOS (Sue)

PMOS:
$$I_0 = \frac{1}{2} M_P \frac{W}{L} Cox (|V_{gS}| - |V_T|)^2 (|T_A| |V_{dS}|)$$
 $M_P Cox = |K_P| \frac{W}{L} = 40$
 $V_{gS} = V_J - V_S = V_{in} - S$
 $V_{dS} = V_{d-V_S} = V_{o-S}$
 $V_{dS} = V_{o-S}$
 $V_$

VIL:
$$PMOS$$
 ([ivear) $NMOS$ (sat)

 $PMOS$: $I_{D} = \mu_{P} \frac{VV}{L} Gex \left[\left(|V_{GS}| - |V_{TH}| \right) |V_{DS}| - \frac{1}{2} |V_{DS}|^{2} \right]$
 $k_{P} = 5 \cdot 4$. $\frac{V}{L} = \frac{1}{40} \quad V_{GS} = V_{IN} - 5 \quad V_{DS} = V_{O} - 5$
 $I_{D} = 5 \cdot 4 \times 40 \quad \left[\left(\frac{1}{426} - V_{IN} \right) (5 - V_{O}) - \frac{(5 - V_{O})^{2}}{2} \right]$
 $NMOS$: $I_{D} = \frac{1}{2} \int_{A_{D}} Gex \frac{V}{L} \left(\frac{1}{426} - V_{IN} \right) (5 - V_{O}) - \frac{(5 - V_{O})^{2}}{2} \left((4 \wedge V_{IS}) \right)$
 $= \frac{1}{2} \times \frac{1}{40} \times 17.6 \quad (V_{O} - 0.74)^{2} \left((4 \cdot 0.06 V_{O}) \right)$
 $= 0.245 \quad (V_{O} - 0.74)^{2} \left((4 \cdot 0.06 V_{O}) \right)$
 $\frac{216}{0.245} \left[(4.26 - V_{IN}) \left(5 - V_{O} \right) - \frac{(5 - V_{O})^{2}}{2} \right] = \left(V_{O} - 0.74 \right)^{2} \left((4 \cdot 0.06 V_{O}) + (4$

Volt: When Vin = 0. P(lin) - N(sat).

$$\frac{216}{4.245} \left[(426 - Vin)(5 - V_0) - \frac{(5 - V_0)^2}{2} \right] = (V_0 - 274) (140.6 V_0)$$

$$Vin = 0 \qquad V_0 = V_0H = 4.99 \approx 5 V$$

到 Vol:

Since NMOS is always in surmarium. He minimum Vane = 0.74 V = Vol.

VLT: Vo=Vin N(Sat) P(Sat)

NML = |VoL - VILI = 4.01 - 0.74= 3.27 NMH = |Vou - VILI = 5 - 4.26 = 0.74

Tr . Tf:

 $C_{3}d_{1}=2\times66\times10^{-12}\times20\times10^{-6}=2.64\times10^{-16}$. $C_{3}d_{2}=0$ $C_{3}d_{1}=1.836\times10^{-17}$ [$C_{3}d_{2}=2.35$] $\times10^{-17}$.

$$C_{L} = \Sigma = \frac{2.2 \times 10^{-14} \text{ F}}{1 - 3.48 \times 10^{-8} \text{ s}}$$

$$T_{f} = 1.264 \times 10^{-15} \text{ s}$$

$$V_{LT} = \frac{V_{LN} + \sqrt{\beta_{N}} (V_{M} - |V_{M}|)}{1 + \sqrt{\beta_{N}} (V_{M} - |V_{M}|)} = 1$$

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$$\frac{\sqrt{\beta_{N}} = A \quad V_{LN} = 0.14 \quad V_{M} = 1.6 \quad |V_{M}| = 1.44}{1.66 \quad A = 1 + H}$$

$$A = 1 + 3.3 = \sqrt{\beta_{N}}$$

$$\frac{\beta_{N}}{\beta_{N}} = 18.78 = \frac{M_{N} \log W_{N}}{M_{N} \log W_{M}} = \frac{K_{N}}{K_{N}} \times \frac{W_{N} \log W_{N}}{W_{N} \log W_{M}}$$

$$\frac{K_{N}}{K_{N}} = \frac{3.4}{11.6} = 0.2755$$

$$\frac{W_{N} / L_{N}}{W_{N} / L_{N}} = \frac{1.48}{11.6} \times \frac{2(V_{N} - V_{N})}{V_{N} / L_{N}} = \frac{1.48}{11.6} \times \frac{2(V_{N} - V_{N})}{V_{N} / L_{N}} = \frac{1.48}{11.6} \times \frac{1.16}{0.18} = 1$$

$$V_{N-1} / J_{M-1} = 0.38$$

$$= \frac{4.38 \times (0^{-15})}{2 \times 10^{-15}} \times \frac{1.48}{11.6} \times \frac{1.16}{0.18} = 1$$

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$$T_{r} = t_{LH} = \frac{C_{L}}{\beta_{p} (V_{H} - |V_{tp}|)} \left\{ \frac{2 |V_{tp}|}{(V_{H} - |V_{tp}|)} + \ln(\frac{2 (V_{H} - |V_{tp}|)}{V_{L}} - 1) \right\}$$

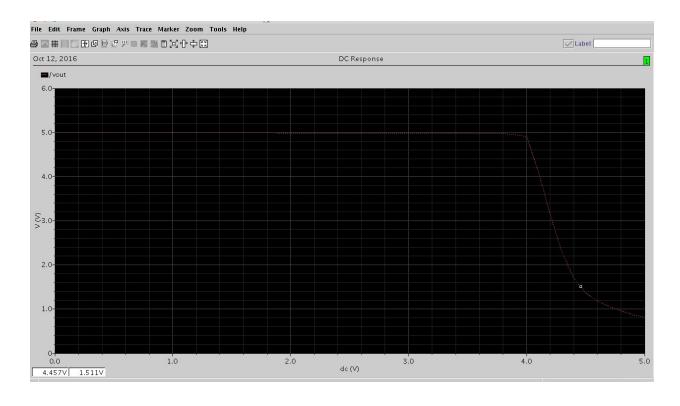
$$= \frac{100 \times 10^{-15}}{\beta_{p} \times 0.83} \left[\frac{1.48}{0.53} + l_{r} \left(\frac{1.76}{0.18} - 1 \right) \right]$$

$$= \frac{438 \times 10^{-15}}{\beta_{p}} < 2 \times 16^{-9}$$

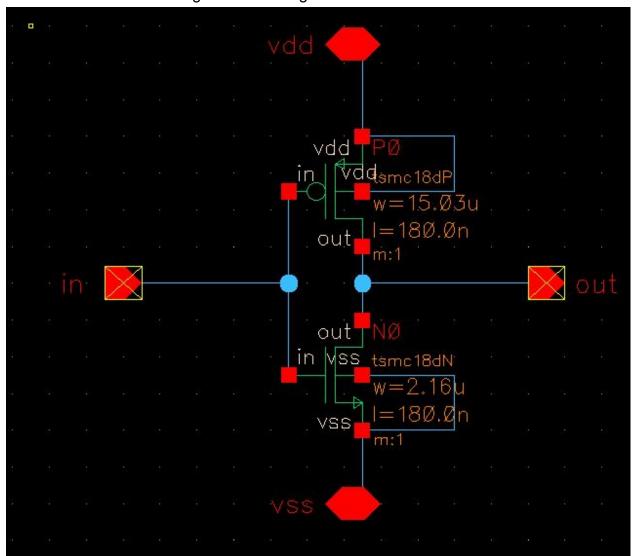
$$\beta_{p} > 219 \times 10^{-6} = L_{p} \frac{\omega_{p}}{L_{p}} \qquad \frac{\omega_{p}}{L_{p}} > \frac{219 \times 10^{-6}}{5.4 \times 10^{-6}} = 45.56 \right]$$

$$Set \frac{\omega_{n}}{L_{n}} \text{ be minimum } \frac{\omega_{n}}{L_{n}} = 12 \frac{\omega_{p/L_{p}}}{\omega_{n/L_{n}}} = 68.2 \text{ or } \frac{\omega_{p}}{L_{p}} = 813.4 > 40.56 \right]$$

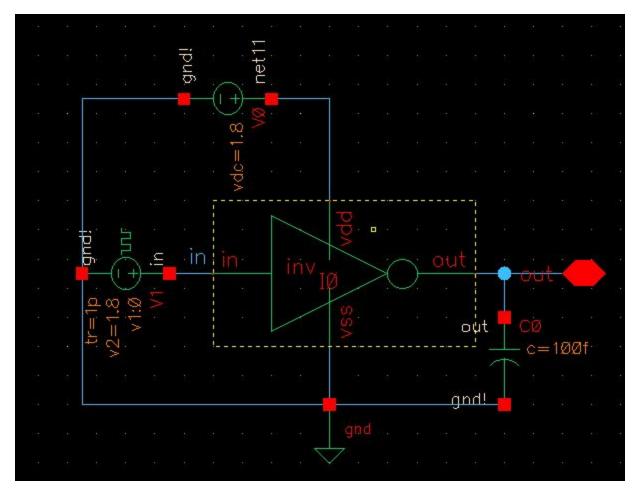
Q1 simulation verification



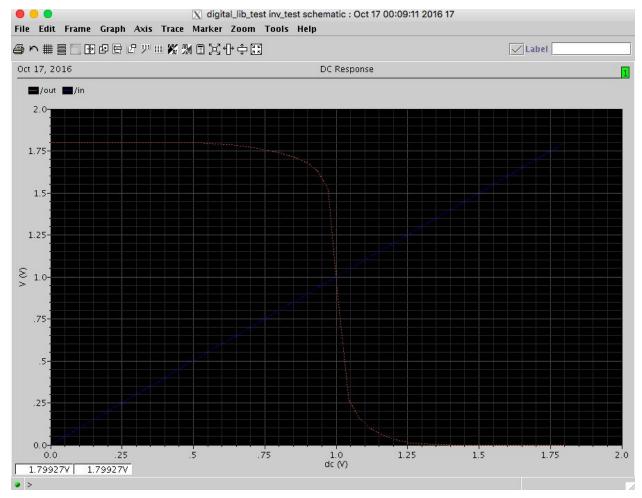
Q2
According to calculation, Wp/Lp=818.4, which is impossible to draw the layout.
We tune the numbers and get the following result to obtain VIt=1.



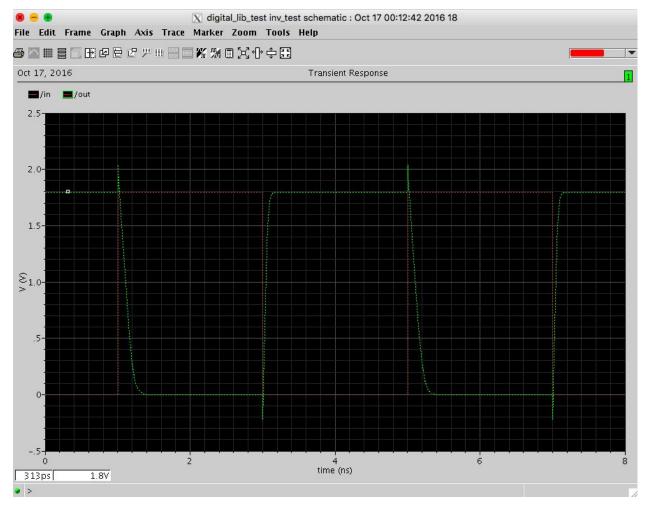
Schematic of inverter designed.



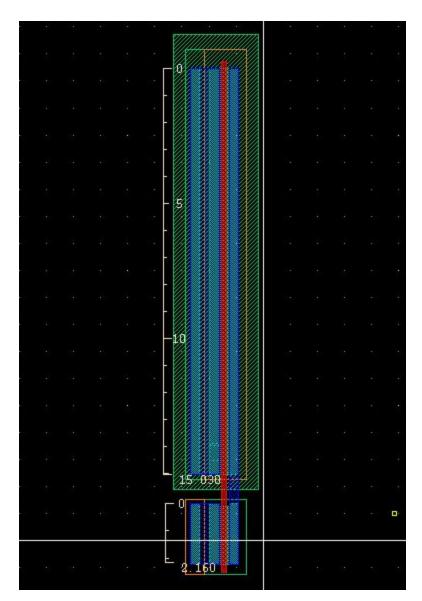
Simulation circuit.



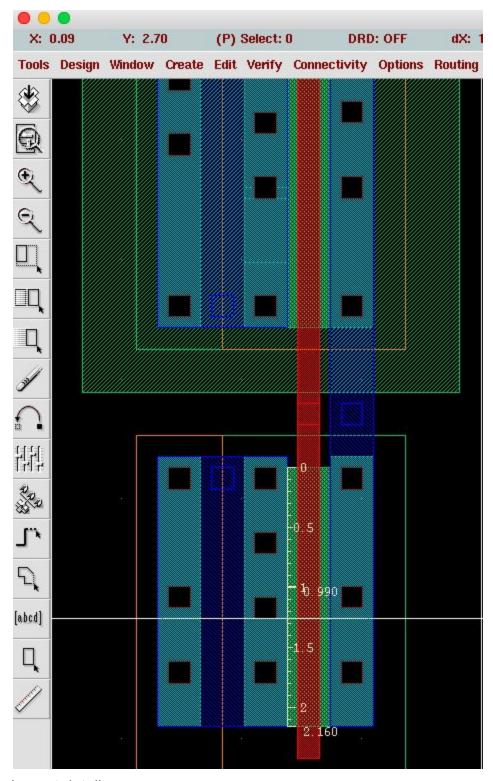
DC analysis



Transient analysis

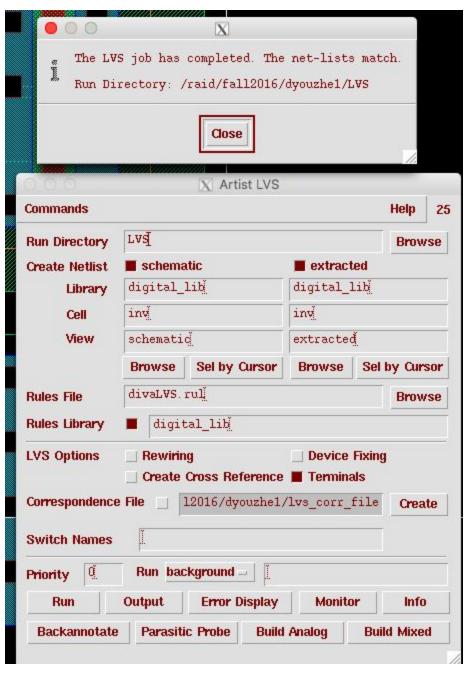


Layout full view

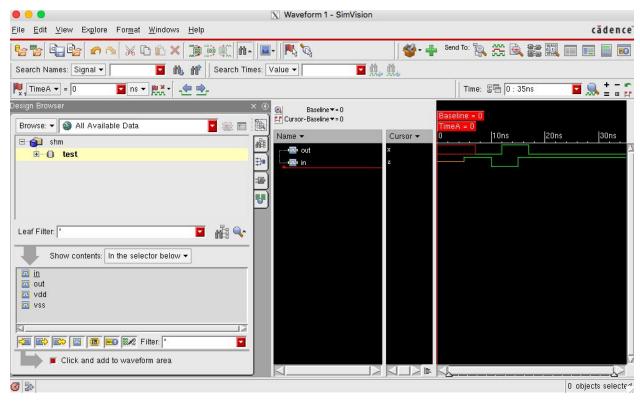


Layout details

DRC check



LVS check



Verilog simulation