**CAD of Digital VLSI Systems**

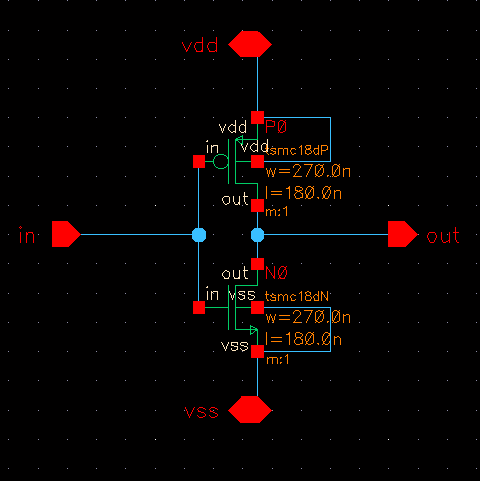
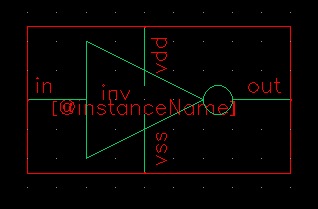
**Homework 2 Report**

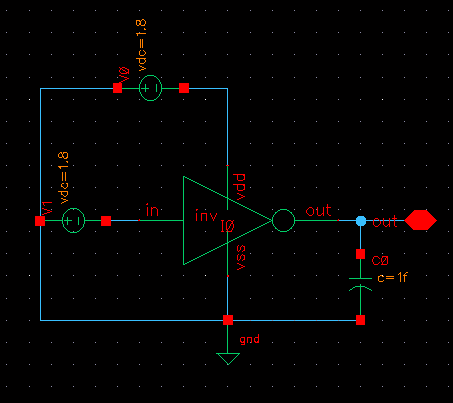
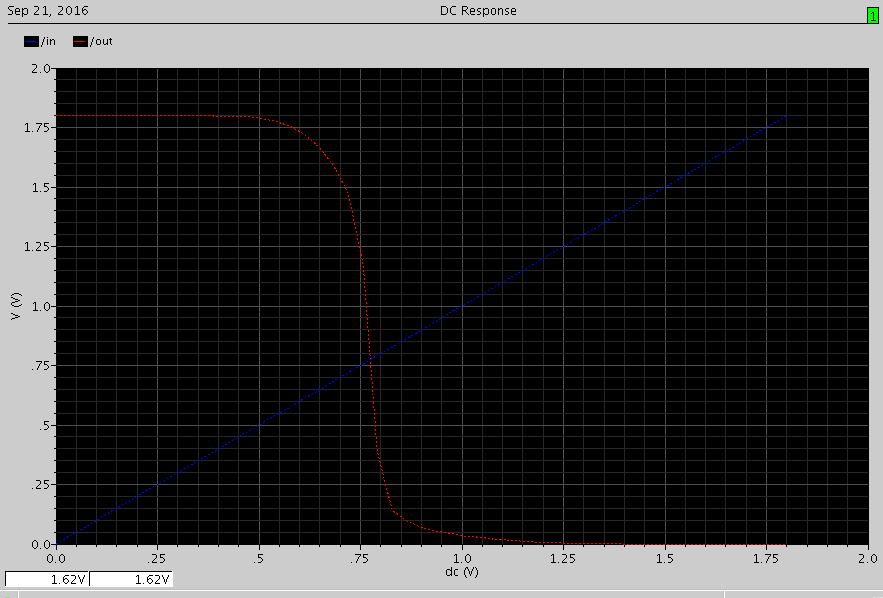
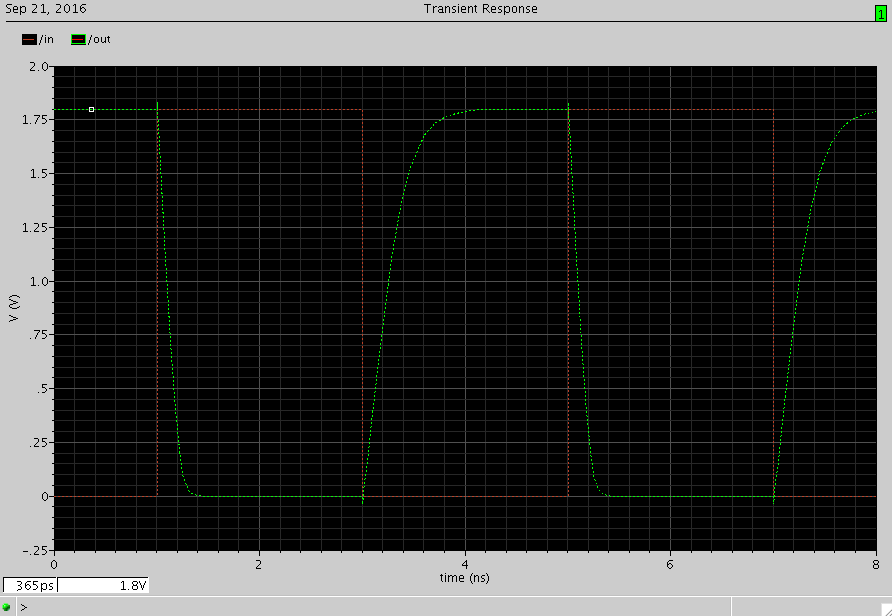
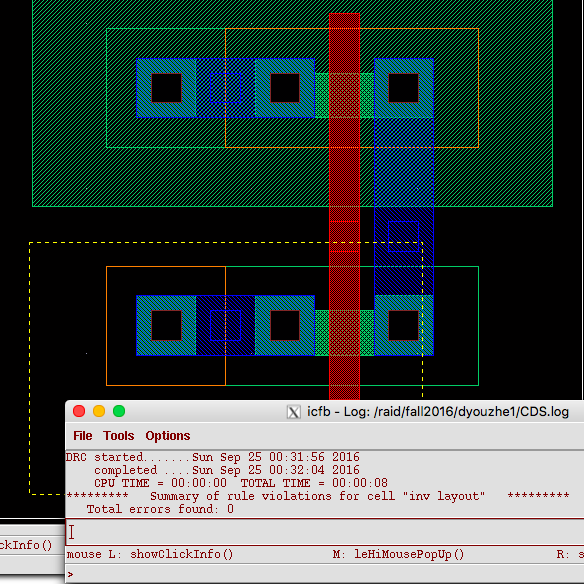
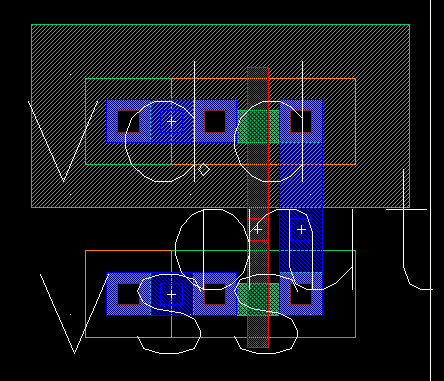
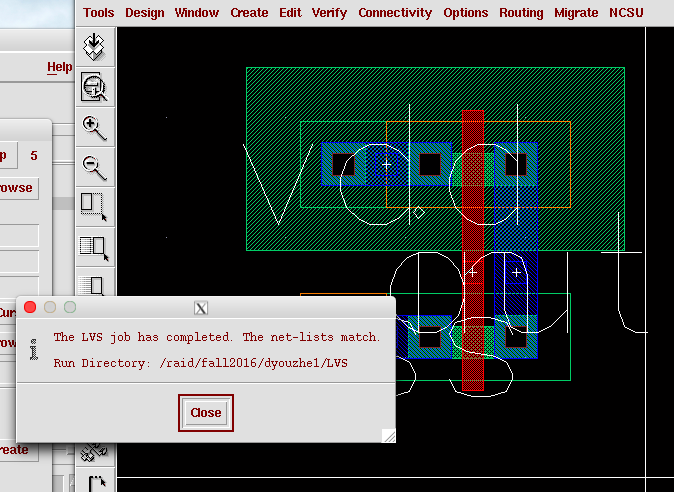
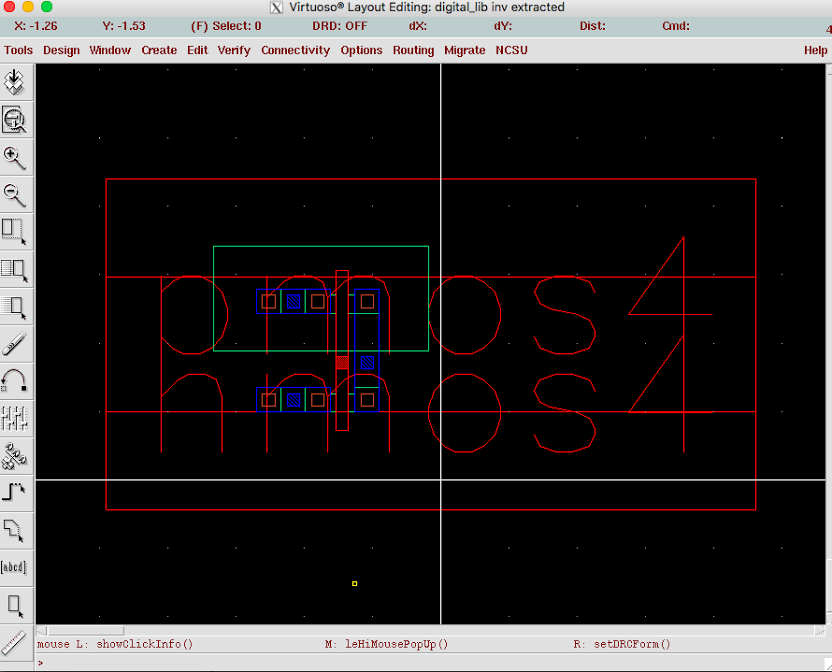
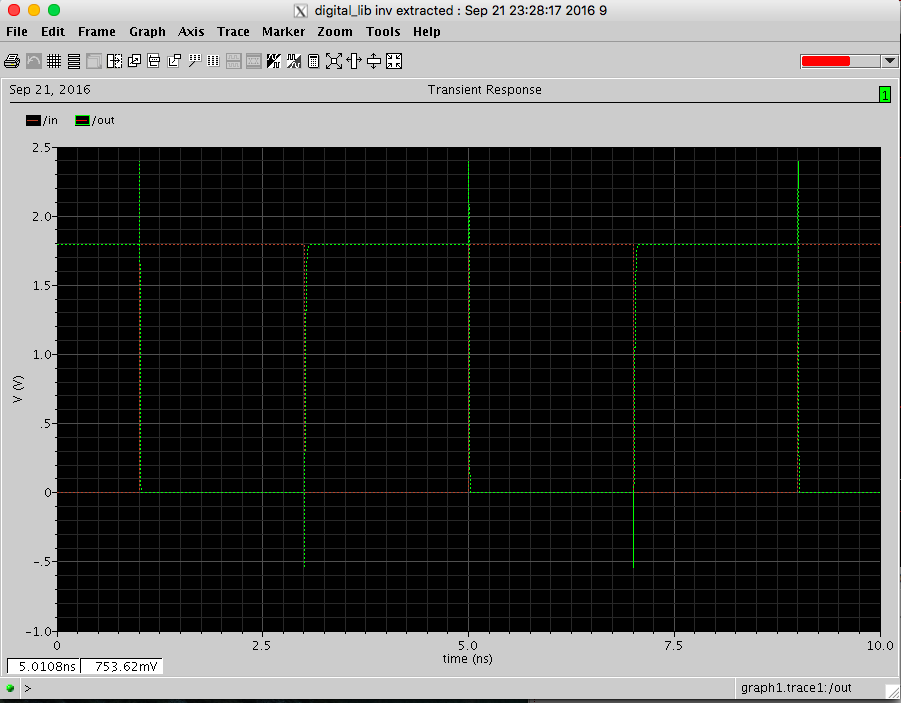
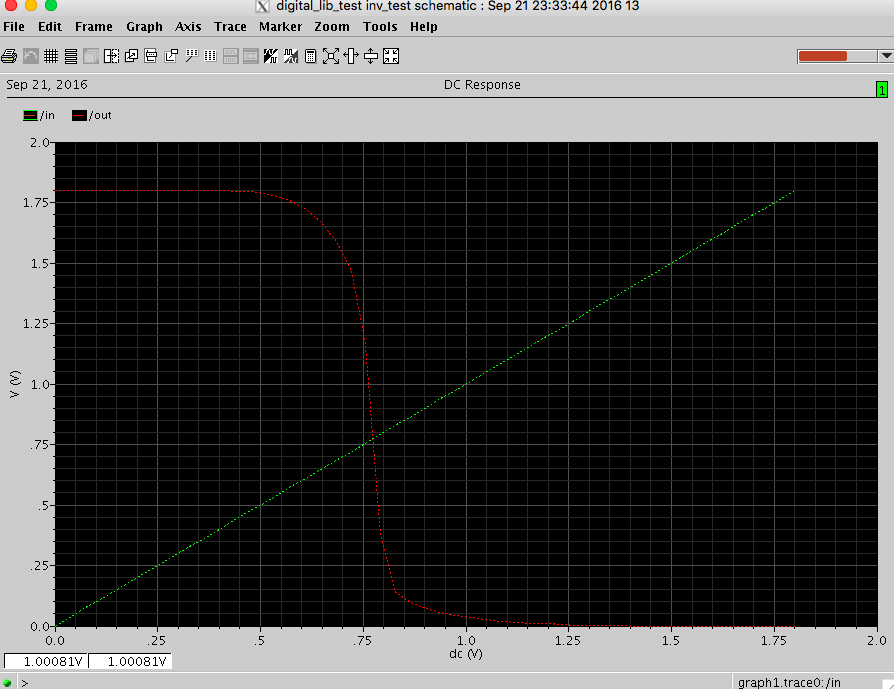
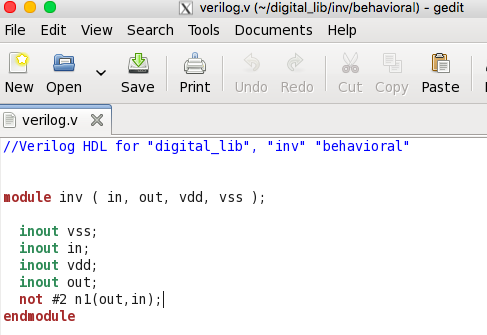
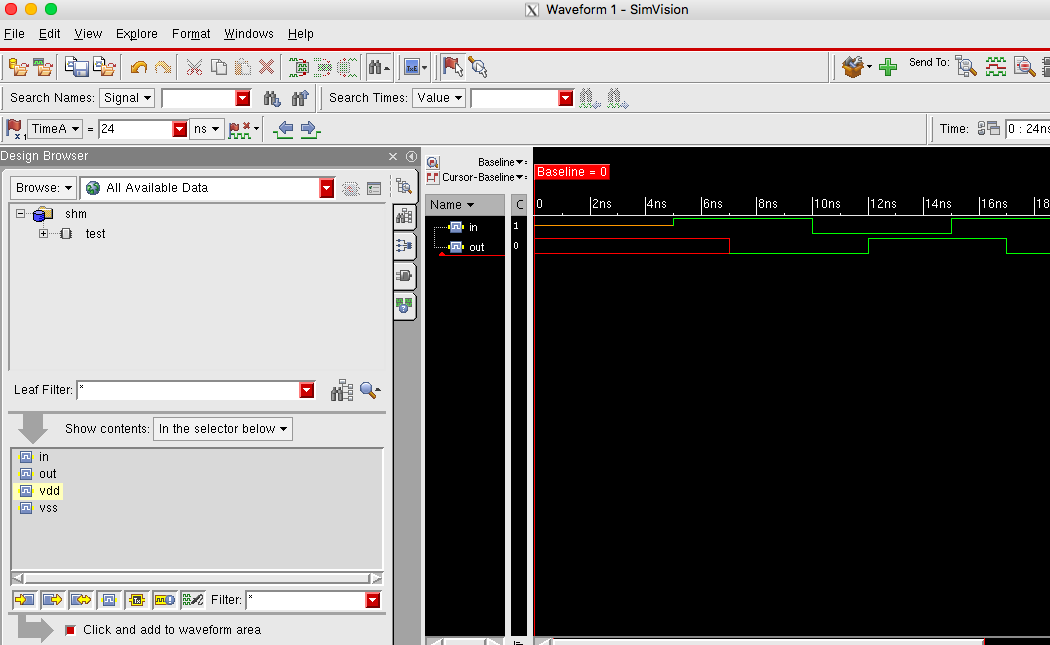
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**Objectives:**

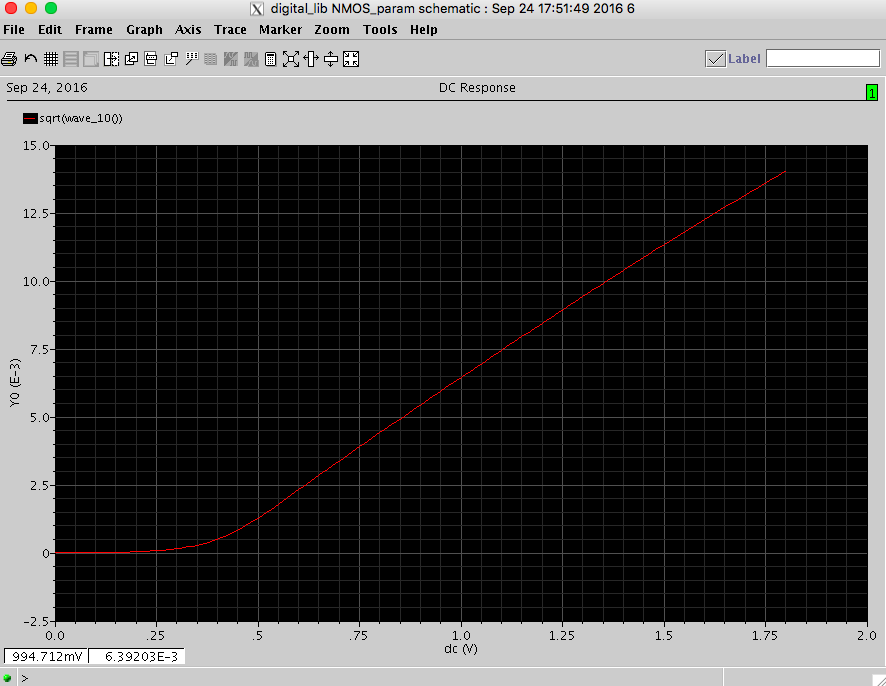
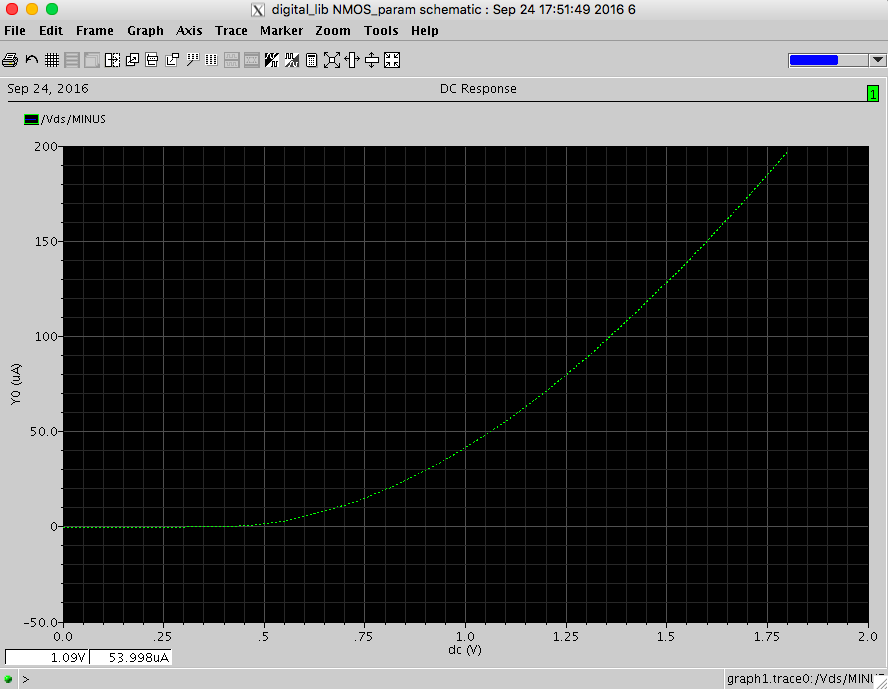
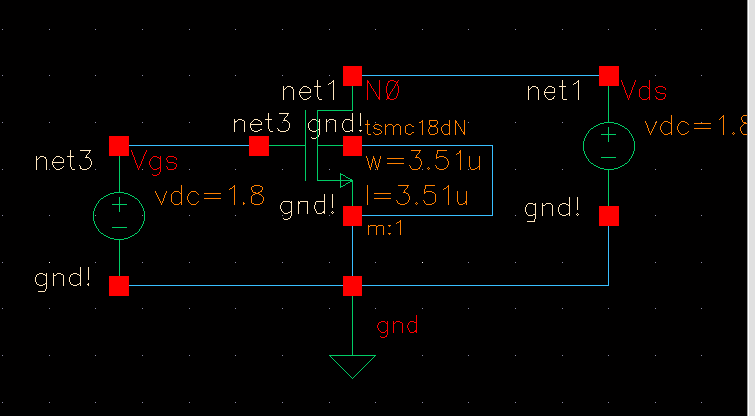
1. To familiarize with the functionality of Cadence.
2. To implement an inverter with schematic, symbol and layout.
3. To simulate the response of the inverter using DC sweep and transient separately.
4. To simulate the functionality of an inverter using hardware programming language such as verilog.

**Procedures and results:**

1. Inverter is essentially a PMOS connected with a NMOS through following circuit. When input is ‘high’, NMOS is activated and the output is connected with gnd. When input is ‘low’, PMOS is activated and the output is now connected with vdd which is ‘high’. MOSFETs are four terminal devices so it is very important to connect ‘body’ with ‘source’. otherwise , a warning message will appear.
2. When design larger and more complex circuit, we need a symbol to represent fundamental building blocks to make our design visually clearer easier to be reused in other schematics. A symbol with same number of pins is created to represent inverter in future simulation.

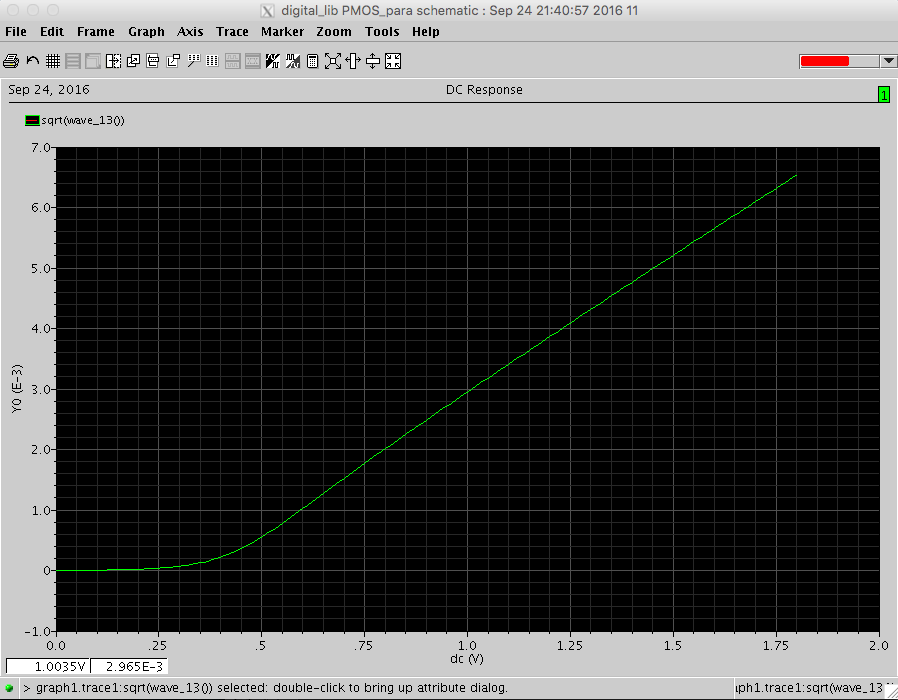
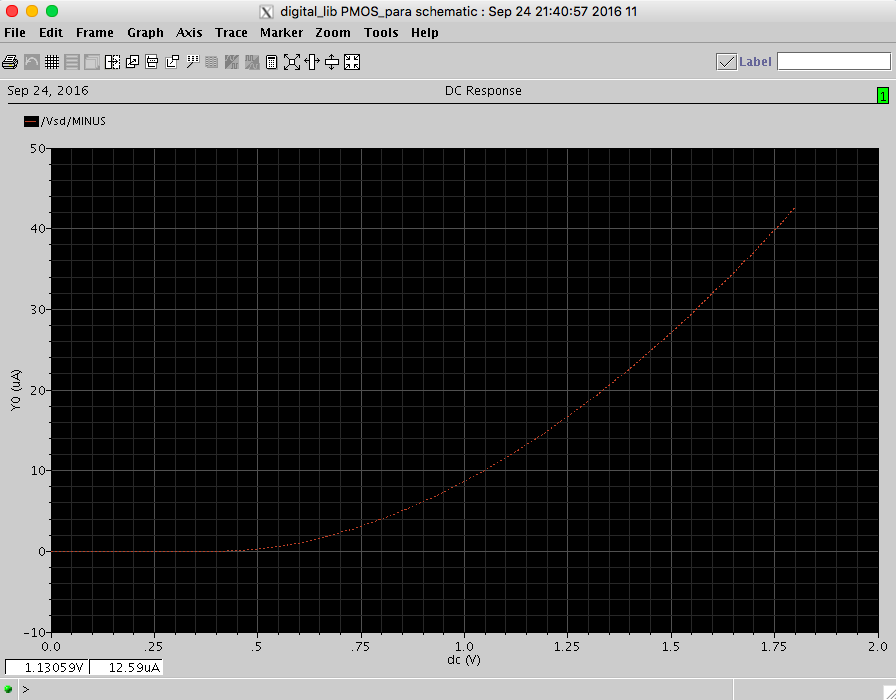
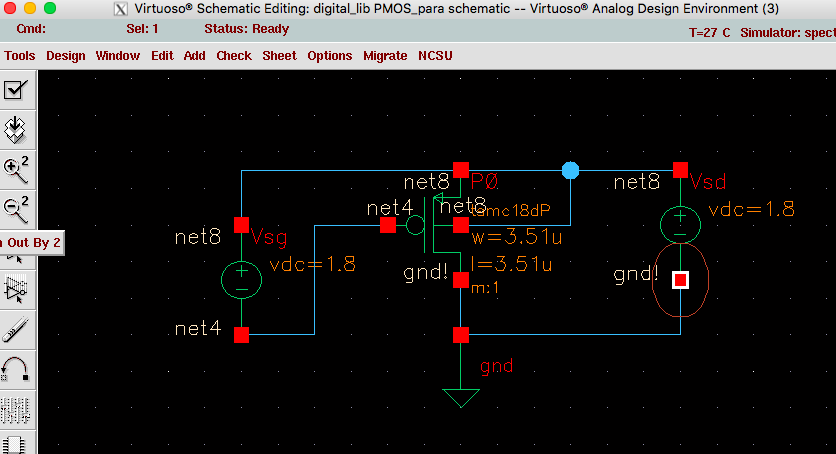
1. To test the functionality of the inverter, two similar circuits are designed to simulate the behavior. First, a DC sweep is connected with the input through the following design. Two DC voltage sources are added to input and vdd and a capacitor is connected to the output to observe the change of output. The result of the simulation is shown in the following graph. While the input voltage (blue line) change from 0 to 1.8, the output (red line) decrease smoothly from 1.8 to 0 due to the effect of the capacitor.The transient response is tested by change the input voltage source to a pulse source, the result is same as expected. The inverter works with certain delay.
2. The layout is the actual layer design of the inverter which will be needed for the foundries to manufacture this device. The layout is done by putting n-type, p-type and metal materials with specific dimension together. Design Rule Check (DRC) must be performed to ensure that the foundry is able to produce this design.  Before sending the design information to the manufacturers, it is very important to make sure that the design is functioning as planned and the layout is equivalent to schematic and this requires an extracted version to perform (1) Layout vs Schematic check (2) dc sweep and transients analysis. 
3. Similar simulation process is carried out to the extracted view. DC sweep and transient analysis show very similar results as shown below.
4. The last step is to use hardware programming language to design this component and simulate its behavior. Verilog is used here and module inv is the descriptive model of an inverter. A test bench is written to toggle the input value every 5 ns fro three times. The output changes accordingly with 2ns delay.

**Part B**

To do the DC sweep, connect the circuit like the following diagram. In Analog environment, sweep Vgs from 0 to 1.8V and plot the current Ids.

From the above two equations, we can conclude that when we plot sqrt(Ids) against Vgs, the gradient will be sqrt(kn) and the x-intercept will be Vton. Taking two points from the graph above: (0.75, 3.90\*10^-3) and (1.5, 0.01132).

Making the same circuit for PMOS where voltage source needed to be inverted at terminals and plot the same graph.

Taking two points from the graph above: (0.75, 1.77\*10^-3) and (1.5, 5.209\*10^-3).