CAD of Digital VLSI Systems

Homework 3

Youzhe Dou

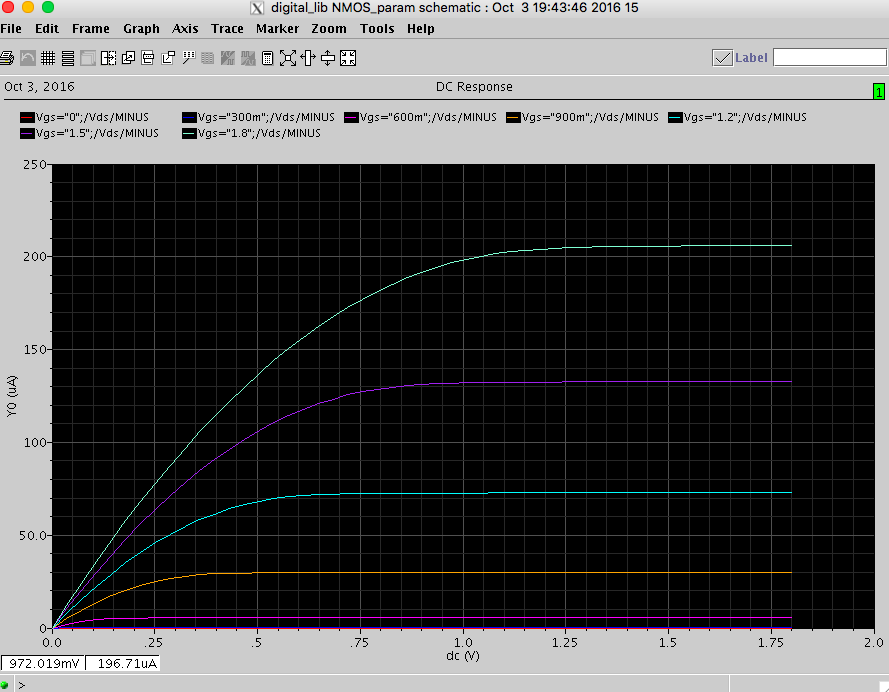


Figure 1 NMOS W=L=10 um

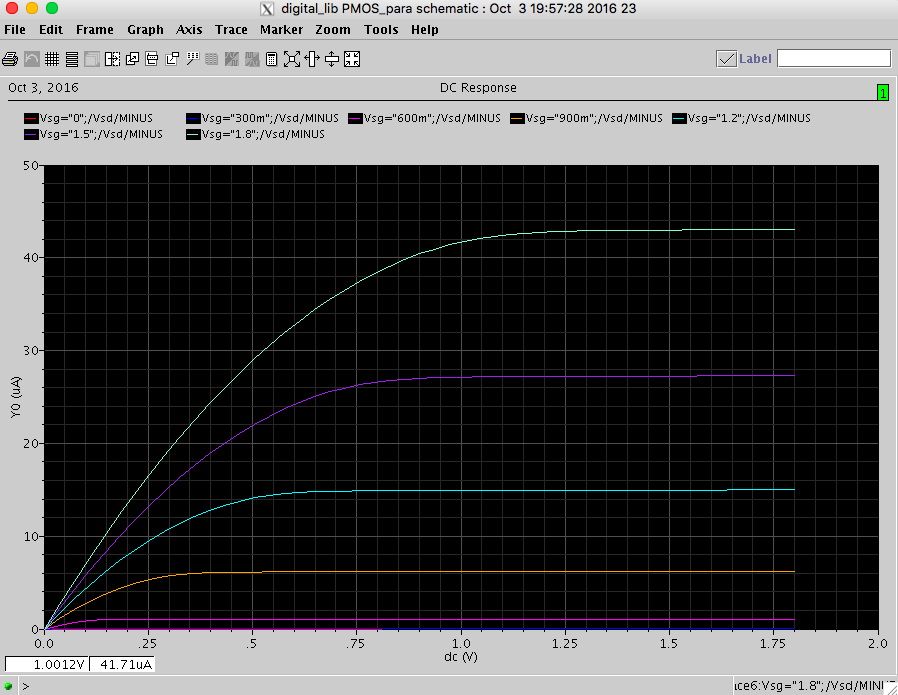


Figure 2 PMOS W=L=10 um

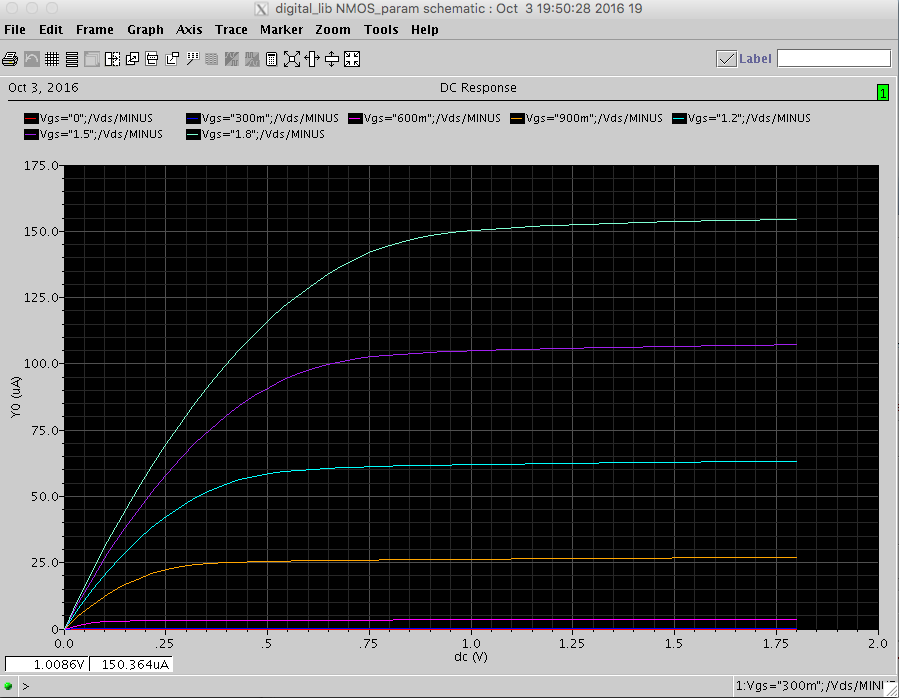


Figure 3 NMOS W=L=500 nm

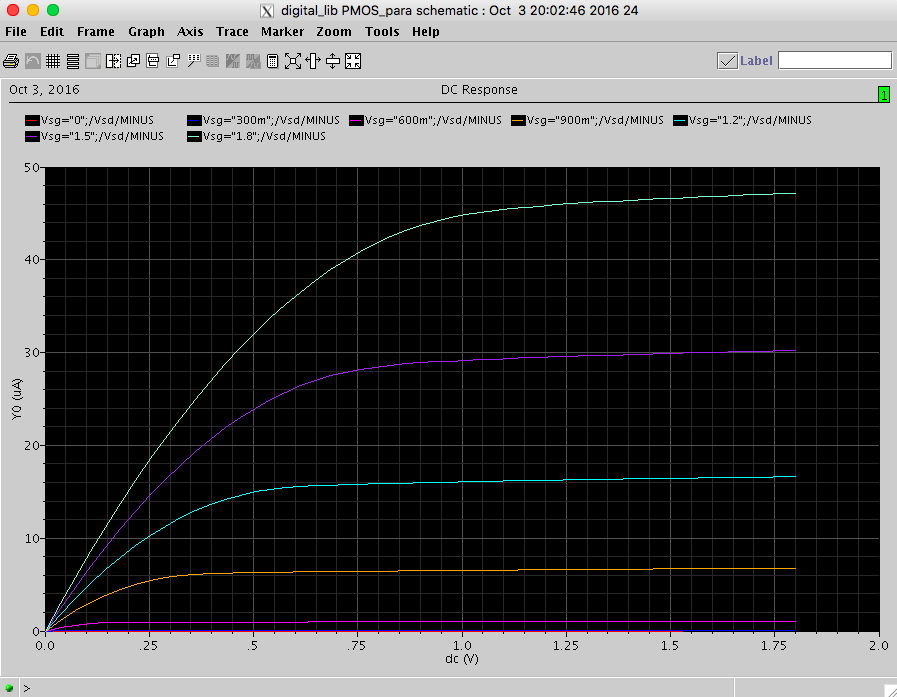
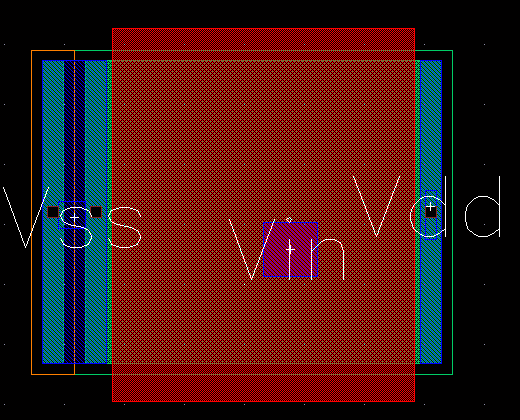


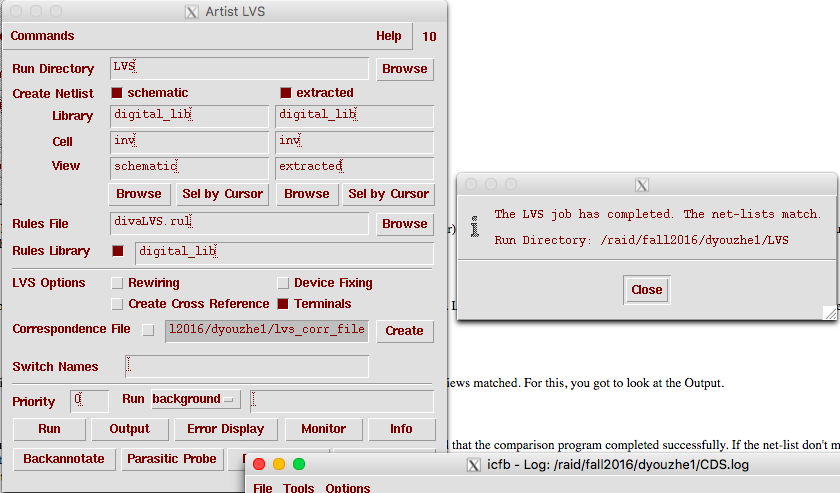
Figure 4 PMOS W=L=500 nm

From the four graphs above, we can see that short channel effect has significant effect on NMOS. When the feature size decreases, corresponding current become smaller. However, the result is not so significant with PMOS.

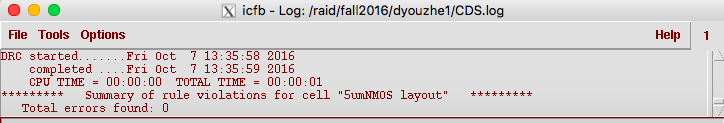
**Part 2 5um NMOS**



Layout



LVS



DRC