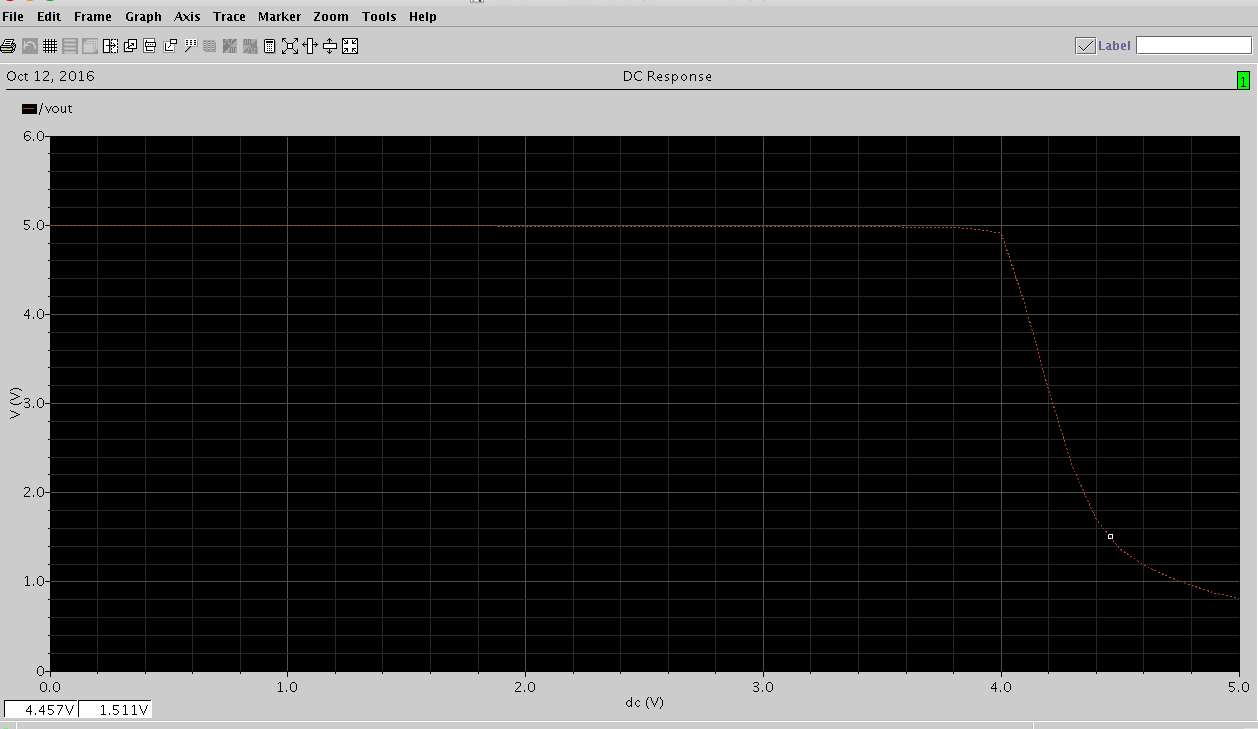
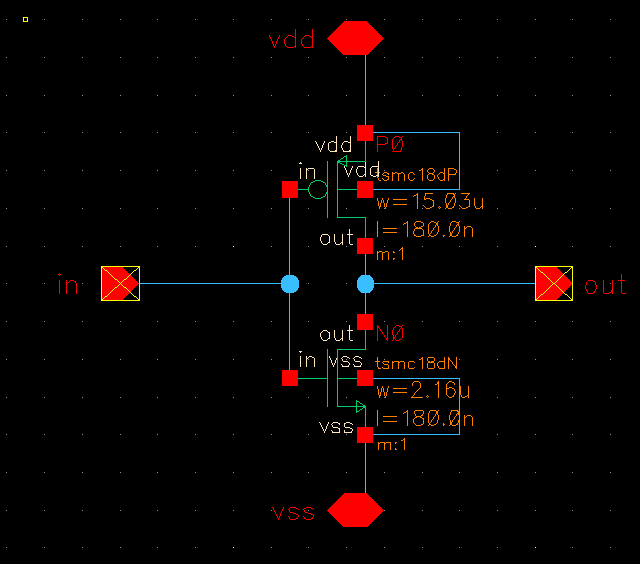
Q1 simulation verification



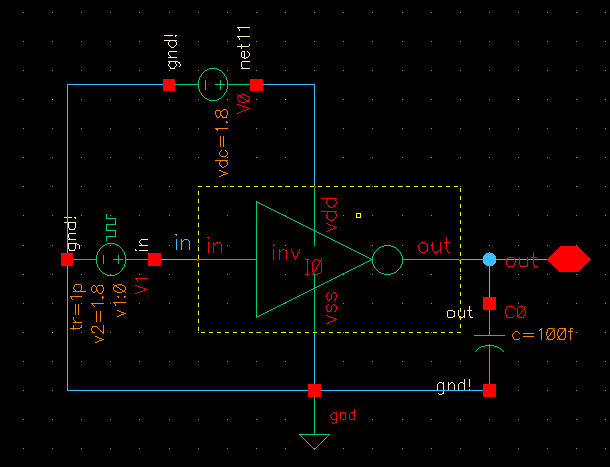
Q2

According to calculation, Wp/Lp=818.4, which is impossible to draw the layout.

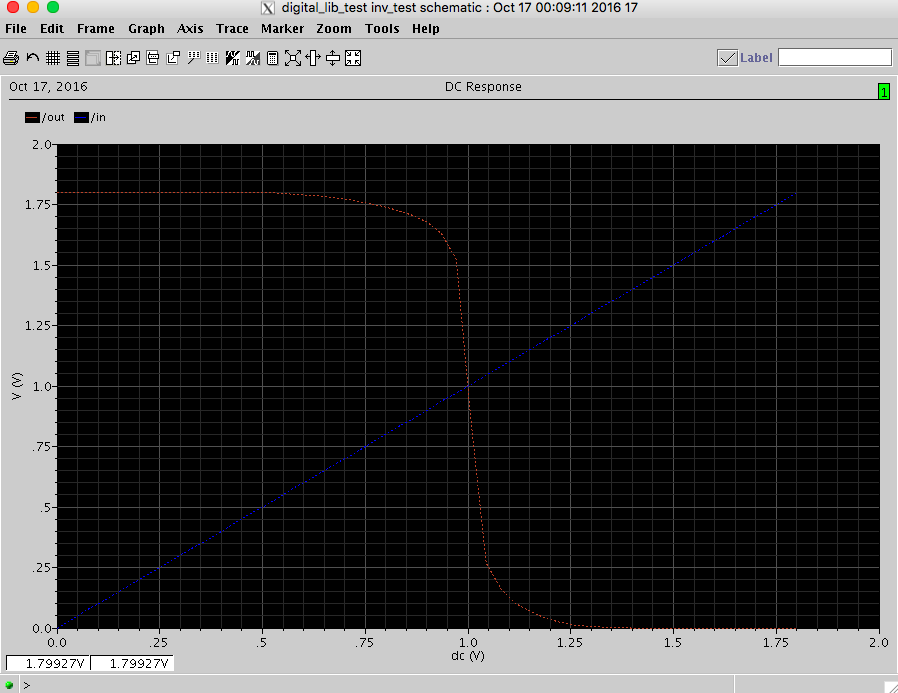
We tune the numbers and get the following result to obtain Vlt=1.



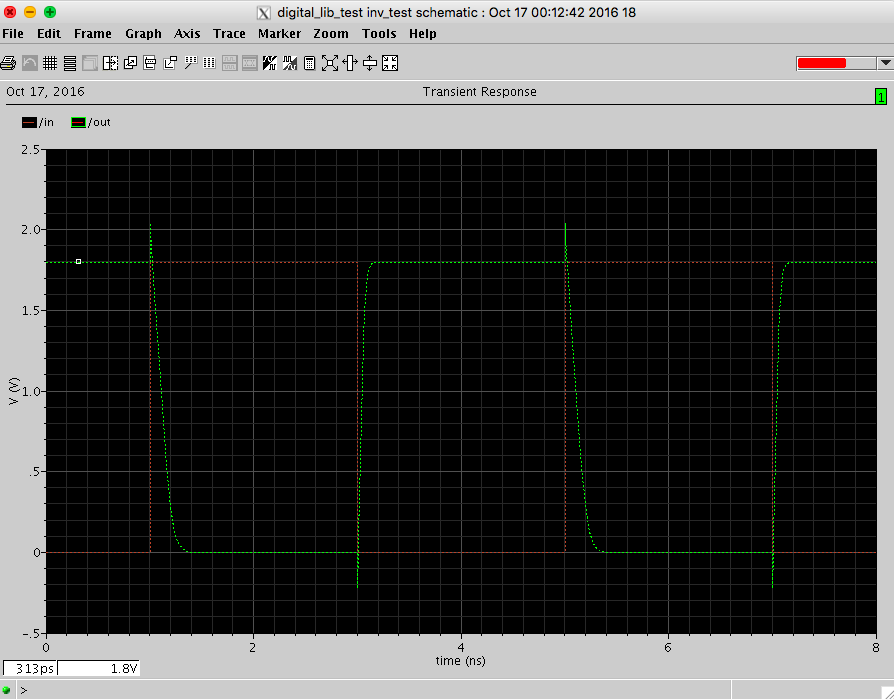
Schematic of inverter designed.



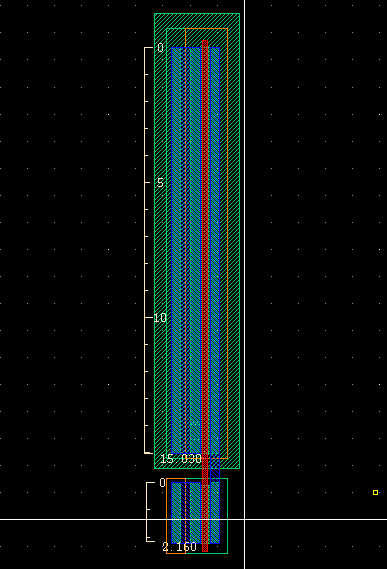
Simulation circuit.



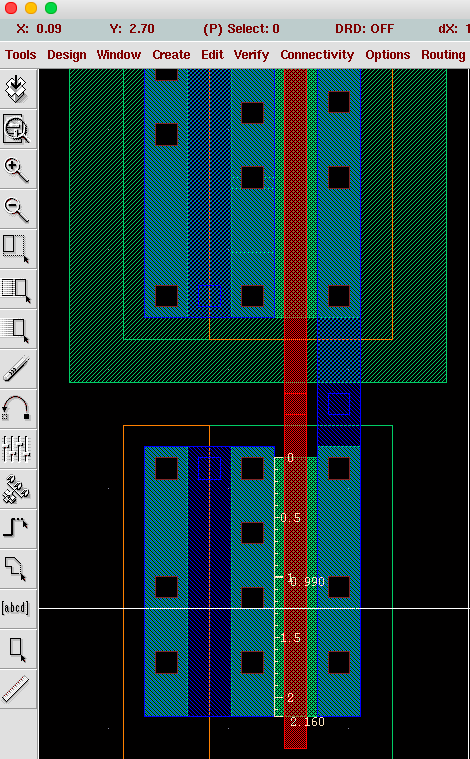
DC analysis



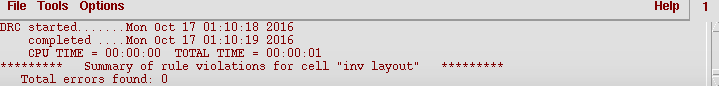
Transient analysis



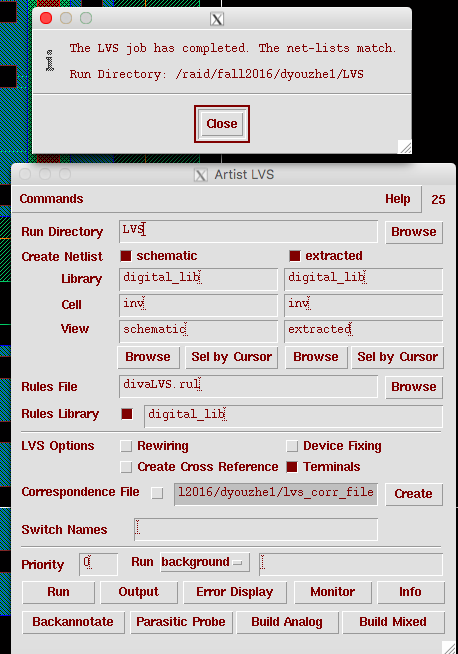
Layout full view



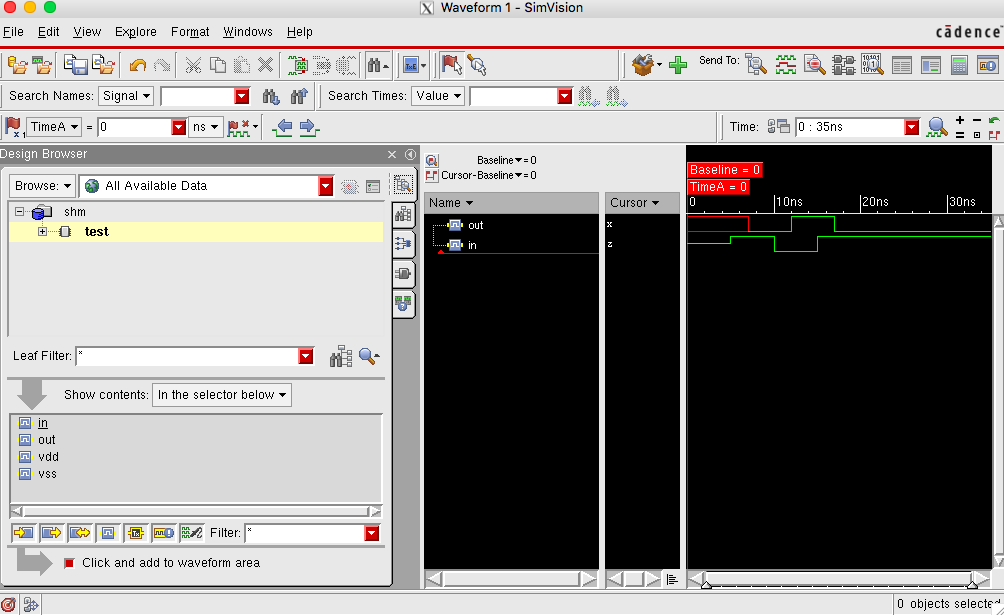
Layout details



DRC check



LVS check



Verilog simulation