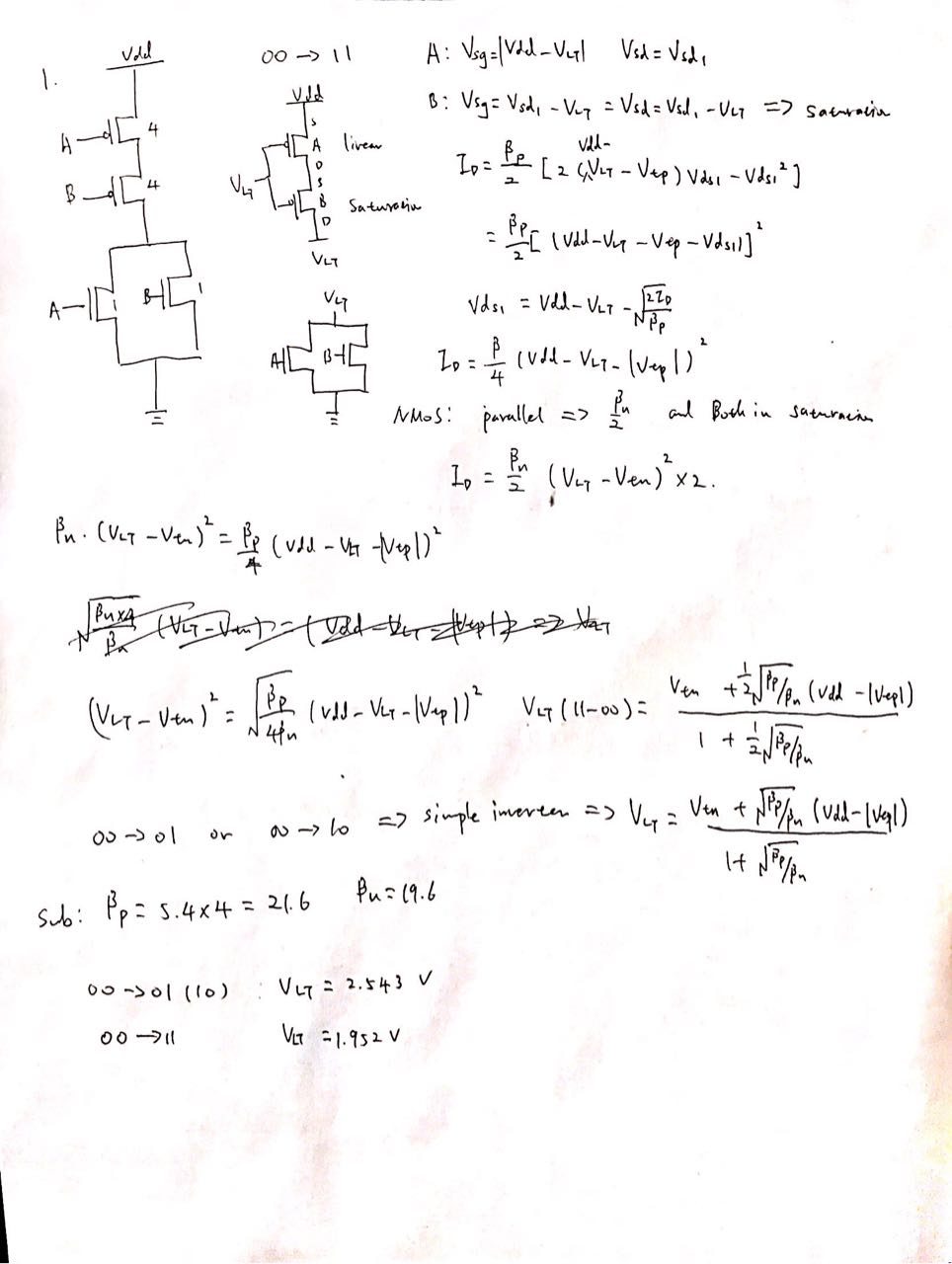
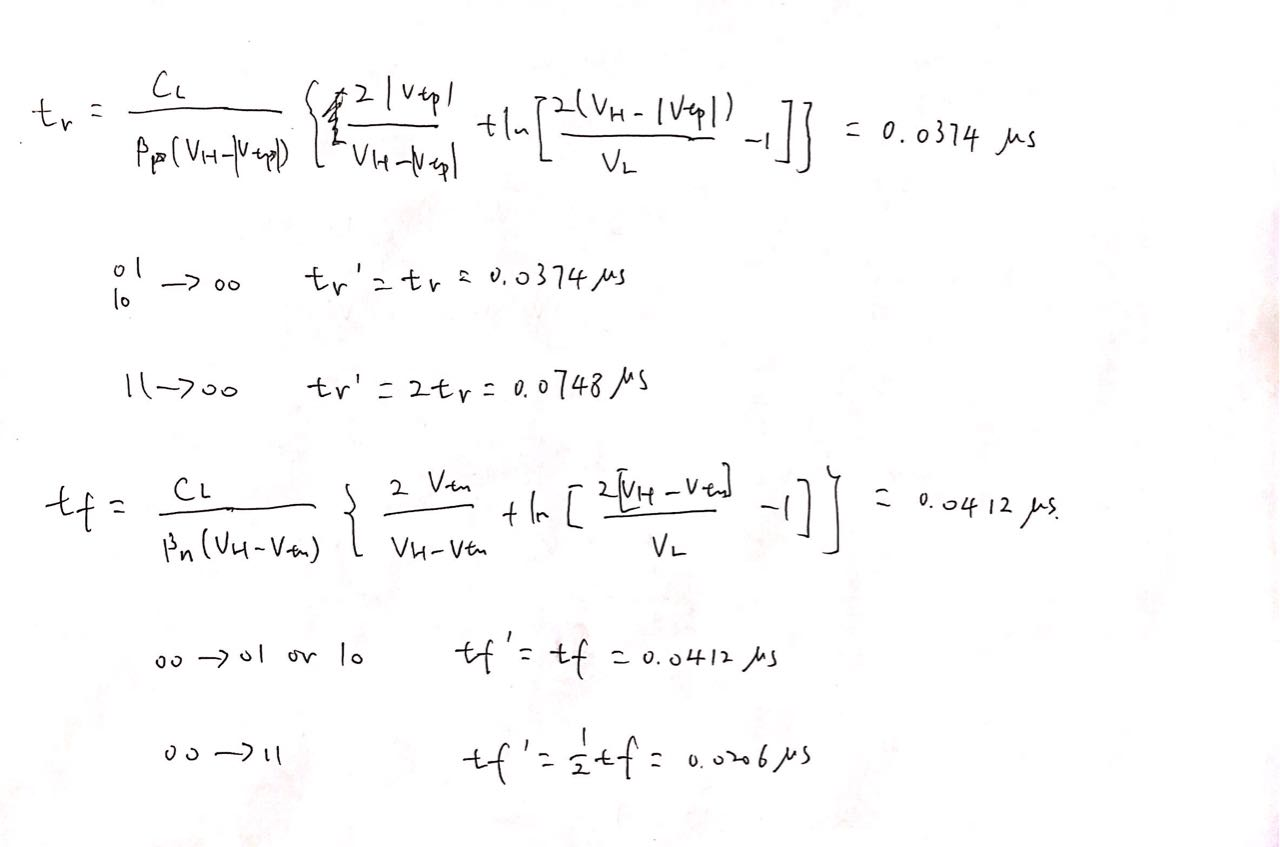
**HW5**

**Youzhe Dou**

1.





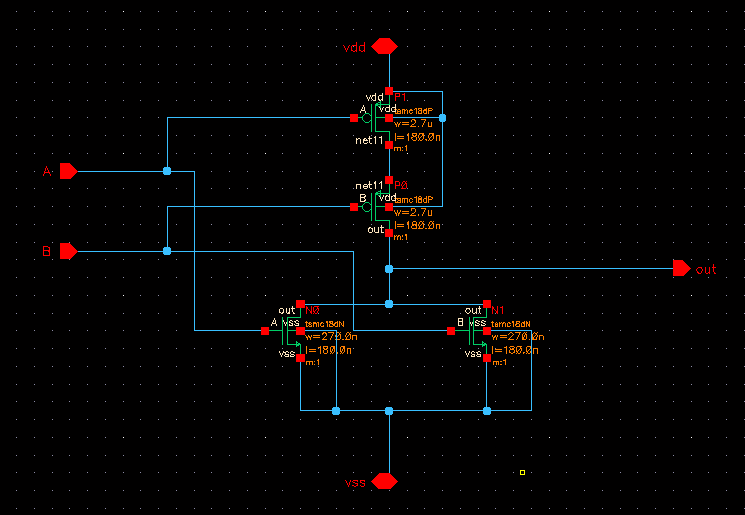
2.

(a)

For a 2-inputs NOR gate, the worst case rising time should be the transition (11-00) and the worst case falling time should be the transition (00-01). After some adjustment to equalize the worst rise and fall time, I came to the following W/L ratio for each gate:

PMOS: 30/2 (2700 nm / 180 nm)

NMOS: 3/2 (270 nm / 180 nm)



(b)

module HW5 (A, B, out, vdd, vss );

inout vdd,vss,A,B,out;

nor #0.03 net1(out,A,B);

endmodule

// Verilog stimulus file.

// Please do not create a module in this file.

// Default verilog stimulus.

initial

begin

io\_A = 1'bz;

io\_B = 1'bz;

io\_out = 1'bz;

io\_vdd = 1'bz;

io\_vss = 1'bz;

#5

io\_A = 1'b1;

io\_B = 1'b1;

#5

io\_A = 1'b0;

io\_B = 1'b0;

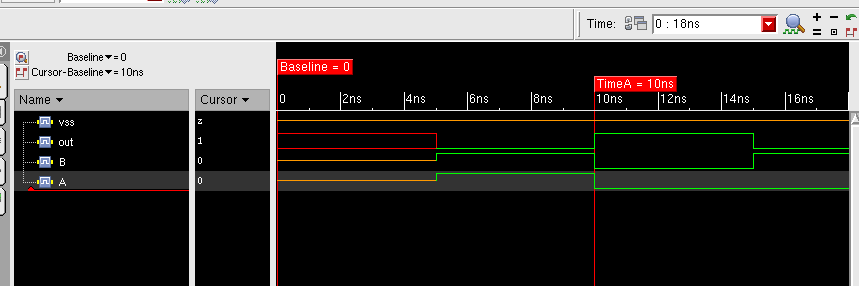
#5

io\_A = 1'b0;

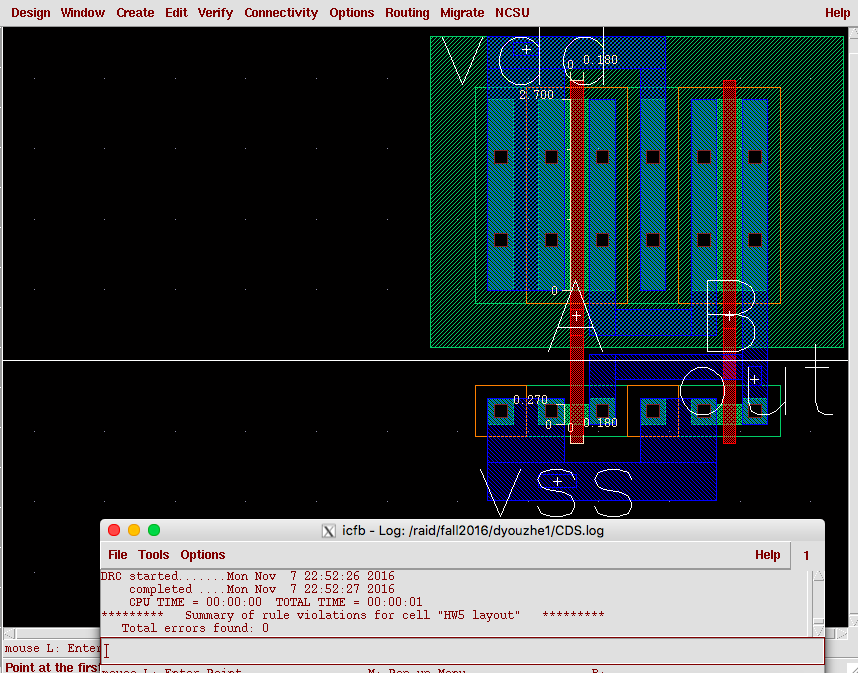
io\_B = 1'b1;

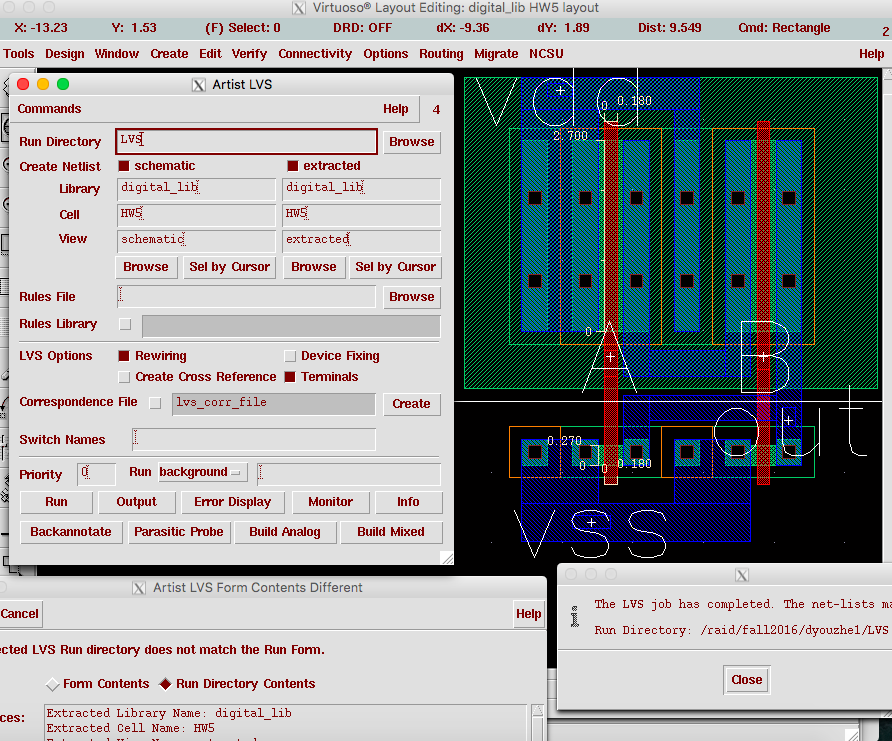
#20 $finish;

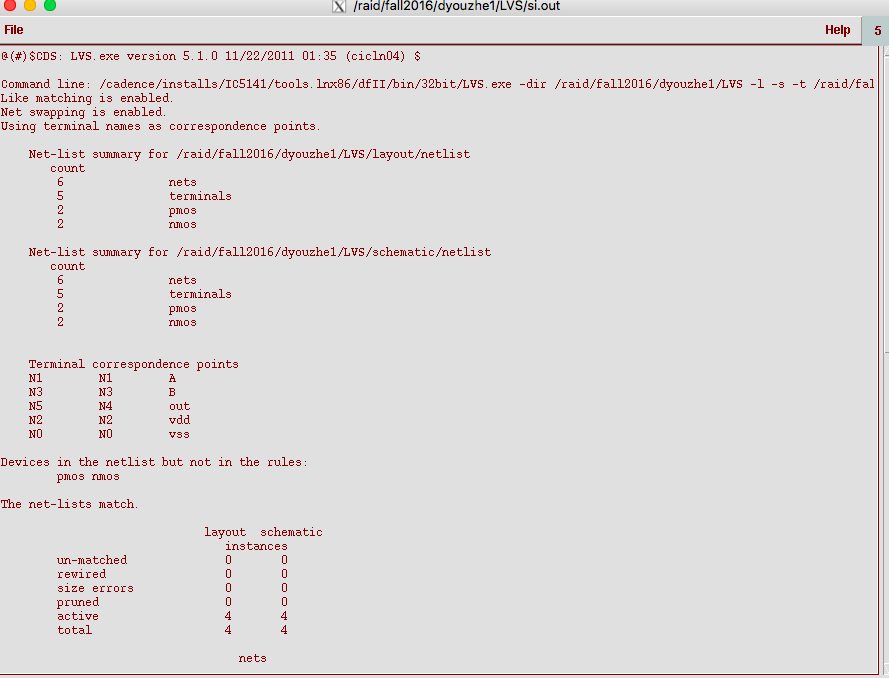
end



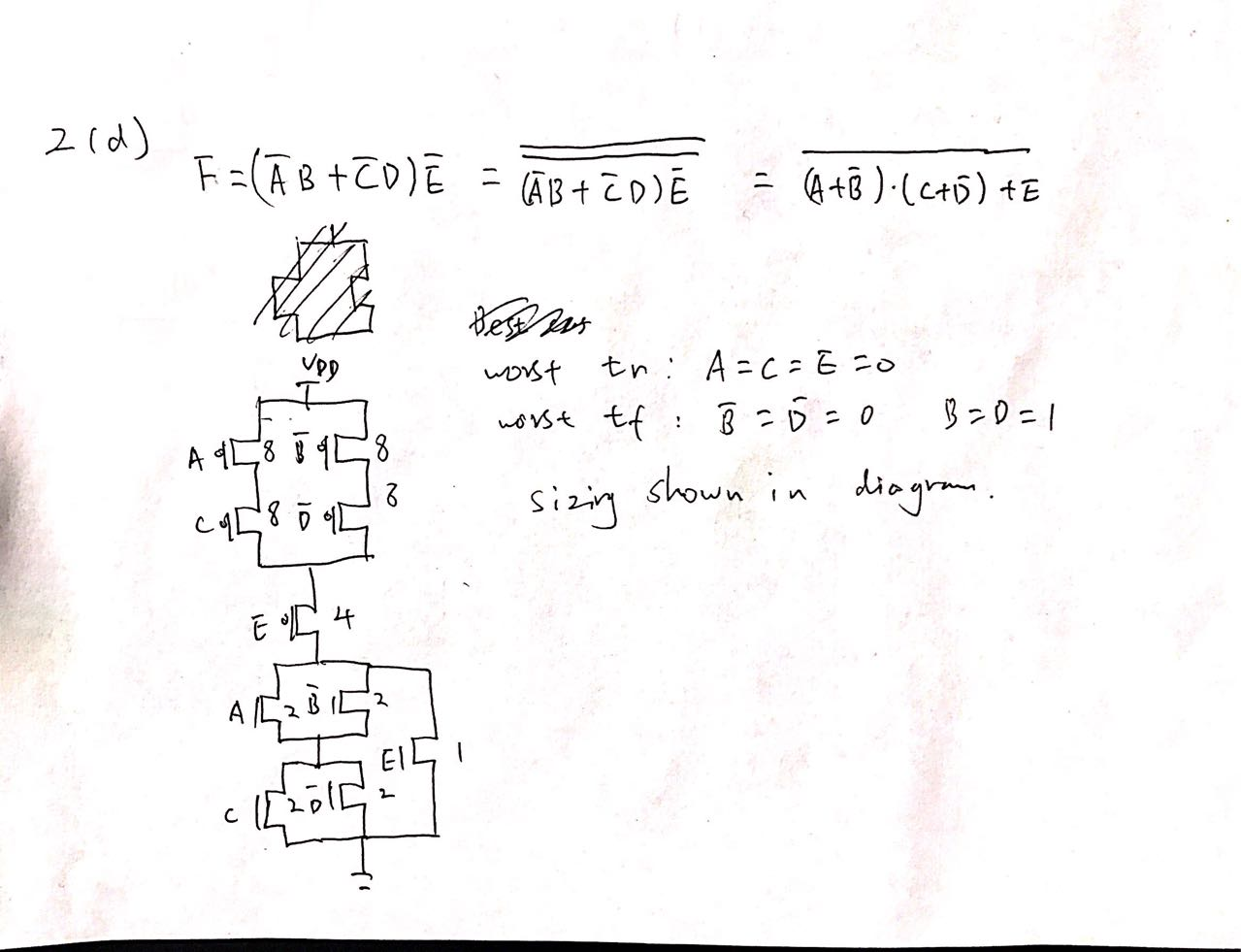
(c)

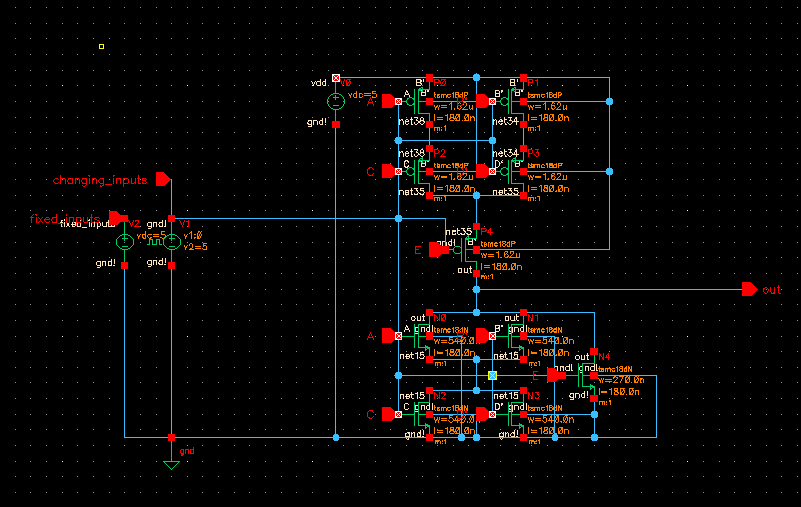


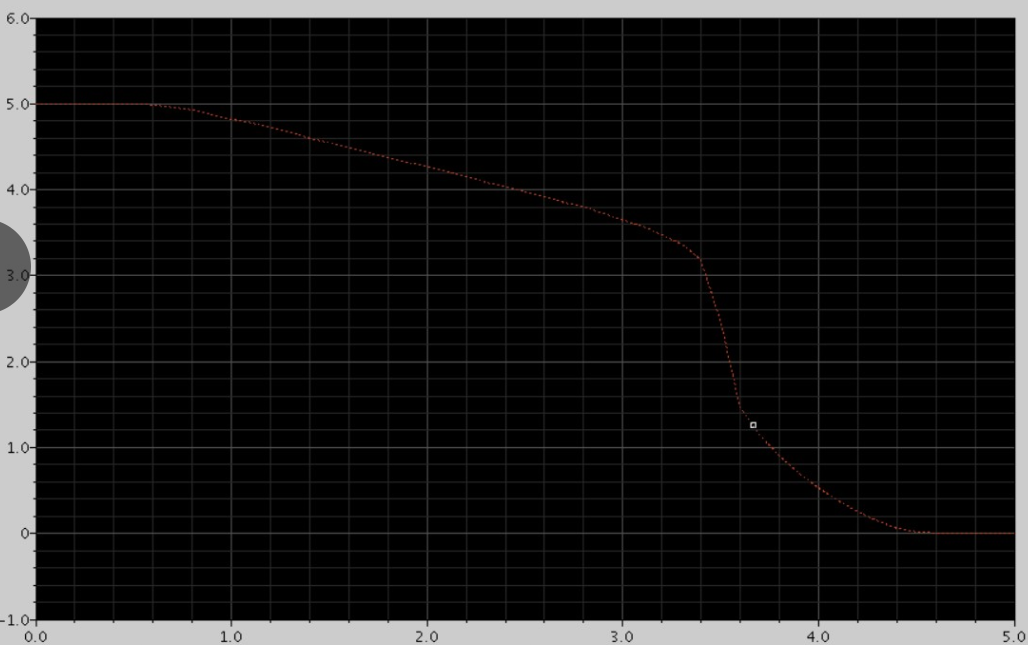


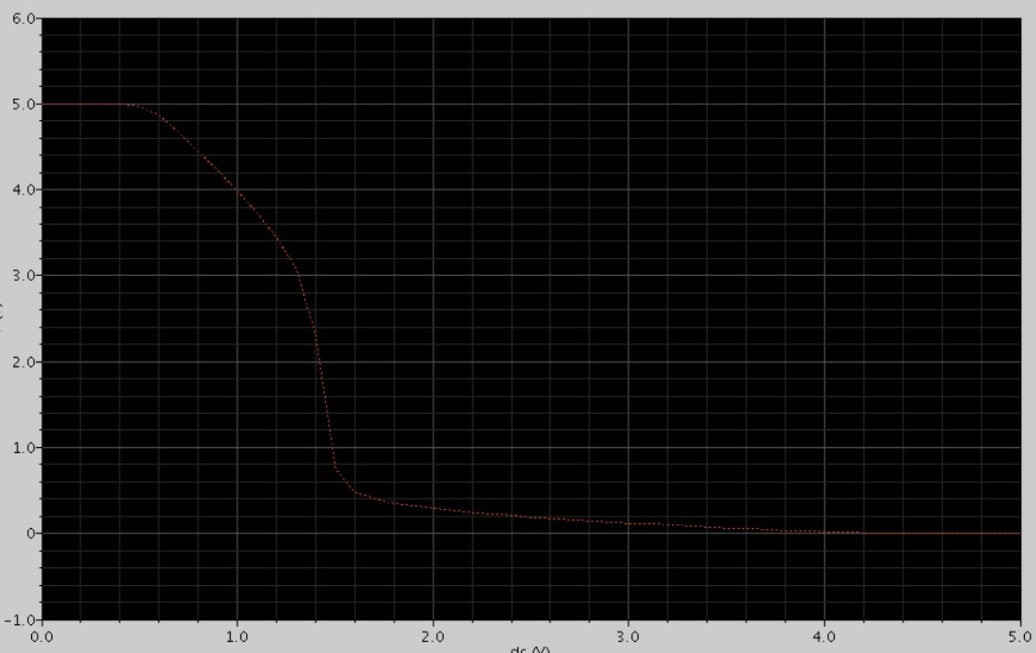


(d)

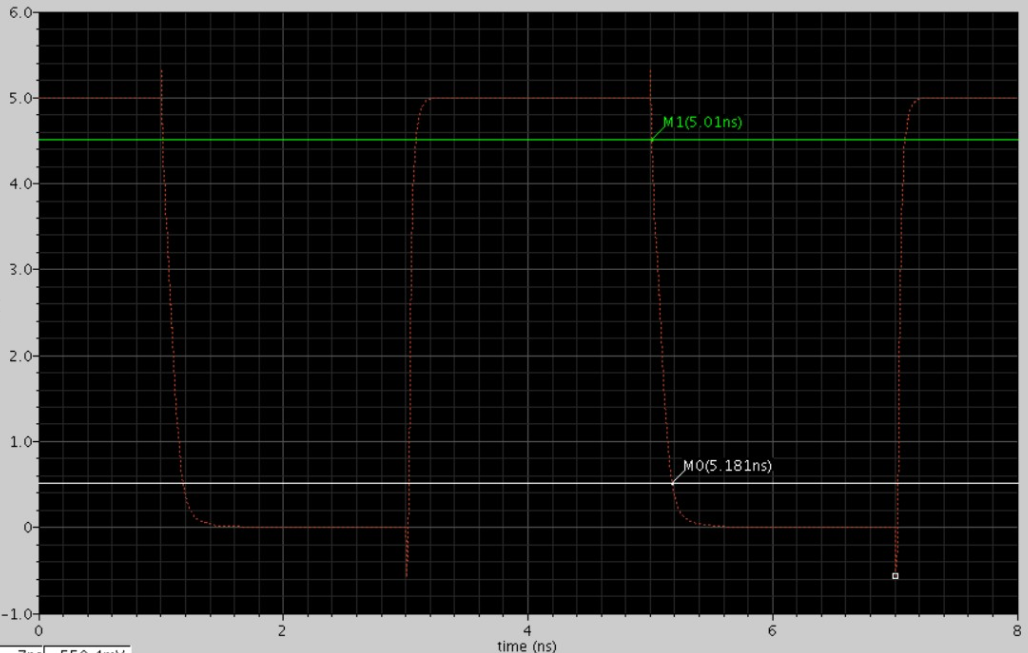




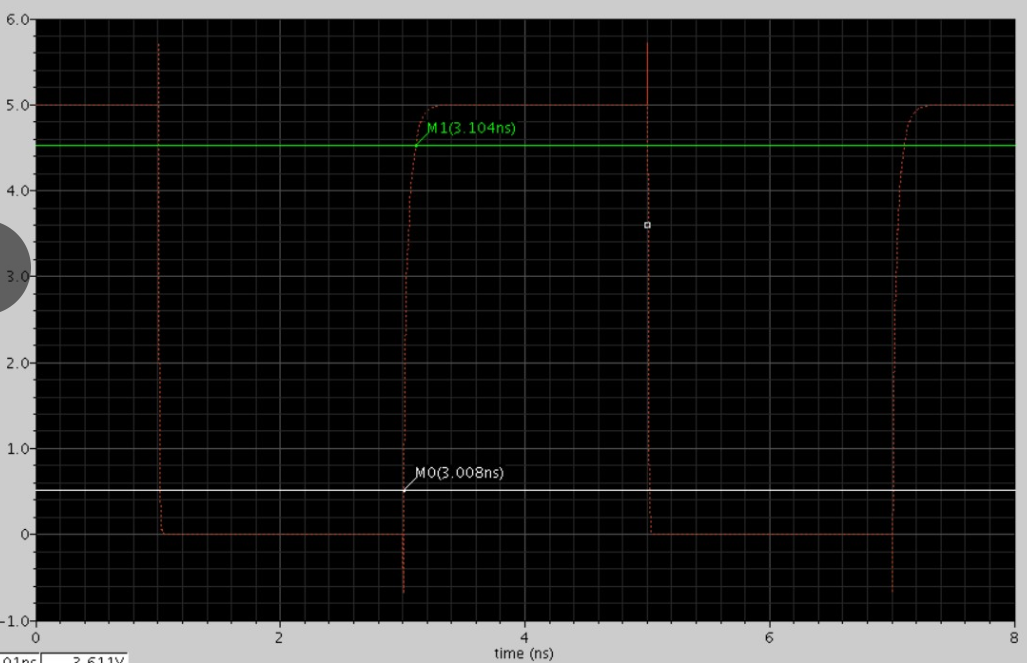




DC analysis for worst case rise and fall time.



Worst fall time=0.17 ns



Worst rise time =0.096 ns

