HW6

Youzhe Dou

Basic building primitives:

NAND gate:

Verilog code:

module HW6nand (out,a,b);

inout a;

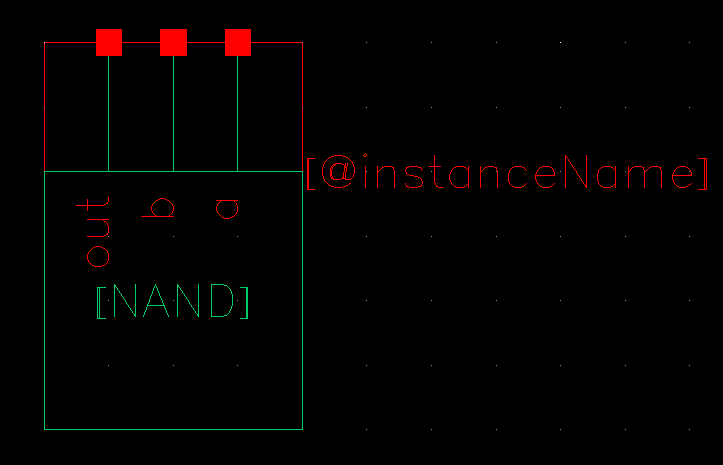
inout b;

inout out;

nand #(1,0.5) n1(out,a,b);

Endmodule

Symbol:



Inverter:

Verilog code:

module HW6inv (in,out);

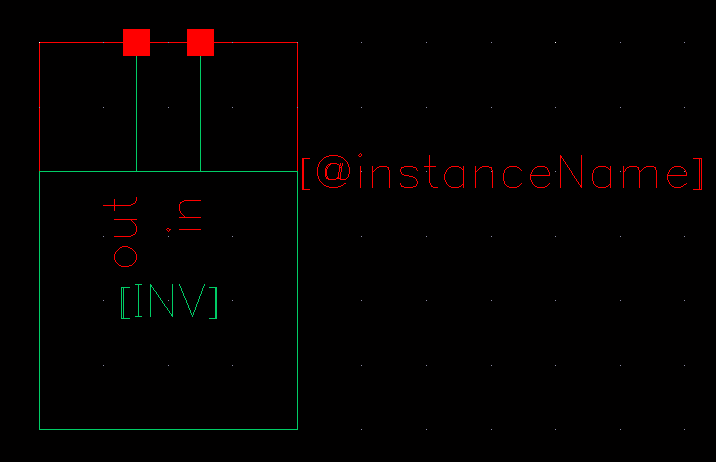
inout in;

inout out;

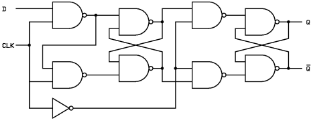
not #1 inv1(out,in);

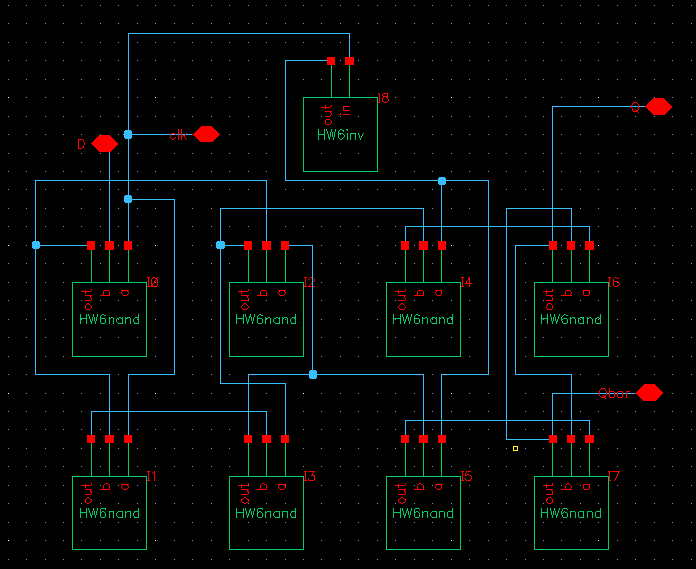
Endmodule

Symbol:

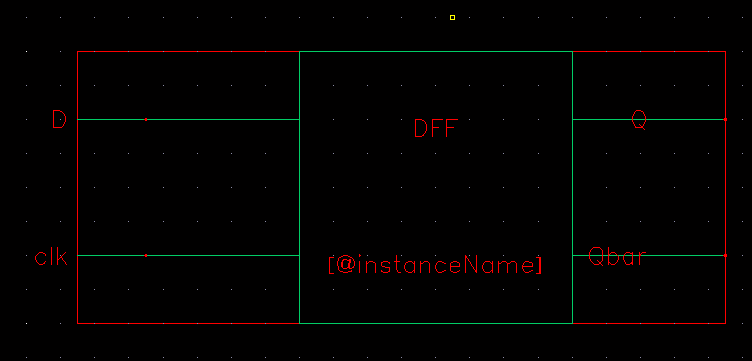


From NAND and inverter, we can build a D Flip-Flop using master slave structure in schematic.

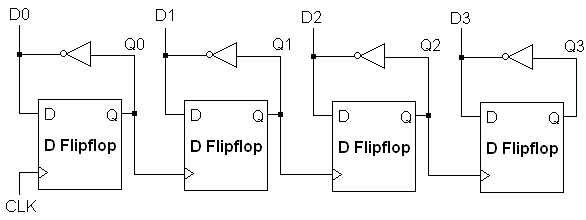


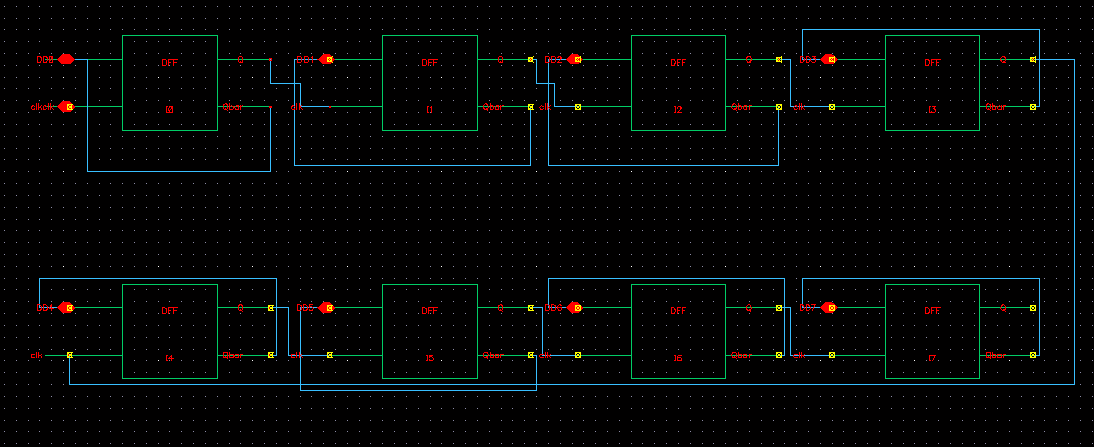


Generate a symbol for DFF:



Build the 8 bits counter in schematic using the following structure.





Verilog simulation of 8-bits counter:

module HW6nand (out,a,b);

inout a;

inout b;

inout out;

nand #(1,0.5) n1(out,a,b);

Endmodule

module HW6inv (in,out);

inout in;

inout out;

not #1 inv1(out,in);

Endmodule

module DFF\_d(d, clk, q,qbar);

inout d;

inout clk;

wire wire [7:0] Q;

wire clk\_bar;

HW6inv i1(clk\_bar,clk);

HW6nand n0(Q[0],d,clk);

HW6nand n1(Q[1],Q[0],clk);

HW6nand n2(Q[2],Q[0],Q[3]);

HW6nand n3(Q[3],Q[1],Q[2]);

HW6nand n4(Q[4],Q[2],clk\_bar);

HW6nand n5(Q[5],Q[3],clk\_bar);

HW6nand n6(Q[6],Q[4],Q[7]);

HW6nand n7(Q[7],Q[5],Q[6]);

assign q=Q[6];

assign qbar=Q[7];

endmodule

module HW6Top(clk,cnt\_out);

inout clk;

inout [7:0] cnt\_out;

wire [7:0] Q1;

wire [7:0] Q2;

DFF\_d d0( Q2[0],clk,Q1[0],Q2[0]);

DFF\_d d1( Q2[1],Q1[0],Q1[1],Q2[1]);

DFF\_d d2( Q2[2],Q1[1],Q1[2],Q2[2]);

DFF\_d d3( Q2[3],Q1[2],Q1[3],Q2[3]);

DFF\_d d4( Q2[4],Q1[3],Q1[4],Q2[4]);

DFF\_d d5( Q2[5],Q1[4],Q1[5],Q2[5]);

DFF\_d d6( Q2[6],Q1[5],Q1[6],Q2[6]);

DFF\_d d7( Q2[7],Q1[6],Q1[7],Q2[7]);

assign cnt\_out=Q2;

Endmodule

initial

begin

io\_clk = 1'bz;

io\_cnt\_out[7:0] = 8'bzzzzzzzz;

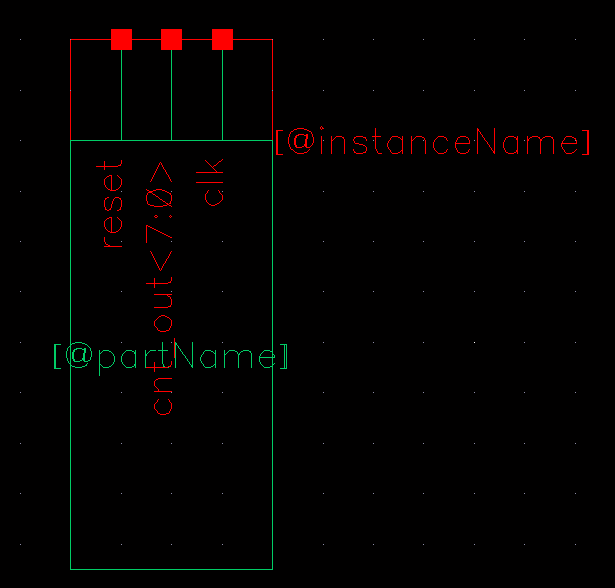
#50

io\_clk = 1'b0;

#1000000 $finish;

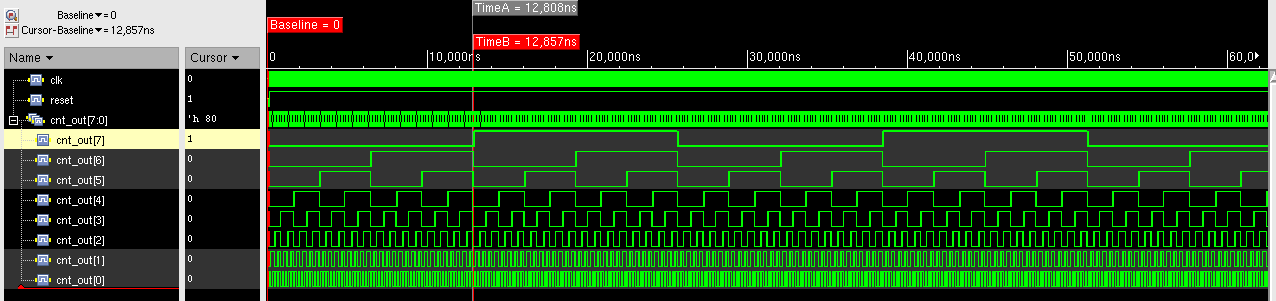
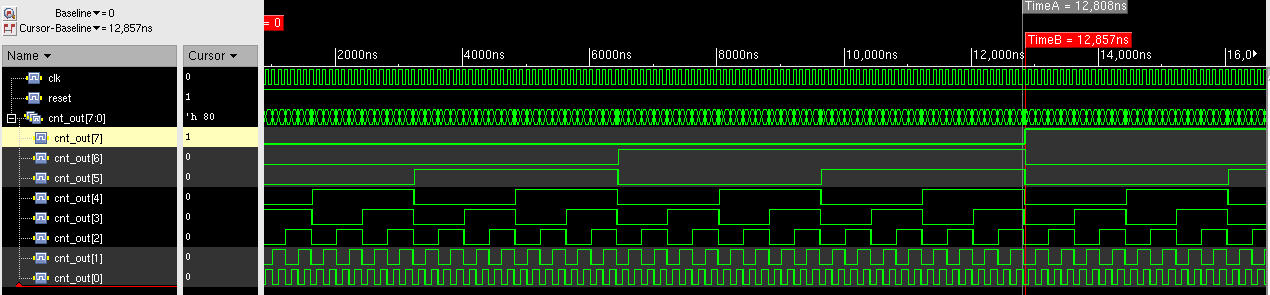
end

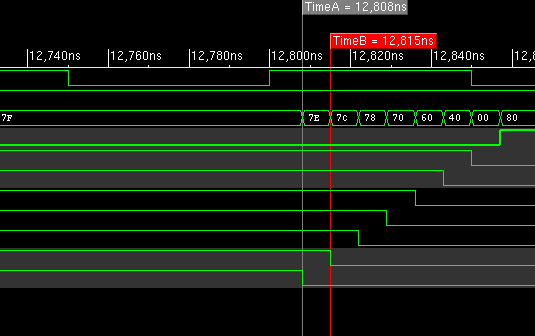
always #50 io\_clk = ~io\_clk;



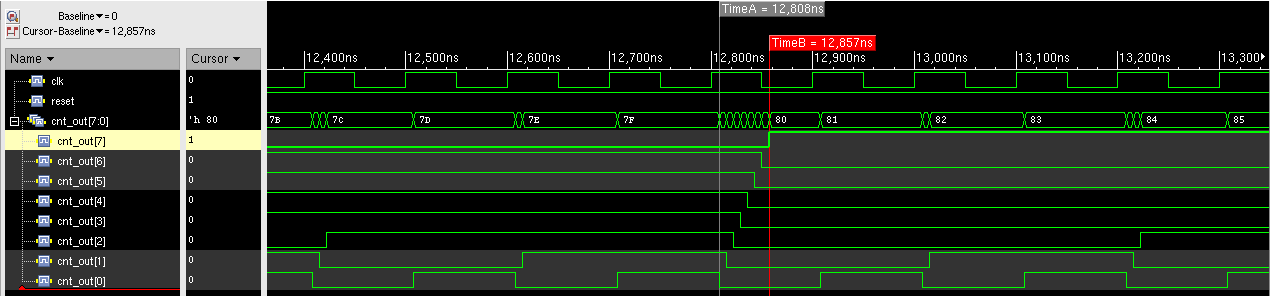
Waveform:

Showing all the states:





The longest delay through one DFF is 7 ns (12815-12808).



Therefore the longest delay for 8 bits counter is 57ns (12857-12800). This happens when the most significant bit toggles.

Therefore the maximum frequency is 1/49\*10^9=17.544 MHz.