Dual-Channel PWM Generator

Principle of Operation: Dual-Channel PWM Generator

The pulse-width modulation (PWM) signal is generated using two Numerically Controlled Oscillators (NCOs)—one for determining the PWM frequency and the other for setting the duty cycle. The NCO operates based on the principles of phase accumulation and waveform synthesis.

The output frequency fo of the PWM signal is defined by:

$$fo = (FCW * fclk) / (2^N)$$

where:

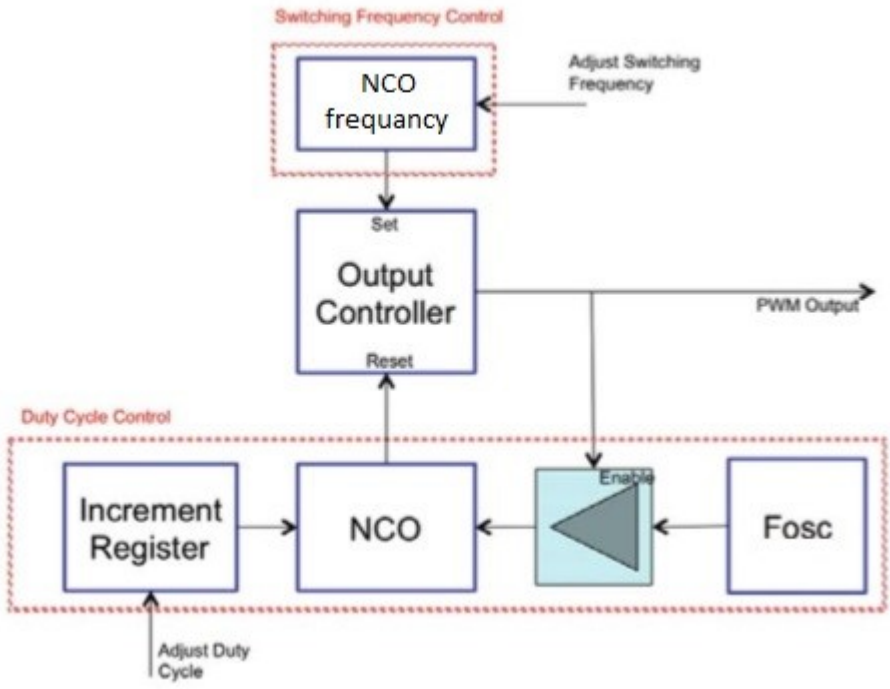
- fclk is the system clock frequency,

- 2^N represents the resolution of the phase accumulator,

- FCW is the frequency control word.

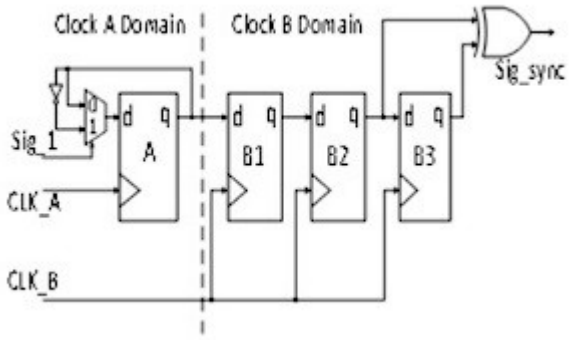
The duty cycle (pulse-on time) is calculated as:

$$Ton = duty / (fo * 100)$$



PWM Generator Control Interface

The frequency and duty cycle control words are stored in registers and updated using a 33 MHz clock, with data and write-enable signals facilitating transmission. To ensure precise synchronization with the 100 MHz PWM controller frequency, the write-enable signal is aligned using a pulse-toggle synchronizer. To mitigate PWM pulse signal glitches, control signals are applied only after the completion of the current PWM signal period, and the phase accumulator values are reset to maintain signal integrity.



Testbench Implementation

Manual Test Mode

In this mode, the user sets the desired frequency (Hz) and duty cycle (%) for both channels. The test computes the required control words for frequency and duty cycle, writes them to the appropriate registers, and averages the output PWM period and duty cycle over a variable number of cycles. The measured output values are then compared with the expected values from the test.

The allowable frequency and duty cycle errors can be adjusted using the FREQ_ERROR and DUTY_ERROR parameters. For faster simulations, the frequency error is set to 0.8 Hz. The NCO accumulator bit size can be modified via the W_DUTY and W_PERIOD parameters.

Random Test Mode

In this mode, random frequency and duty cycle values are assigned to both channels. The measured PWM output frequency and duty cycle are then compared against the expected values to validate correctness.