

CLASE 1

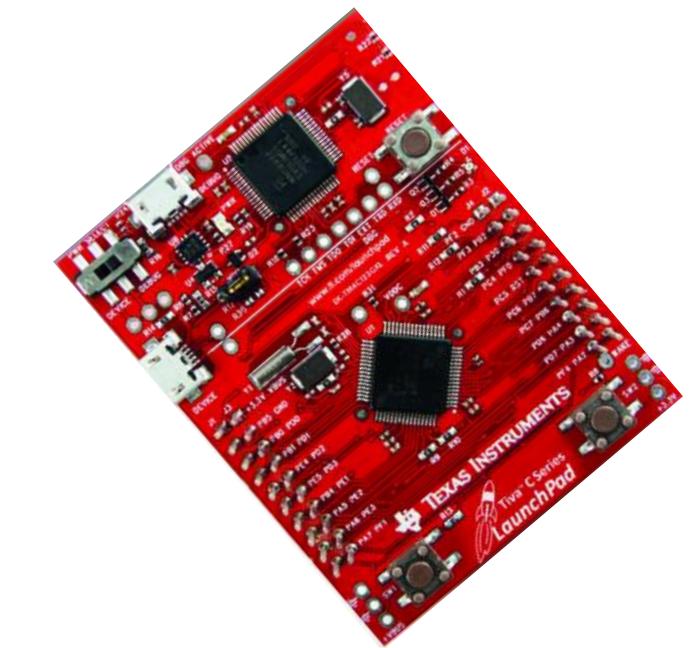
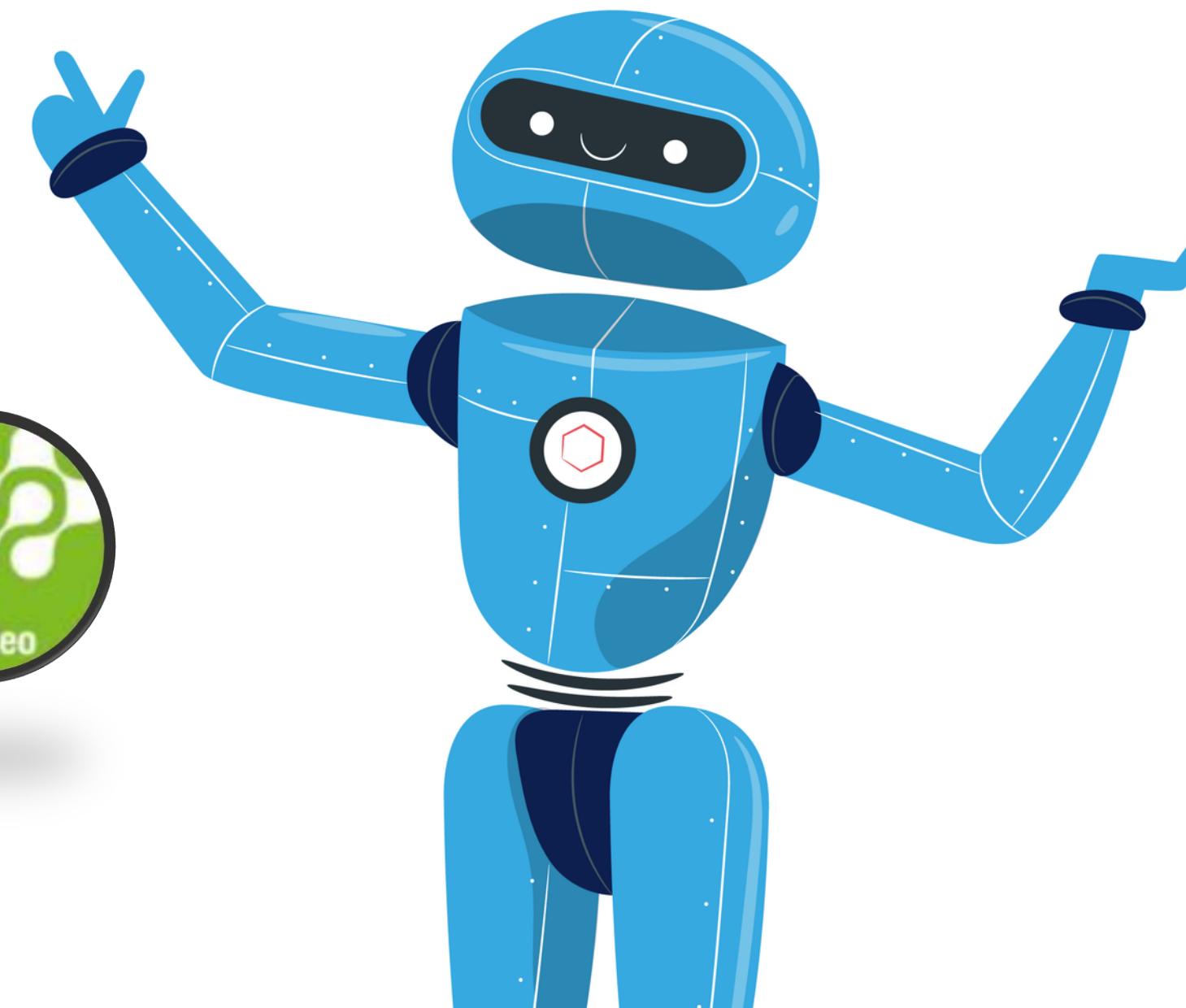
INTRODUCCION A LOS

MICROCONTROLADORES

ARM



life.augmented



INTRODUCCION A LA ARQUITECTURA ARM

arm

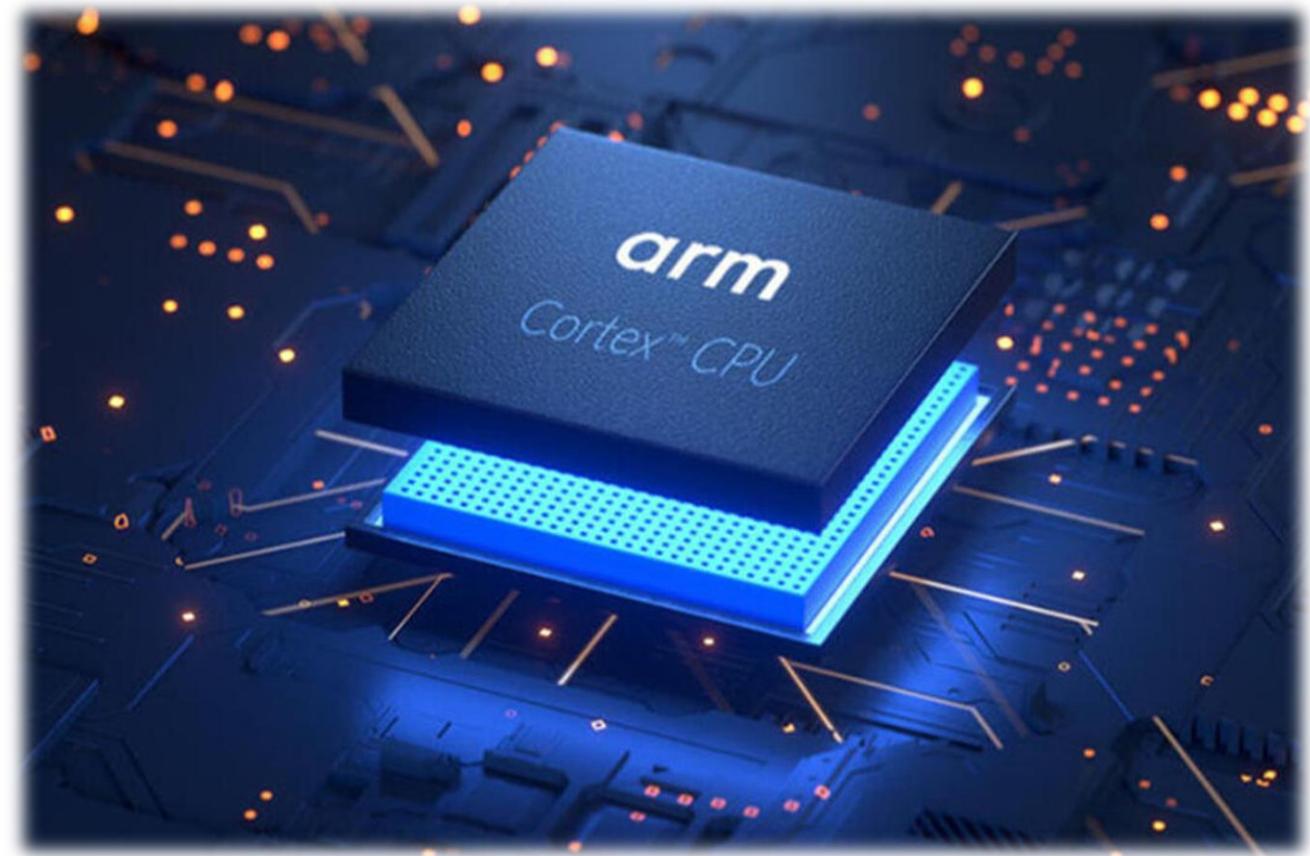
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¿QUE ES ARM?



ARM Holdings



PROCESADOR ARM



DIFERENCIA ENTRE PROCESADOR ARM Y ARQUITECTURA ARM

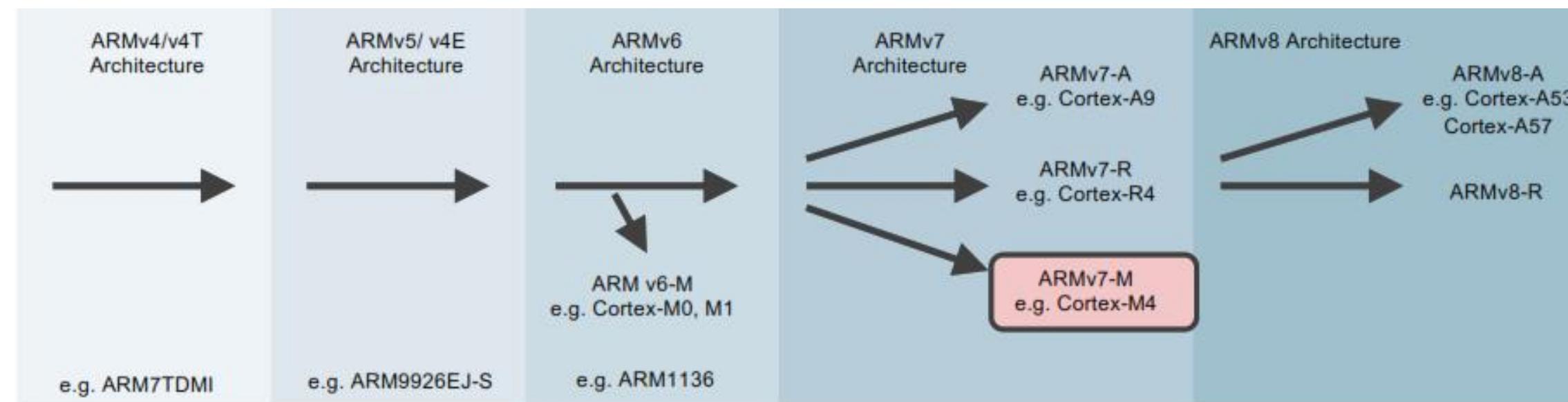
- **ARQUITECTURA ARM**

- Describe los detalles de instrucciones, modelo de programación, interrupciones, mapa de memoria.
- Esta documentada en el manual de referencia de la arquitectura.

- **PROCESADOR ARM**

- Desarrollado en base a una de las arquitecturas ARM
- Contiene detalles de implementación real, como diagramas de tiempos, mapa concreto de memoria.

Su documentación principal es la hoja de características (processor's Technical Reference Manual).



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ESPECIFICACIONES DE LA ARQUITECTURA

Instruction set

- La función de cada instrucción.
- Cómo se representa esa instrucción en la memoria (su codificación).

Register set

- Cuántos registros hay.
- El tamaño de los registros.
- La función de los registros.
- Su estado inicial.

Exception model

- Los diferentes niveles de privilegio.
- Los tipos de excepciones.
- Qué sucede al aceptar o regresar de una excepción.

Memory model

- Cómo se ordenan los accesos a la memoria.
- Cómo se comportan las cachés, cuándo y cómo el software debe realizar un mantenimiento explícito.

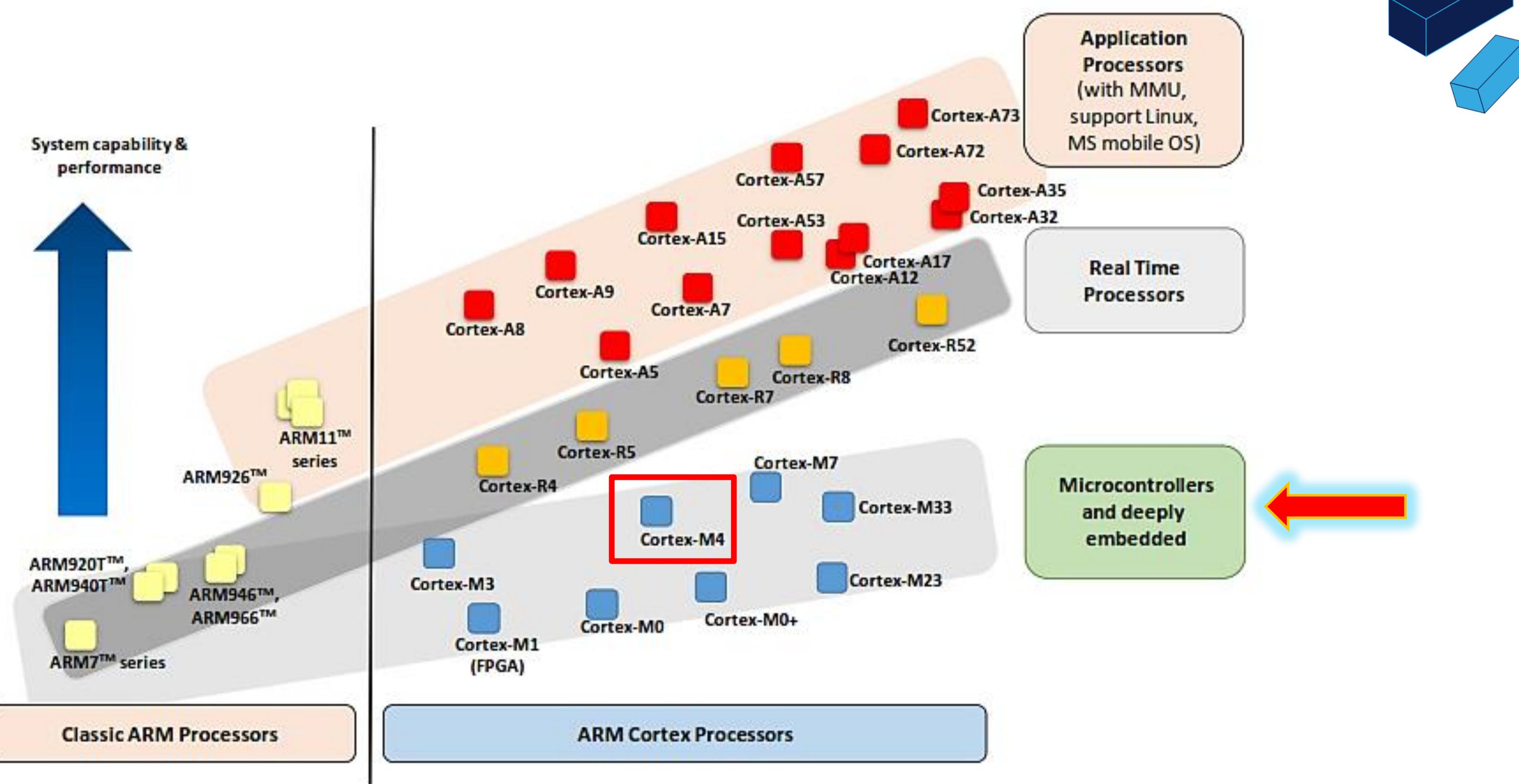
Debug, trace, and profiling

- Cómo se establecen y activan los puntos de interrupción.
- Qué información se puede capturar con las herramientas de rastreo y en qué formato.

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LA FAMILIA DE PROCESADORES ARM



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CARACTERISTICAS DE LA ARQUITECTURA ARM

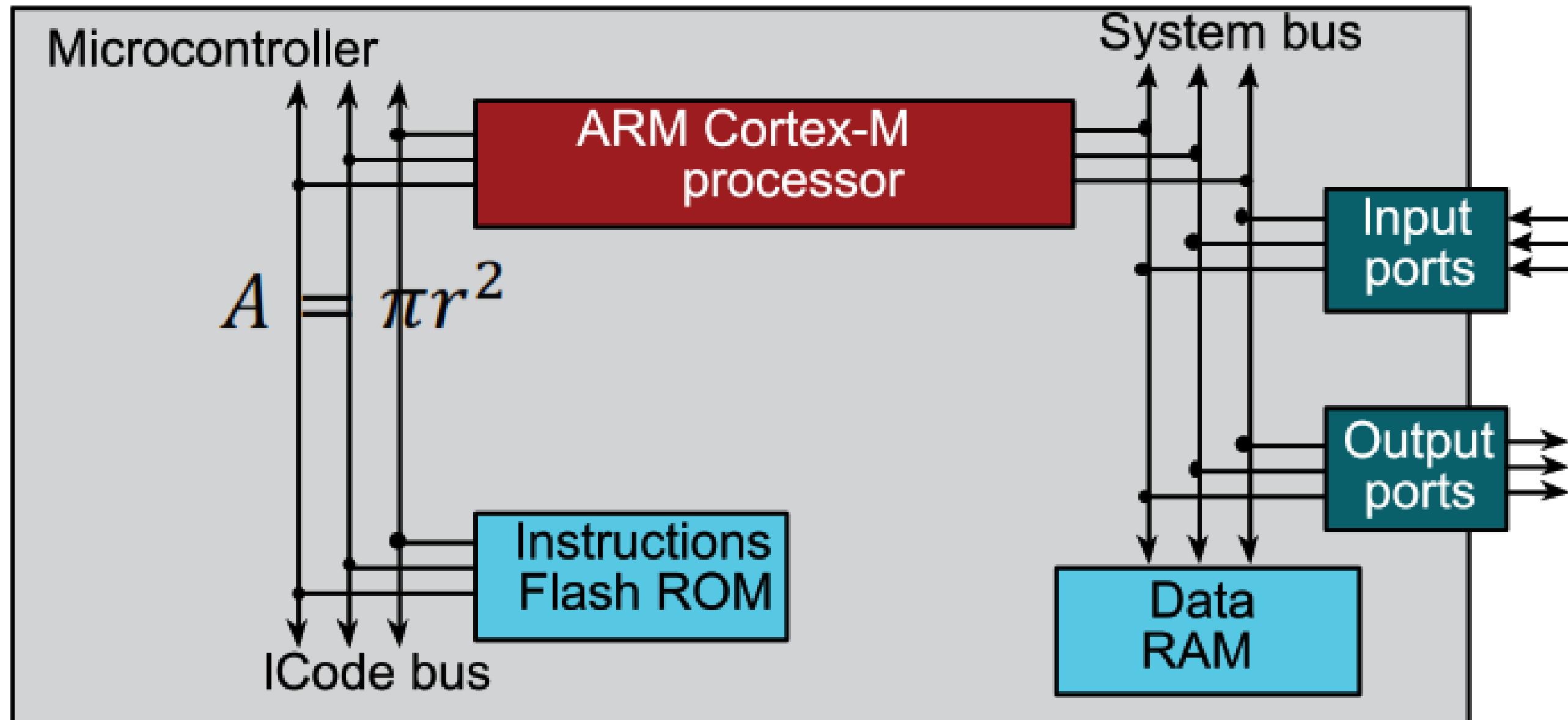
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PROCESADOR CORTEX - M

- Arquitectura Hardvard vs Von Neuman.
- Diferentes buses para instrucciones y datos.
 - ICode bus → Fetch op codes from ROM
 - System bus → Data from RAM and I/O
 - Dcode bus → Debugging
 - PPB bus → Private peripherals



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PROCESADOR CORTEX - M

BUS AMBA (Advanced Microcontroller Bus Architecture)

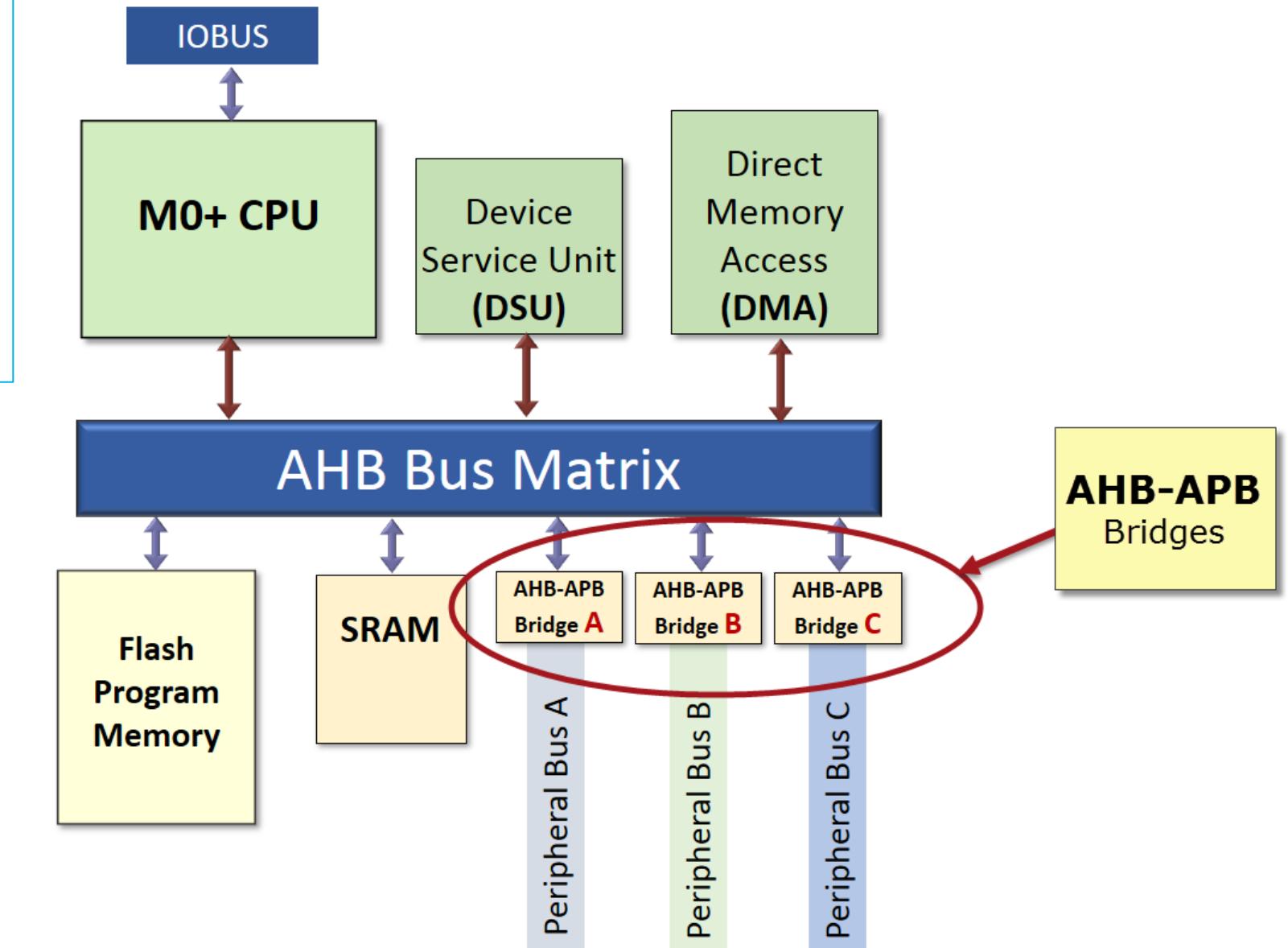
Advanced High-performance Bus (AHB)

- conectar componentes que necesitan mayor ancho de banda en un bus compartido.
- alto rendimiento.
- operación canalizada.
- Transferencia en ráfaga.
- Comunicación maestro esclavo

Advanced Peripheral Bus (APB)

- se utiliza para conectar periféricos de ancho de banda bajo.
- Low power
- Interfaz simple
- Apta para muchos periféricos

Los dos puentes AHB / APB, proporcionan conexiones sincrónicas completas entre el AHB y los dos buses APB, lo que permite una selección flexible de la frecuencia periférica.

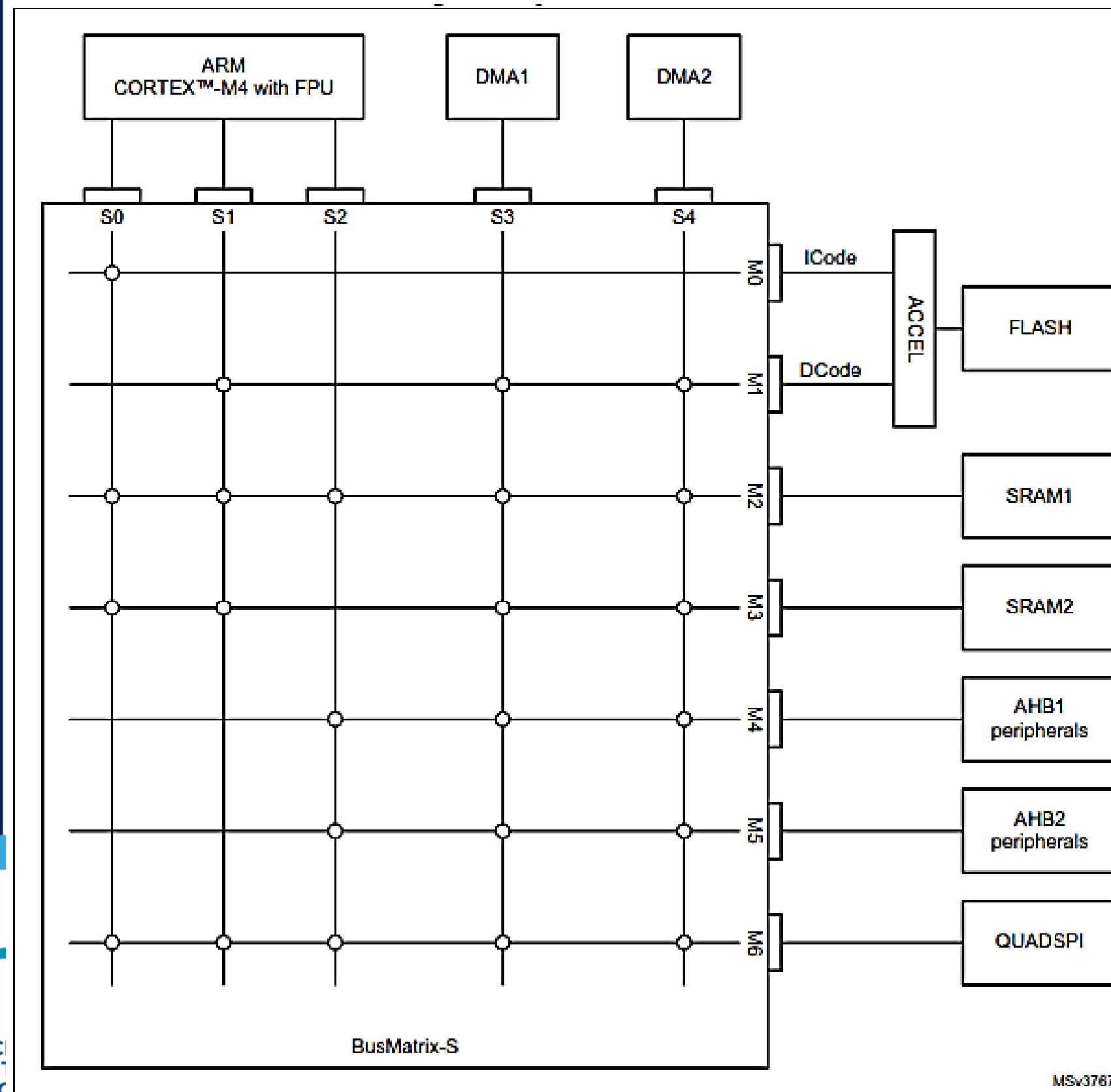


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BUS MATRIX



La matriz de bus proporciona acceso de un maestro a un esclavo, lo que permite el acceso concurrente y operación eficiente incluso cuando varios periféricos de alta velocidad funcionan simultáneamente

S0: I-Bus

S1: D-Bus

S2: S-Bus

S3, S4: DMA-Bus

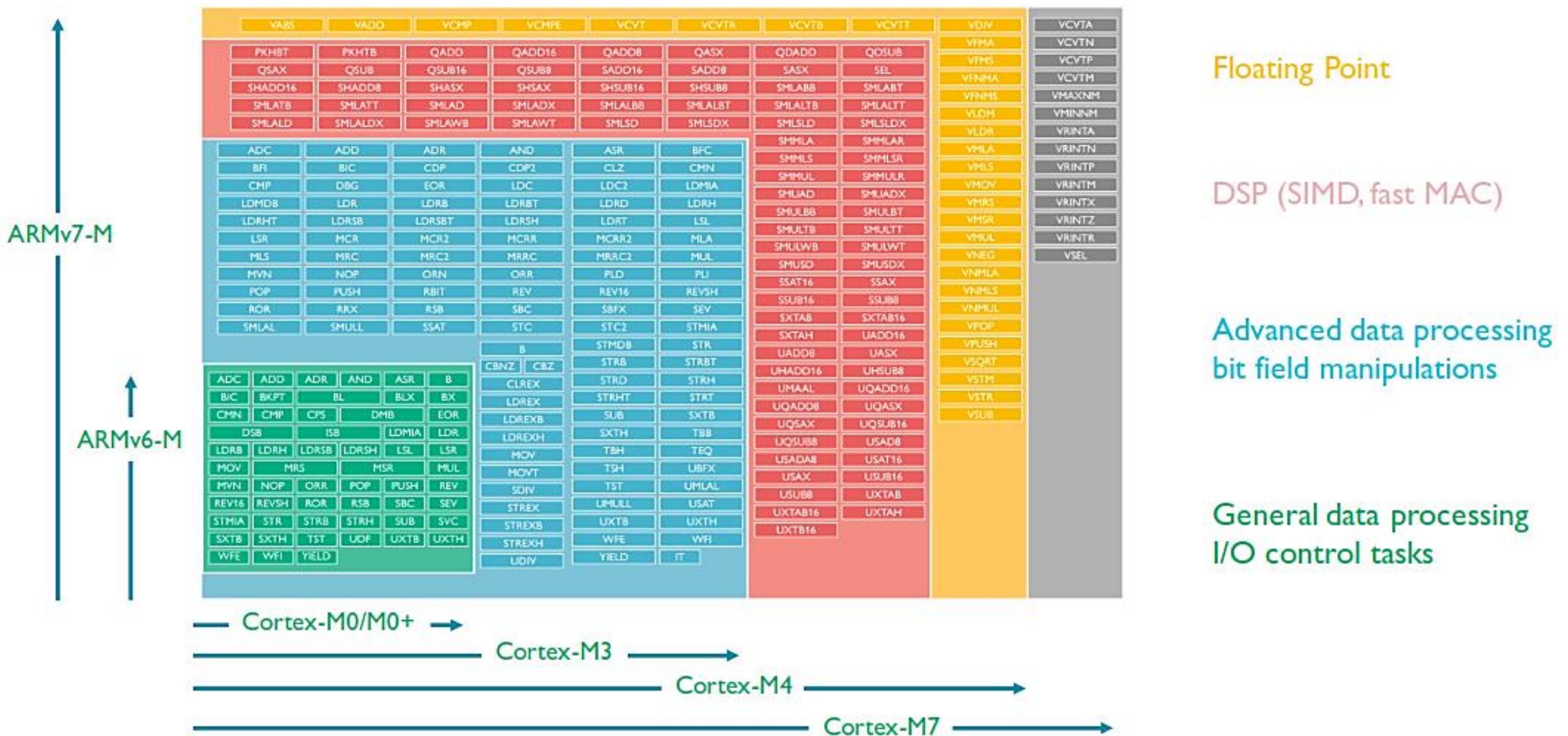
STM32L412XX

- Five masters:
 - Cortex®-M4 with FPU core I-bus
 - Cortex®-M4 with FPU core D-bus
 - Cortex®-M4 with FPU core S-bus
 - DMA1
 - DMA2
- Seven slaves:
 - Internal Flash memory on the ICode bus
 - Internal Flash memory on DCode bus
 - Internal SRAM1
 - Internal SRAM2
 - AHB1 peripherals including AHB to APB bridges and APB peripherals (connected to APB1 and APB2)
 - AHB2 peripherals
 - The external memory controller (QUADSPI)

PROCESADOR CORTEX - M

CONJUNTO DE INSTRUCCIONES DE LOS PROCESADORES CORTEX-M

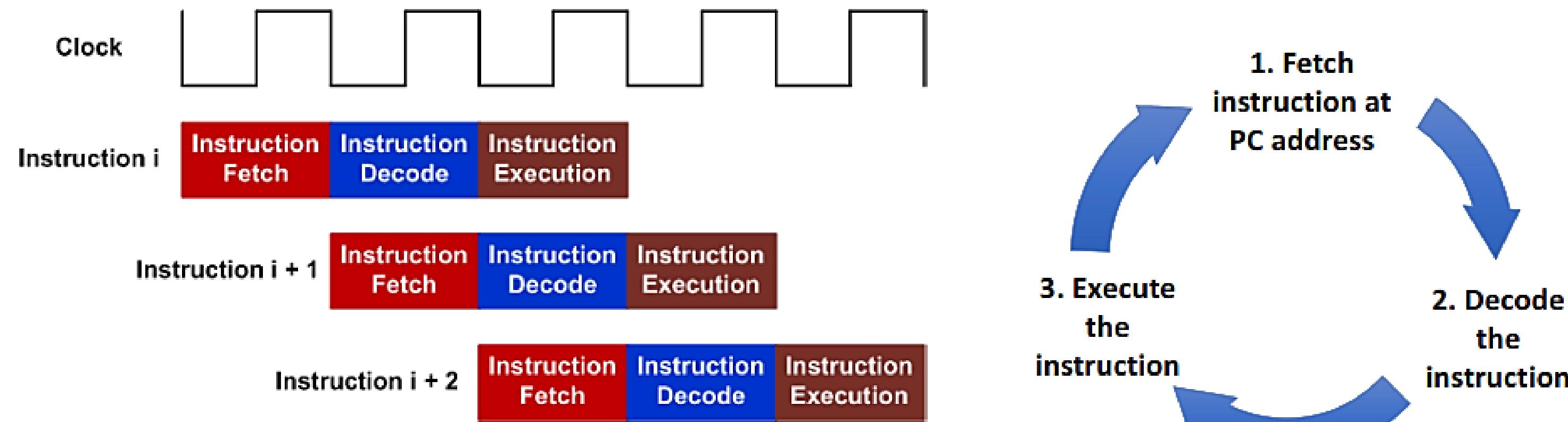
Todos los procesadores Cortex-M admiten un conjunto de instrucciones llamado Thumb. Sin embargo, diferentes procesadores Cortex-M admiten diferentes subconjuntos de las instrucciones disponibles en Thumb ISA



PROCESADOR CORTEX - M

Three-state pipeline: Fetch, Decode, Execution

- La **canalización (Pipelining)** permite que los recursos de hardware se utilicen por completo.
- Se puede obtener una instrucción de 32 bits o dos instrucciones de 16 bits.



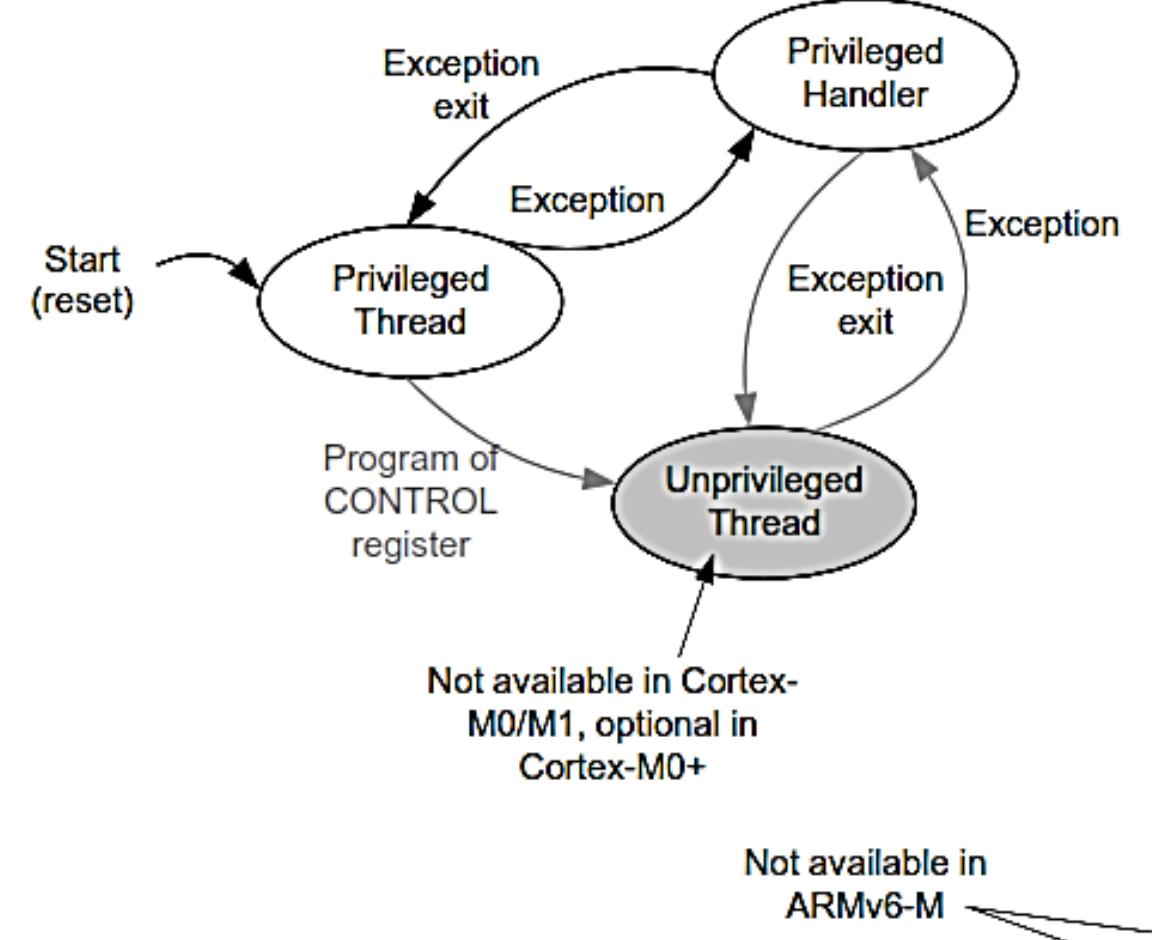
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PROCESADOR CORTEX - M

Programmer's model

Los registros R0 a R15, PSR, CONTROL y PRIMASK están disponibles para todos los procesadores Cortex-M. Dos registros especiales **FAULTMASK** y **BASEPRI**- están disponibles solo en Cortex-M3, Cortex-M4, Cortex-M7 y Cortex-M33, y el banco de registros de coma flotante y **FPSCR** está disponible en Cortex -M4 / M7 / M33 dentro de la unidad de coma flotante opcional.



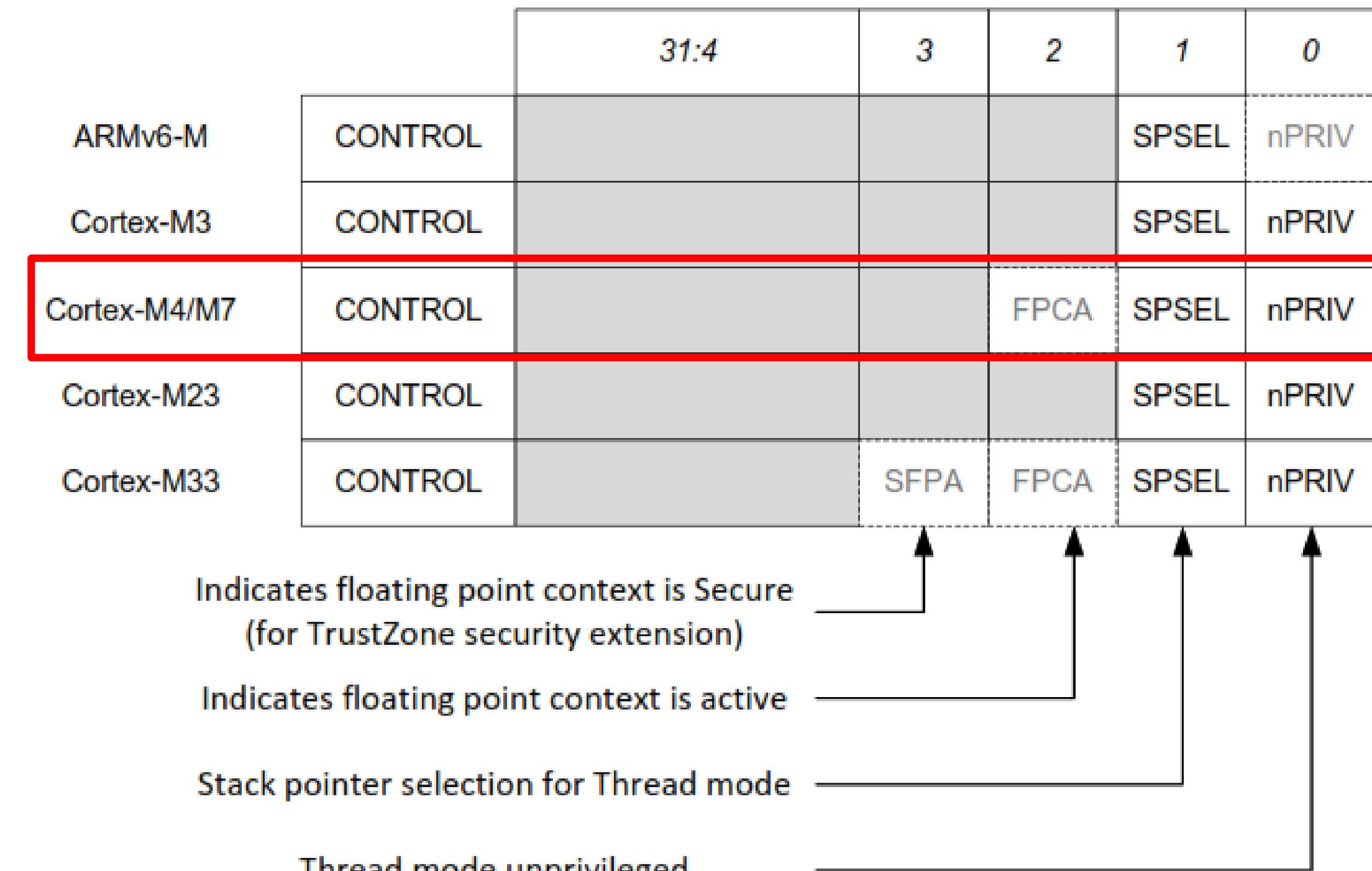
Available on the Cortex-M4 with FPU only				
Floating Point Unit				
R0	S0	D0		
R1	S2	D1		
R2	S4	D2		
R3	S6	D3		
R4	S8	D4		
R5	S10	D5		
R6	S12	D6		
R7	S14	D7		
R8	S16	D8		
R9	S18	D9		
R10	S20	D10		
R11	S22	D11		
R12	S24	D12		
R13 (MSP)	S26	D13		
R13 (PSP)	S28	D14		
R14	S30	D15		
R15	FPSCR Floating Point Status and Control Register			
Main Stack Pointer (MSP), Process Stack Pointer (PSP)				
Link Register (LR)				
Program Counter (PC)				
Name				
xPSR	Program Status Registers			
PRIMASK				
FAULTMASK				
BASEPRI				
CONTROL				
Functions				
Interrupt Mask Registers				
Control Register				
Special Registers				

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PROCESADOR CORTEX - M

CONTROL REGISTER



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PROCESADOR CORTEX - M

PROGRAM STATUS REGISTER

	31	30	29	28	27	26:25	24	23:20	19:16	15:10	9	8	7	6	5	4:0	Exception Number
ARMv6-M (Cortex-M0/M0+)	N	Z	C	V			T										↓
ARMv7-M (Cortex-M3)	N	Z	C	V	Q	ICI/IT	T			ICI/IT						Exception Number	
ARMv7E-M (Cortex-M4/M7)	N	Z	C	V	Q	ICI/IT	T		GE[3:0]	ICI/IT						Exception Number	
ARMv8-M Baseline (Cortex-M23)	N	Z	C	V			T									Exception Number	
ARMv8-M Mainline (Cortex-M33)	N	Z	C	V	Q	ICI/IT	T		GE[3:0]	ICI/IT						Exception Number	

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PROCESADOR CORTEX - M

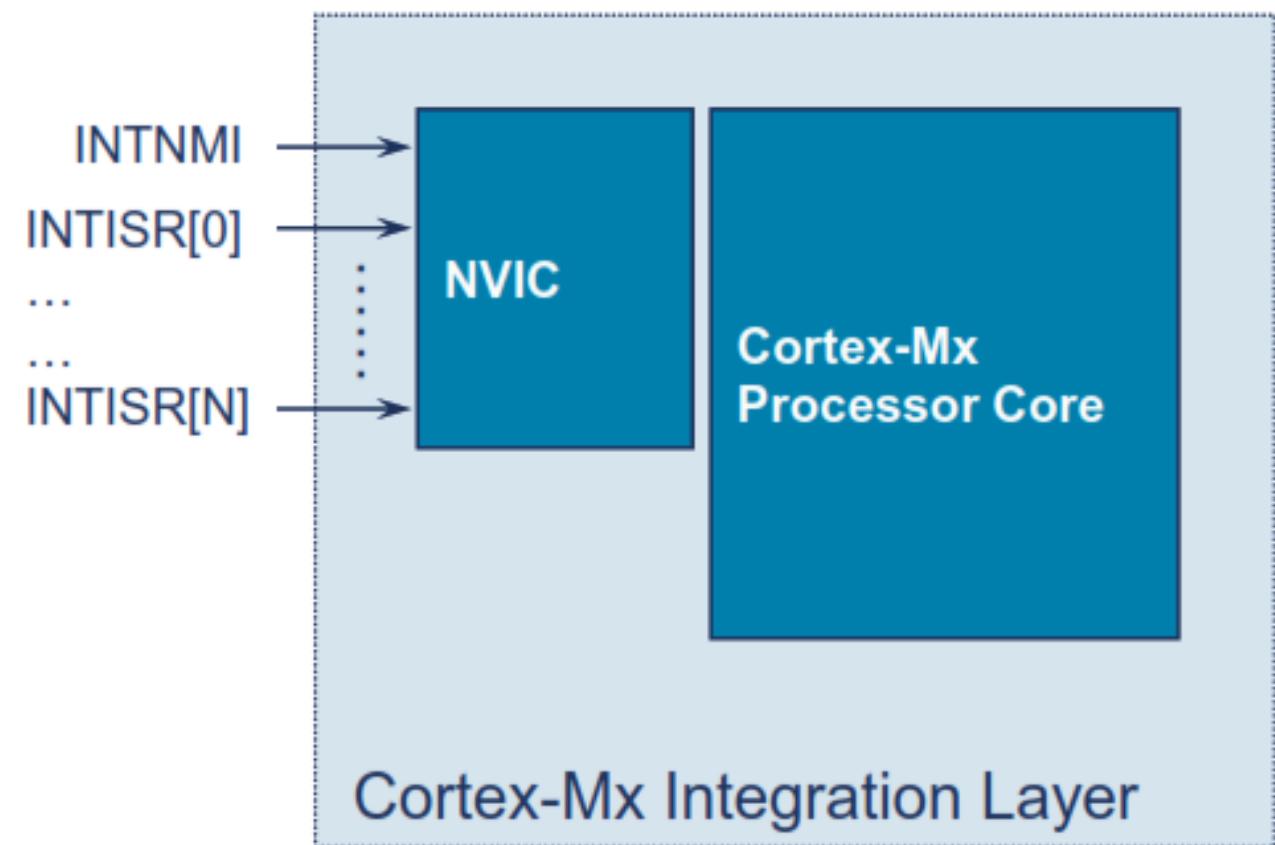
Exception model and NVIC

Todos los procesadores Cortex-M incluyen Controlador de interrupción vectorial anidado (NVIC) y comparten el mismo modelo de excepción.

- Reset
- Non-maskable Interrupts
- Faults
- PendSV
- SVCall
- External Interrupt
- SysTick Interrupt

INTERRUPT HANDLING

- Interrupts are a sub-class of exception
- Automatic save and restore of processor registers (xPSR, PC, LR, R12, R3-R0)
- Allows handler to be written entirely in 'C'



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PROCESADOR CORTEX - M

Exception model and NVIC

Exception Type	ARMv6-M (Cortex-M0/M0+/M1)	ARMv7-M (Cortex-M3/M4/M7)	ARMv8-M Baseline (Cortex-M23)	ARMv8-M Mainline (Cortex-M33)	Vector Table	Vector address offset (initial)
495		Not supported in Cortex-M3/M4/M7	Not supported in Cortex-M23		Interrupt#479 vector	0x0000007BC
256					Interrupt#239 vector	0x0000003FC
255					Interrupt#31 vector	0x0000000BC
31	Device Specific Interrupts	Device Specific Interrupts	Device Specific Interrupts	Device Specific Interrupts	Interrupt#1 vector	0x000000044
17					Interrupt#0 vector	0x000000040
16					SysTick vector	0x00000003C
15	SysTick	SysTick	SysTick	SysTick	PendSV vector	0x000000038
14	PendSV	PendSV	PendSV	PendSV	Not used	0x000000034
13	Not used	Not used	Not used	Not used	Debug Monitor vector	0x000000030
12		Debug Monitor		Debug Monitor	SVC vector	0x00000002C
11	SVC	SVC	SVC	SVC	Not used	0x000000028
10			Not used	Not used	Not used	0x000000024
9		Not used			Not used	0x000000020
8	Not used		Not used	SecureFault	SecureFault (ARMv8-M Mainline)	0x00000001C
7				Usage Fault	Usage Fault vector	0x000000018
6		Usage Fault	Not used	Bus Fault	Bus Fault vector	0x000000014
5		Bus Fault		MemManage (fault)	MemManage vector	0x000000010
4	MemManage (fault)				HardFault vector	0x00000000C
3	HardFault	HardFault	HardFault	HardFault	NMI vector	0x000000008
2	NMI	NMI	NMI	NMI	Reset vector	0x000000004
1					MSP initial value	0x000000000
0						

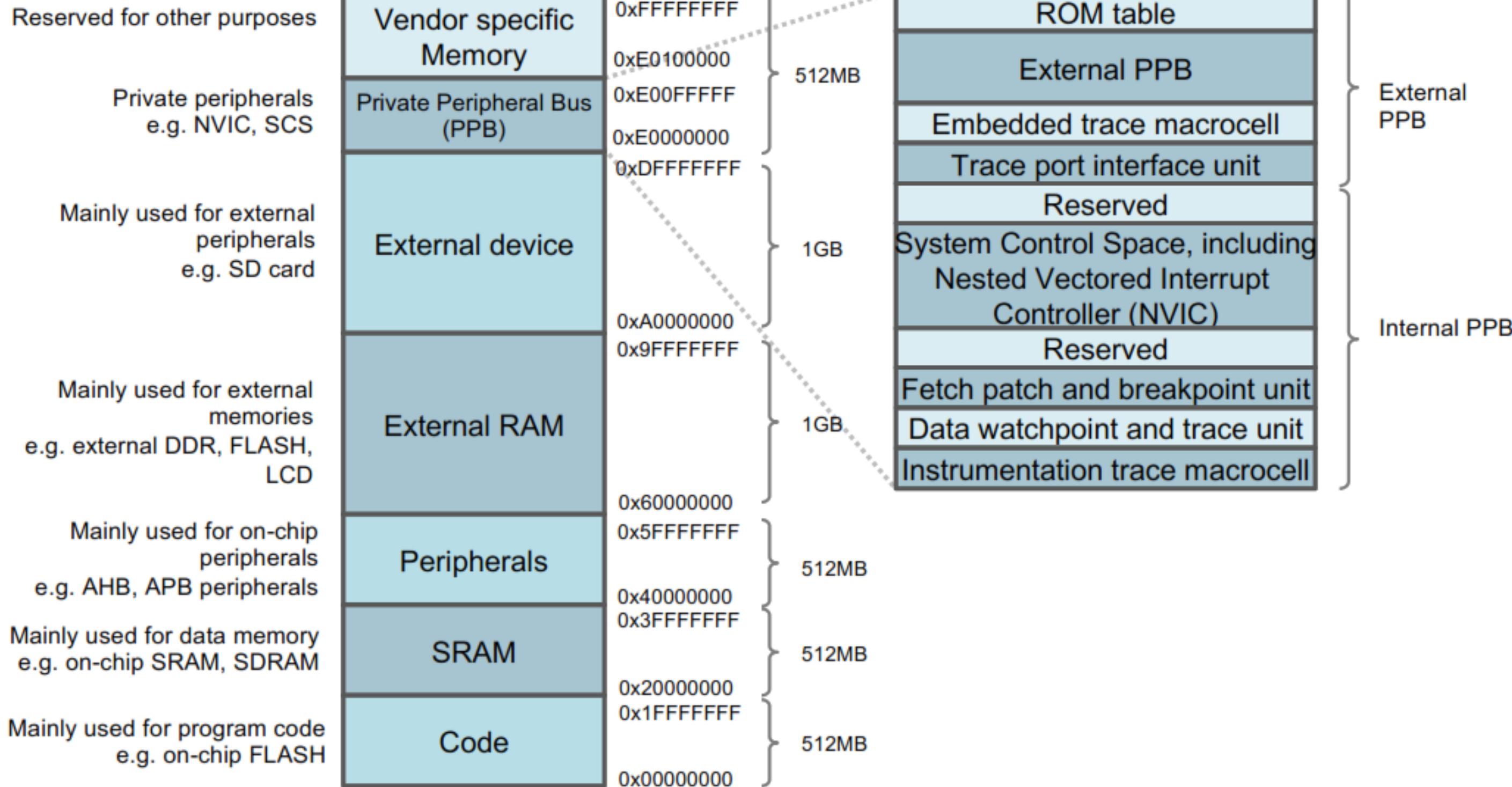
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PROCESADOR CORTEX - M

Memory MODEL



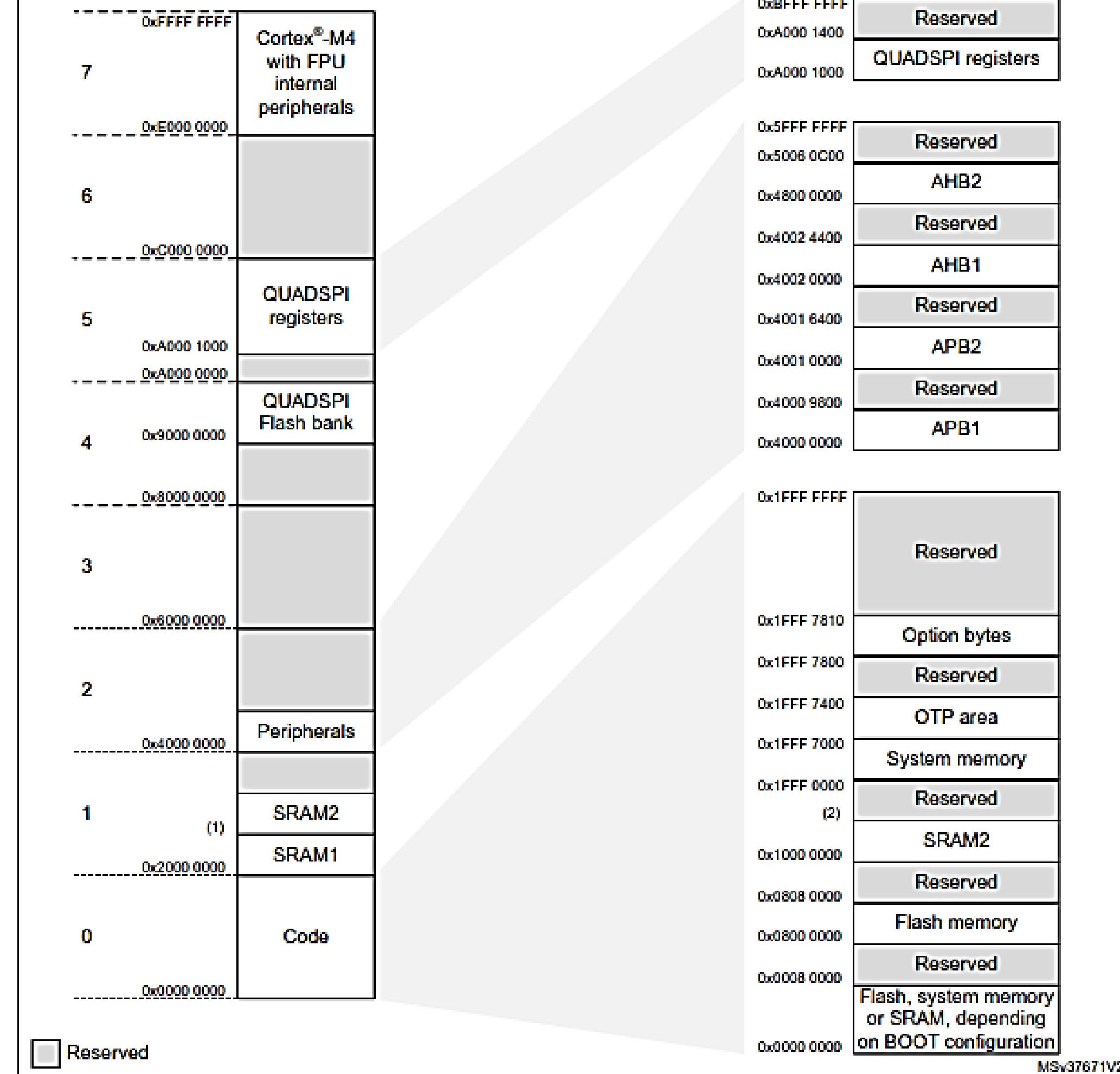
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Memory MODEL



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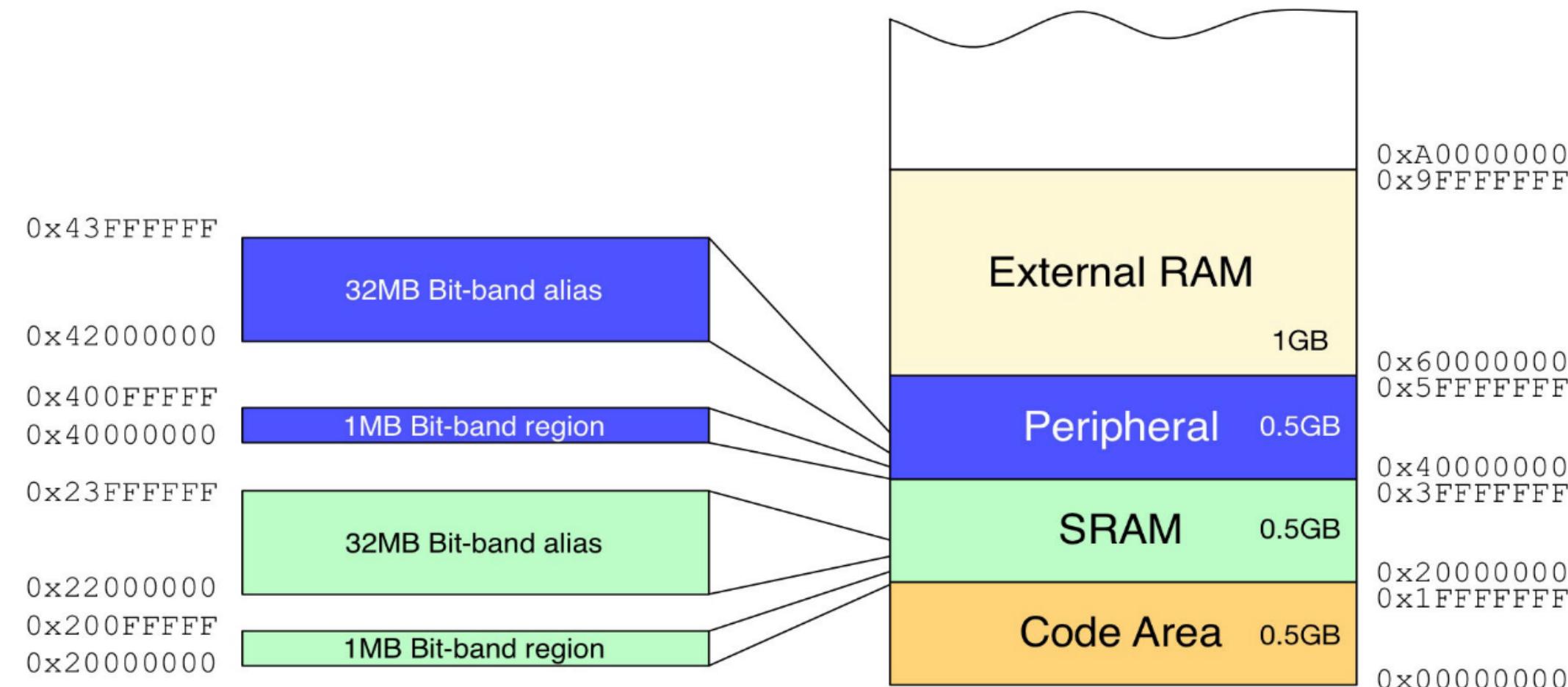


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Memory MODEL: Bit Band

Los procesadores Cortex-M3 y Cortex-M4 tienen una característica opcional llamada banda de bits que permite que dos rangos de direcciones de 1 MB (uno en SRAM, desde 0x20000000, el otro en Peripheral, desde 0x40000000) sean direccionables mediante bits a través de direcciones de alias de banda de bits.

- Bit- Banding es un método para realizar modificaciones atómicas bit a bit en la memoria.



PROCESADOR CORTEX - M

Memory MODEL: Bit Band

- Una fórmula de mapeo muestra cómo hacer referencia a cada palabra en la región alias a un bit correspondiente, o bit de destino, en la región BITBAND. La fórmula de mapeo es:

$$\text{bit_word_offset} = (\text{byte_offset} \times 32) + (\text{bit_number} \times 4)$$

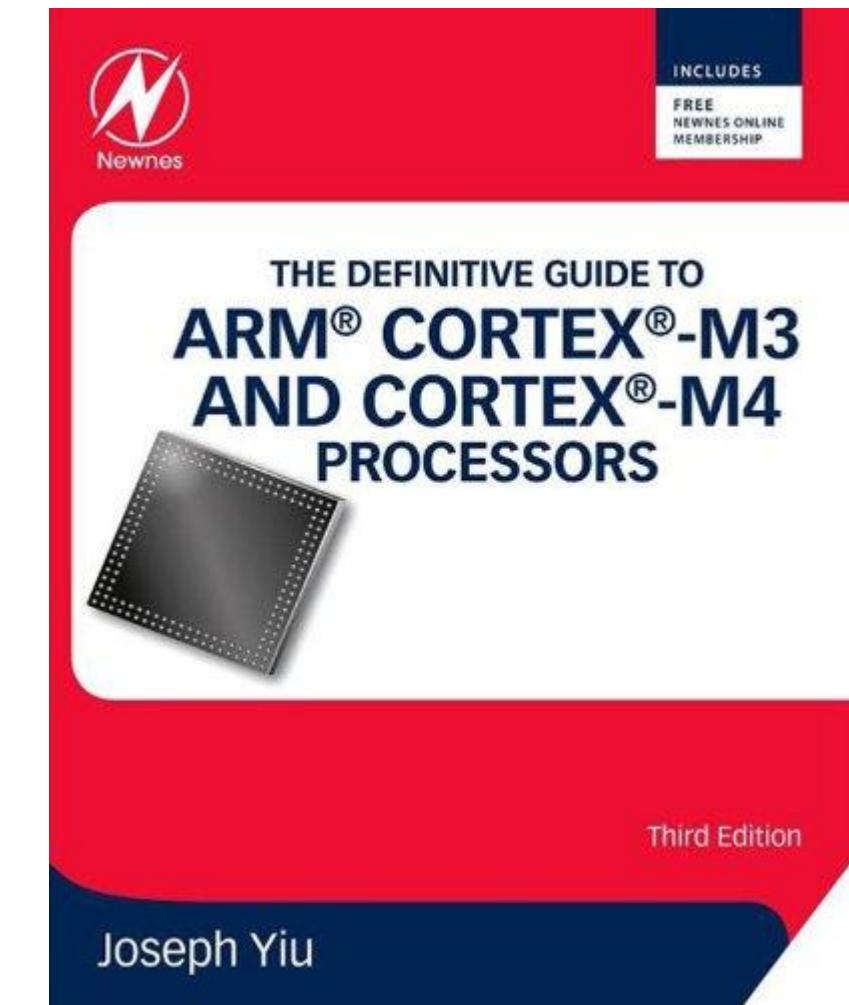
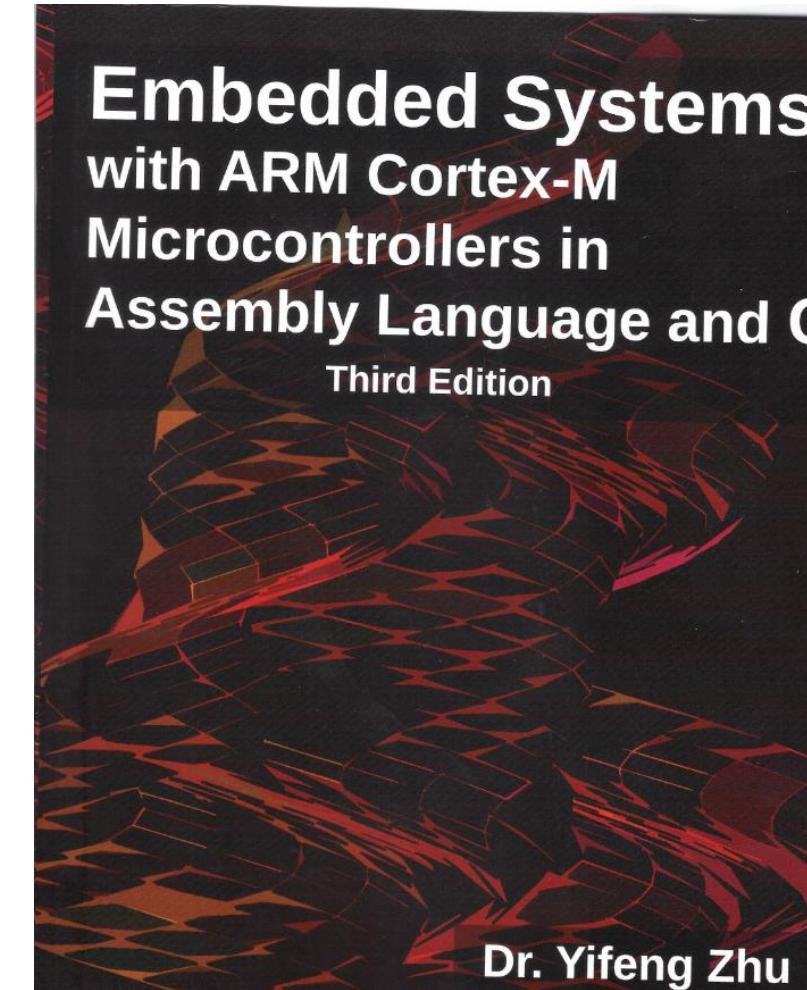
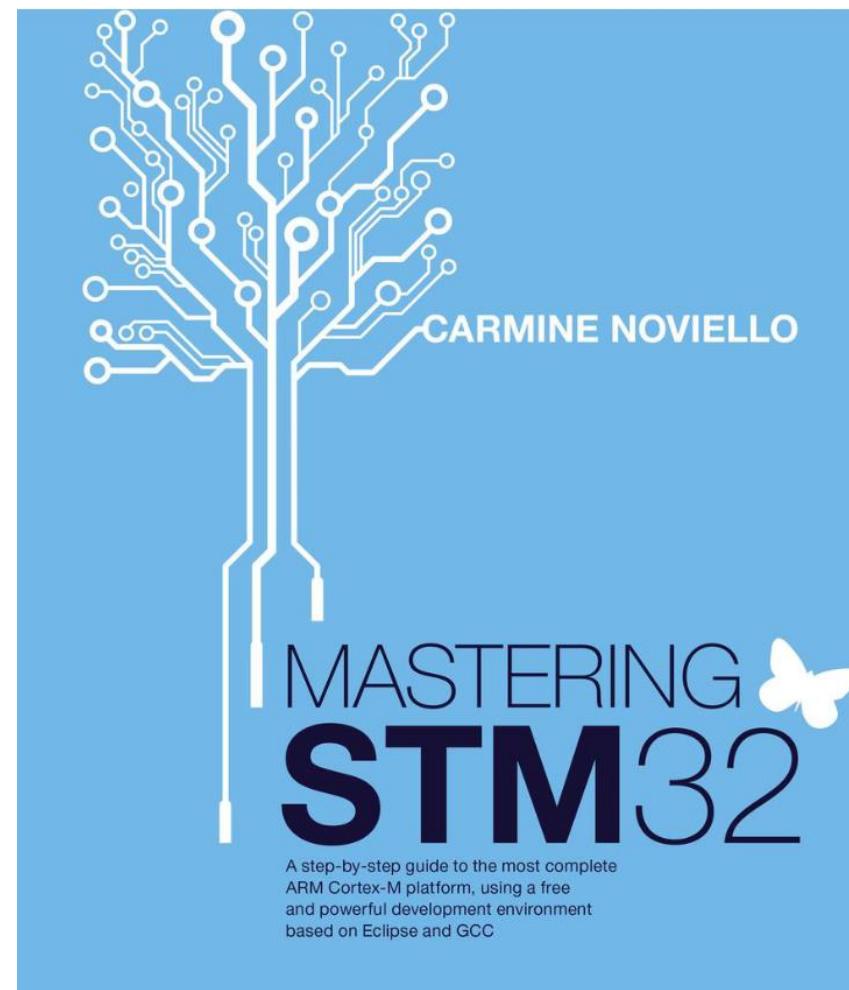
$$\text{bit_word_addr} = \text{bit_band_base} + \text{bit_word_offset}$$

Donde:

- ✓ **bit_word_offset**, es la posición del bit de destino en la región de memoria bit-band.
- ✓ **bit_word_addr**, es la dirección de la palabra en la región de memoria de alias que se asigna al bit de destino.
- ✓ **bit_band_base**, es la dirección inicial de la región de alias
- ✓ **byte_offset** es el numero del byte en la región bit-band que contiene el bit objetivo.
- ✓ **bit_number** es el bit posición, 0 a 7, de el bit objetivo.

PROCESADOR CORTEX - M

REFERENCIAS

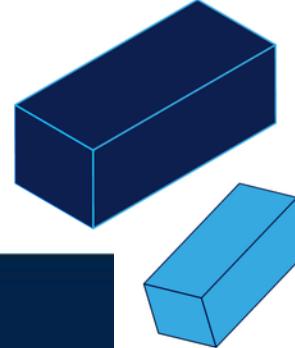


STM32

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Software



**STM32
CubeMX**

**STM32
CubeProgrammer**

**STM32
CubeIDE**

**STM32
CubeMonitor**

Hardware

**NUCLEO-L412KB
NUCLEO-F401RE**



**STM32
Nucleo**

Flexible prototyping



Discovery
kits



Evaluation
boards

Key feature
prototyping

Full feature
evaluation



Customer support



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Customer Support**



community.st.com

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OC**



wiki.st.com/stm32mpu
wiki.st.com/stm32mcu



github.com/STMicroelectronics



STM32 MCUs

32-bit Arm® Cortex®-M



High
Performance

STM32F2

398 CoreMark
120 MHz Cortex-M3

STM32F4

608 CoreMark
180 MHz Cortex-M4

STM32F7

1082 CoreMark
216 MHz Cortex-M7

STM32H7

Up to 3224 CoreMark
Up to 550 MHz
Cortex-M7
240 MHz Cortex-M4



Mainstream

STM32G0

142 CoreMark
64 MHz Cortex-M0+

STM32G4

569 CoreMark
170 MHz Cortex-M4

STM32F0

106 CoreMark
48 MHz Cortex-M0

STM32F1

177 CoreMark
72 MHz Cortex-M3

STM32F3

245 CoreMark
72 MHz Cortex-M4

Optimized for
mixed-signal applications



Ultra-low-
power

STM32L0

75 CoreMark
32 MHz Cortex-M0+

STM32L1

93 CoreMark
32 MHz Cortex-M3

STM32L4+

409 CoreMark
120 MHz Cortex-M4

STM32U5

651 CoreMark
160 MHz Cortex-M33

STM32L4

273 CoreMark
80 MHz Cortex-M4

STM32L5

443 CoreMark
110 MHz Cortex-M33



Wireless

STM32WL

162 CoreMark
48 MHz Cortex-M4
48 MHz Cortex-M0+

STM32WB

216 CoreMark
64 MHz Cortex-M4
32 MHz Cortex-M0+

Cortex-M0+
Radio co-processor

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STM32

Ecosystem



STM32Cube



Evaluation tools



Software tools



Embedded
Software



Hardware
Tools



Security



MadeForSTM32



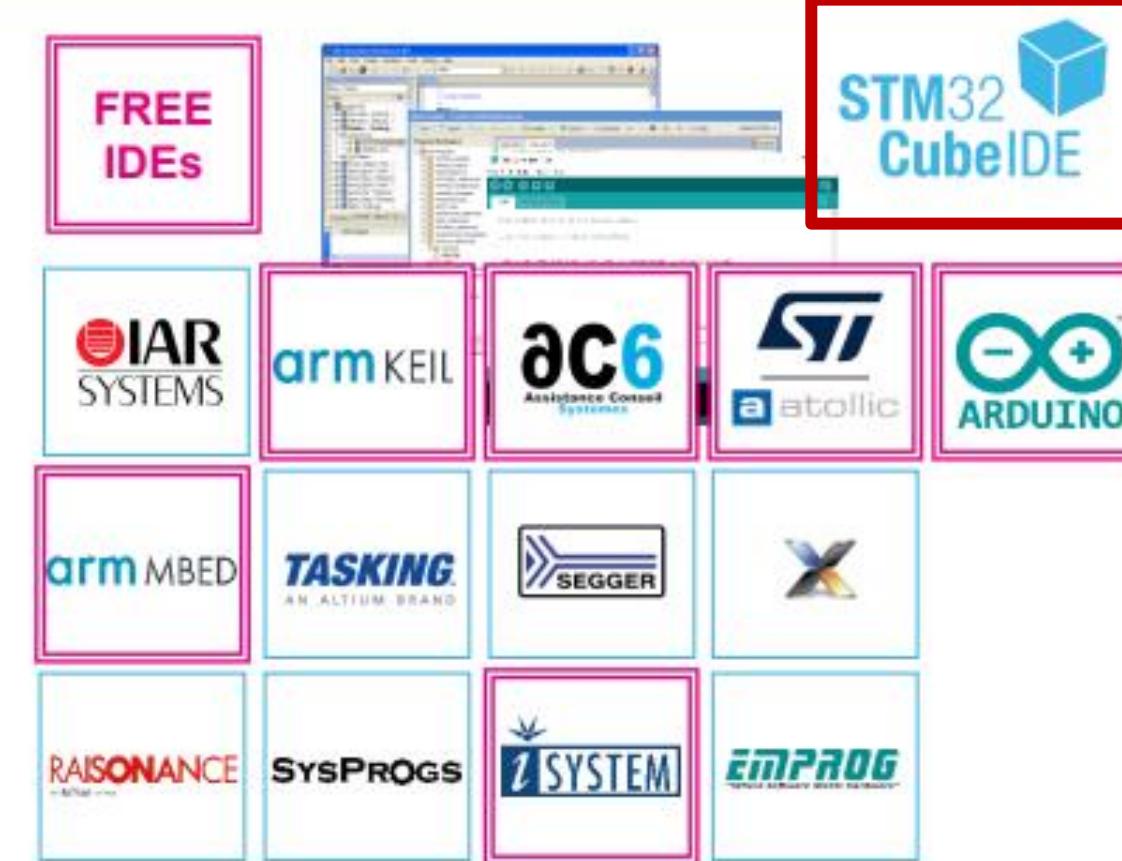
ST Partners

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A C/C++ flow in three steps



STM32CubeMX, GUI Builders
Configure & Generate Code



ST and Partner IDEs
Compile and Debug



STM32CubeProg/Monitor
Monitor, Program & Utilities

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Ingresar a la página oficial de ST y descargarlo

STM32L4 SERIES

STM32L4 is optimized to reduce power consumption and increase flexibility

External level shifter no longer needed
Separate V_{DD} supplies (down to 1.08 V)

28 μ A/MHz using external SMPS
Dedicated V_{12} to the core (down to 1.05 V)

Down to 200 nA keeping 16 Kbytes of SRAM active in Standby mode

Wake up MCU with any peripheral
(Communication I/Fs, analog circuits, timers ...)

I/O level kept in low-power modes
Optimization of system consumption

Down to 8 nA for I/O wake-up
with additional Shutdown mode

RTC available for all power modes
(from Active down to V_{BAT})

2 nA V_{BAT} mode with charging capability
Automatic switch to maintain power
for RTC and backup registers

USB crystal-less capable
(Dedicated crystal oscillator is no
longer needed for USB functions)

Internal oscillator from 100 kHz to 48 MHz
($\pm 0.25\%$ int. clock accuracy over voltage/temperature with LSE)



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STM32L4 SERIES

Best power consumption numbers with full flexibility

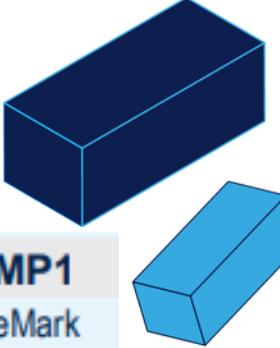
Wake-up time	V _{BAT}		
250 µs	2 nA / 200 nA*		Tamper detection: 2 I/Os, RTC
14 µs	8 nA / 200 nA*		Wake-up sources: reset pin, 5 I/Os, RTC
14 µs	34 nA / 280 nA*		Wake-up sources: + BOR, IWDG
5 µs	200 nA / 440 nA*		Wake-up sources: + all I/Os, PVD, LCD, COMPs, I ² C, LPUART, LPTIM
4 µs	720 nA / 950 nA*		Wake-up sources: + all I ² C, UART
6 cycles	3.2 µA / 3.4 µA*		Wake-up sources: any interrupt or event
	8 µA/MHz ** / 20 µA/MHz **		
	28 µA /MHz ** / 79 µA /MHz		
	35 µA/MHz ** / 90µA/MHz		

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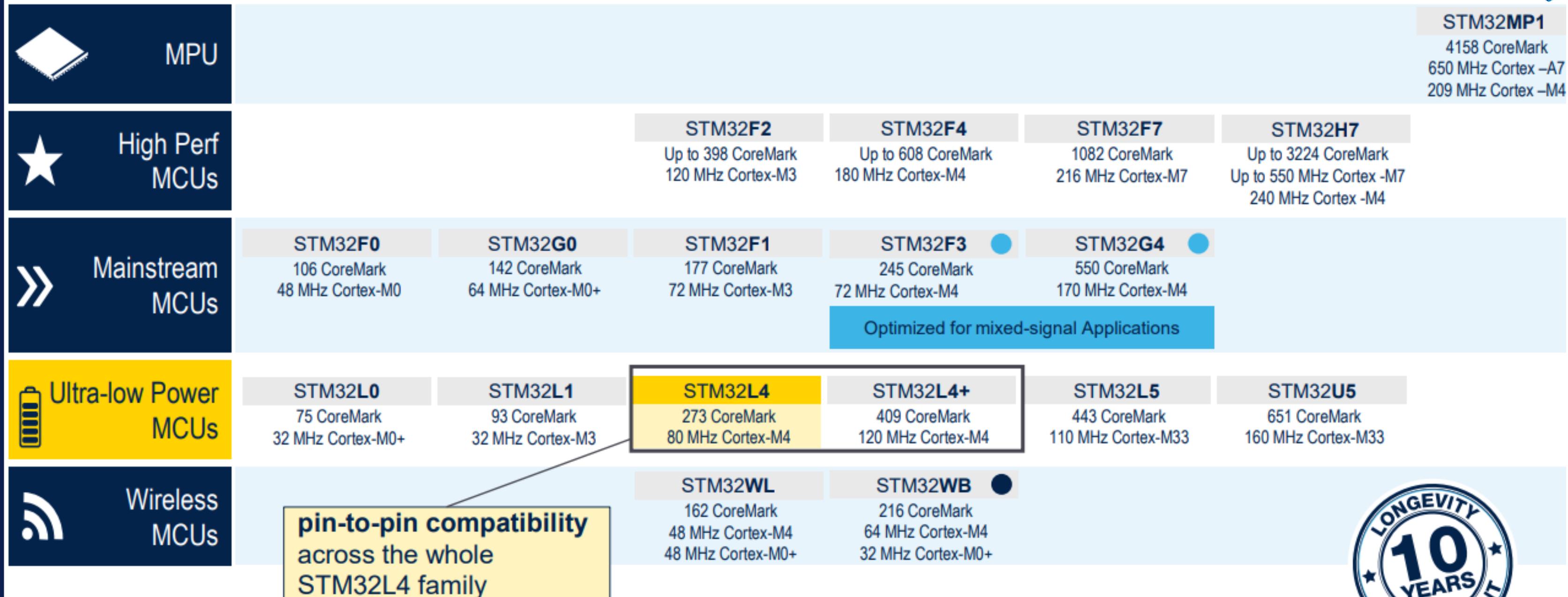
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STM32L4 SERIES



STM32MP1
4158 CoreMark
650 MHz Cortex -A7
209 MHz Cortex -M4



● Optimized for mixed-signal applications

● Cortex-M0+ Radio co-processor



STM32L4 SERIES

STM32L4 completes the ultra-low-power family

Cost-smart
ULP champion

STM32L0

Cortex-M0+ at 32 MHz
1.65 to 3.6V
8-/16-bit applications
Wide range of pin-counts

3 product lines,
Cost-effective,
Smaller packages,
USB, LCD, Analog
8 to 192 Kbytes of Flash,
Up to 20 Kbytes of SRAM

Broad-range
foundation

STM32L1

Cortex-M3 at 32 MHz
1.65 to 3.6V
Wide choice of
memory sizes

3 product lines,
USB, LCD, AES,
Rich Analog
True EEPROM,
Dual-bank Flash memory
(RWW),
32 to 512 Kbytes of Flash,
Up to 80 Kbytes of SRAM

ULP With
performance

STM32L4

Cortex-M4 w/ FPU at 80 MHz
1.71 to 3.6V
High-performance,
advanced analog circuits

5 product lines,
5-MSPS ADC,
PGA, Compar.,
DAC, Op Amp, USB
OTG, LCD, AES
64 Kbytes to 1 Mbyte
Up to 320 Kbytes of SRAM

ULP with
more performance

STM32L4+

Cortex-M4 w/ FPU at 120 MHz
1.71 to 3.6V
Wide choice of
memory sizes

4 product lines,
5-MSPS ADC,
PGA, Compar.,
DAC, Op Amp, USB
OTG, LCD, AES
1 to 2 Mbytes of Flash,
Up to 640 Kbytes of SRAM

Advanced
security

STM32L5

Cortex-M33 w/ FPU at 110 MHz
1.71 to 3.6V
Wide choice of
memory sizes

1 product line,
5-MSPS ADC,
PGA, Compar.,
DAC, Op Amp,
USB Type C, AES
256 to 512 Kbytes of Flash,
Up to 256 Kbytes of SRAM

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STM32L4 SERIES

Feature	STM32 L412xx	STM32 L422xx	STM32 L431xx	STM32 L432xx	STM32 L433xx	STM32 L442xx	STM32 L443xx	STM32 L451xx	STM32 L452xx	STM32 L462xx
ADC	ADC1 ADC2	ADC1 ADC2	ADC1							
DAC	-	-	DAC1							
COMP	COMP1 -	COMP1 -	COMP1 COMP2							
DFSDM	-	-	-	-	-	-	-	DFSDM1	DFSDM1	DFSDM1
LCD	-	-	-	-	LCD	-	LCD	-	-	-
AES	-	AES	-	-	-	AES	AES	-	-	AES
TIM	TIM1 TIM2 - TIM6 - TIM15 TIM16									
I2C	I2C1 I2C2 I2C3 -	I2C1 I2C2 I2C3 -	I2C1	I2C1	I2C1 I2C2 I2C3 -	I2C1 I2C2 I2C3 -	I2C1 I2C2 I2C3 -	I2C1 I2C2 I2C3 I2C4	I2C1 I2C2 I2C3 I2C4	I2C1 I2C2 I2C3 I2C4

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STM32L4 SERIES

Feature	STM32 L412xx	STM32 L422xx	STM32 L431xx	STM32 L432xx	STM32 L433xx	STM32 L442xx	STM32 L443xx	STM32 L451xx	STM32 L452xx	STM32 L462xx
USART	USART1 USART2 USART3 -	USART1 USART2 USART3 UART4	USART1 USART2 USART3 UART4	USART1 USART2 USART3 UART4						
LPUART	LPUART1	LPUART1	LPUART1							
SPI	SPI1 SPI2 -	SPI1 SPI2 -	SPI1 SPI2 SPI3	SPI1 -	SPI1 SPI2 SPI3	SPI1 -	SPI1 SPI2 SPI3	SPI1 SPI2 SPI3	SPI1 SPI2 SPI3	SPI1 SPI2 SPI3
SAI	-	-	SAI	SAI	SAI	SAI	SAI	SAI	SAI	SAI
SWPMI	-	-	SWPMI1	SWPMI1	SWPMI1	SWPMI1	SWPMI1	-	-	-
SDMMC	-	-	SDMMC	-	SDMMC	-	SDMMC	SDMMC	SDMMC	SDMMC
USB	USB FS	USB FS	-	USB FS	USB FS	USB FS	USB FS	-	USB FS	USB FS
CAN1	-	-	CAN1	CAN1	CAN1	CAN1	CAN1	CAN1	CAN1	CAN1

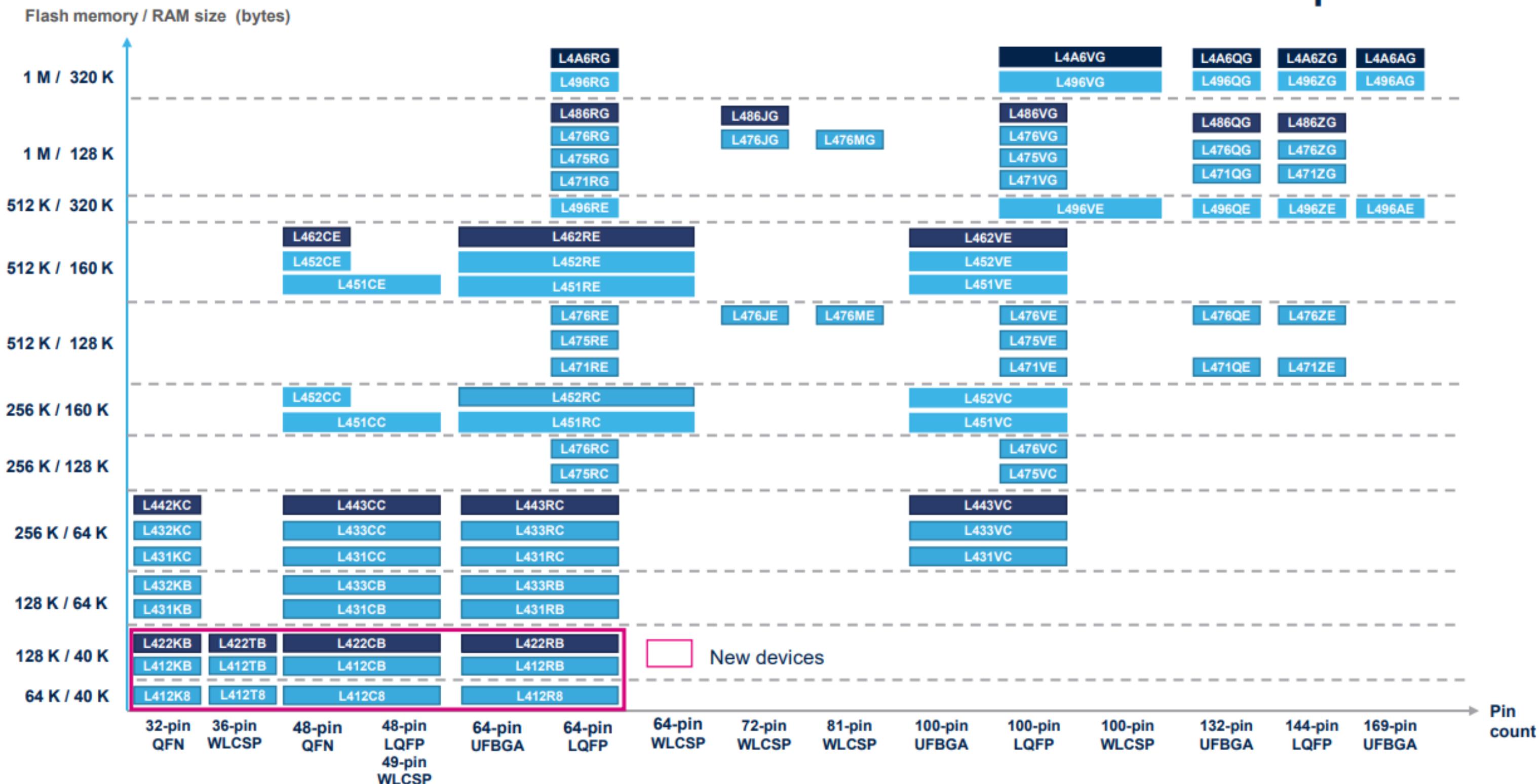
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STM32 SERIES

STM32L4 portfolio



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STM32F4 MCU Series

32-bit Arm® Cortex®-M4 – Up to 180 MHz



Product lines	F _{CPU} (MHz)	Flash (Kbytes)	RAM (KB)	Ethernet I/F IEEE 1588	2x CAN	Camera I/F	SDRAM I/F	Dual Quad-SPI	SAI	SPDIF RX	Chrom-ART Graphic Accelerator™	TFT LCD Controller	MPI DS1	
Advanced lines														
STM32F469 ²	180	512 K to 2056 K	384	•	•	•	•	•	•	•	•	•	•	•
STM32F429 ²	180	512 K to 2056 K	256	•	•	•	•	•	•	•	•	•	•	•
STM32F427 ²	180	1024 K to 2056 K	256	•	•	•	•	•	•	•	•	•	•	•
Foundation lines														
STM32F446	180	256 K to 512 K	128		•	•	•	•	•	•	•	•	•	•
STM32F407 ²	168	512 K to 1024 K	192	•	•	•								
STM32F405 ²	168	512 K to 1024 K	192		•									
Access lines														
STM32F401	84	128 K to 512 K	up to 96	Down to 128	Down to 10	Down to 3x3								•
STM32F410	100	64 K to 128 K	32	Down to 89	Down to 6	Down to 2.553x 2.579				•	•	BAM	-	
STM32F411	100	256 K to 512 K	128	Down to 100	Down to 12	Down to 3.034x 3.22						BAM	•	
STM32F412	100	512 K to 1024 K	256	Down to 112	Down to 18	Down to 3.653x 3.651	•	•	•	•	•	BAM	+LPM ¹	
STM32F413 ²	100	1024 K to 1536 K	320	Down to 115	Down to 18	Down to 3.951x 4.039	•	•	•	•	•	BAM	+LPM ¹	•

Notes:

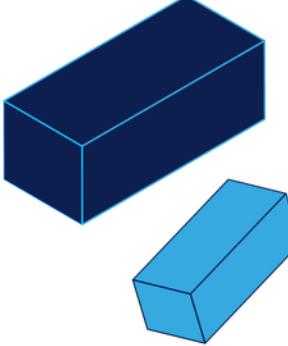
1. Link Power Management

2. The same devices are also found with embedded HW AES encryption (128-/256-bit)

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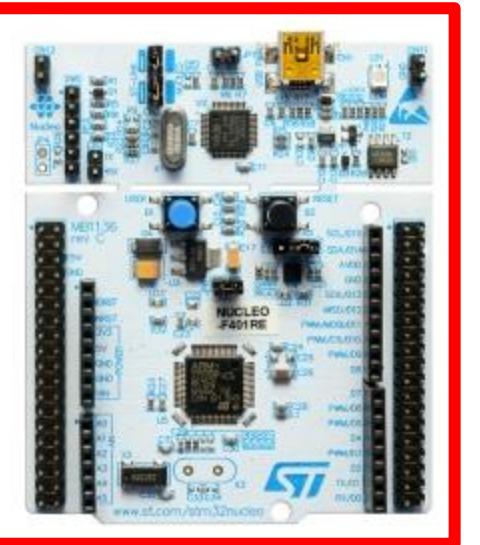
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STM32 SERIES

NUCLEO-F401



HARDWARE TOOLS

The STM32 Nucleo boards category page. It includes an image of three Nucleo boards (blue, green, and white) and a title "STM32 Nucleo boards". Below the title is a blue button labeled "Flexible prototyping". A red box highlights the entire "STM32 Nucleo boards" section.



Discovery kits

Key feature prototyping



Evaluation board

Full feature evaluation

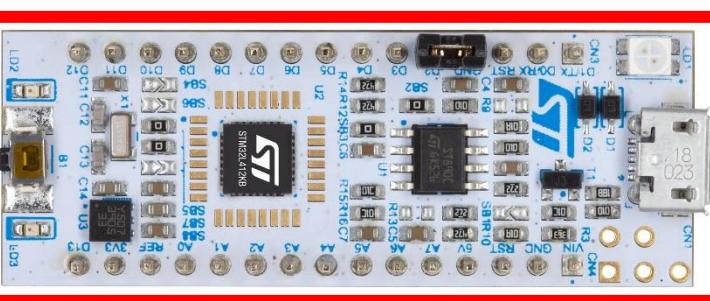
SOFTWARE TOOLS

The STM32Cube software tools page. It features a laptop displaying the STM32Cube interface, a circular icon for "STM32 Cube", and the text "STM32Cube adds major enhancements to boost software development". A red arrow points from the "Flexible prototyping" button in the hardware tools section to this software tools section.

STM32
CubeMX

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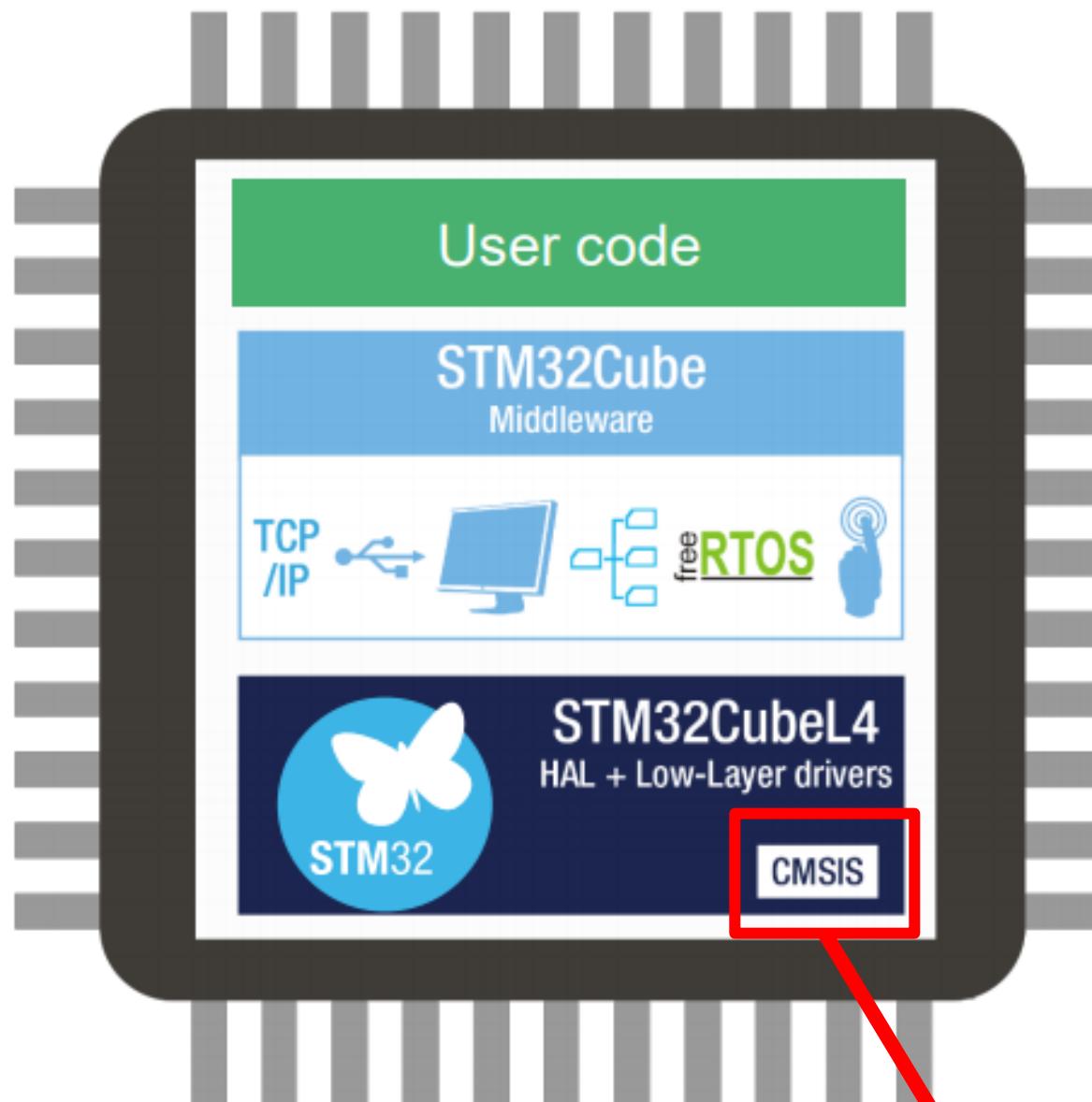
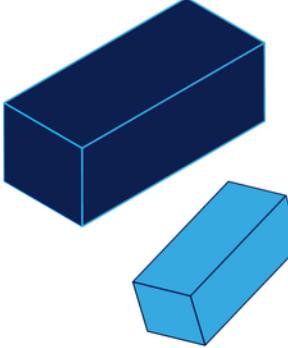
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NUCLEO-L412KB

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STM32 SERIES



EMBEDDED SOFTWARE

- Open-source TCP/IP stack (lwIP)
- USB Host and Device library from ST **Qualified HAL firmware**
- STemWin graphical stack library from ST and SEGGER
- Open-source FAT file system (FatFs)
- Open-source real-time OS (FreeRTOS)
- Touch-sensing library
- Dozens of examples
- STM32L4 Hardware Abstraction Layer (HAL) portable APIs
- **High-performance, light-weight low-layer (LL) APIs**
- High coverage for most STM32 peripherals
- Production-ready and fully qualified
- Dozens of usage examples
- Open-source BSD license

STM32 SERIES



Debug support ■

- STM32L4 provides on-chip debug support
 - MCU programming
 - Application debugging
 - Code analysis

Application benefits

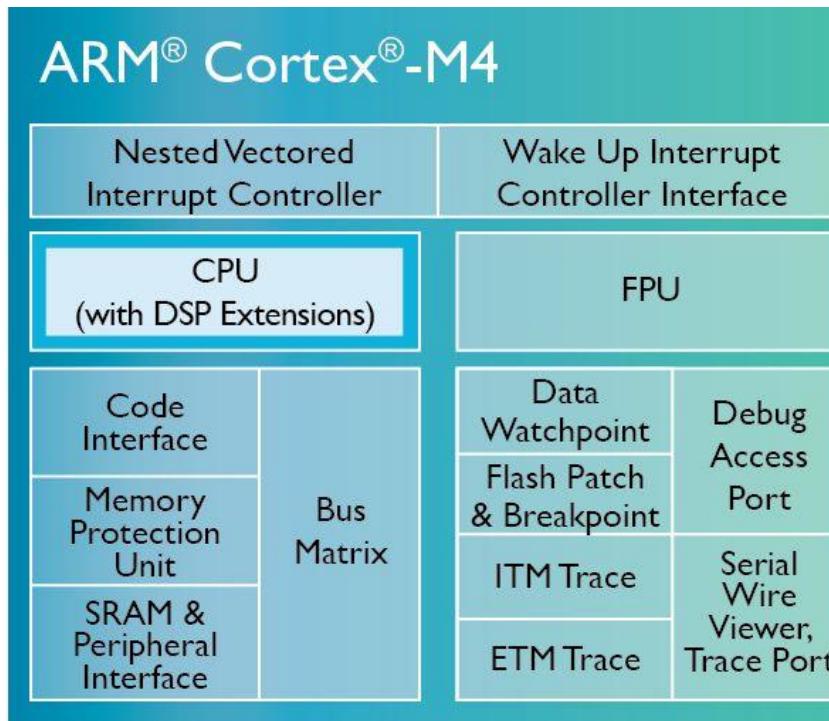
- Basic debugging features
- Advanced features (Embedded Trace Macrocell) to quickly identify malfunctioning code
- Coverage and profiling features

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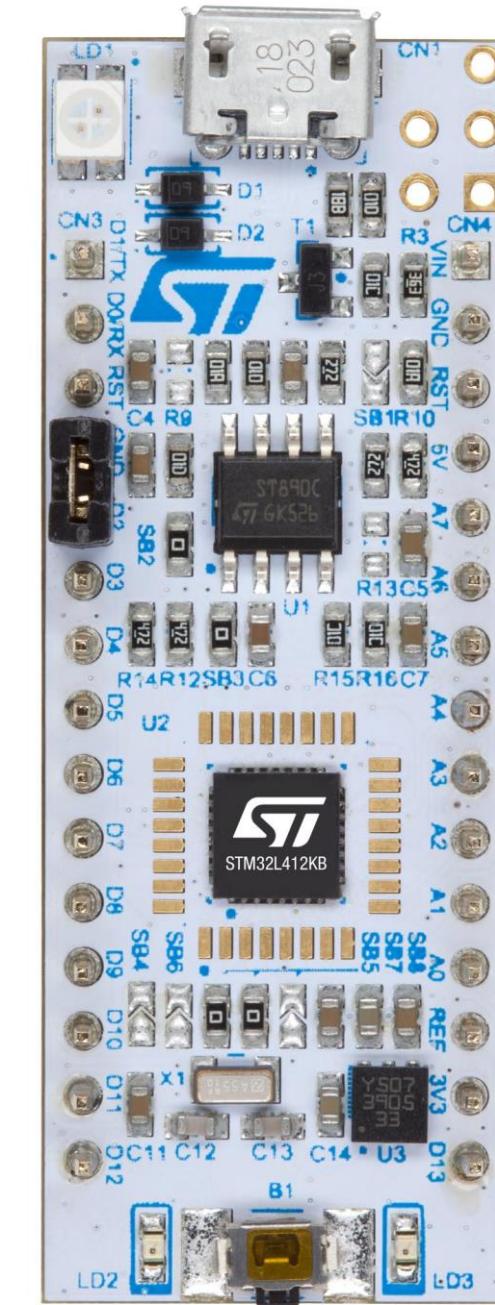
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STM32 SERIES



SMT32 NUCLEO-32 BOARDS

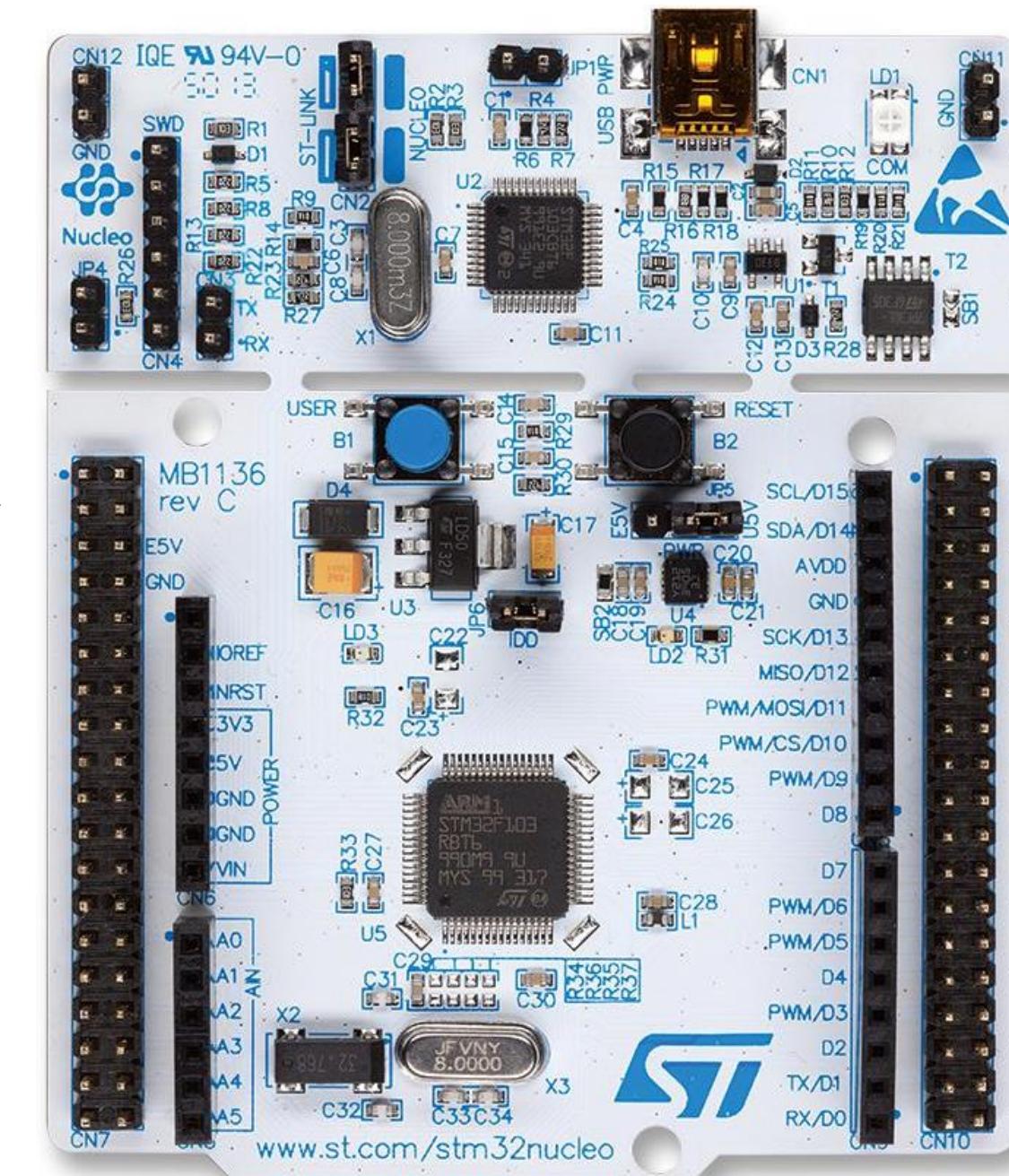


NUCLEO-L412KB

- **STLINK-V2**
 - **LED DE USUARIO → PB3**
 - **RESET BUTTON**
 - **PINES COMPATIBLES CON ARDUINO NANO**

STM32 SERIES

SMT32 NUCLEO-64 BOARDS



NUCLEO-F401RE

- STLINK-V2
- LED DE USUARIO → PA5
- PUSH BUTTON -> PC13
- RESET BUTTON
- PINES COMPATIBLES CON ARDUINO UNO

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