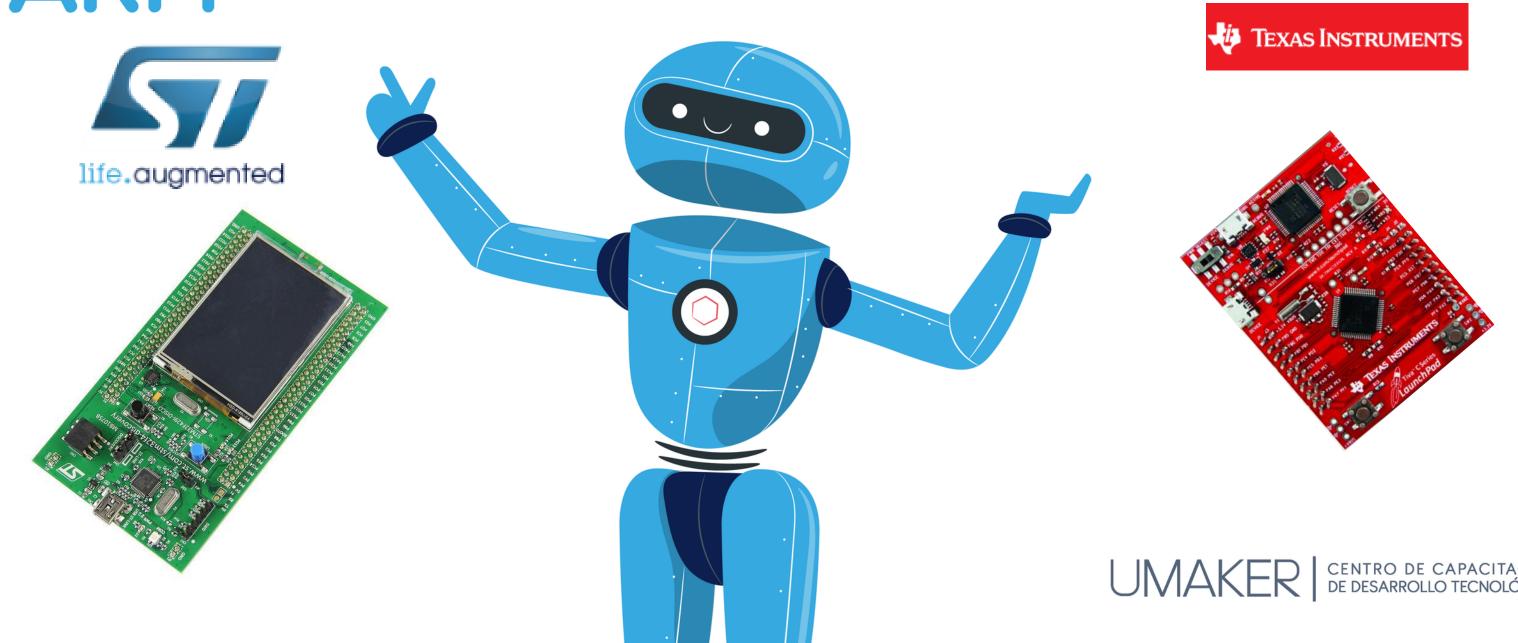
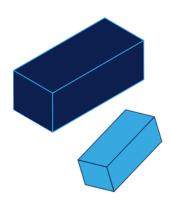
CLASE 8: TIMERS

MICROCONTROLADORES ARM

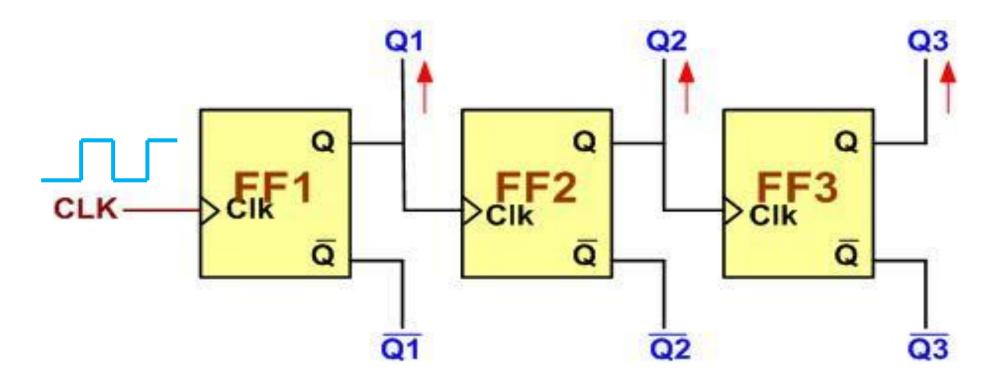




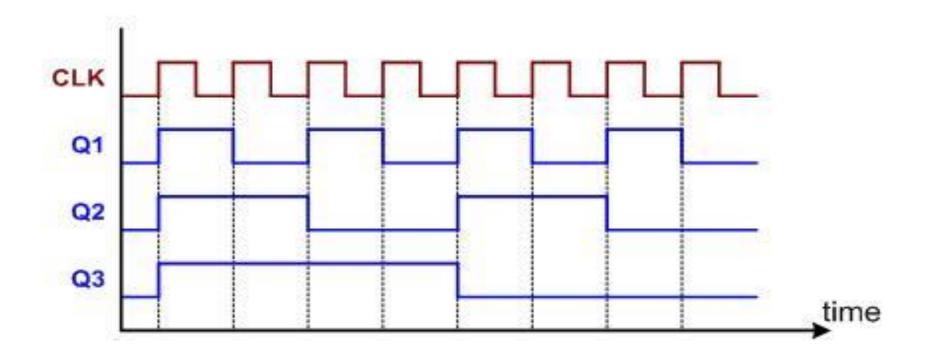




A 3-bit Counter

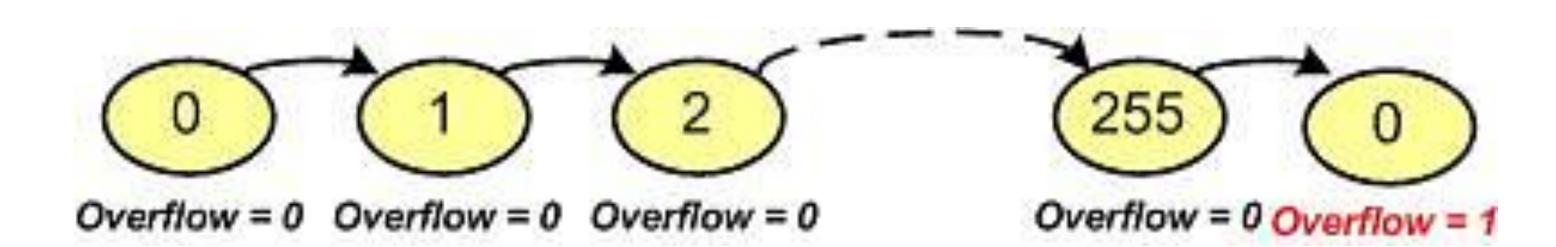


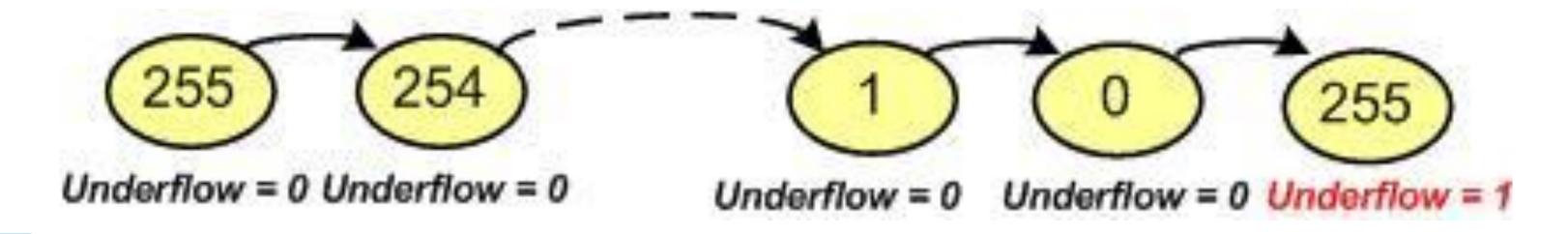






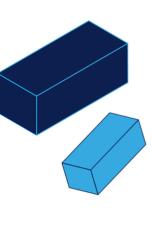
An 8-bit up/down counter stages



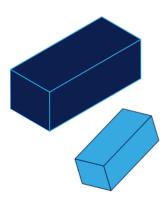


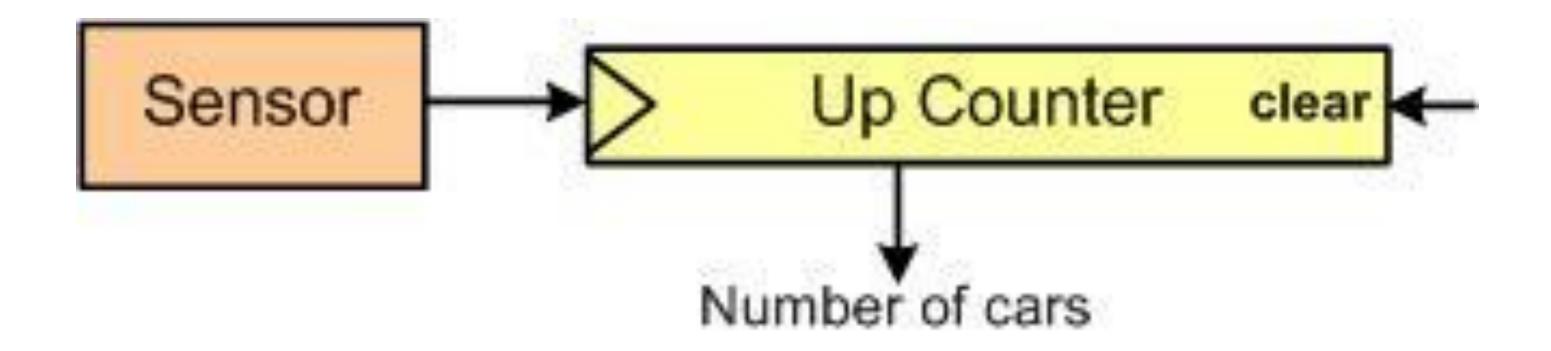






Counting Events Using a Counter

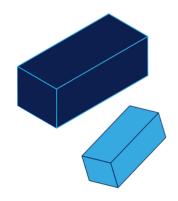


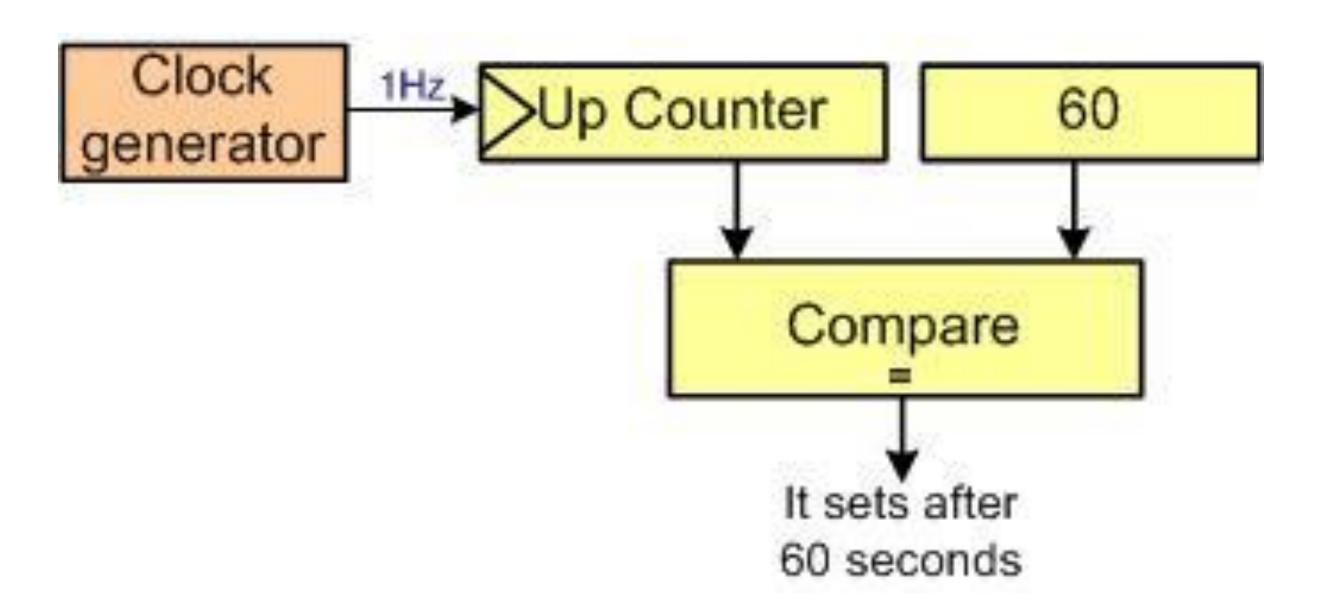






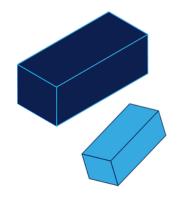
Using Counter as a Timer

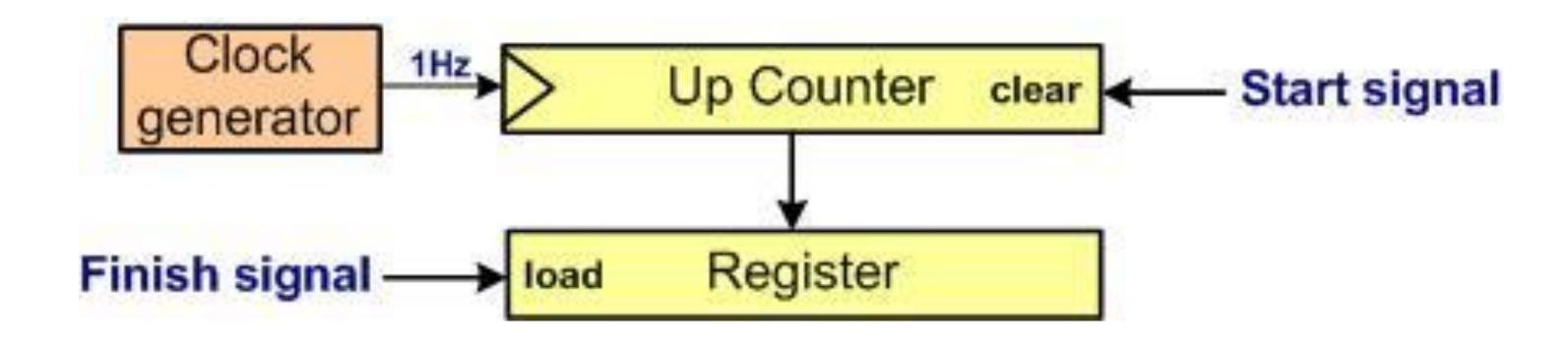






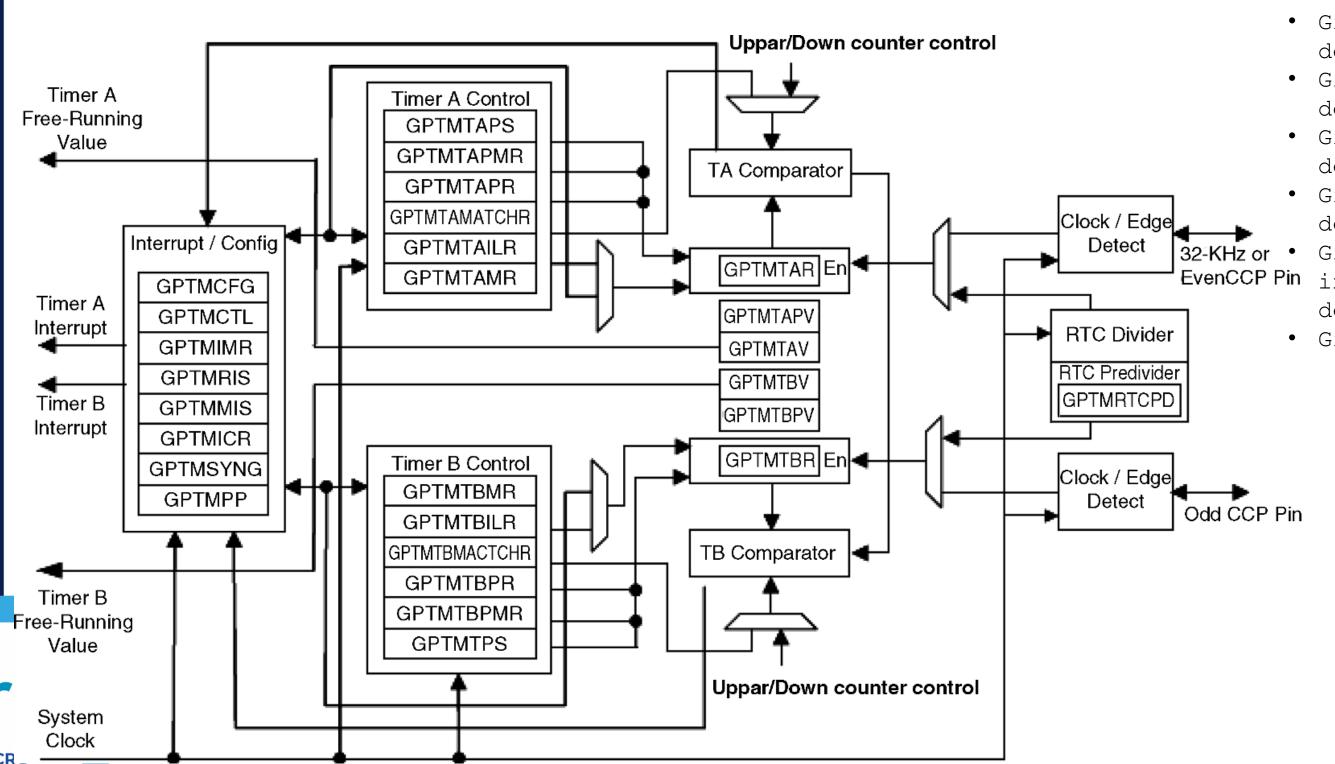
Capturing







Contiene seis bloques GPTM de 16/32 bits y seis bloques Wide GPTM de 32/64 bits



CONTRO-LADORES ARM

- Grupo de registro de control del temporizador A.
- Grupo de registro de control del temporizador B.
- Grupo de registro de estado del temporizador A.
- Grupo de registro de estado del temporizador B.
- 32-KHz or Grupo de registro de EvenCCP Pin interrupción y configuración de los temporizadores A y B.
 - Grupo de controles externos.

PINES DISPONIBLES

En el diagrama de bloques, los pines específicos Capture Compare PWM (CCP) disponibles dependen del dispositivo TM4C123GH6PM.

imer Up/Down Counter		Even CCP Pin	Odd CCP Pin		
16/32-Bit Timer 0	Timer A	TOCCP0	-		
10/32-bit filliel 0	Timer B	-	T0CCP1		
16/32-Bit Timer 1	Timer A	T1CCP0	-		
10/32-Bit filler 1	Timer B	-	T1CCP1		
16/32-Bit Timer 2	Timer A	T2CCP0	-		
10/32-bit filler 2	Timer B	-	T2CCP1		
16/32-Bit Timer 3	Timer A	T3CCP0	-		
10/32-bit filler 3	Timer B	-	T3CCP1		
16/32-Bit Timer 4	Timer A	T4CCP0	-		
10/32-Bit Tilllel 4	Timer B	-	T4CCP1		
16/32-Bit Timer 5	Timer A	T5CCP0	-		
10/32-Bit filler 3	Timer B	-	T5CCP1		
32/64-Bit Wide Timer 0	Timer A	WT0CCP0	-		
32/04-bit Wide Tilliel 0	Timer B	-	WT0CCP1		
32/64-Bit Wide Timer 1	Timer A	WT1CCP0	-		
32/04-bit Wide Tilliel T	Timer B	-	WT1CCP1		
32/64-Bit Wide Timer 2	Timer A	WT2CCP0	-		
32/04-bit Wide Tilliel 2	Timer B	-	WT2CCP1		
32/64-Bit Wide Timer 3	Timer A	WT3CCP0	-		
32/04-bit Wide Tilliel 3	Timer B	-	WT3CCP1		
32/64-Bit Wide Timer 4	Timer A	WT4CCP0	-		
52/04-Dit Wide Tilliel 4	Timer B	-	WT4CCP1		
32/64-Bit Wide Timer 5	Timer A	WT5CCP0	-		
52/04-Dit Wide Tilliel 5	Timer B	-	WT5CCP1		



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MODOS DE CONFIGURACION

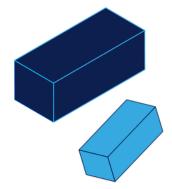
El software configura el GPTM usando el registro GPTM Configuration (GPTMCFG) el registro GPTM Timer A Mode (GPTMTAMR) y el GPTM Timer B Mode (GPTMTBMR). Cuando está en uno de los modos concatenados, el temporizador A y el temporizador B solo pueden funcionar en un modo. Sin embargo, cuando se configura en un modo individual, el temporizador A y el temporizador B se pueden configurar de forma independiente en cualquier combinación de los modos individuales.

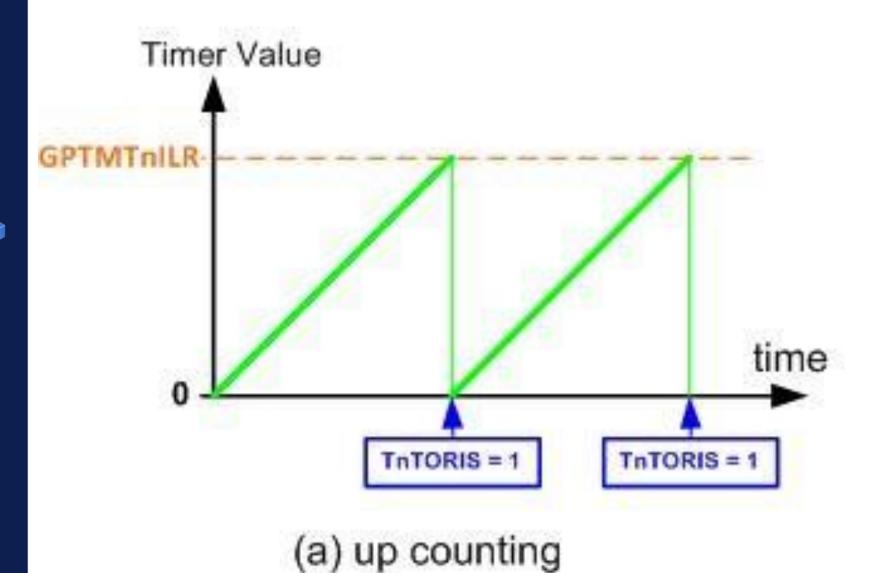
Mode	Timer Use	Count Direction	Counter Size		Prescaler Size ^a		Prescaler Behavior
			16/32-bit GPTM	32/64-bit Wide GPTM	16/32-bit GPTM	32/64-bit Wide GPTM	(Count Direction)
One-shot	Individual	Up or Down	16-bit	32-bit	8-bit	16-bit	Timer Extension (Up), Prescaler (Down)
	Concatenated	Up or Down	32-bit	64-bit	-	-	N/A
Periodic	Individual	Up or Down	16-bit	32-bit	8-bit	16-bit	Timer Extension (Up), Prescaler (Down)
	Concatenated	Up or Down	32-bit	64-bit	-	-	N/A
RTC	Concatenated	Up	32-bit	64-bit	-	-	N/A
Edge Count	Individual	Up or Down	16-bit	32-bit	8-bit	16-bit	Timer Extension (Both)
Edge Time	Individual	Up or Down	16-bit	32-bit	8-bit	16-bit	Timer Extension (Both)
PWM	Individual	Down	16-bit	32-bit	8-bit	16-bit	Timer Extension

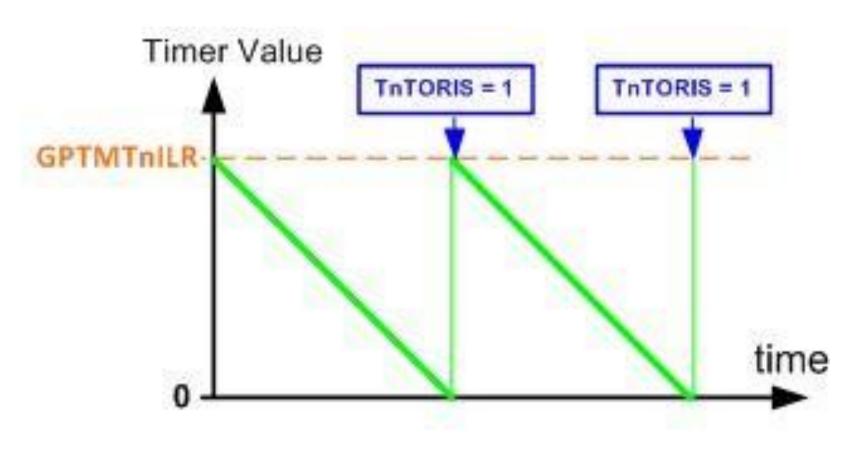


) DE CAPACITACIÓN RROLLO TECNOLÓGICO

MODOS DE CONFIGURACION



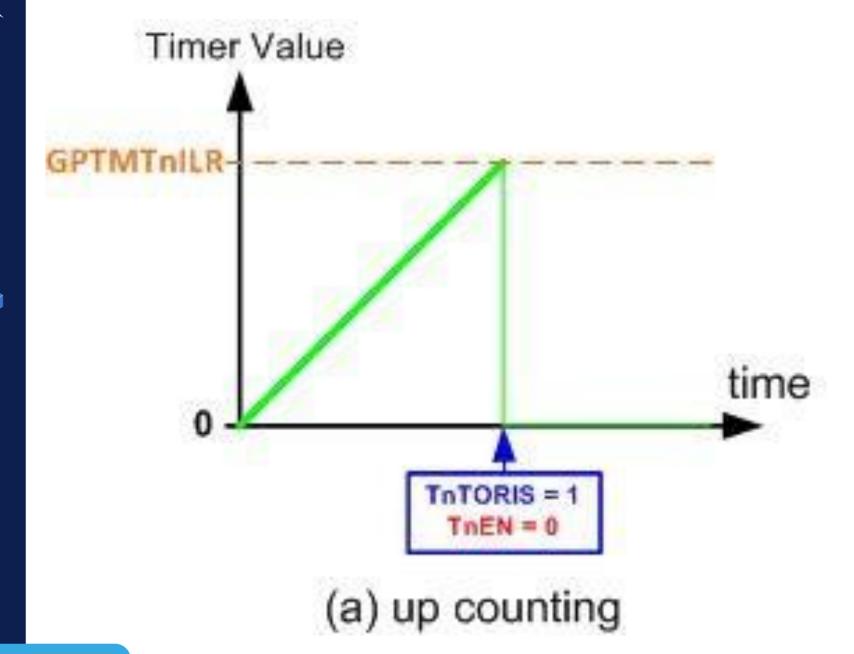


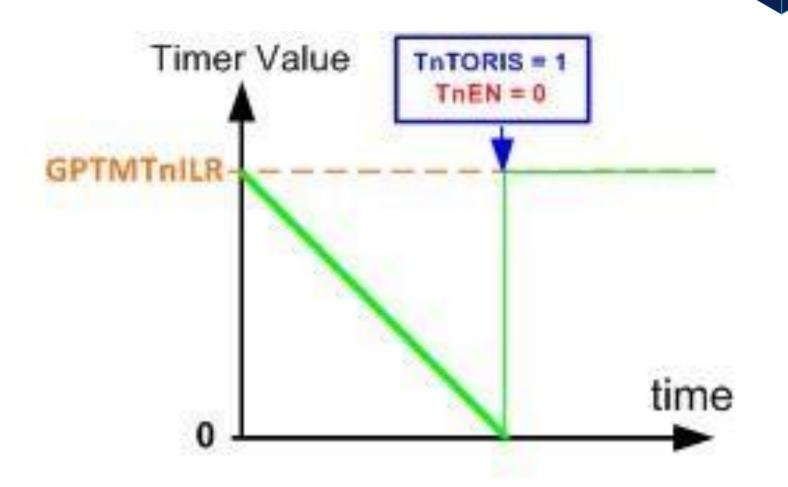


(b) down counting



MODOS DE CONFIGURACION



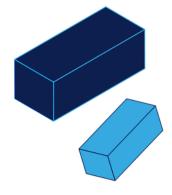


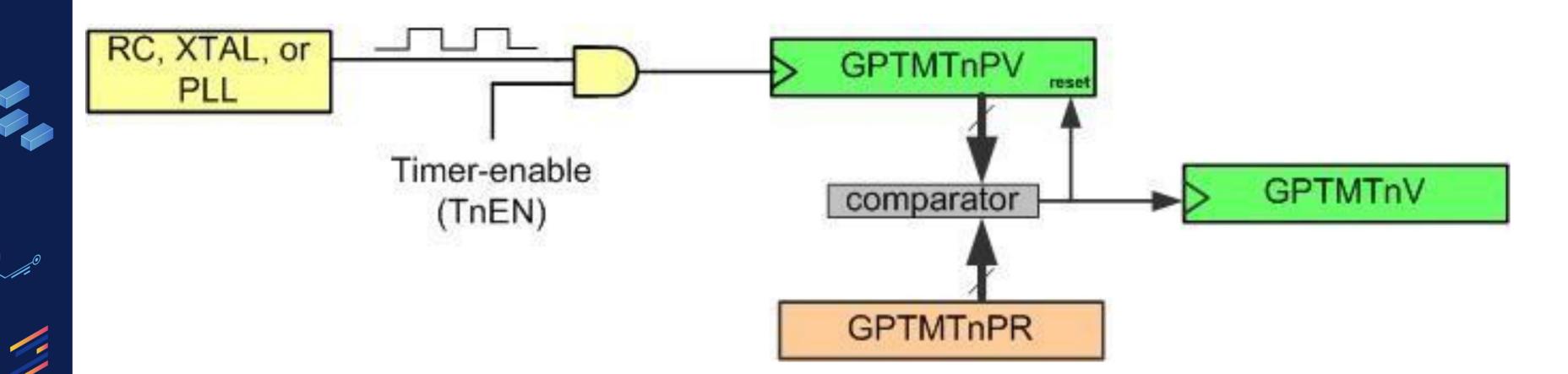
(b) down counting





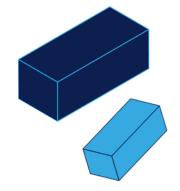


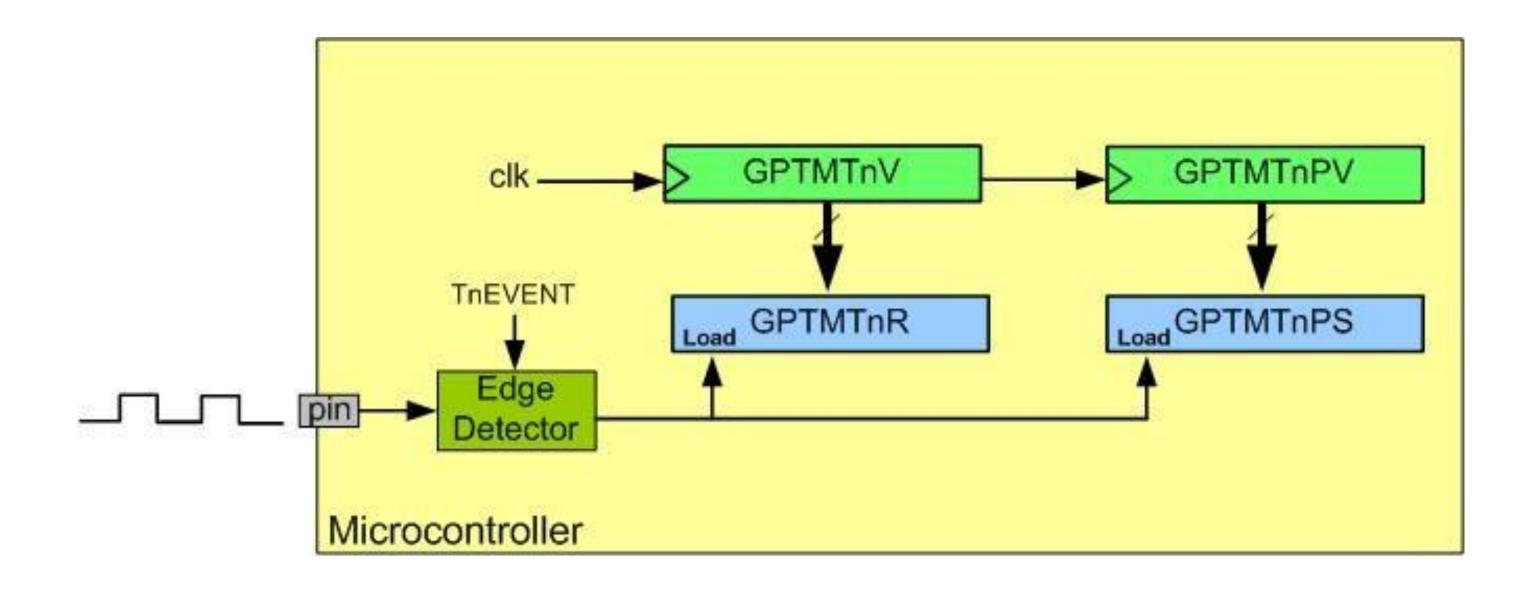






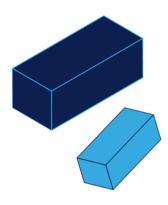
Input Edge Time Capturing

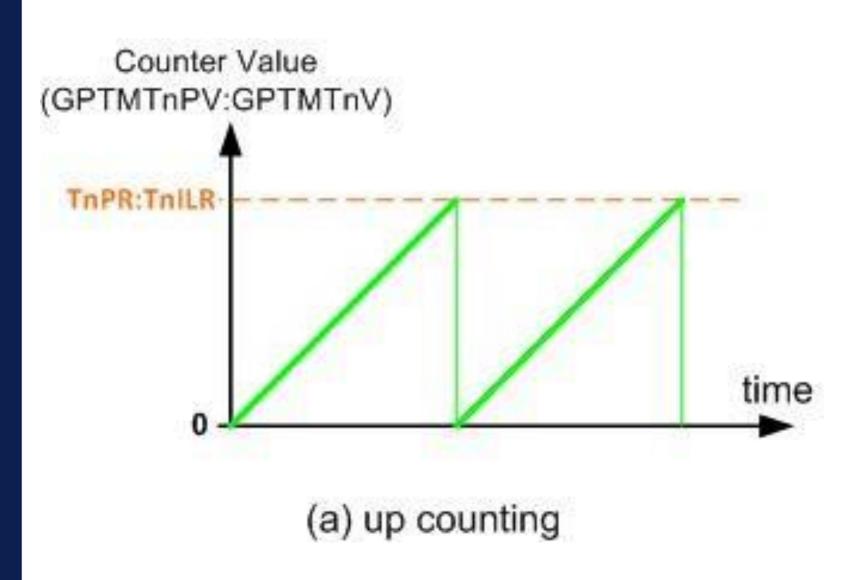


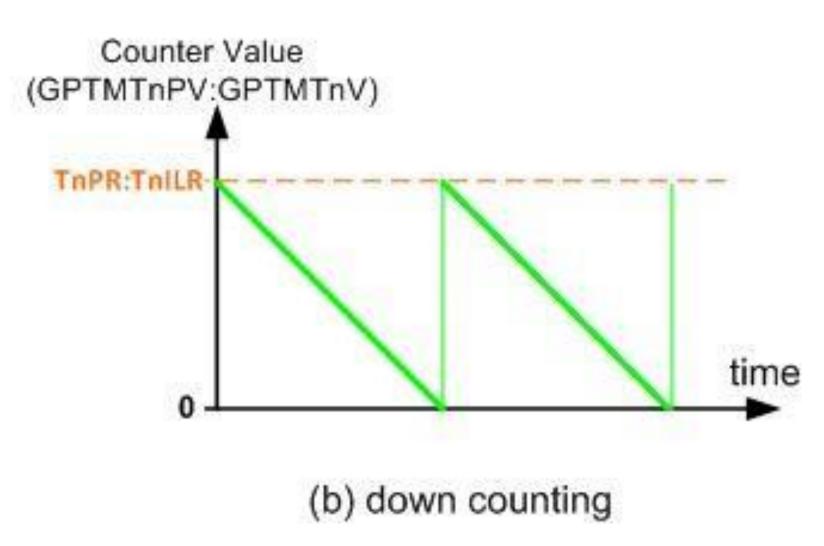




Counting in Input Edge-Time Mode

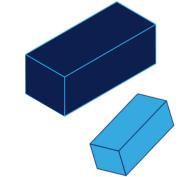


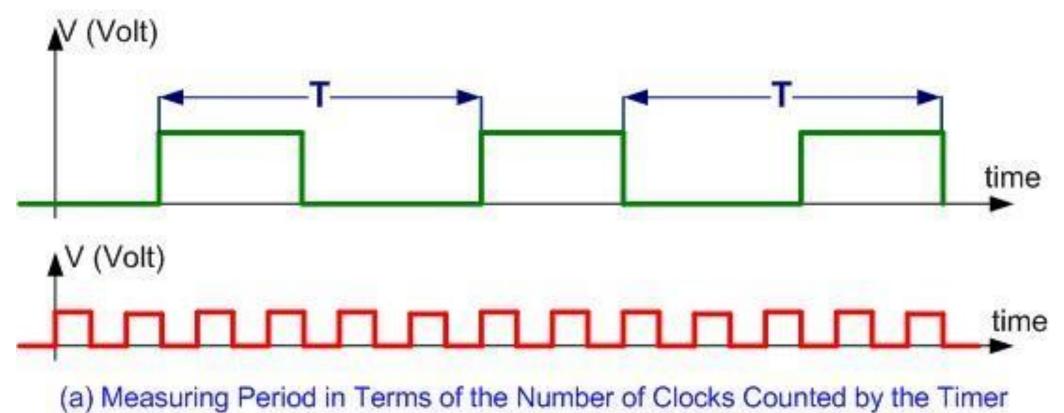


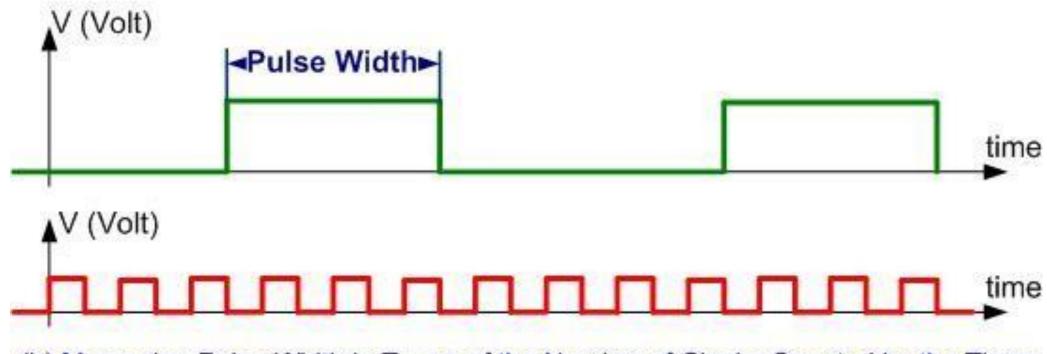




Measuring Period and Pulse Width





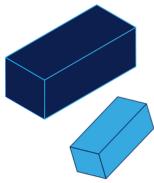


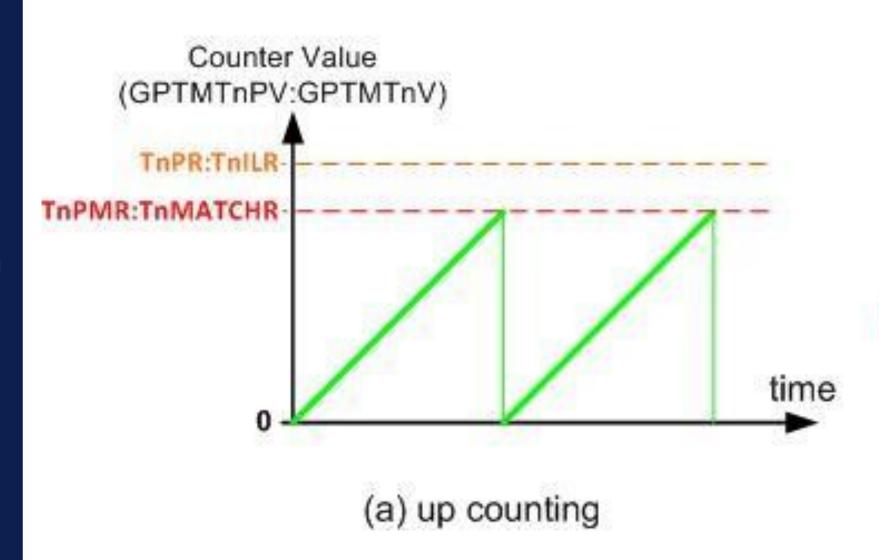


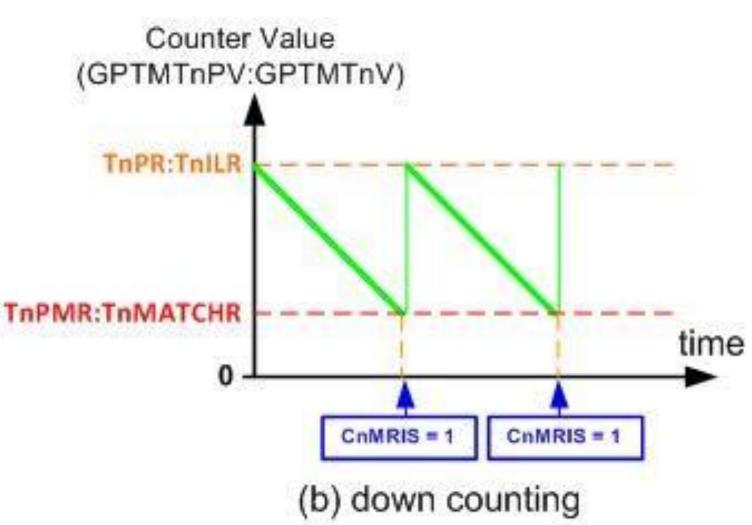
(b) Measuring Pulse Width in Terms of the Number of Clocks Counted by the Timer



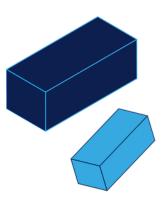
Counting in the Input Edge-Count Mode









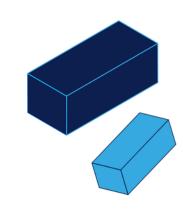


EJEMPLO DE CONFIGURACION





CONFIGURACION EN MODO PERIODICO CON INTERRUPCION



$$F_{CLOCK_CNT} = \frac{F_{CLOCK_PSC}}{PSC + 1}$$

$$UpdateEvent = \frac{F_{CLOCK_PSC}}{(PSC+1)(ARR+1)}.....(hz)$$

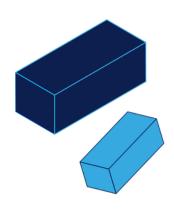
$$UpdateEvent = \frac{16000000}{(15+1)(999+1)} = 1000Hz = 1khz$$

$$CountingPeriod = \frac{(PSC+1)(ARR+1)}{F_{CLOCK_PSC}}.....(segundos)$$

$$CountingPeriod = \frac{(15+1)(999+1)}{160000000} = 0.001 = 1ms$$







```
void TIMER0A_PeriodicMode(void){
   /*0. HABILITAR EL RELOJ*/
   SYSCTL_RCGCTIMER_R = SYSCTL_RCGCTIMER_R0;
   while(!(SYSCTL_PRTIMER_R & 1));
   /*1. DESHABILITAR EL TIMER*/
   TIMERO_CTL_R &=~ TIMER_CTL_TAEN;
   /*2. CONFIGURAR EL REGISTRO CFG*/
   TIMERO_CFG_R = 0x4;
                                                //TIMER0 -> 16bit
    /*3. CONFIGURAR EL REGISTRO TnMR*/
   TIMERO_TAMR_R = 0 \times 2;
                                                //TIMEROA-> CONTEO PERIODICO
   TIMERO_TAMR_R |= TIMER_TAMR_TACDIR;
                                                //UP COUNTER
    /*4.CONFIGURAR EL REGISTRO TNILR Y TNPR*/
                                                //FreqCount = 16MHZ/16 = 1MHZ <-> T = 1uS
    TIMERØ TAPR R = 16-1;
                                                 // 1ms = X*(10^{-6}) -> 1000
                                                 //50ms-> PERIODO DE CONTEO
   TIMERO_TAILR_R = 50000-1;
    /*5. CONFIGURACION DE INTERRUPCIONES*/
   TIMERO_IMR_R |= TIMER_IMR_TATOIM;
                                                   //se habilita la mascara para la actualizacion de evento
   TIMERØ ICR R = TIMER ICR TATOCINT;
                                                   //clear flag
   //envic
    NVIC_PRI4_R = 1<<29;
                                                    //prioridad 2 para la interrupcion del timer0a
   NVIC_ENO_R = 1 << 19;
                                                       //se habilita la interrupcion
    //6. habilitar el timer*/
   TIMERO_CTL_R = TIMER_CTL_TAEN;
                                                   //se habilita el conteo
    return;
```



CONFIGURACION EN MODO PERIODICO CON INTERRUPCION

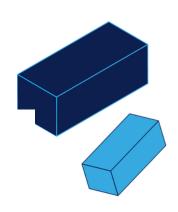
```
void TIMER0A_Handler(void){
   if(TIMER0_RIS_R & TIMER_RIS_TATORIS){
      TIMER0_ICR_R |= TIMER_ICR_TATOCINT;
      //CODE
```



CONFIGURACION EN MODO EDGE COUNT

LADORES

```
void TIMER1A_edgeCountMode(void){
   /*habilitar clk*/
   SYSCTL_RCGC1_R = SYSCTL_RCGC1_TIMER1;
   while(!(SYSCTL_PRTIMER_R & SYSCTL_PRTIMER_R1));
                                                         //timer 1 listo
   SYSCTL_RCGC2_R |= SYSCTL_RCGC2_GPIOB;
   while(!(SYSCTL_PRGPIO_R & SYSCTL_PRGPIO_R1));
                                                           //gpiob listo
   /*CONFIGURACION DEL PB4 COMO SU FUNCION ALTERNATIVA*/
   GPIO_PORTB_DEN_R = 1 << 4;
                                                           //PB4 -> DIGITAL
   GPIO PORTB AFSEL R = 1<<4;
                                                           //PB4 -> FUNCION ALTERNATIVA
   GPIO PORTB PCTL R = GPIO PCTL PB4 T1CCP0;
                                                           //establecer funcion alternativa para TIMER1A
   /*CONFIGURACION DEL TIMER1A*/
   TIMER1 CTL_R &=~ TIMER_CTL_TAEN;
   TIMER1_CFG_R = TIMER_CFG_16_BIT;
                                                           //TIMER1A-> 16-bit
   TIMER1_TAMR_R |= TIMER_TAMR_TAMR_CAP;// | TIMER_TAMR_TACMR;//TIMER1A-> capture mode
   TIMER1_TAMR_R = TIMER_TAMR_TACDIR;
                                                           //TIMER1A-> counter up
   TIMER1_CTL_R &=\sim (0xF<<2);
                                                           //rising edge
   /*CONFIGURACION DEL LA INTERRUPCION*/
   TIMER1_IMR_R |= TIMER_IMR_CAEIM;
                                                           //Capture event
   TIMER1_ICR_R |= TIMER ICR CAECINT;
   //NVIC
   NVIC_PRI4_R = 1 << 13;
                                                           //prioridad 1
   NVIC ENØ R = 1 << 21;
                                                           //se habilita la interrupcion
   /*se habilita el timer1a*/
   TIMER1_CTL_R |= TIMER_CTL_TAEN;
                                                           //timer1a -> enable
   return;
```

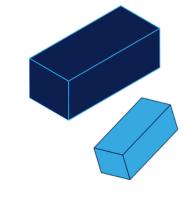




CONFIGURACION EN MODO EDGE COUNT

```
void TIMER1A_Handler(void){
   if(TIMER1_RIS_R & TIMER_RIS_CAERIS){
      TIMER1_ICR_R |= TIMER_ICR_CAECINT;
      //CODE
   data = TIMER1_TAR_R; //TAV
   TIMER1_TAV_R = 0;
}
```





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