GPIO

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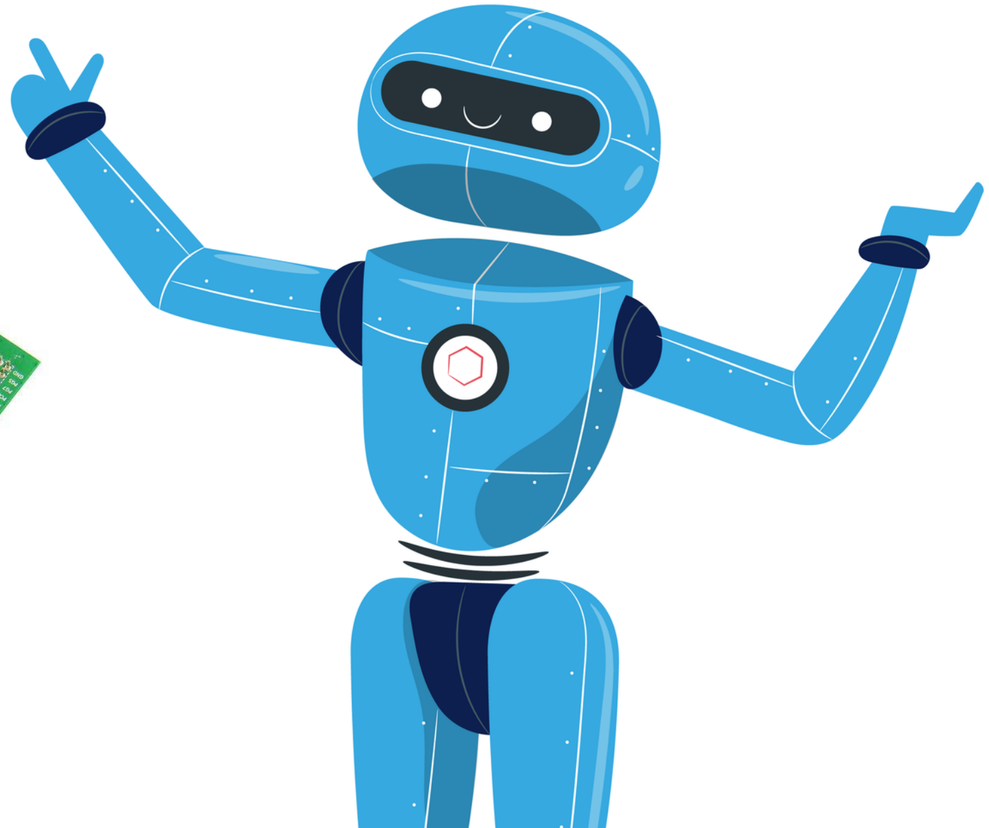
ARM

life.augmented



TEXAS INSTRUMENTS

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GPIO

- Configuración de los GPIO en modo salida digital.
- Configuración de los GPIO en modo entrada digital.
- Manejo de display de 7 segmentos.

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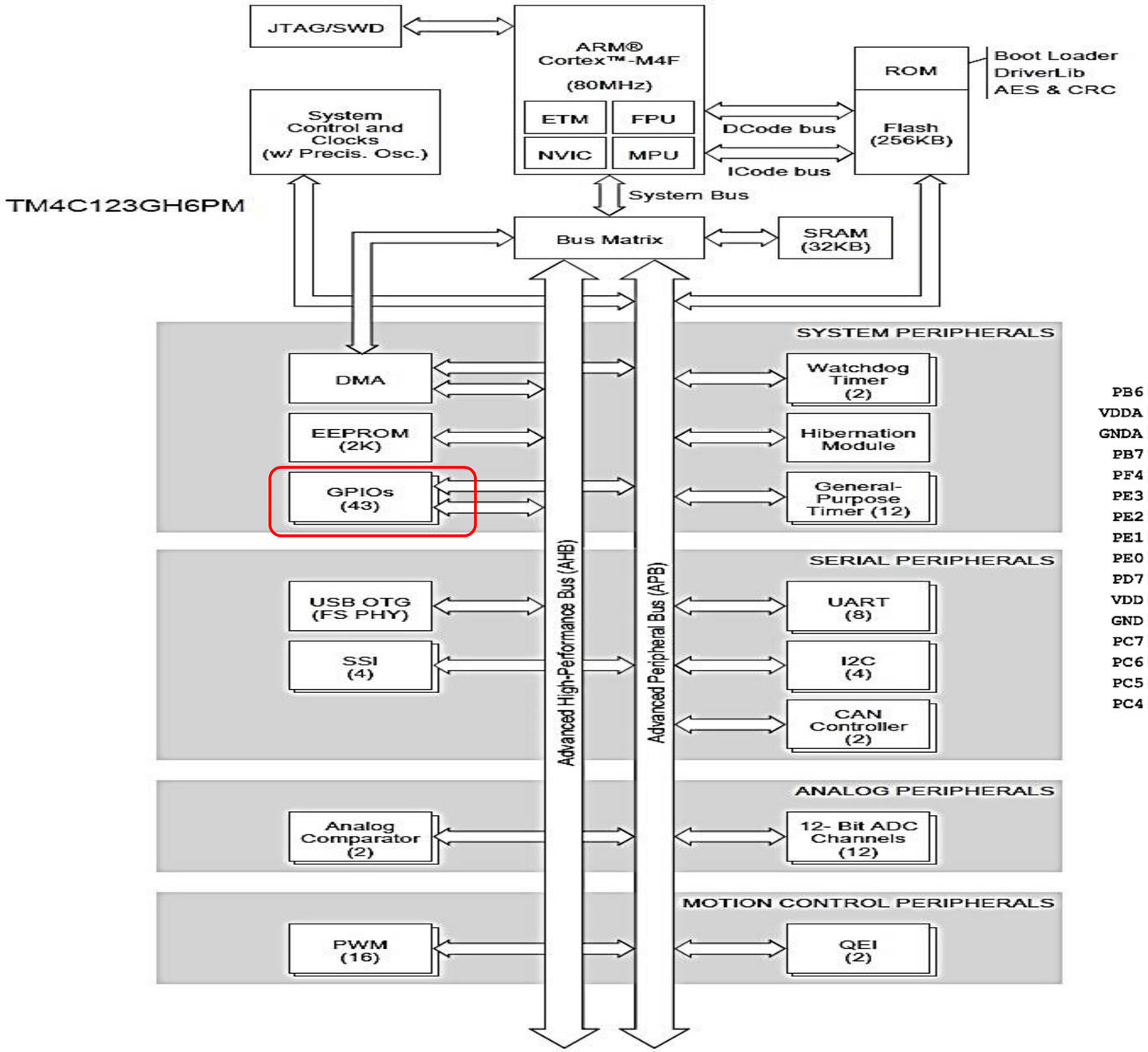
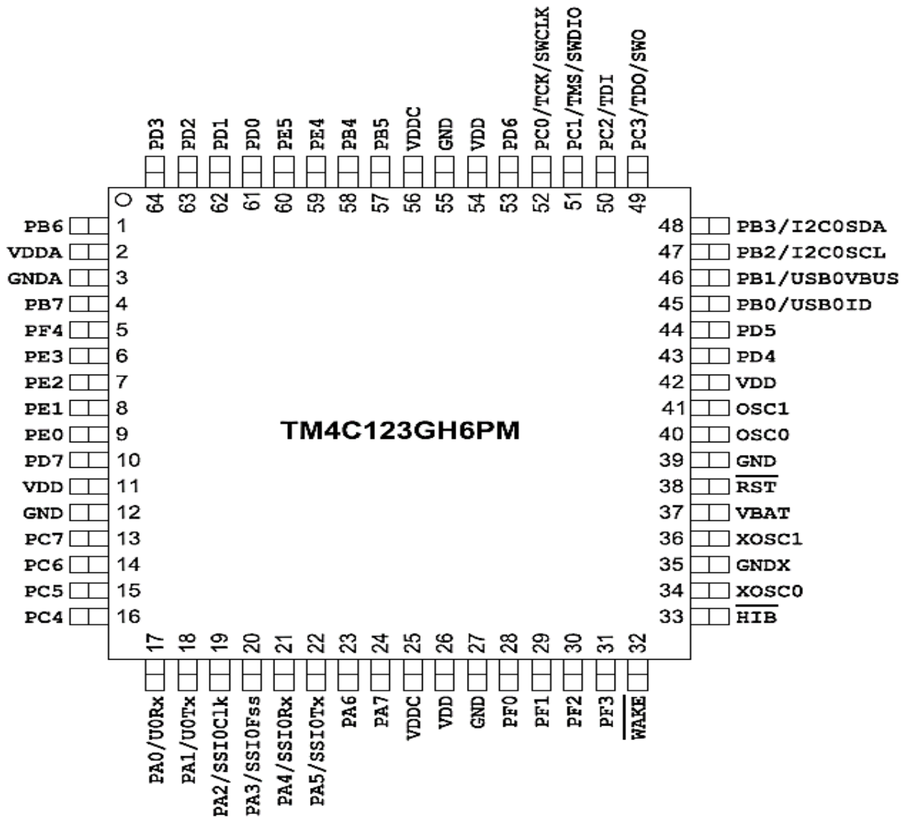
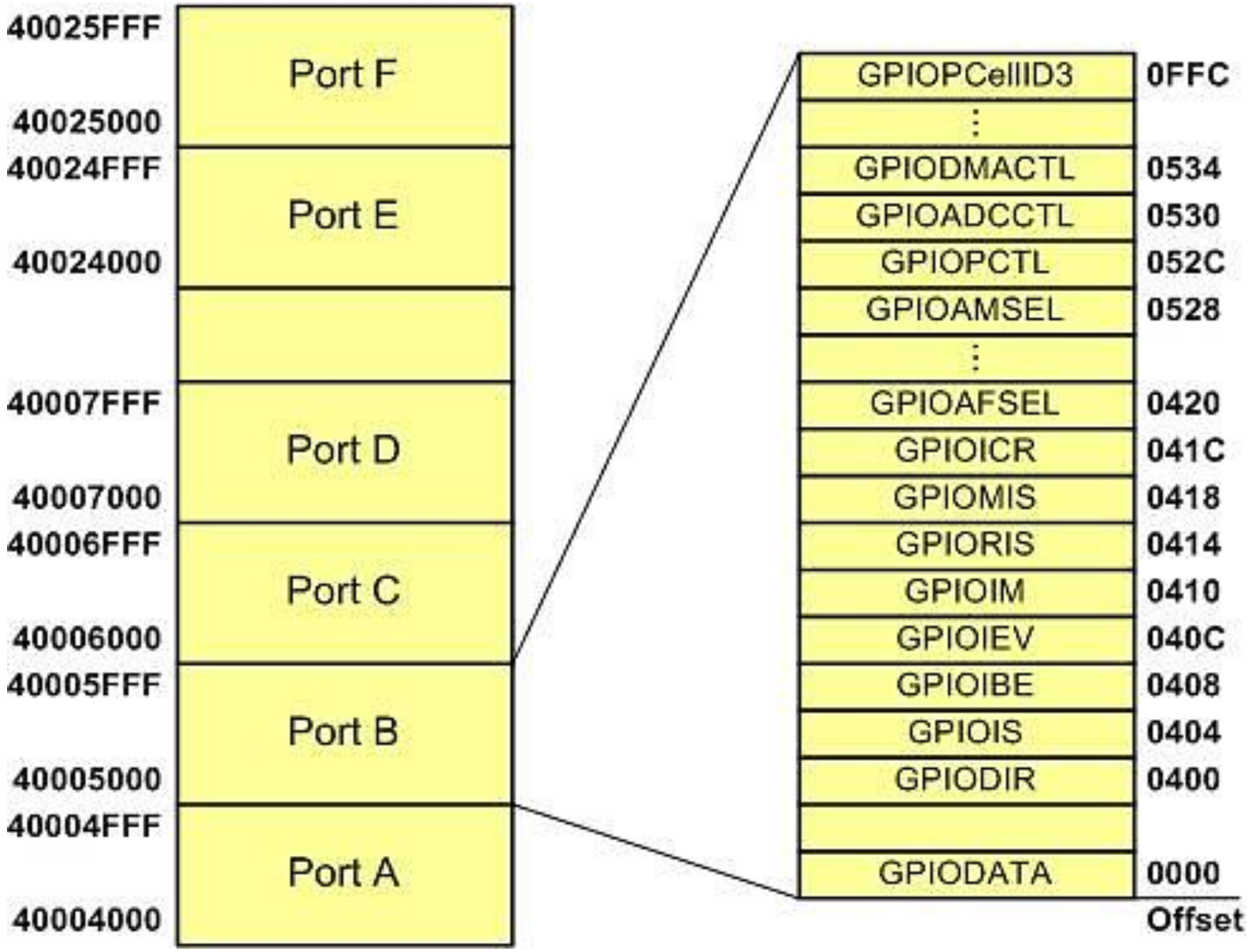
GPIO


TM4C123GH6PM
JTAG/SWD
ARM® Cortex™-M4F (80MHz)
ETM
FPU
NVIC
MPU
System Control and Clocks (w/ Precis. Osc.)
ROM
Boot Loader
DriverLib
AES & CRC
Flash (256KB)
DCode bus
ICode bus
System Bus
Bus Matrix
SRAM (32KB)
SYSTEM PERIPHERALS
DMA
EEPROM (2K)
GPIOs (43)
Watchdog Timer (2)
Hibernation Module
General-Purpose Timer (12)
SERIAL PERIPHERALS
USB OTG (FS PHY)
SSI (4)
UART (8)
I2C (4)
CAN Controller (2)
ANALOG PERIPHERALS
Analog Comparator (2)
12- Bit ADC Channels (12)
MOTION CONTROL PERIPHERALS
PWM (16)
QEI (2)
Advanced High-Performance Bus (AHB)
Advanced Peripheral Bus (APB)


TM4C123GH6PM
PD3 64
PD2 63
PD1 62
PD0 61
PE5 60
PE4 59
PB4 58
PB5 57
VDDC 56
GND 55
VDD 54
PD6 53
PC0/TCK/SWCLK 52
PC1/TMS/SWDIO 51
PC2/TDI 50
PC3/TDO/SWO 49
PB6 1
VDDA 2
GNDA 3
PB7 4
PF4 5
PE3 6
PE2 7
PE1 8
PE0 9
PD7 10
VDD 11
GND 12
PC7 13
PC6 14
PC5 15
PC4 16
48 PB3/I2C0SDA
47 PB2/I2C0SCL
46 PB1/USB0VBUS
45 PB0/USB0ID
44 PD5
43 PD4
42 VDD
41 OSC1
40 OSC0
39 GND
38 RST
37 VBAT
36 XOSC1
35 GNDX
34 XOSC0
33 HIB
17 PA0/U0Rx
18 PA1/U0Tx
19 PA2/SSI0Clk
20 PA3/SSI0Fss
21 PA4/SSI0Rx
22 PA5/SSI0Tx
23 PA6
24 PA7
25 VDDC
26 VDD
27 GND
28 PF0
29 PF1
30 PF2
31 PF3
32 WAKE

GPIO

(GPIO Memory Map)



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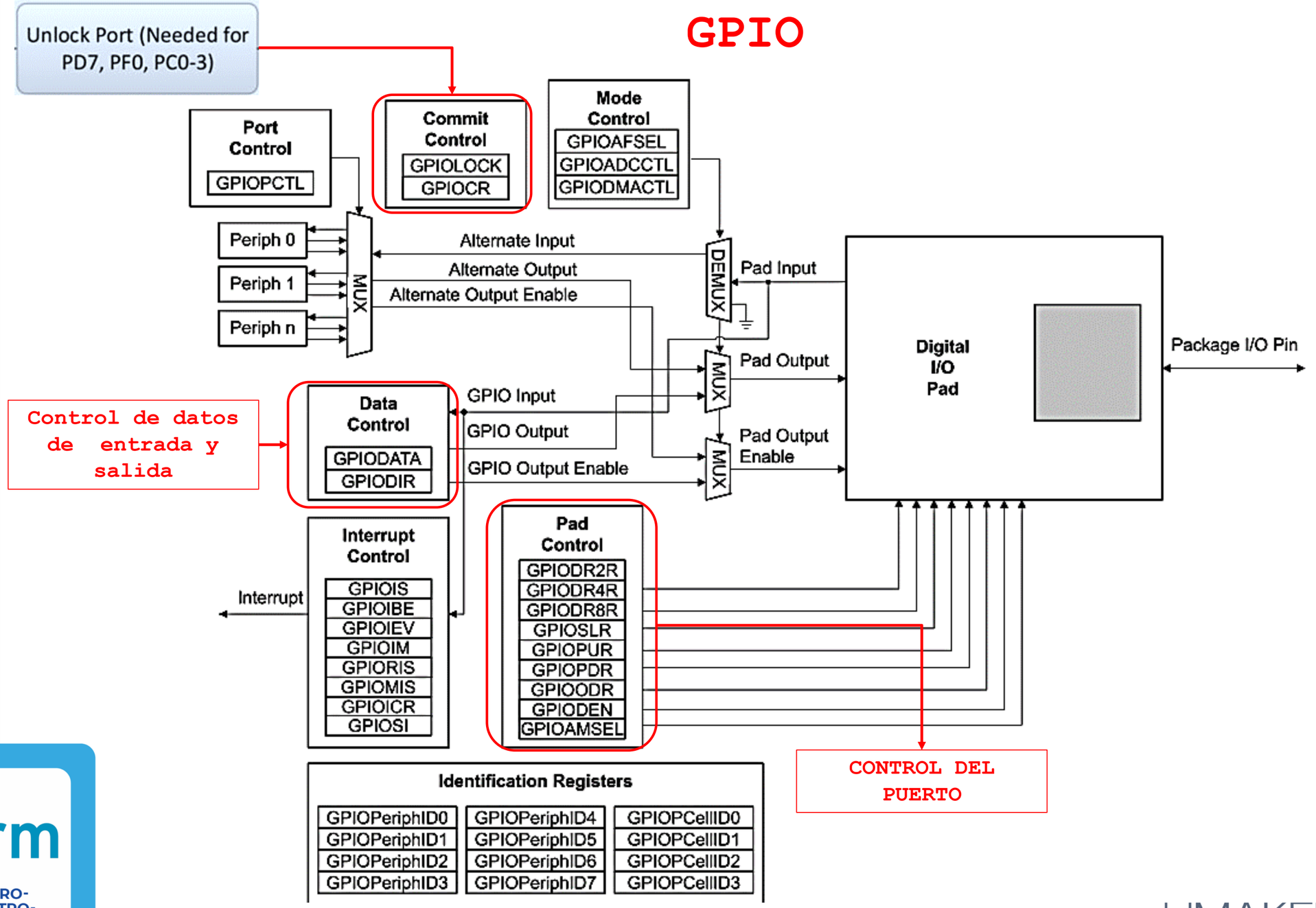
GPIO



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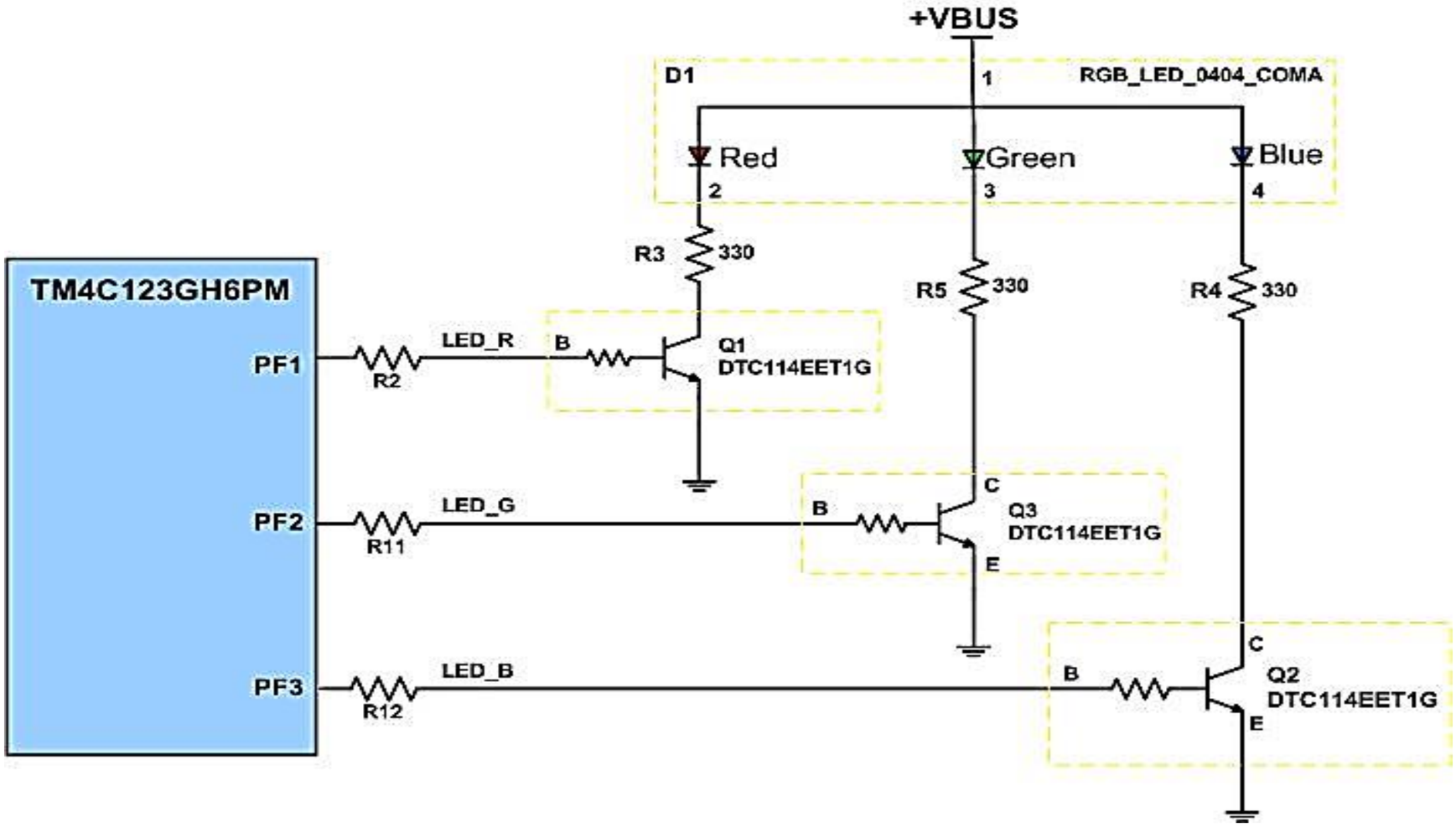
LED connection in TI Tiva LaunchPad

(LED connection to PORTF in TI Tiva LaunchPad)



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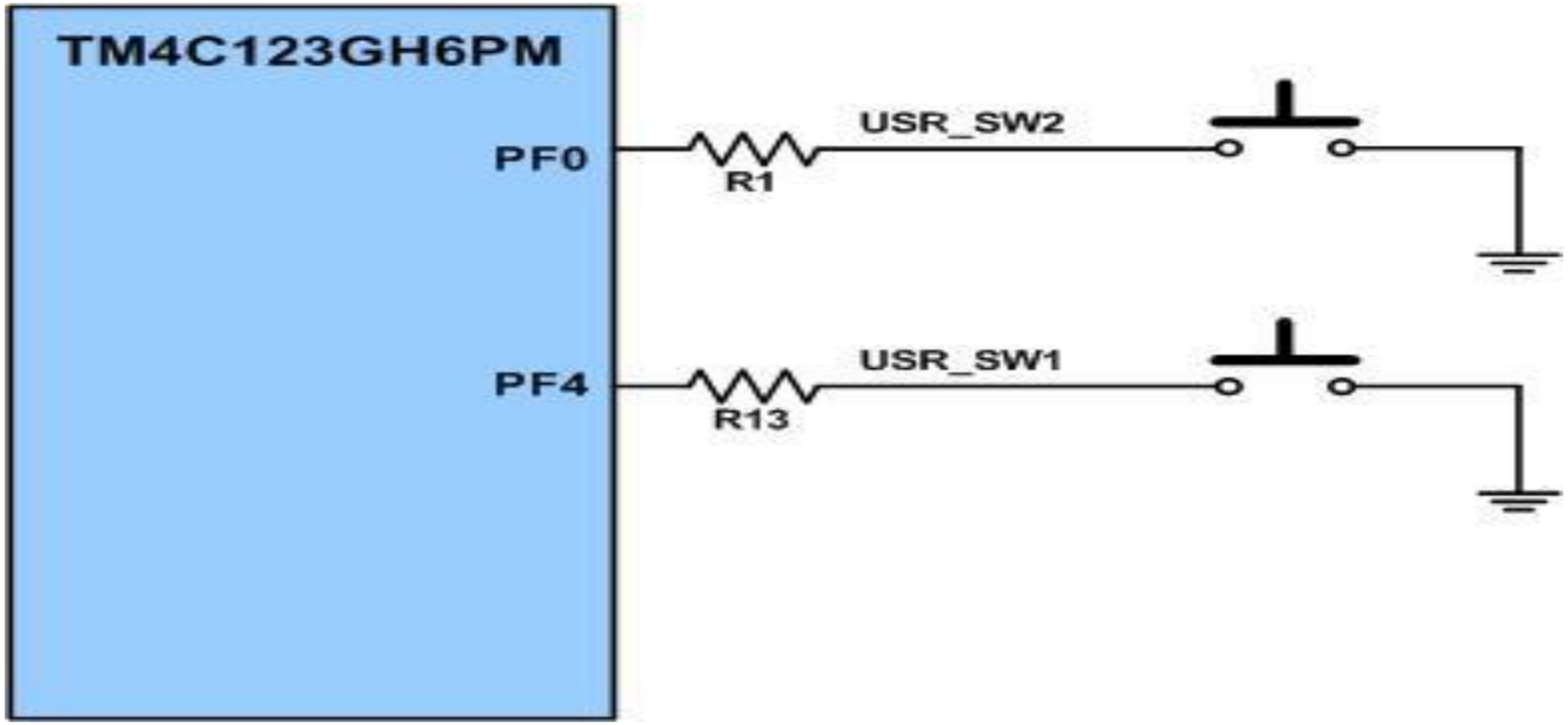
Reading a switch in TI Tiva LaunchPad

(Push-button Switches Connected to the Microcontroller in the Tiva LaunchPad Board)



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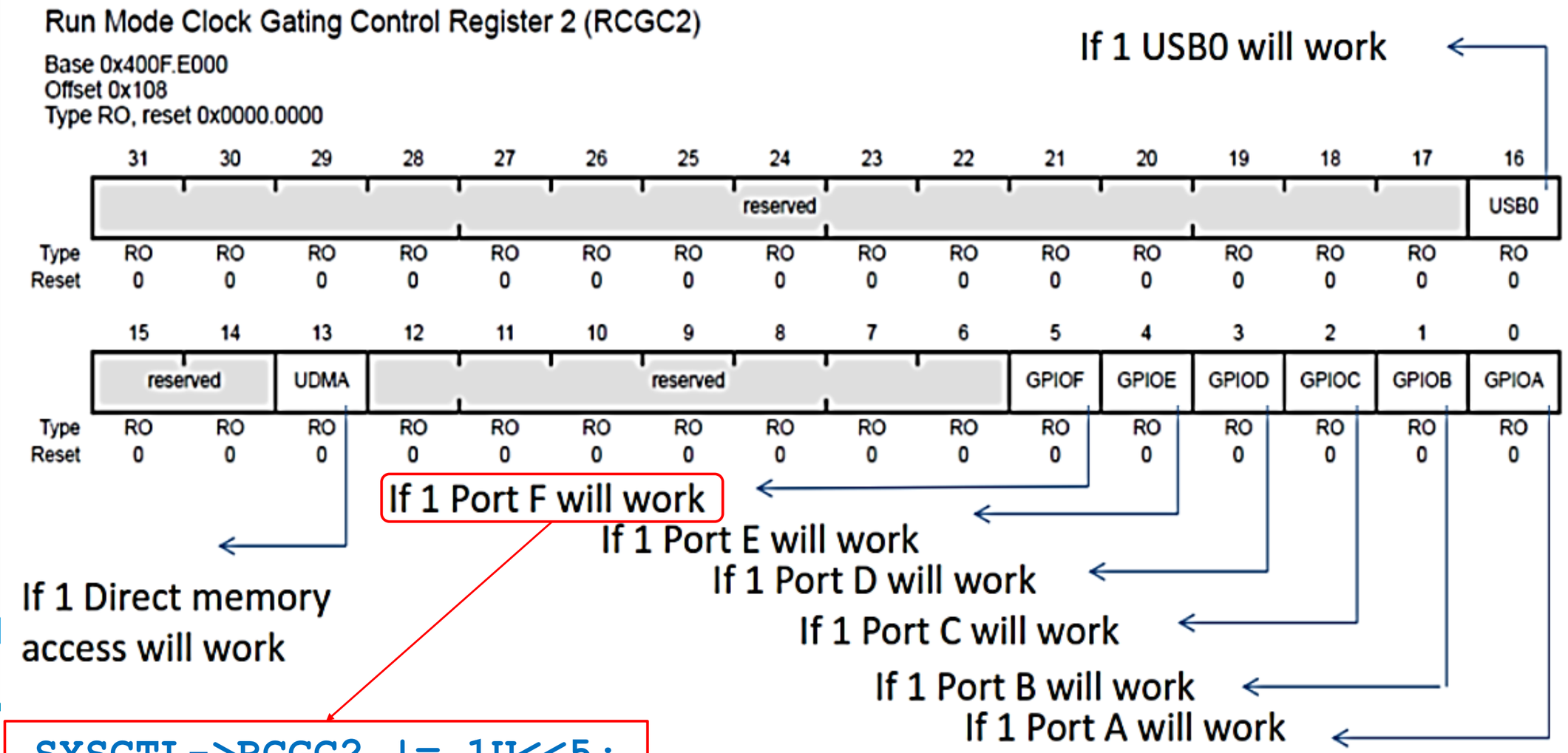
GPIO

1. CLOCK

Run Mode Clock Gating Control Register 2 (RCGC2)




```
SYSCTL->RCGC2 |= 1U<<5;
```

GPIO

1. CLOCK

General-Purpose Input/Output Run Mode Clock Gating Control(RCGCGPIO)

General-Purpose Input/Output Run Mode Clock Gating Control (RCGCGPIO)

Base 0x400F.E000
Offset 0x608
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved										R5	R4	R3	R2	R1	R0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

If 1 Port F will work
If 1 Port E will work
If 1 Port D will work
If 1 Port C will work
If 1 Port B will work
If 1 Port A will work

This register should be used to control the clocking for the GPIO modules. To support legacy software, the RCGC2 register is available. **A write to the RCGC2 register also writes the corresponding bit in this register**.

```
SYSCTL->RCGCGPIO |= 1U<<5;
```

GPIO

1. CLOCK

General-Purpose Input/Output Peripheral Ready (PRGPIO)

General-Purpose Input/Output Peripheral Ready (PRGPIO)

Base 0x400F.E000
Offset 0xA08
Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved										R5	R4	R3	R2	R1	R0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

```
While(!(SYSCTL->PRGIO & 1U<<5));
```

Value description

0: GPIO Port X is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.

1: GPIO Port x is ready for access.

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GPIO

2. GPIODIR

Register 2: GPIO Direction (GPIODIR), offset 0x400

The **GPIODIR** register is the data direction register. Setting a bit in the **GPIODIR** register configures the corresponding pin to be an output, while clearing a bit configures the corresponding pin to be an input. All bits are cleared by a reset, meaning all GPIO pins are inputs by default.

GPIO Direction (GPIODIR)

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
Offset 0x400
Type R/W, reset 0x0000.0000

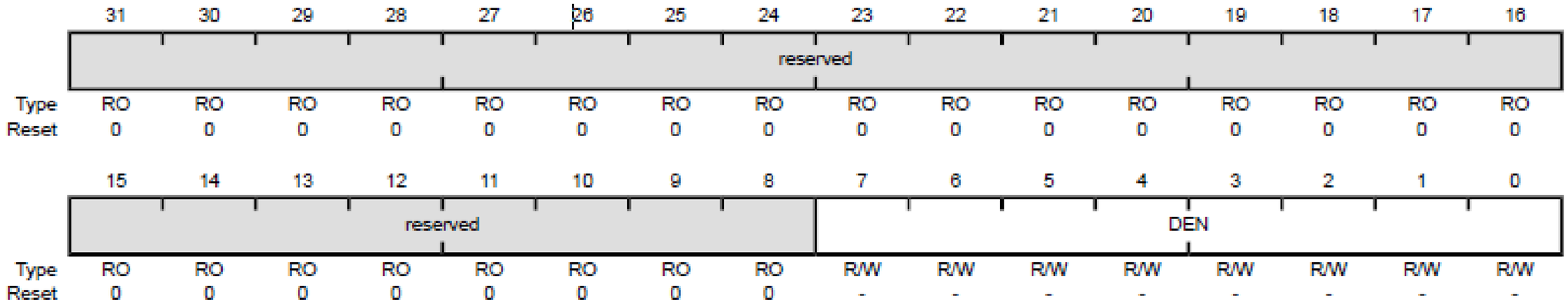
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								DIR							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Input 0,output =1

GPIO

3. GPIODEN (GPIO Digital Enable)

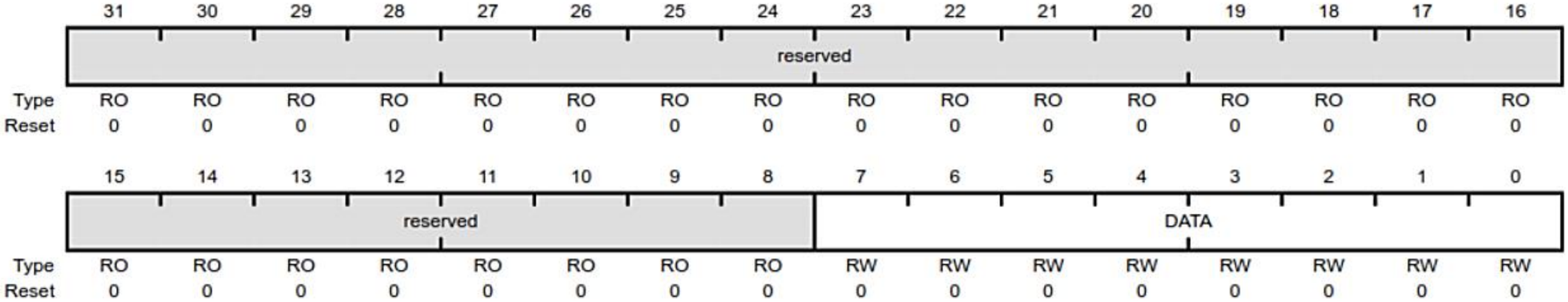


Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	DEN	R/W	-	Digital Enable

Value	Description
0	The digital functions for the corresponding pin are disabled.
1	The digital functions for the corresponding pin are enabled.

The reset value for this register is 0x0000.0000 for GPIO ports that are not listed in Table 10-1 on page 648.

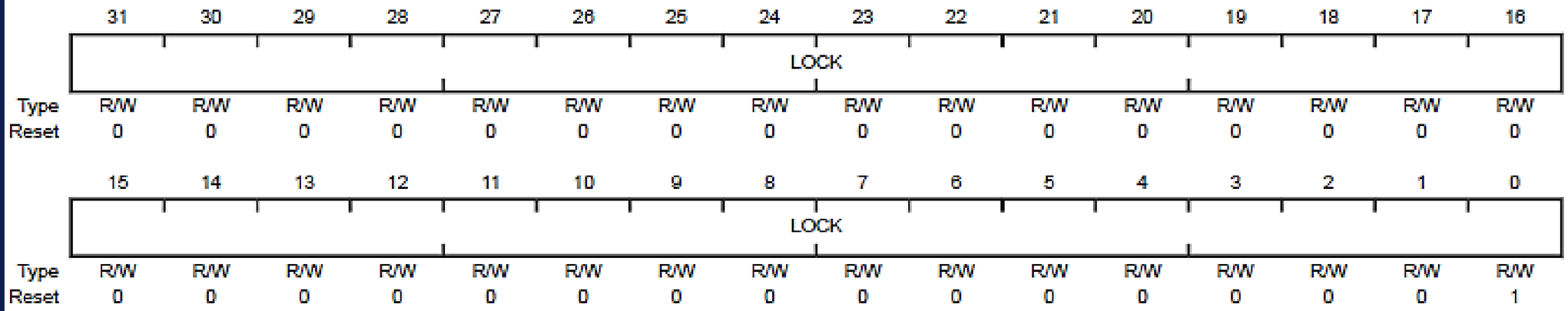
4. GPIODATA (GPIO Data)



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	DATA	RW	0x00	GPIO Data This register is virtually mapped to 256 locations in the address space. To facilitate the reading and writing of data to these registers by independent drivers, the data read from and written to the registers are masked by the eight address lines [9:2]. Reads from this register return its current state. Writes to this register only affect bits that are not masked by ADDR[9:2] and are configured as outputs. See “Data Register Operation” on page 654 for examples of reads and writes.

GPIO

5. GPIOLOCK



Bit/Field	Name	Type	Reset	Description
31:0	LOCK	R/W	0x0000.0001	GPIO Lock A write of the value 0x4C4F.434B unlocks the GPIO Commit (GPIOCR) register for write access.A write of any other value or a write to the GPIOCR register reapplies the lock, preventing any register updates. A read of this register returns the following values:

```
GPIOF->LOCK = 0x4C4F434B;
GPIOF->CR |= 0x1F;
```

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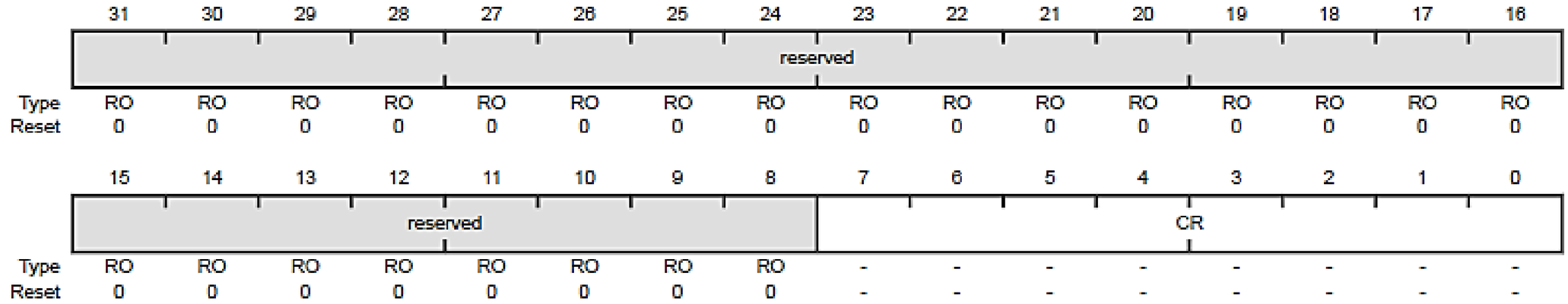
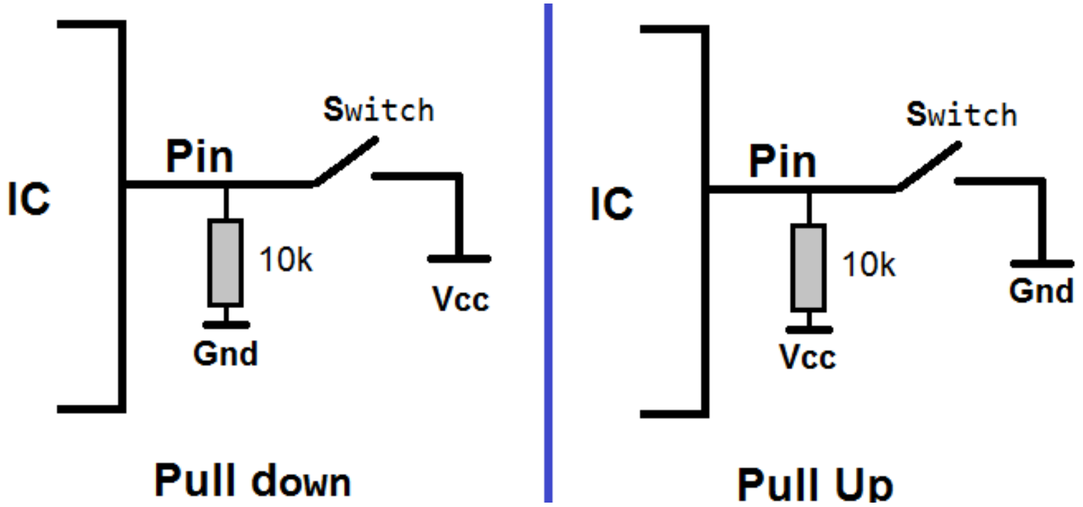
6. GPIOCR

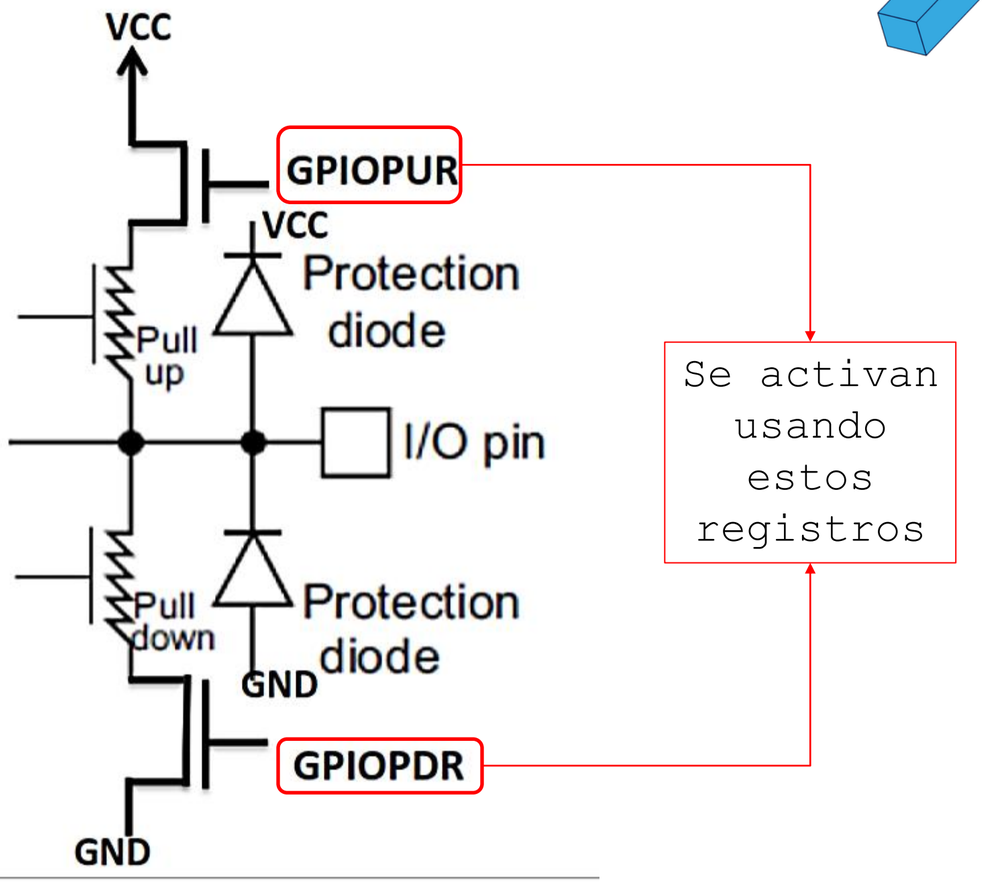


Este registro está diseñado para evitar la programación accidental de los registros que controlan la conectividad al hardware de depuración NMI y JTAG / SWD. Inicializando los bits del registro GPIOCR a 0 para PD7, PF0 y PC [3: 0].

GPIO

En la tiva-c está disponible una resistencia pull-up interna y una resistencia pull-down interna en cada pin.





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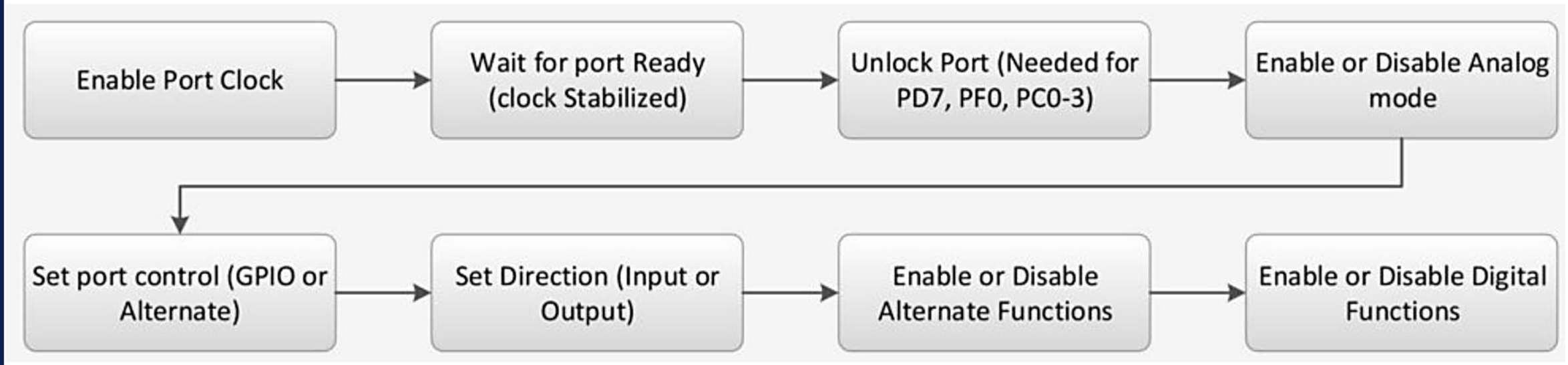
CONFIGURACION

PROCESO DE CONFIGURACION



PROCESO DE CONFIGURACION

```
/*Enable clock GPIOF*/
SYSCTL->RCGCGPIO |= 1<<5;
while(!(SYSCTL->PRGPIO & 1U<<5));
/*config output pins*/
/*UNLOCK*/
GPIOF->LOCK = 0x4C4F434B;
GPIOF->CR |= 0x1F;
//PF1, PF2, PF3
GPIOF->DEN |= 1<<3 | 1<< 2 | 1<<1;
GPIOF->DIR |= 1<<3 | 1<< 2 | 1<<1;
/*config input pins*/
//PF0, PF4
GPIOF->DIR &=~ (1<<4 | 1); //10001
GPIOF->DEN |= (1<<4 | 1);
GPIOF->PUR |= (1<<4 | 1);
```

ESCRITURA

```
GPIOF->DATA |= 1U<<1;  //PF1 -> HIHG
```

ESCRITURA

```
SW2 = (GPIOF->DATA & 0x1U); //read PF0
```

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DISPLAY DE 7 SEGMENTOS

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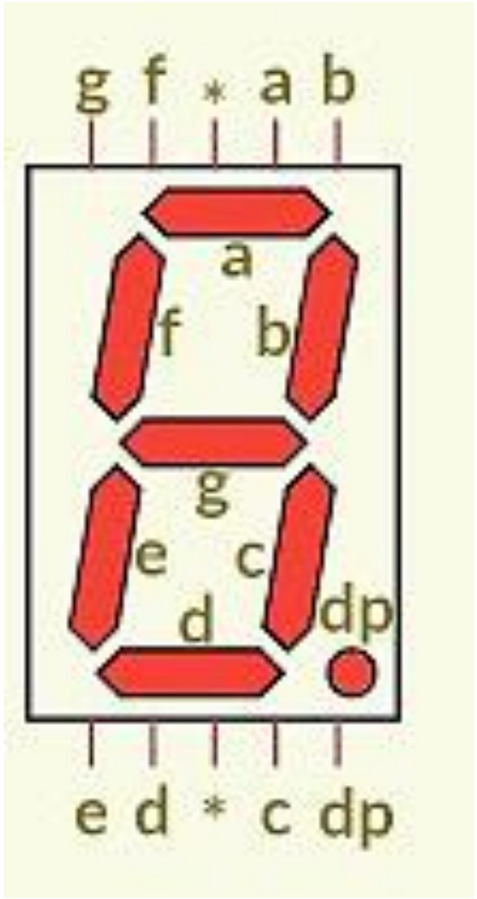
DISPLAY 7 SEGMENTOS CATADO COMUN



Num	D7	D6	D5	D4	D3	D2	D1	D0	Hex value
	.	g	f	e	d	c	b	a	
0	0	0	1	1	1	1	1	1	0x3F
1	0	0	0	0	0	1	1	0	0x06
2	0	1	0	1	1	0	1	1	0x5B
3	0	1	0	0	1	1	1	1	0x4F
4	0	1	1	0	0	1	1	0	0x66
5	0	1	1	0	1	1	0	1	0x6D
6	0	1	1	1	1	1	0	1	0x7D
7	0	0	0	0	0	1	1	1	0x07
8	0	1	1	1	1	1	1	1	0x7F
9	0	1	1	0	1	1	1	1	0x6F

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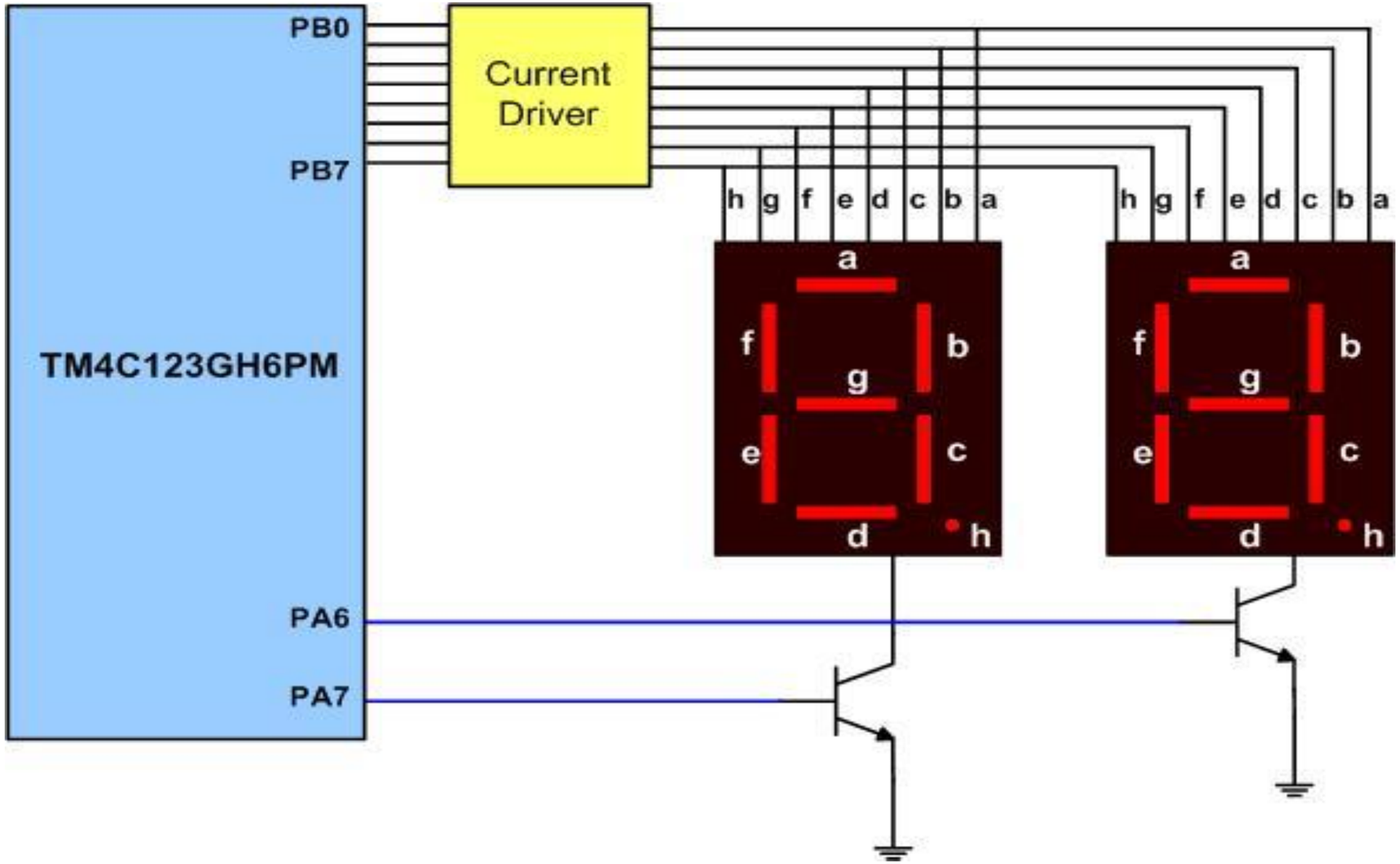
DISPLAY 7 SEGMENTOS CATADO COMUN

MULTIPLEXACION



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