SNx4HCT245 Octal Bus Transceivers With 3-State Outputs

1 Features

- Operating voltage range of 4.5 V to 5.5 V
- High-Current 3-state outputs drive bus lines directly or up to 15-LSTTL loads
- Low power consumption, 80-µA maximum I_{CC}
- Typical t_{pd} = 14 ns
- ±6-mA output drive at 5 V
- Low input current of 1 µA maximum
- Inputs are TTL-voltage compatible

2 Applications

- Factory Automation and Control
- Grid Infrastructure
- Electronic Point of Sale
- Multi-Function Printers
- Motor Drives
- Storage
- Telecom Infrastructure

3 Description

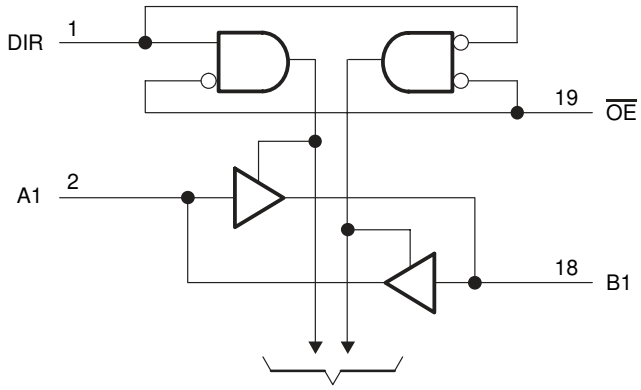
The SNx4HCT245 octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The SNx4HCT245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN54HCT245	J (CDIP, 20)	24.20 mm × 6.92 mm
	FK (LCCC, 20)	8.89 mm × 8.89 mm
	W (CFP, 20)	13.09 mm × 6.92 mm
SN74HCT245	DW (SOIC, 20)	12.80 mm × 7.50 mm
	N (PDIP, 20)	24.33 mm × 6.35 mm
	NS (SO, 20)	12.60 mm × 5.30 mm
	PW (TSSOP, 20)	6.50 mm × 4.40 mm
	DB (SSOP, 20)	7.80 mm × 7.20 mm
	DGS (VSSOP, 20)	5.10 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

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4 Revision History

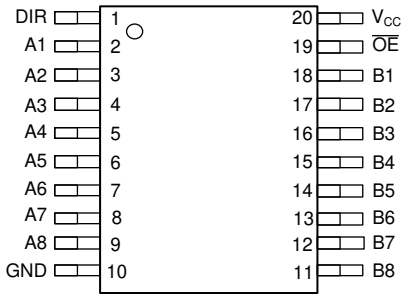
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (September 2022) to Revision H (December 2022)	Page
• Added DGS package information	1
• Added DGS package values in the *Thermal Information* table	5

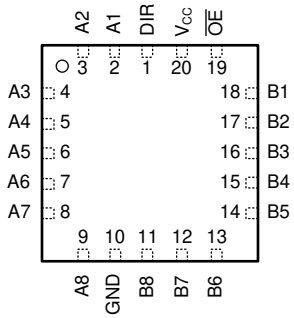
Changes from Revision F (August 2016) to Revision G (September 2022)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	1

Changes from Revision E (August 2003) to Revision F (August 2016)	Page
• Deleted Ordering Information, see POA at the end of the datasheet	1
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Updated values in the *Thermal Information* table	5

5 Pin Configuration and Functions



J, W, DB, DW, N, NS, PW or DGS Packages 20-Pin CDIP, CFP, SSOP, SOIC, PDIP, SO, TSSOP or VSSOP Top View



FK Package 20-Pin LCCC Top View

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	DIR	I	Direction select. High = A to B, Low = B to A
2	A1	I/O	Channel 1 port A
3	A2	I/O	Channel 2 port A
4	A3	I/O	Channel 3 port A
5	A4	I/O	Channel 4 port A
6	A5	I/O	Channel 5 port A
7	A6	I/O	Channel 6 port A
8	A7	I/O	Channel 7 port A
9	A8	I/O	Channel 8 port A
10	GND	—	Ground
11	B8	O/I	Channel 8 port B
12	B7	O/I	Channel 7 port B
13	B6	O/I	Channel 6 port B
14	B5	O/I	Channel 5 port B
15	B4	O/I	Channel 4 port B
16	B3	O/I	Channel 3 port B
17	B2	O/I	Channel 2 port B
18	B1	O/I	Channel 1 port B
19	$\overline{OE}$	I	Output enable, active low. High = all ports in high impedance mode, Low = all ports active
20	V_{CC}	—	Power supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall time				500	ns
T_A	Operating free-air temperature	SN54HCT245	–55		125	°C
		SN74HCT245	–40		85	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC[1]		SNx4HCT245									UNIT
		J (CDIP)	W (CFP)	FK (LCCC)	DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	DGS (VSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	—	—	—	84.6	70.4	43.4	68.9	94.9	118.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.7	60.8	37.1	44.3	36.5	29.5	34.7	30.2	57.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.8	100.4	36.1	40.2	38.1	24.3	36.4	45.7	73.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	—	—	—	11.1	11.3	15	11.6	1.5	5.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	—	—	—	39.7	37.7	24.2	36	45.1	72.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.5	8.5	4.3	—	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-Level Output Voltage		$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	T_A = 25°C	4.5 V	4.4	4.499		V
					SN54HCT245		4.4			
					SN74HCT245		4.4			
				I_{OH} = –6 mA	T_A = 25°C		3.98	4.3		
					SN54HCT245		3.7			
					SN74HCT245		3.84			
V_{OL}	Low-Level Output Voltage		$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	T_A = 25°C	4.5 V		0.001	0.1	V
					SN54HCT245				0.1	
					SN74HCT245				0.1	
				I_{OL} = 6 mA	T_A = 25°C			0.17	0.26	
					SN54HCT245				0.4	
					SN74HCT245				0.33	
I_I	Input Current	DIR or $\overline{OE}$	$V_I = V_{CC}$ or 0	T_A = 25°C		5.5 V		±0.1	±100	nA
				SN54HCT245					±1000	
				SN74HCT245					±1000	
I_{OZ}	Off-State Output Current	A or B	$V_O = V_{CC}$ or 0	T_A = 25°C		5.5 V		±0.01	±0.5	µA
				SN54HCT245					±10	
				SN74HCT245					±5	
I_{CC}	Supply Current		$V_I = V_{CC}$ or 0	I_O = 0	T_A = 25°C	5.5 V			8	µA
					SN54HCT245				160	
					SN74HCT245				80	
ΔI_{CC} [1]	Supply-Current Change		One input at 0.5 V or 2.4 V, Other inputs at 0 or VCC	T_A = 25°C		5.5 V		1.4	2.4	mA
				SN54HCT245					3	
				SN74HCT245					2.9	

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_i (2)	Input Capacitance	DIR or $\overline{OE}$	T_A = 25°C	4.5 V to 5.5 V		3	10	pF
			SN54HCT245				10	
			SN74HCT245				10	

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.
(2) Parameter C_i does not apply to transceiver I/O ports.

6.6 Switching Characteristics: C_L = 50 pF

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	A or B	B or A	4.5 V	T_A = 25°C		16	22	ns
				SN54HCT245			33	
				SN74HCT245			28	
			5.5 V	T_A = 25°C		14	20	
				SN54HCT245			30	
				SN74HCT245			25	
t_{en}	$\overline{OE}$	A or B	4.5 V	T_A = 25°C		25	46	ns
				SN54HCT245			69	
				SN74HCT245			58	
			5.5 V	T_A = 25°C		22	41	
				SN54HCT245			62	
				SN74HCT245			52	
t_{dis}	$\overline{OE}$	A or B	4.5 V	T_A = 25°C		26	40	ns
				SN54HCT245			60	
				SN74HCT245			50	
			5.5 V	T_A = 25°C		23	36	
				SN54HCT245			54	
				SN74HCT245			45	
t_t		A or B	4.5 V	T_A = 25°C		9	12	ns
				SN54HCT245			18	
				SN74HCT245			15	
			5.5 V	T_A = 25°C		8	11	
				SN54HCT245			16	
				SN74HCT245			14	

6.7 Switching Characteristics: C_L = 150 pF

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	A or B	B or A	4.5 V	T_A = 25°C		20	30	ns
				SN54HCT245			45	
				SN74HCT245			38	
			5.5 V	T_A = 25°C		18	27	
				SN54HCT245			41	
				SN74HCT245			34	
t_{en}	$\overline{OE}$	A or B	4.5 V	T_A = 25°C		36	59	ns
				SN54HCT245			89	
				SN74HCT245			74	
			5.5 V	T_A = 25°C		30	53	
				SN54HCT245			80	
				SN74HCT245			67	
t_t		A or B	4.5 V	T_A = 25°C		17	42	ns
				SN54HCT245			63	
				SN74HCT245			53	
			5.5 V	T_A = 25°C		14	38	
				SN54HCT245			57	
				SN74HCT245			48	

6.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load	40	pF

6.9 Typical Characteristics

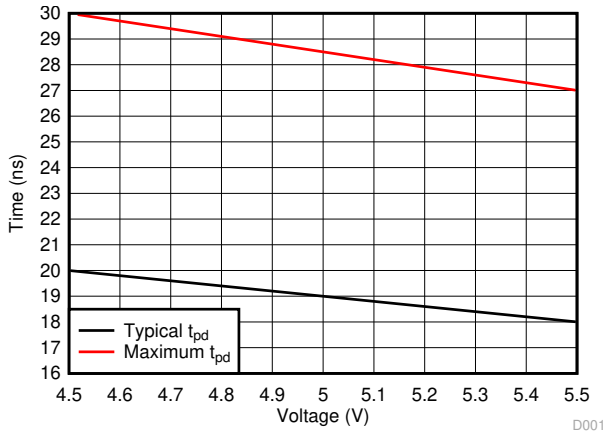
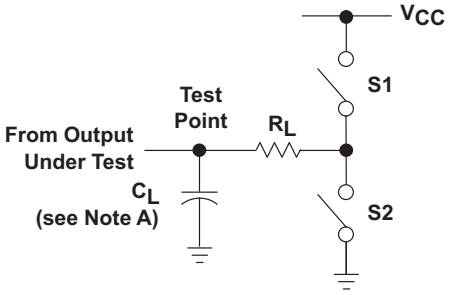


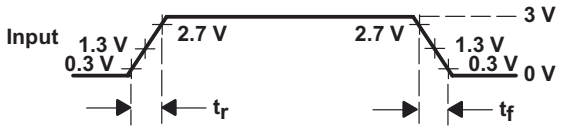
Figure 6-1. Propagation Delay Over Operating Voltage Range, T_A = 25°C

7 Parameter Measurement Information

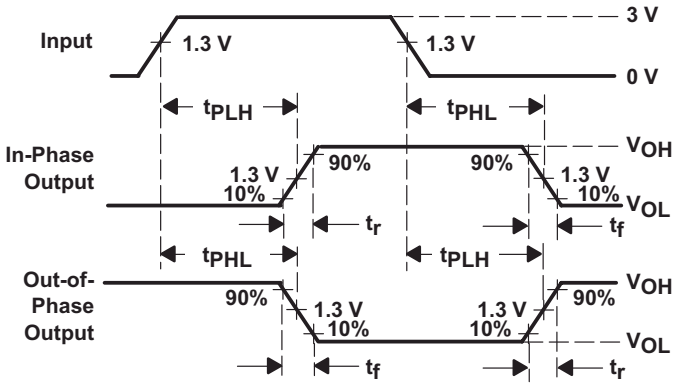


LOAD CIRCUIT

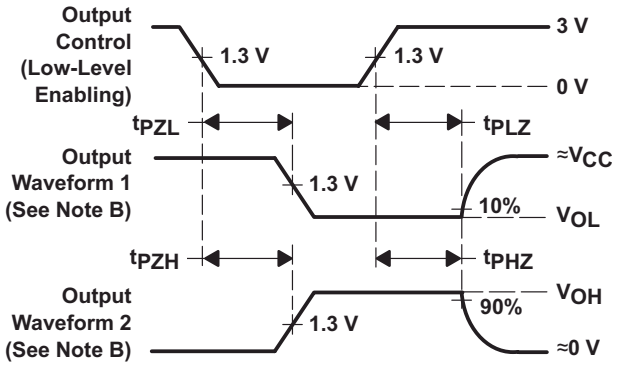
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4HCT245 is a bidirectional buffer with direction control and active low output enable. This device is commonly used in logic systems for isolation and increasing drive strength.

8.2 Functional Block Diagram

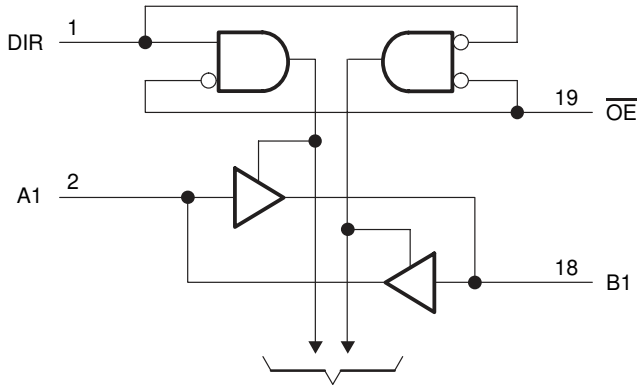


Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

Voltage operating range from 4.5 V to 5.5 V is forgiving of 5-V power supply rail accuracy. Outputs can operate up to 15 LSTTL loads. This device has balanced propagation delay, typically 14 ns, and balanced output drive of ±6 mA at 5 V. It has low power consumption of only 80-µA maximum static supply current. The center V_{CC} and GND pin configurations minimize high-speed switching noise. Inputs are TTL-voltage compatible.

8.4 Device Functional Modes

This device is a standard '245 logic function. It has an active low output enable, a direction pin, and eight communication channels.

Table 8-1. Function Table

INPUTS(1)		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SNx4HCT245 is a versatile device with many available applications. The application chosen as an example here is connecting a master and slave device through a ribbon cable. This configuration is common due to losses in this type of cable.

9.2 Typical Application

Logic transceivers are commonly seen in back plane and ribbon cable applications where a signal direct from an FPGA or MCU would be too weak to reach the distant end. The transceiver acts as an amplifier to get the signal across the line, and since it is bidirectional, data can be sent from master to slave or slave to master. The additional buffer on the direction line is necessary to ensure the direction signal can always reach the distant end.

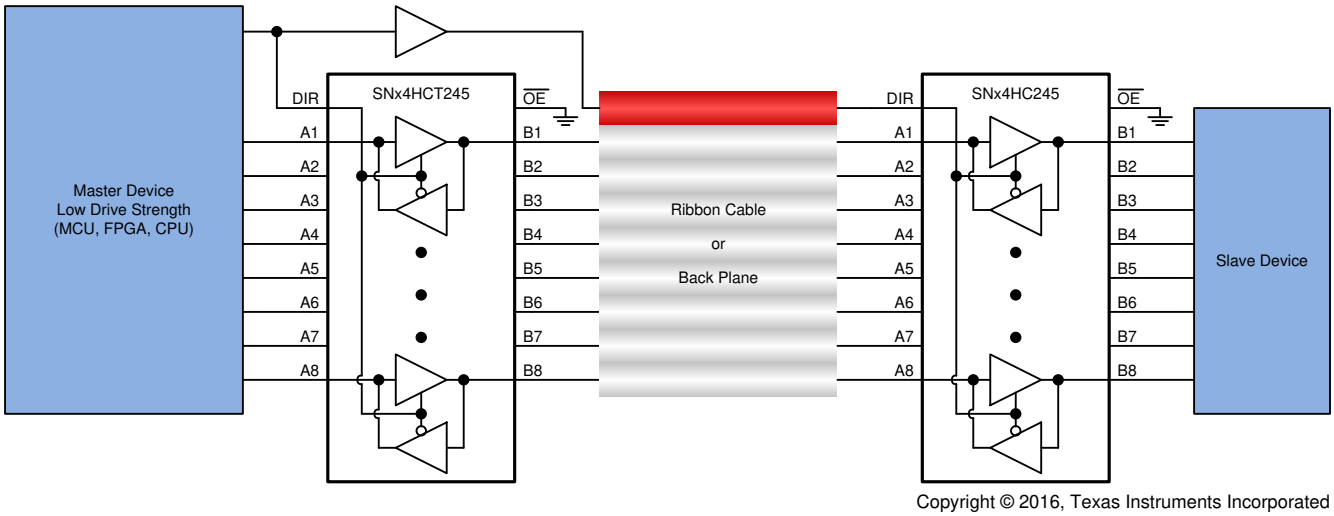


Figure 9-1. Typical application for SNx4HC245

9.2.1 Design Requirements

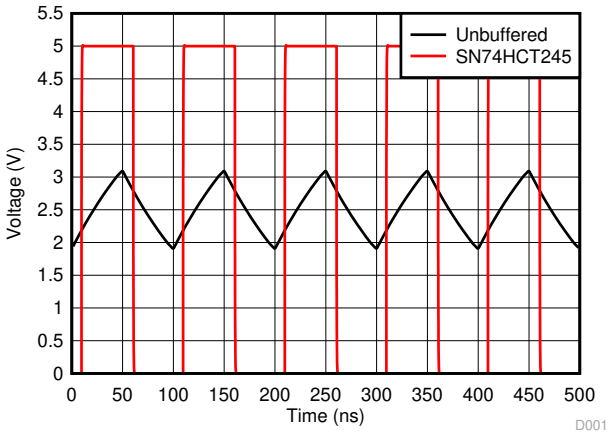
This device uses CMOS technology and has balanced output drive. Care must be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive, but the high drive also creates faster edges into light loads, so routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs: See (Δt/ΔV) in the *Recommended Operating Conditions*.
   - Specified high and low levels: See (VIH and VIL) in the *Recommended Operating Conditions*.
2. Recommended Output Conditions
   - Load currents should not exceed 35 mA per output and 70 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curve

It is common to see significant losses in ribbon cables and back planes. The plot shown in Figure 9-2 is a simplified simulation of a ribbon cable from a 5-V, 10-MHz low drive strength source. It shows the difference between an input signal from a weak driver like an MCU or FPGA compared to a strong driver like the SN74HCT245 when measured at the distant end of the cable. By adding a high-current drive transceiver before the cable, the signal strength can be significantly improved, and subsequently the cable can be longer.



Unbuffered line is directly connected to low current source, SN74HCT245 line is buffered through the transceiver. Both signals are measured at the distant end of the ribbon cable.

Figure 9-2. Simulated Outputs From Ribbon Cable With a 5-V, 10-MHz Source

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple VCC pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only six channels of an eight channel transceiver are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient.

The output enable pin disables the output section of the part when asserted. This does not disable the input section of the IOs, so they cannot float when disabled.

Figure 11-1 shows the proper method to terminate unused channels using a large resistance (in this example, 10-kΩ resistors). This avoids overloading the outputs , and maintains a valid voltage on the inputs. Note that it is also valid to tie both sides of an unused transceiver directly to ground or V_{CC}; however, the two sides must never be tied to different states directly.

11.2 Layout Example

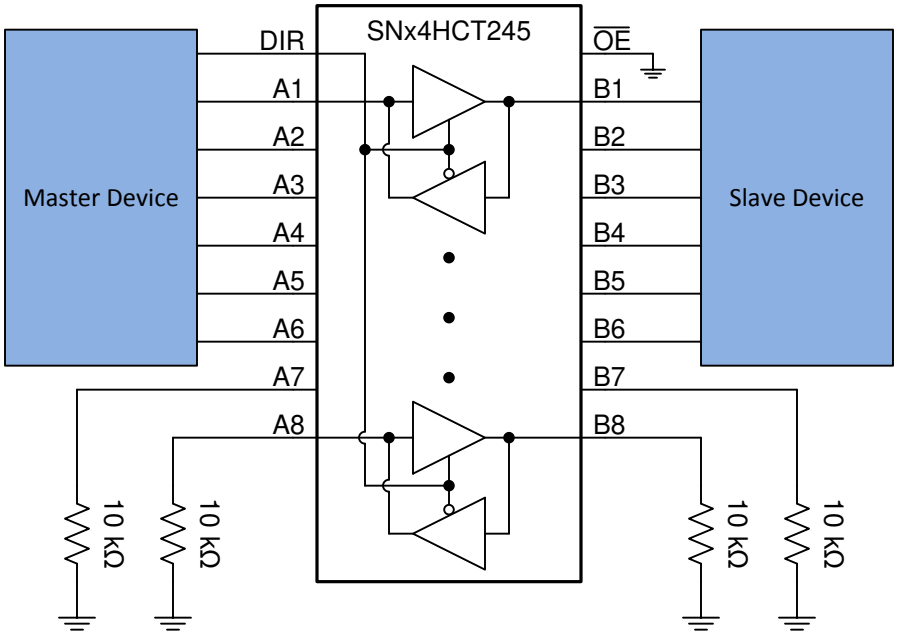


Figure 11-1. Proper Termination of $\overline{OE}$ Pin And Unused Channels 7 and 8

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HCT245	Click here	Click here	Click here	Click here	Click here
SN74HCT245	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8550601VRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8550601VR A SNV54HCT245J	Samples
5962-8550601VSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8550601VS A SNV54HCT245W	Samples
85506012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	85506012A SNJ54HCT 245FK	Samples
8550601RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8550601RA SNJ54HCT245J	Samples
JM38510/65553BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65553BRA	Samples
JM38510/65553BSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65553BSA	Samples
M38510/65553BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65553BRA	Samples
M38510/65553BSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65553BSA	Samples
SN54HCT245J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HCT245J	Samples
SN74HCT245DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT245	Samples
SN74HCT245DBRG4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT245	Samples
SN74HCT245DGSR	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HT245	Samples
SN74HCT245DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT245	Samples
SN74HCT245DWE4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT245	Samples
SN74HCT245DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT245	Samples
SN74HCT245DWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT245	Samples
SN74HCT245DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT245	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT245N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT245N	Samples
SN74HCT245NE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT245N	Samples
SN74HCT245NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT245	Samples
SN74HCT245PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT245	Samples
SN74HCT245PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HT245	Samples
SN74HCT245PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT245	Samples
SN74HCT245PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT245	Samples
SN74HCT245PWT	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT245	Samples
SNJ54HCT245FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	85506012A SNJ54HCT 245FK	Samples
SNJ54HCT245J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8550601RA SNJ54HCT245J	Samples
SNJ54HCT245W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54HCT245W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54HCT245, SN54HCT245-SP, SN74HCT245 :

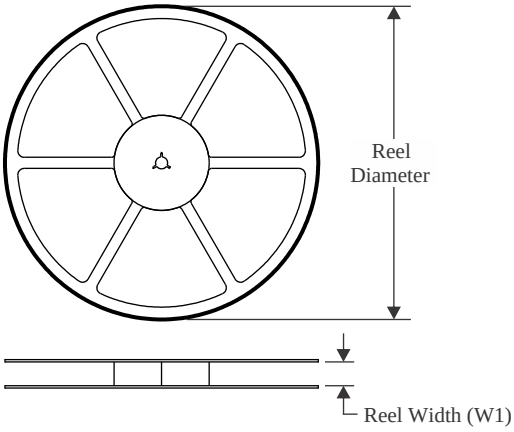
- Catalog : SN74HCT245, SN54HCT245
- Military : SN54HCT245
- Space : SN54HCT245-SP

NOTE: Qualified Version Definitions:

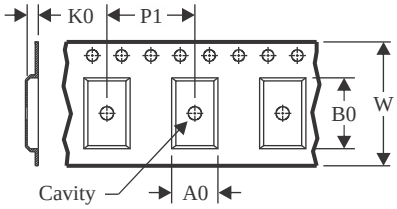
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

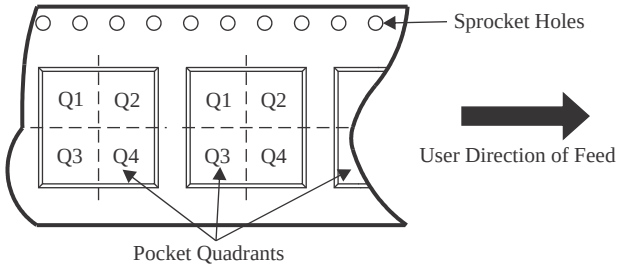


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

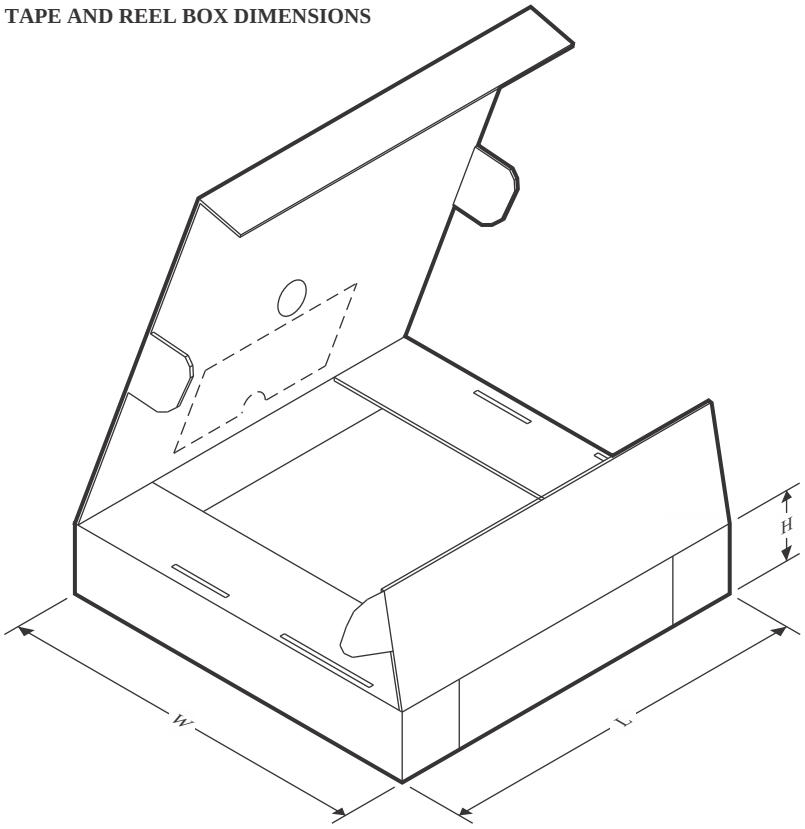
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HCT245DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74HCT245DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HCT245DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HCT245NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HCT245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HCT245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HCT245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74HCT245PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HCT245PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HCT245PWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

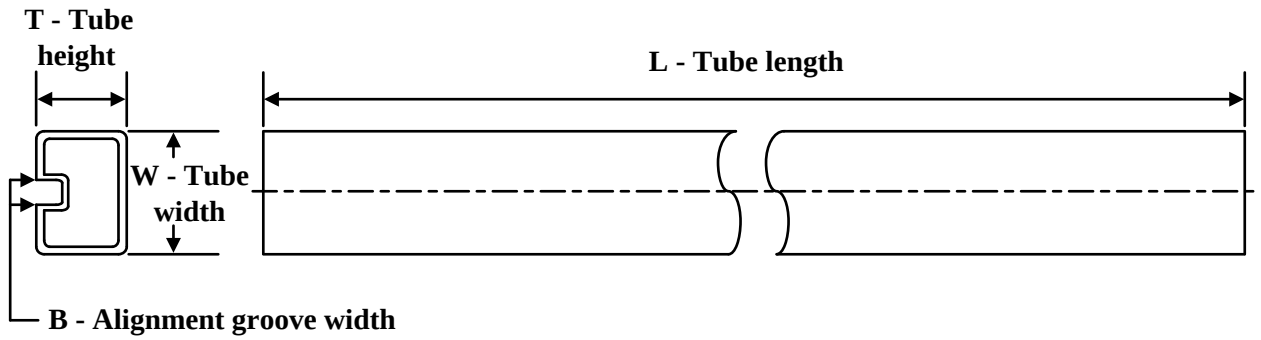
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT245DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74HCT245DGSR	VSSOP	DGS	20	5000	356.0	356.0	35.0
SN74HCT245DWR	SOIC	DW	20	2000	356.0	356.0	41.0
SN74HCT245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HCT245NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HCT245PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HCT245PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HCT245PWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74HCT245PWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HCT245PWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HCT245PWT	TSSOP	PW	20	250	356.0	356.0	35.0

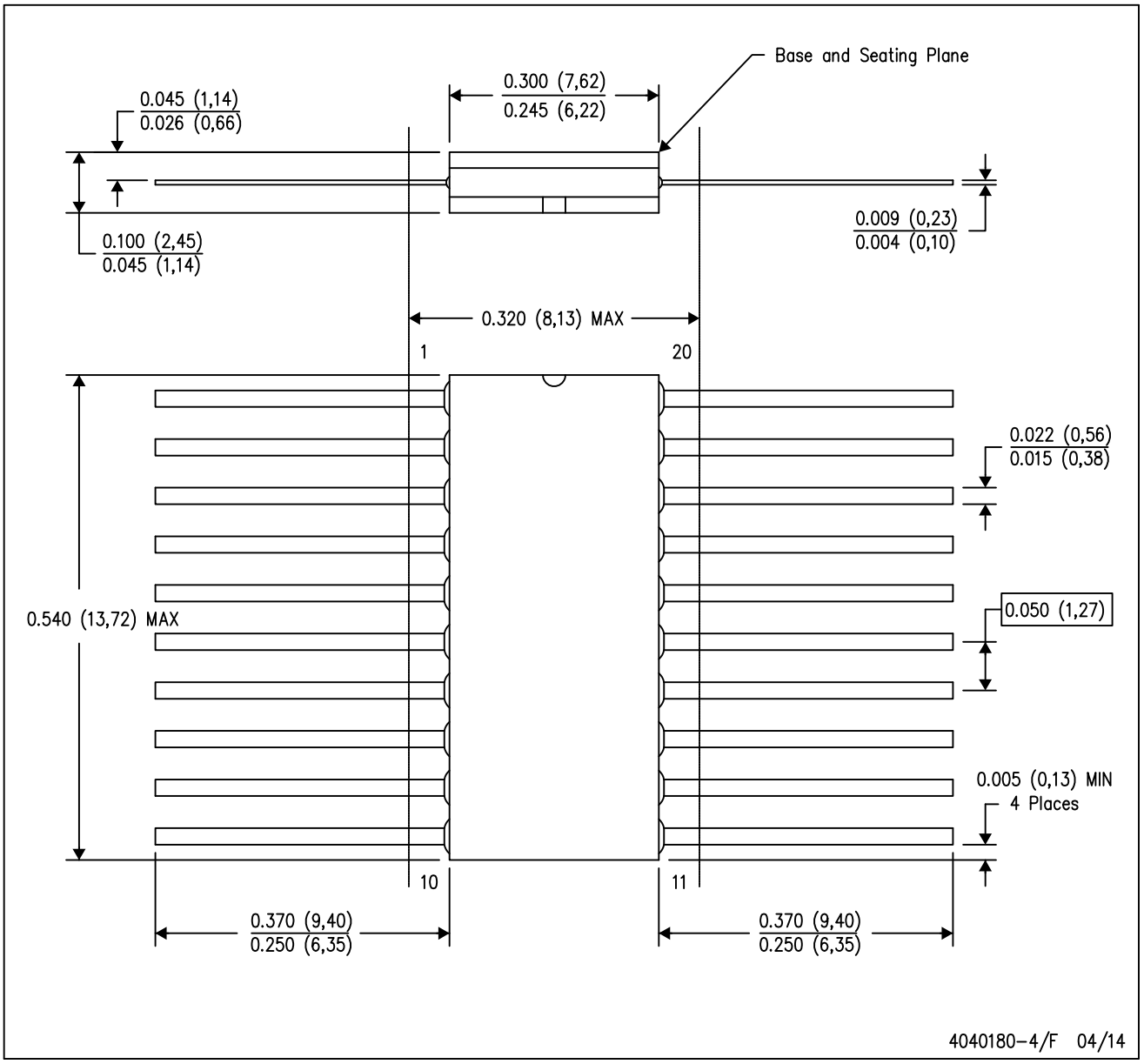
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8550601VSA	W	CFP	20	25	506.98	26.16	6220	NA
85506012A	FK	LCCC	20	1	506.98	12.06	2030	NA
JM38510/65553BSA	W	CFP	20	1	506.98	26.16	6220	NA
M38510/65553BSA	W	CFP	20	1	506.98	26.16	6220	NA
SN74HCT245DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HCT245DWE4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HCT245N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HCT245NE4	N	PDIP	20	20	506	13.97	11230	4.32
SN74HCT245PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54HCT245FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54HCT245W	W	CFP	20	1	506.98	26.16	6220	NA

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



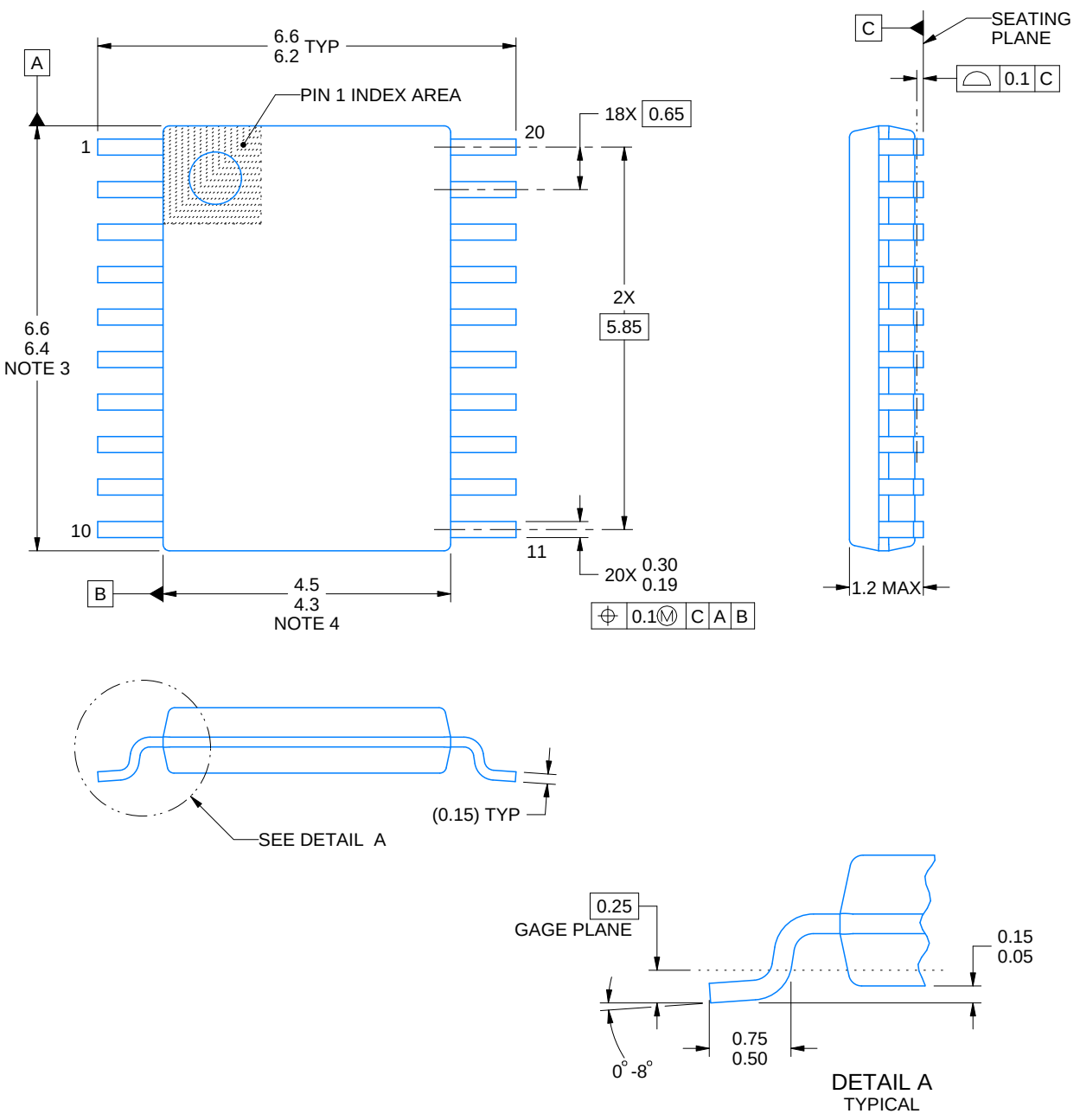
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

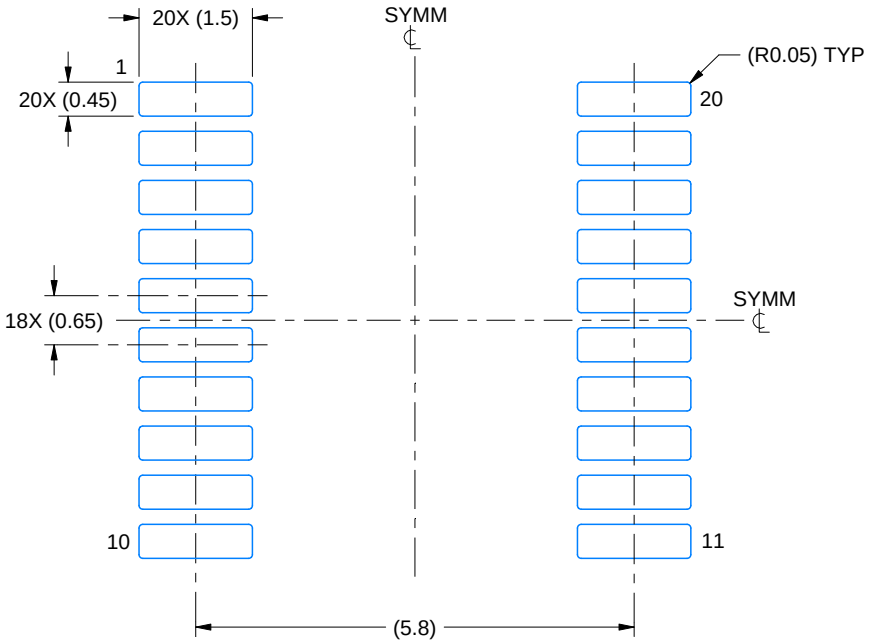
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



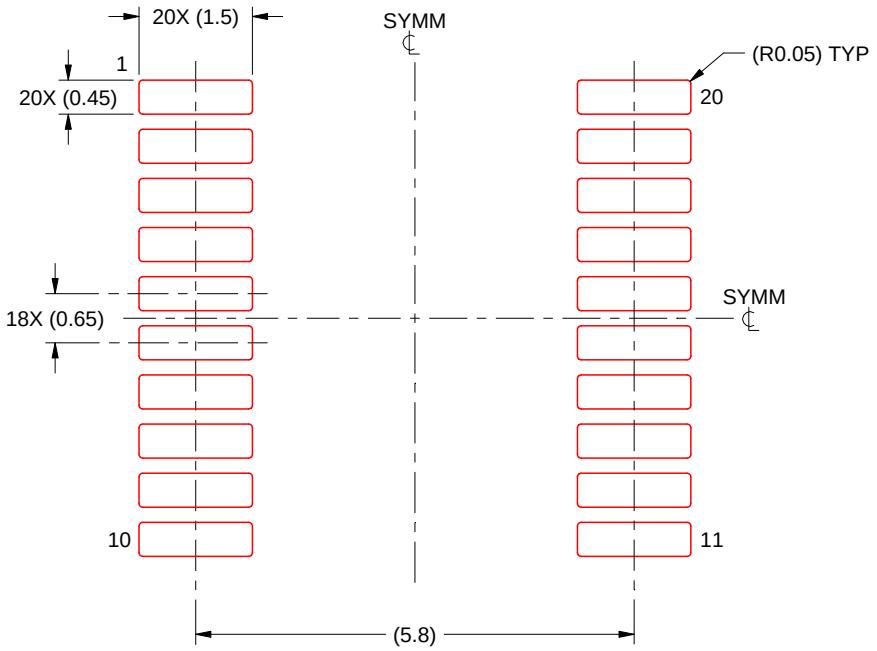
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



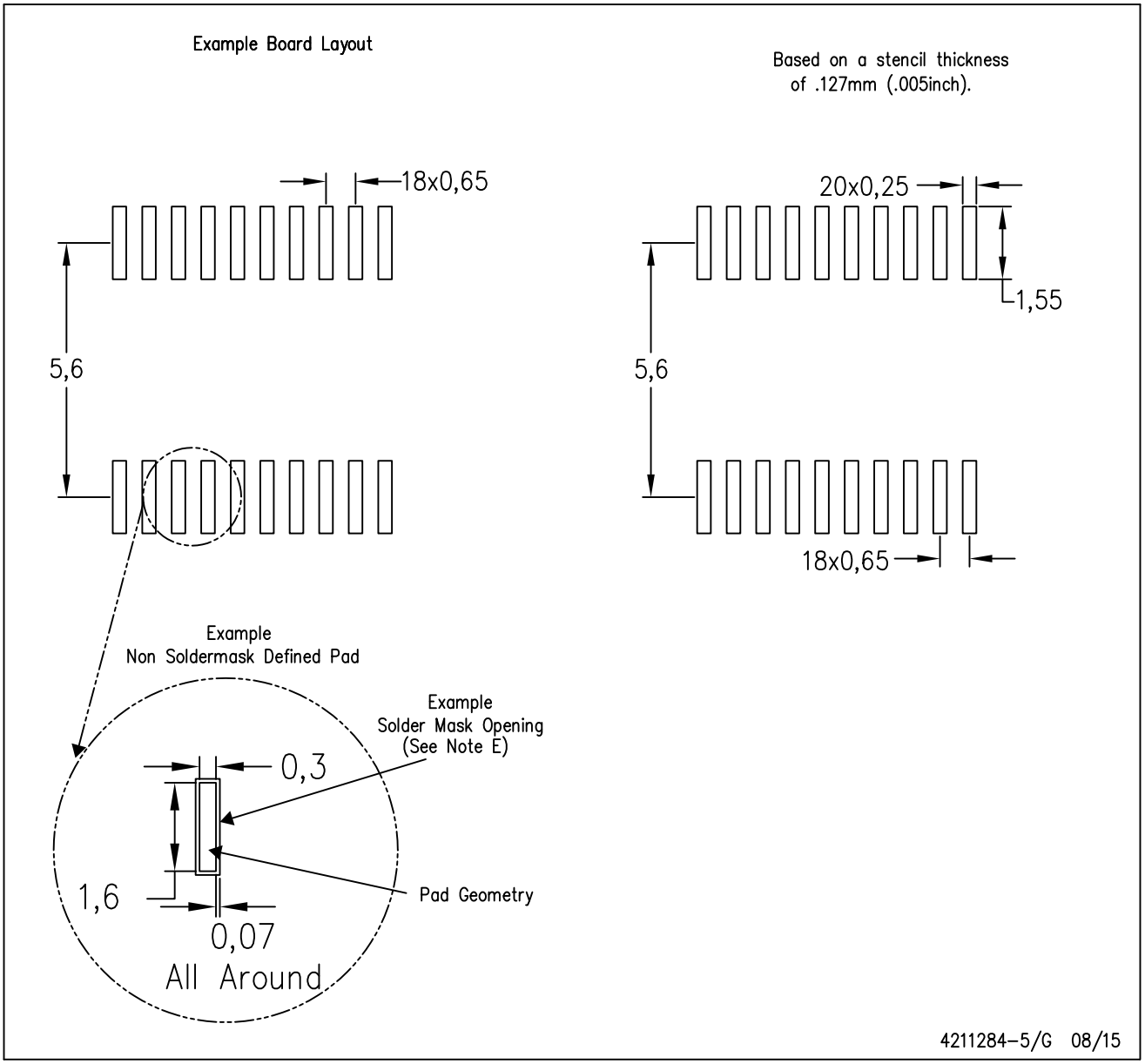
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



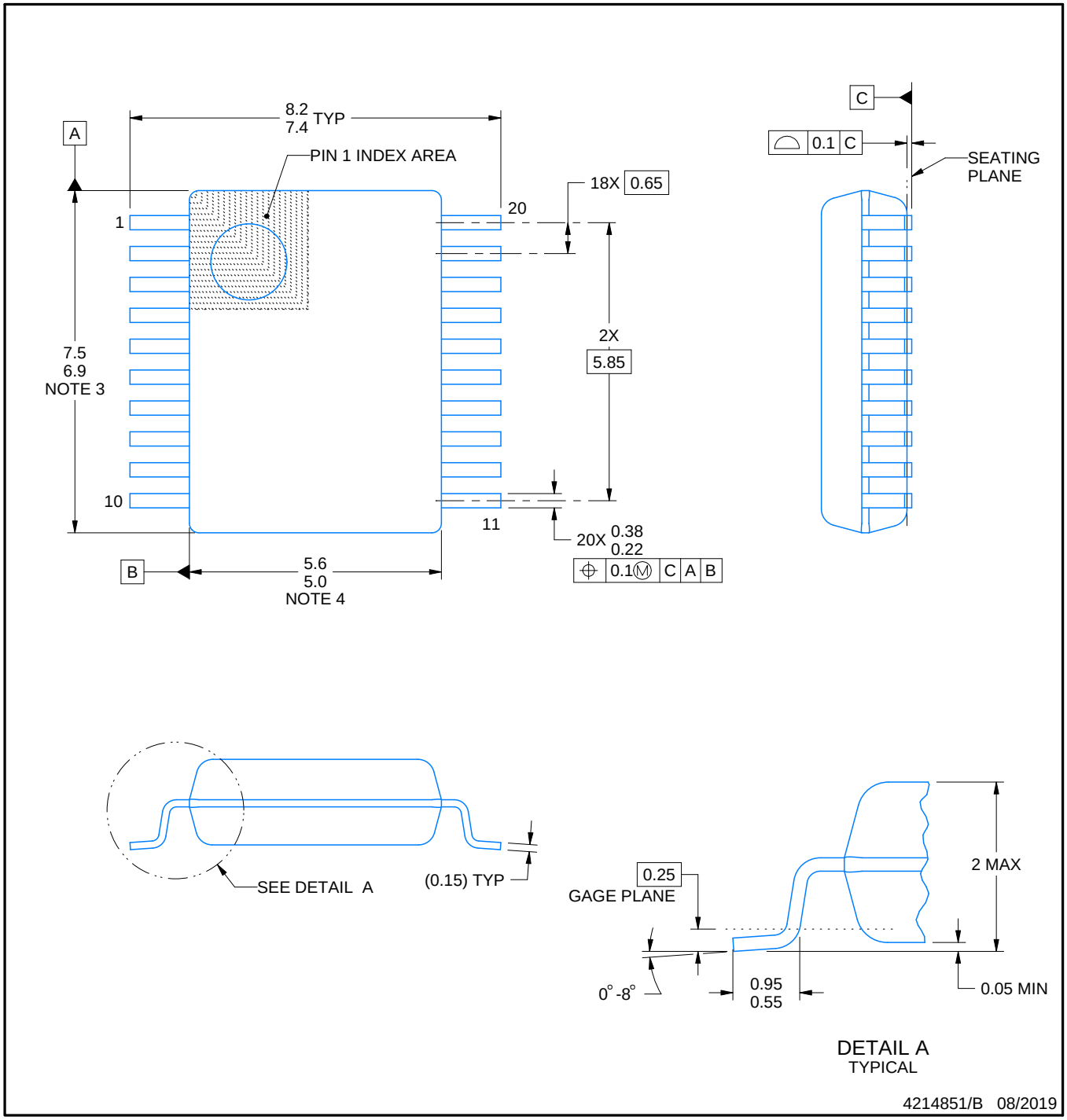
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DB0020A

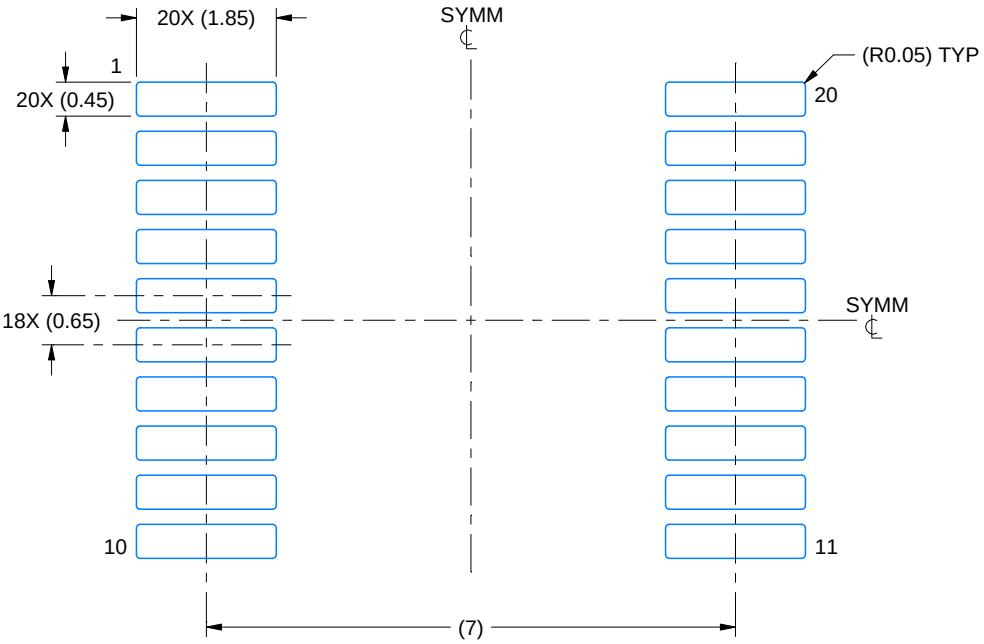
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

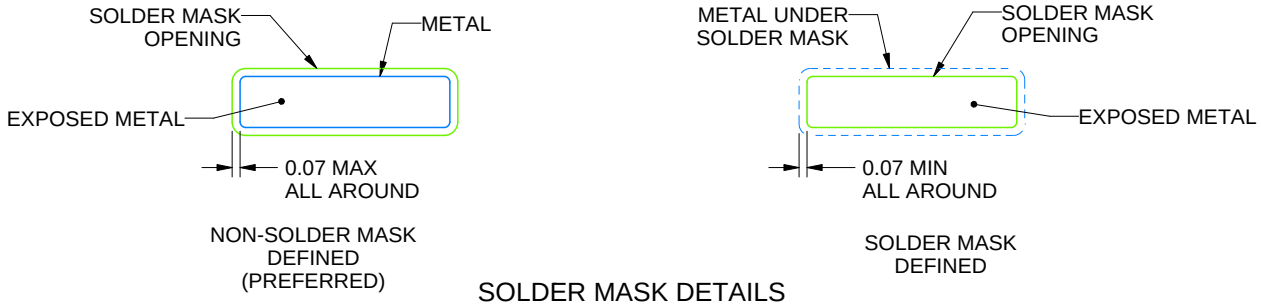


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

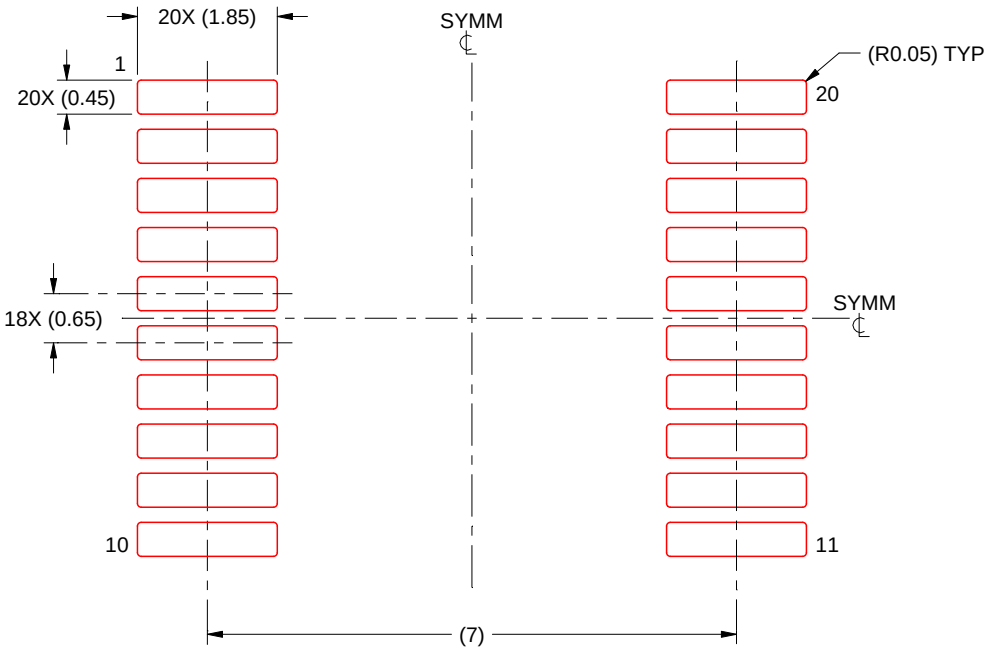
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

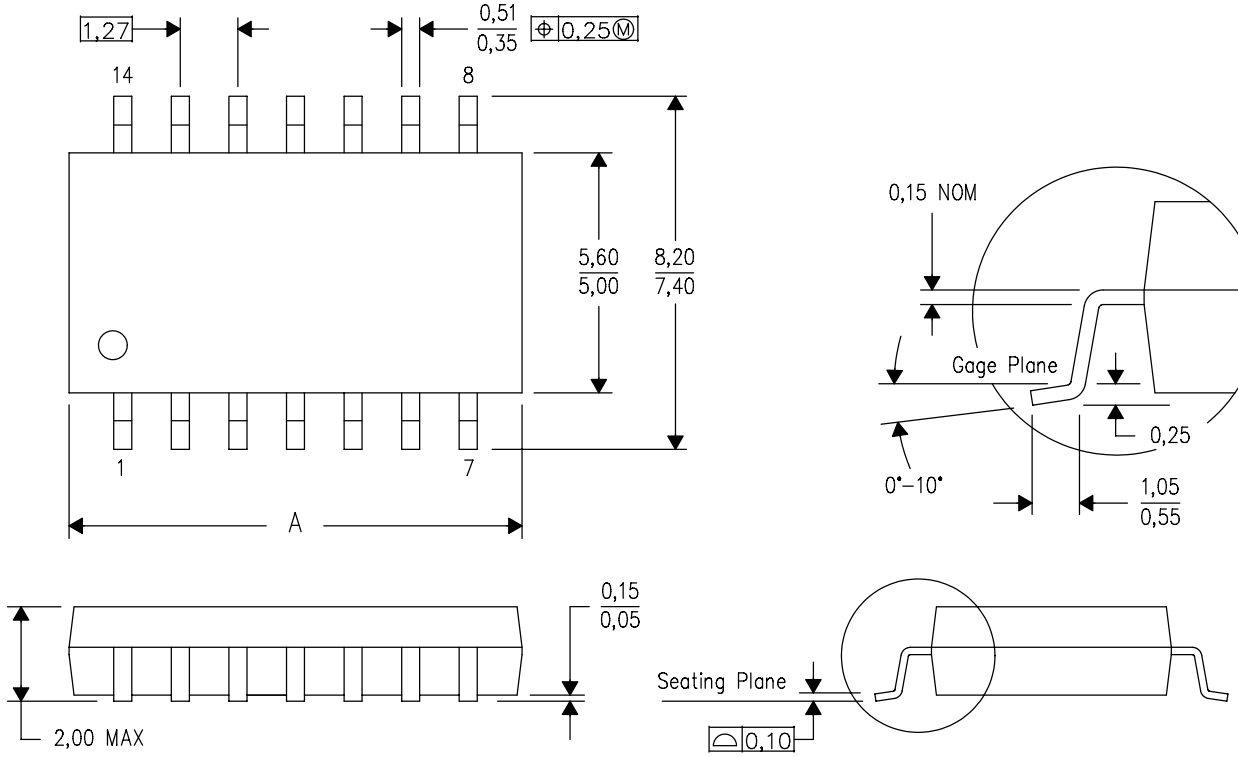
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

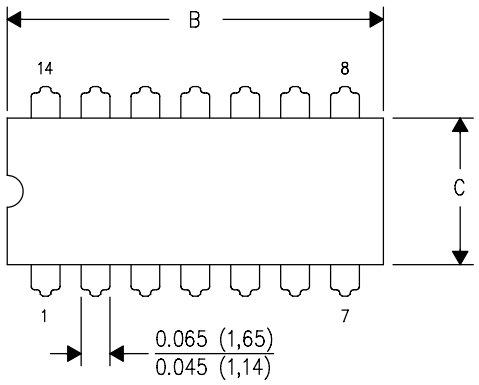
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

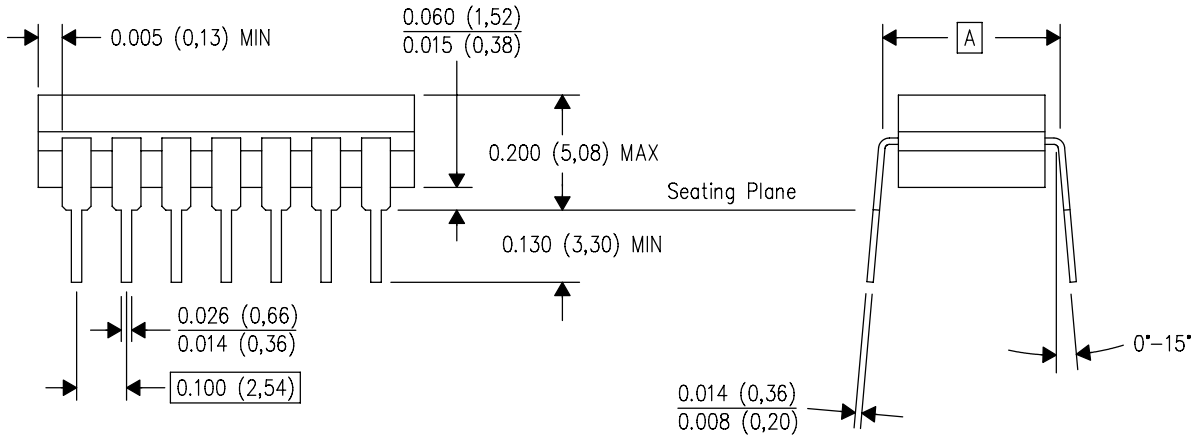
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

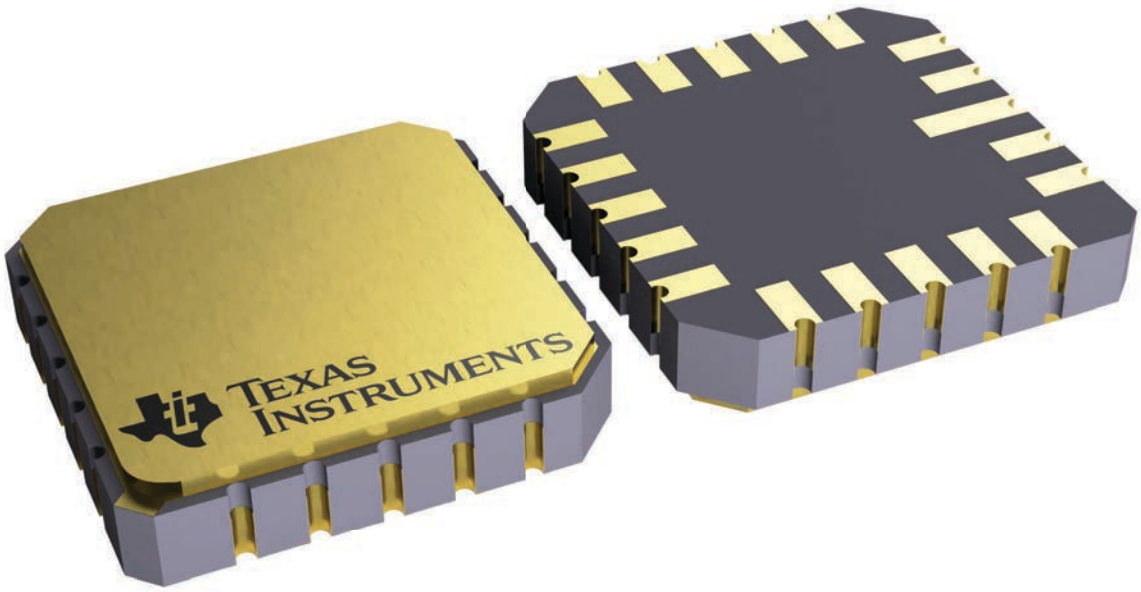
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

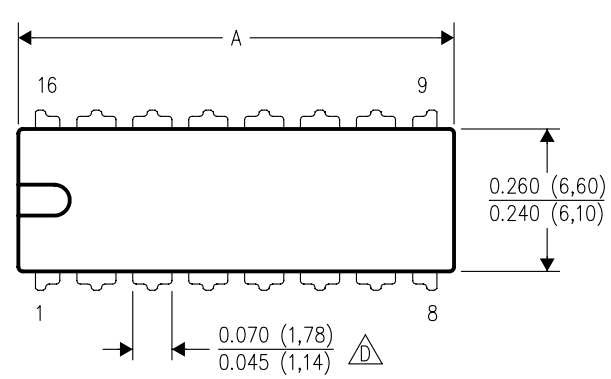


4229370VA\

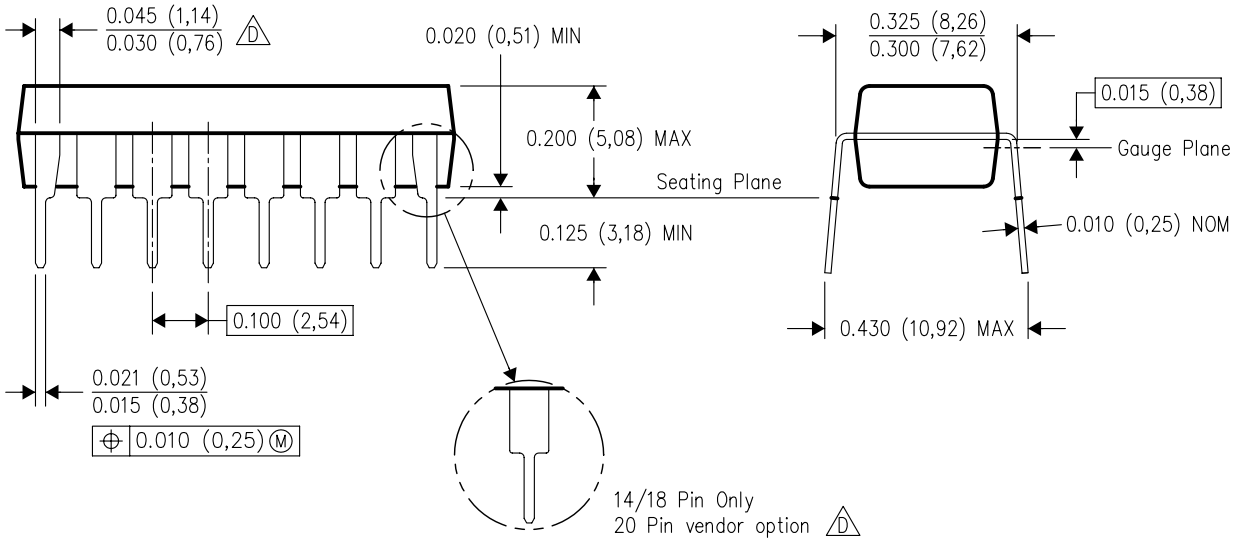
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

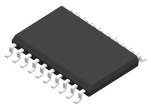


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

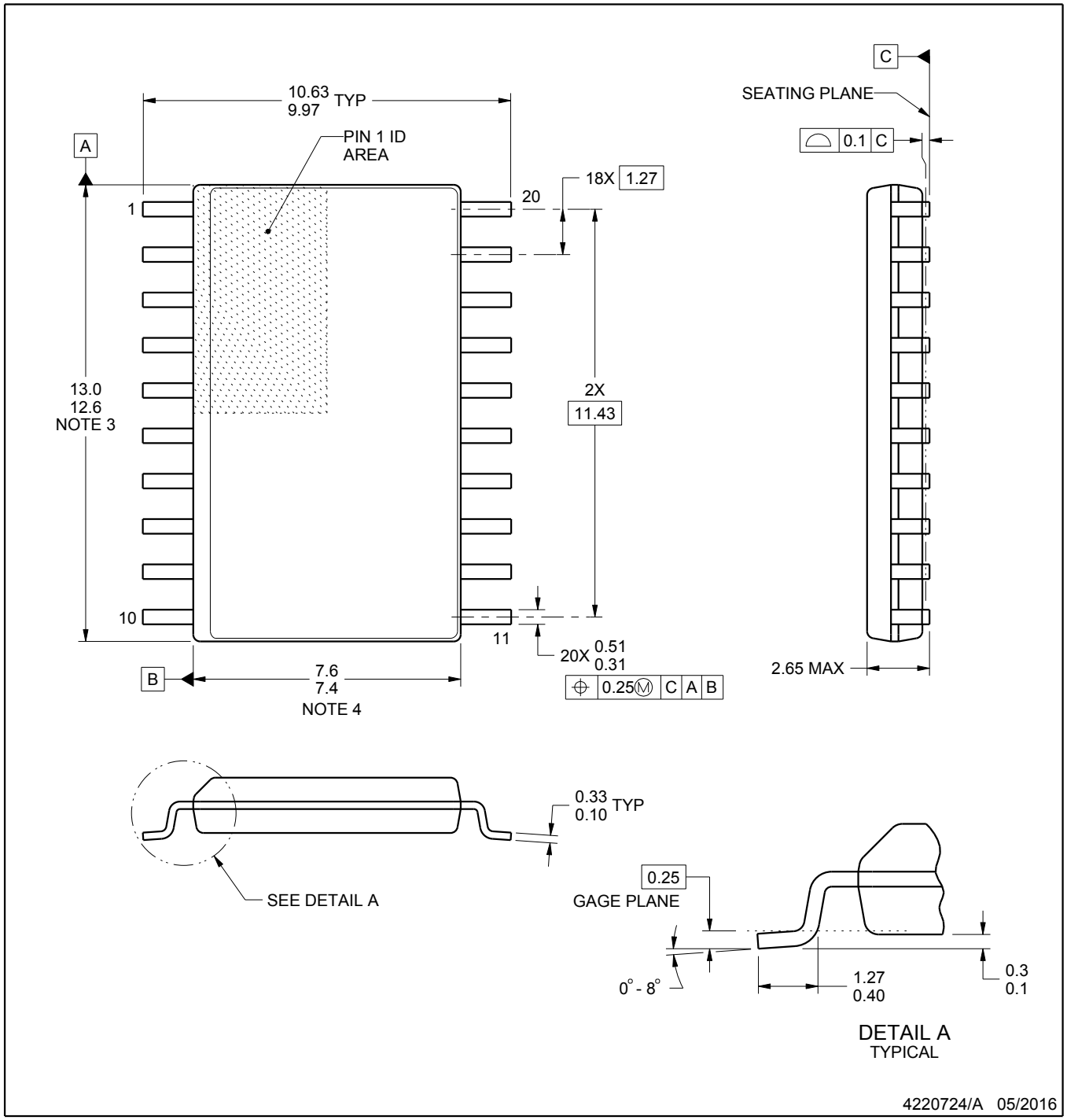


PACKAGE OUTLINE

DW0020A

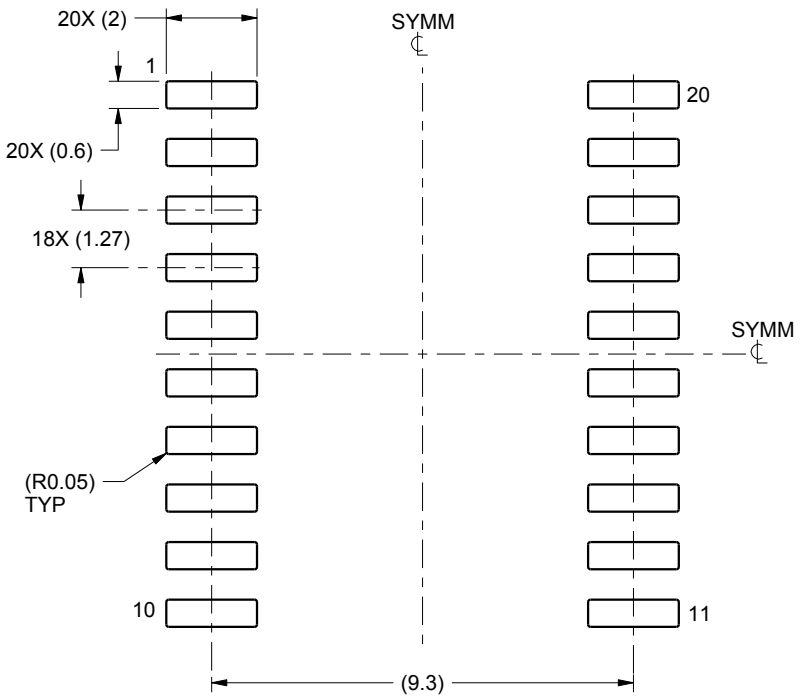
SOIC - 2.65 mm max height

SOIC

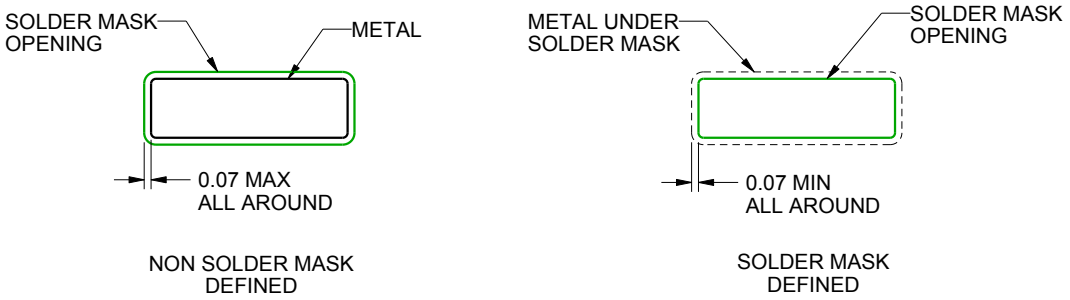


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

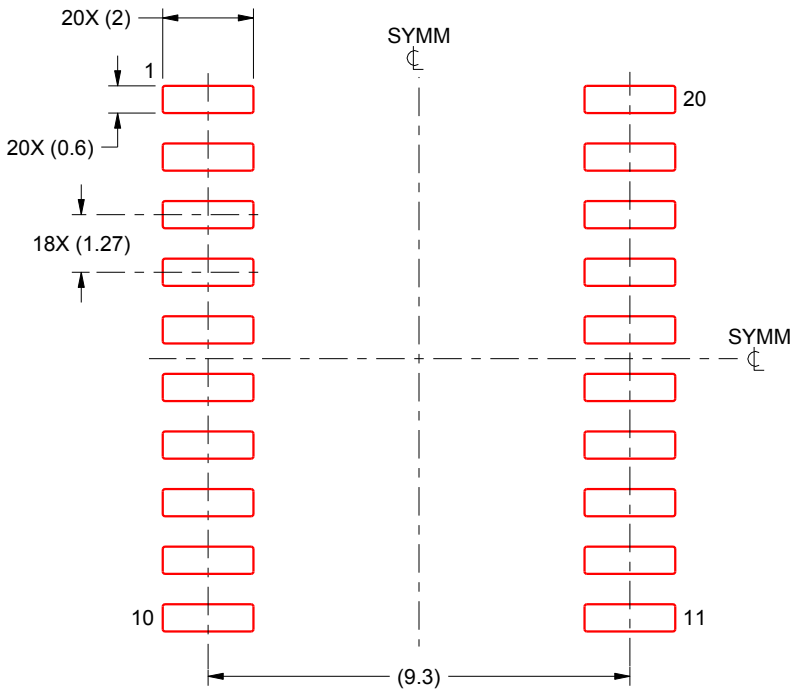


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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