ITE 聯陽半導體
ITE Tech. Inc.

IT9852E
IT9854E
IT9856TE
IT9866TE

HD Display and Smart Control SoC

Preliminary Specification V0.9.1

ITE TECH. INC.

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Revision History

Date	Revision	Page No.
2016/05/11	● Change naming of PWM from PWM0 … PWM5 to PWM1 … PWM6	21
2016/05/25	● Change signal name from SPI MOSI to SPI DOUT, SPI MISO to SPI DIN on Table 4-13 and Table 5-13	21, 46
2016/07/06	● Add IT9866TE	-
2016/08/11	● Update IT9852E/IT9854E package information	57
2016/09/12	● Update power sequence for memory power	55
2016/11/22	● Modify IVDD to 1.3 when the CPU run at 400MHz	53
2017/12/20	● Modify Table 7-1. Reset Timing Table	55
2018/01/11	● Update DC operation condition for VDD_CORE and VDD_MEM	53

CONTENTS

FIGURES

TABLES

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1. Features

- **Host Processor**
  - 400MHz 32-bit ARM9 CPU
  - 16KB instruction cache and 16KB data cache

- **Audio Processor**
  - 200MHz 32-bit RISC CPU with DSP extensions
  - 8KB instruction cache, 8KB data cache
  - Supports audio CODEC
    - MPEG 1/2/2.5 audio layer 1/2/3
    - WMA decoder
    - MPEG-2/4 AAC-LC decoder
    - FLAC decoder

- **Micro Controller**
  - 200MHz 32-bit RISC CPU
  - 16KB SRAM for instruction/data access

- **Display Interface**
  - 1280x800 16/18/24 bpp (RGB565/RGB666/RGB8888)
  - Resolution: Max. 4096*4096 true color mode
  - Supports 6/9/16/18/24 bits RGB I/F and 8/9/16/18/24 bits CPU I/F
  - Supports C-STN with frame buffer
  - HW 90°/180°/270° rotate and mirror
  - Supports TFT or TFD (with or without frame-buffer)
  - Supports three channel gamma correction
  - Supports hardware cursor
  - Supports CCIR601/CCIR656 interface
  - Supports digital TCON

- **2D Graphics Acceleration**
  - Bit Block Transfer (BitBlt) with ROP3 operation
  - Supports mask plan with 1bpp, 2bpp, 4bpp and 8bpp format.
  - Supports color expansion with 1bpp, 2bpp, 4bpp and 8bpp format
  - Coordinates transform
  - One clipping window

- **USB Host/Device**
  - Provides two host/device controller
  - Compliant with USB specification version 2.0
  - Compatible with EHCI 1.0
  - Supports point-to-point communications with one HS/FS/LS device
  - Both host and device support isochronous/interrupt/control/bulk transfers
  - Compatible with EHCI data structures

- **Memory Controller**
  - IT9852E supports 16MB 16-bit DDR2
  - 64MB 16-bit DDR2 supported by IT9854E/IT9856TE/IT9866TE
  - Supports Ping-Pong bank with tilling memory access

- **Ethernet MAC**
  - Compliant with full IEEE 802.3-2002 specifications
  - Supports IEEE 802.1Q VLAN tag detection for reception frames
  - Supports CSMA/CD Protocol for Half-Duplex operation
  - Supports IEEE 802.3x flow-control for Full-Duplex operation
  - Supports IEEE 1588-2002 Time stamping on the transmit and received frames
  - IEEE 802.3 compliant RMII PHY interface

- **JPEG Encoder/Decoder**
  - Fully compliant with Baseline JPEG standard ISO/IEC 10918
  - Supports up to 256 million pixel (16376 * 16376)
  - Supports 422, 420, 411, 400, 444 decode
  - Supports 422, 420 encode
  - Supports downloadable Quantization and Huffman table
  - Interleaved and non-interleave scan decode
  - Supports motion JPEG for 720p@30fps (1280x720)

- **Video Encoder/Decoder**
  - *H.264 Decoder
    - High/main profile, level 3.1
    - B Frame not supported
    - Real-time decode for 720p@30fps (1280x720)

- **Image Signal Processor**
  - Input data YUV format: 444, 420, 422
  - Output data RGB format: 888, 565, 444
  - Image and video scaling engine for scaling up and down
  - 2-tap vertical, 2-tap horizontal scaling filter
  - Configurable filter coefficients
  - Supports color correction matrix
  - Supports color conversion
  - Supports de-interlace filter
  - Supports 2 layer High color OSD
  - Supports dither for 4-, 5-, 6-bits RGB channel precision

■ **DMA**
- Provides 8 configurable DMA channels
- Supports chain transfer
- Memory-to-memory, memory-to-peripheral, and peripheral-to-peripheral transfer
- Group round-robin arbitration scheme with 4 priority levels
- Supports 8-, 16-, and 32-bit wide data transaction
- Supports big-endian and little-endian

■ **Power Management**
- Flexible clock divider to slow down clock
- Dynamic gating clock
- Separate clock source to disable unused peripherals
- Wakeup from external event

■ **GPIO**
- Independent input, output and output enable buses for bi-directional I/O pins
- Each port can separately trigger the GPIO interrupt when it is programmed as input pin.
- Each port interrupt generation can be triggered by rising edge, falling edge, both edges, or high/low level when the interrupt option is set.

■ **IIC**
- Provides two IIC interfaces
- Supports standard, and fast mode through programming the clock division register
- Supports 7-bit, 10-bit and general call addressing mode
- Glitch suppression throughout the de-bounce circuit
- Programmable slave address
- Master-transmit, Master-receive, Slave-transmit and Slave-receive modes provided
- Configurable multi-master mode supported
- Slave mode general call address detection

■ **UART/IrDA**
- Four UART interfaces
- Baud rate up to 6.25M bps
- Firmware compatible with high-speed NS 16C550A UART
- IrDA 1.3 SIR with up to 115.2kbps data rate
- SIR pulse width programmable as 1.6us or 3/16 of the baud-rate pulse width
- Supports IrDA 1.3 FIR
- Multi-frame transmission and reception in FIR mode

■ **Interrupt Controller**
- Provides both edge and level-triggered interrupt sources with positive and negative directions
- Provides de-bounce circuit for interrupt source

■ **PWM**
- Provides six independent 32-bit timers with PWM
- Programmable duty cycle and frequency
- Supports external clock source
- It can merge two timers into a 64-bit timer.
- Supports incrementing and decrementing mode

■ **SPI**
- Supports TI SSP, Motorola SPI, National Semiconductor Microwire, and SPIDIF interface
- Supports master and slave modes
- Internally or externally controlled serial bit clock
- Internally or externally controlled frame/sync
- Programmable frame/sync polarity
- Programmable serial bit clock polarity, phase, and frequency
- Programmable serial bit data sequence (MSB or LSB first)
- Programmable threshold interrupt of transmit/receive FIFO

■ **RTC**
- Separated second, minute, hour, and day counter
- Programmable auto second, minute, hour or day alarm
- Generates power on signal when alarm occurs

■ **Remote Controller**
- Hardware programmable to receive remote controller signal

■ **Wiegand Controller**
- Provides two Wiegand interfaces
- Supports up to maximum 128-bit code length
- Auto detects code length

■ **Watch Dog**
- During timeout, outputs are system reset or interrupt.
- 32-bit down counter
- A variable time-out period of reset

- **SD/MMC Controller**
  - Two MMC/SD interfaces
  - Fully compliant with MMCA v3.3
  - Compliant with low-voltage support and 4 bits data of MMCA v4.0
  - Compliant with SD/SDHC
  - FAT16/FAT32 boot loader

- **CCIR601/656**
  - CCIR601/656 input for video capture

- **TS Input/Output Interface**
  - Supports TS serial mode
  - 32 PID filters
  - Maximum bit rate up to 100 Mbits

- **Booting**
  - Configurable booting media select
  - SD/MMC/eMMC booting
  - SPI-NAND booting
  - NOR booting

- **Suitable Product**
  - Video intercom system
  - Access control and entrance system
  - White goods display and control
  - Sports equipment display and control
  - thermostat
  - Smart home controller
  - Display controller
  - **Finger recognition machine
  - **Face recognition machine
  -

Note:

1. IT9852E does not support H.264 decoder.
2. The biometrics application is for IT9866TE only.

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2. General Description

2.1 Introduction

The IT9850 series is high performance HD display and smart control SOC. (The IT9850 series include IT9852E, IT9854E, IT9856TE and IT9866TE package.) It equips 2D Graphics Accelerator allowing for some special user interface designing, JPEG/H.264 HD decoding engine allowing users to have smooth experience while watching images and clips, audio engines allowing users to have joyful feeling while watching images and surely some other useful interfaces allowing users to have a more flexible using experience to be with their platform.

2.2 Multimedia Processor

2.2.1 High Performance 2D Graphics Accelerator

This engine supports bitblt, blending, rotation and scale function.

2.2.2 Powerful H.264 and JPEG Engine

The engines in the IT9850 offer users the ability to play those clips by video stream. The H.264 decoder engine can perform up to 1280x720p@30fps size clip decoding. Except for H.264 decoders, IT9850 has JPEG engine inside. The JPEG engine can perform up to 256M-pixel still JPEG decoding and perform up to 1280x720p@30fps motion JPEG clip decoding.

There is a video scaling engine for scaling up or down to the target display size.

2.2.3 Powerful Audio Solution

IT9850 embeds a 32-bit RISC CPU and a DSP engine. It can support MPEG-1 and MPEG-2 layer 2 audio decoder, MP3 decoder, HE-AAC decoder and FLAC decoder. IT9850 provides IIS as well. You can choose adopt another high performance IIS interface DAC freely for your consideration between performance and cost aspect.

2.2.4 High performance USB2.0 I/F

IT9850 supports a USB2.0 Host and a USB2.0 Device I/Fs. Users can have high speed data transfer experience through the USB2.0 I/F.

2.2.5 Flexible SPI-NAND/NOR flash controller and flash card I/Fs

IT9850 has various external cards, I/F, SPI-NAND flash I/F and NOR flash I/F. About external cards I/F, IT9850 builds in SD/MMC card controllers. If users want some other external cards I/F, IT9850 provides a USB host I/F allowing for an external card bus chip.

IT9850 provides SPI-NAND and NOR flash I/F. Users can choose SLC or MLC NAND Flash for both booting code and multimedia contents storage space. Besides SPI-NAND, NOR and SD are the other solutions for users to choose as a booting code storage space.

2.2.6 Display Interface

IT9850 supports various LCD I/Fs, such as RGB I/F, CPU I/F and CCIR601 I/F. To have better LCD supporting flexibility, IT9850 builds in digital T-con. With digital T-cons, users can save extra cost. Based on all these I/Fs, IT9850 can support resolution up to 1280x800 on true color mode.

Having the flexible display I/F, It will be easier to pick up the kind of LCM required for users' platform.

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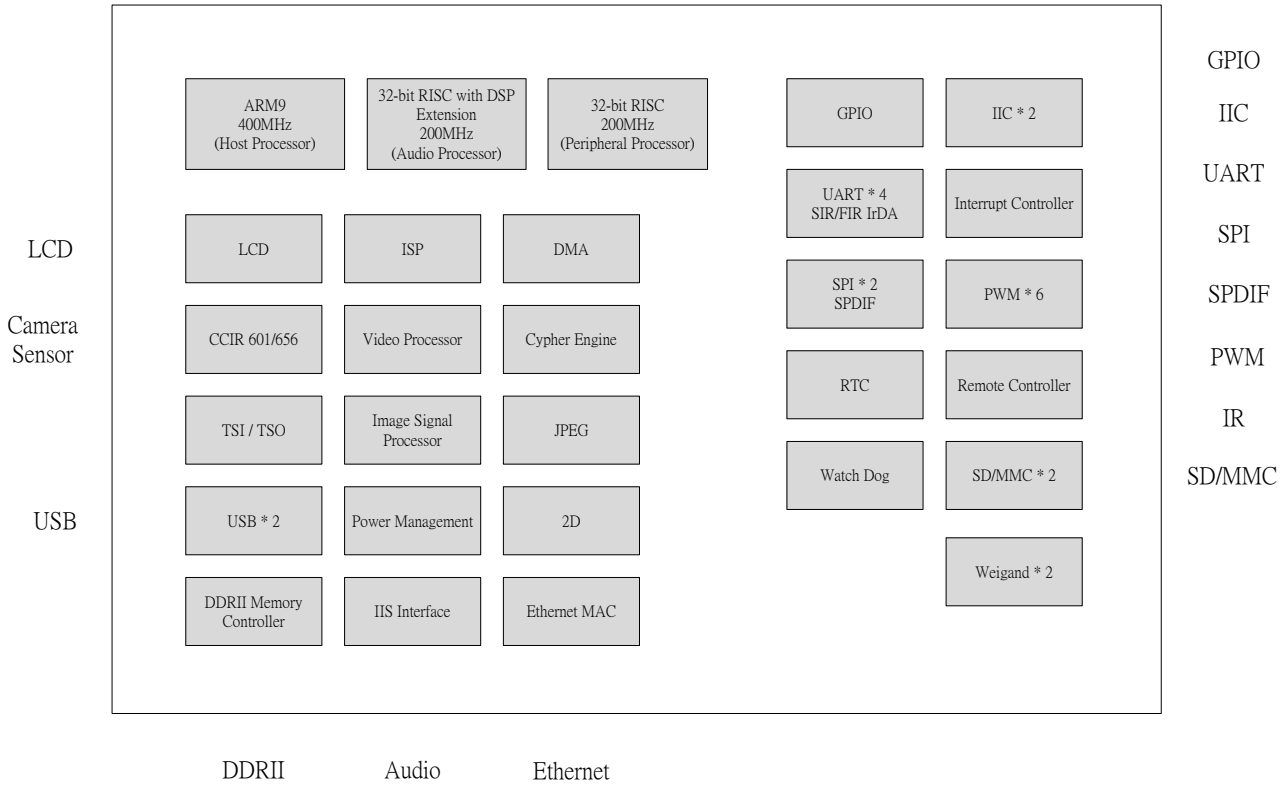
3. Block Diagram



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4. Pin Description

4.1 IT9852E/IT9854E Pin Location

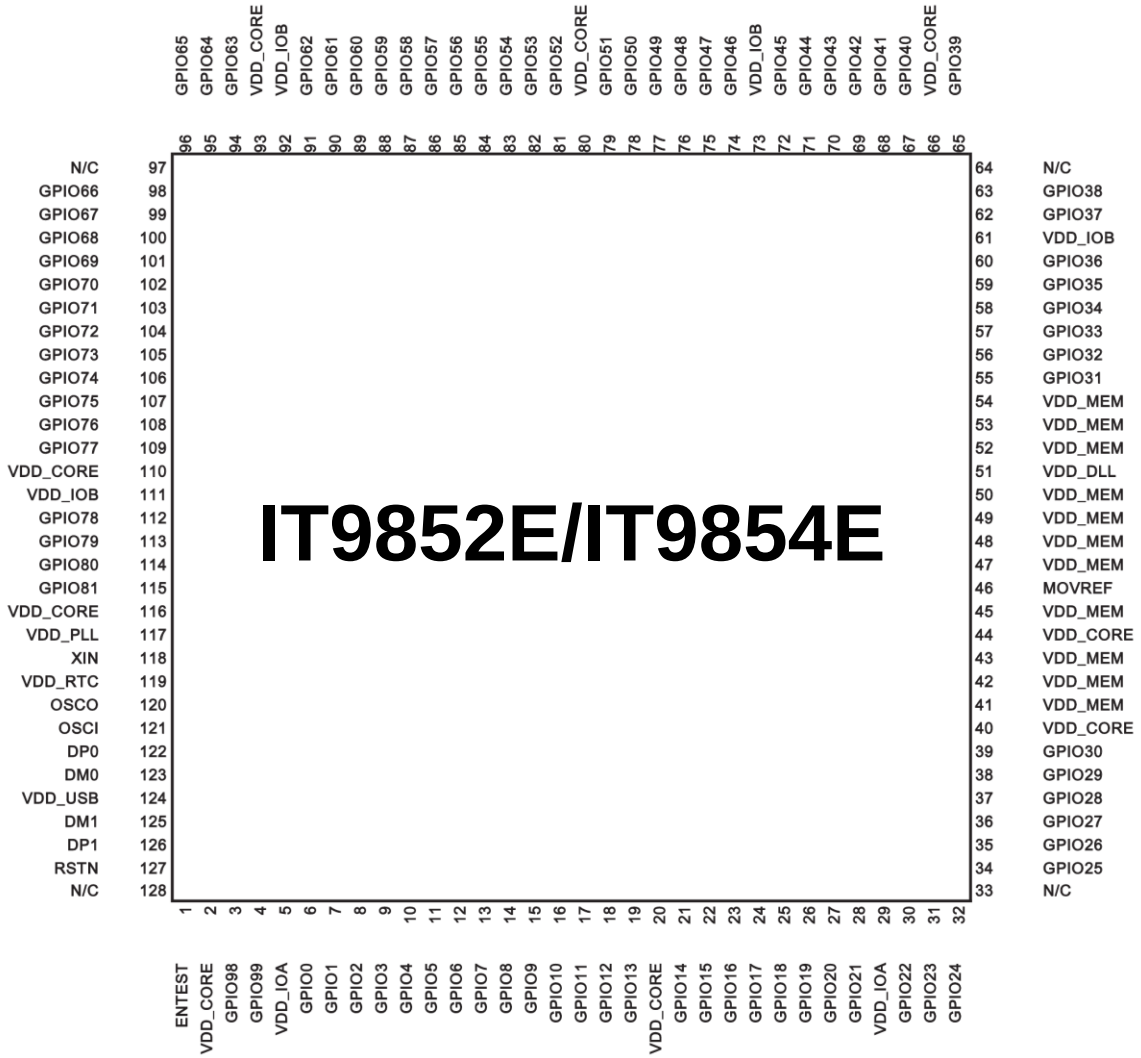

Table 4-1. IT9852E/IT9854E Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	ENTEST	33	NC	65	GPIO39	97	NC
2	VDD_CORE	34	GPIO25	66	VDD_CORE	98	GPIO66
3	GPIO98	35	GPIO26	67	GPIO40	99	GPIO67
4	GPIO99	36	GPIO27	68	GPIO41	100	GPIO68
5	VDD_IOA	37	GPIO28	69	GPIO42	101	GPIO69
6	GPIO0	38	GPIO29	70	GPIO43	102	GPIO70
7	GPIO1	39	GPIO30	71	GPIO44	103	GPIO71
8	GPIO2	40	VDD_CORE	72	GPIO45	104	GPIO72
9	GPIO3	41	VDD_MEM	73	VDD_IOB	105	GPIO73
10	GPIO4	42	VDD_MEM	74	GPIO46	106	GPIO74
11	GPIO5	43	VDD_MEM	75	GPIO47	107	GPIO75
12	GPIO6	44	VDD_CORE	76	GPIO48	108	GPIO76
13	GPIO7	45	VDD_MEM	77	GPIO49	109	GPIO77
14	GPIO8	46	MOVREF	78	GPIO50	110	VDD_CORE
15	GPIO9	47	VDD_MEM	79	GPIO51	111	VDD_IOB
16	GPIO10	48	VDD_MEM	80	VDD_CORE	112	GPIO78
17	GPIO11	49	VDD_MEM	81	GPIO52	113	GPIO79
18	GPIO12	50	VDD_MEM	82	GPIO53	114	GPIO80
19	GPIO13	51	VDD_DLL	83	GPIO54	115	GPIO81
20	VDD_CORE	52	VDD_MEM	84	GPIO55	116	VDD_CORE
21	GPIO14	53	VDD_MEM	85	GPIO56	117	VDD_PLL
22	GPIO15	54	VDD_MEM	86	GPIO57	118	XIN
23	GPIO16	55	GPIO31	87	GPIO58	119	VDD_RTC
24	GPIO17	56	GPIO32	88	GPIO59	120	OSCO
25	GPIO18	57	GPIO33	89	GPIO60	121	OSCI
26	GPIO19	58	GPIO34	90	GPIO61	122	DP0
27	GPIO20	59	GPIO35	91	GPIO62	123	DM0
28	GPIO21	60	GPIO36	92	VDD_IOB	124	VDD_USB
29	VDD_IOA	61	VDD_IOB	93	VDD_CORE	125	DM1
30	GPIO22	62	GPIO37	94	GPIO63	126	DP1
31	GPIO23	63	GPIO38	95	GPIO64	127	RSTN
32	GPIO24	64	NC	96	GPIO65	128	NC

Table 4-2. IT9852E/IT9854E Pins Listed in Alphabetical Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
DM0	123	GPIO27	36	GPIO59	88	RSTN	127
DM1	125	GPIO28	37	GPIO60	89	VDD_CORE	2
DP0	122	GPIO29	38	GPIO61	90	VDD_CORE	20
DP1	126	GPIO30	39	GPIO62	91	VDD_CORE	40
ENTEST	1	GPIO31	55	GPIO63	94	VDD_CORE	44
GPIO0	6	GPIO32	56	GPIO64	95	VDD_CORE	66
GPIO1	7	GPIO33	57	GPIO65	96	VDD_CORE	80
GPIO2	8	GPIO34	58	GPIO66	98	VDD_CORE	93
GPIO3	9	GPIO35	59	GPIO67	99	VDD_CORE	110
GPIO4	10	GPIO36	60	GPIO68	100	VDD_CORE	116
GPIO5	11	GPIO37	62	GPIO69	101	VDD_DLL	51
GPIO6	12	GPIO38	63	GPIO70	102	VDD_IOA	5
GPIO7	13	GPIO39	65	GPIO71	103	VDD_IOA	29
GPIO8	14	GPIO40	67	GPIO72	104	VDD_IOB	61
GPIO9	15	GPIO41	68	GPIO73	105	VDD_IOB	73
GPIO10	16	GPIO42	69	GPIO74	106	VDD_IOB	92
GPIO11	17	GPIO43	70	GPIO75	107	VDD_IOB	111
GPIO12	18	GPIO44	71	GPIO76	108	VDD_MEM	41
GPIO13	19	GPIO45	72	GPIO77	109	VDD_MEM	42
GPIO14	21	GPIO46	74	GPIO78	112	VDD_MEM	43
GPIO15	22	GPIO47	75	GPIO79	113	VDD_MEM	45
GPIO16	23	GPIO48	76	GPIO80	114	VDD_MEM	47
GPIO17	24	GPIO49	77	GPIO81	115	VDD_MEM	48
GPIO18	25	GPIO50	78	GPIO98	3	VDD_MEM	49
GPIO19	26	GPIO51	79	GPIO99	4	VDD_MEM	50
GPIO20	27	GPIO52	81	MOVREF	46	VDD_MEM	52
GPIO21	28	GPIO53	82	NC	33	VDD_MEM	53
GPIO22	30	GPIO54	83	NC	64	VDD_MEM	54
GPIO23	31	GPIO55	84	NC	97	VDD_PLL	117
GPIO24	32	GPIO56	85	NC	128	VDD_RTC	119
GPIO25	34	GPIO57	86	OSCI	121	VDD_USB	124
GPIO26	35	GPIO58	87	OSCO	120	XIN	118

4.2 IT9852E/IT9854E Pin Description

Table 4-3. Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
2, 20, 40, 44, 66, 80, 93, 110, 116	VDD_CORE	Power	-	Digital Core Supply 1.2V
51	VDD_DLL	Power	-	Memory DLL Supply 1.2V
5, 29	VDD_IOA	Power	-	I/O Supply 3.3V
61, 73, 92, 111	VDD_IOB	Power	-	I/O Supply 3.3V
41, 42, 43, 45, 47, 48, 49, 50, 52, 53, 54	VDD_MEM	Power	-	Memory Chip Supply 1.8V
117	VDD_PLL	Power	-	PLL Supply 1.2V
119	VDD_RTC	Power	-	RTC Supply 3.3V
124	VDD_USB	Power	-	USB Supply 3.3V

Table 4-4. Pin Description of USB Signals

Pin(s) No.	Symbol	Attribute	Power	Description
123	DM0	I/O	VDD_USB	USB data in data negative pin terminal
122	DP0	I/O	VDD_USB	USB data in data positive pin terminal
125	DM1	I/O	VDD_USB	USB data in data negative pin terminal
126	DP1	I/O	VDD_USB	USB data in data positive pin terminal

Table 4-5. Pin Description of GPIO Signals

Pin(s) No.	Symbol	Attribute	Power	Description
6	GPIO0	I/O	VDD_IOA	GPIO0
7	GPIO1	I/O	VDD_IOA	GPIO1
8	GPIO2	I/O	VDD_IOA	GPIO2
9	GPIO3	I/O	VDD_IOA	GPIO3
10	GPIO4	I/O	VDD_IOA	GPIO4
11	GPIO5	I/O	VDD_IOA	GPIO5
12	GPIO6	I/O	VDD_IOA	GPIO6
13	GPIO7	I/O	VDD_IOA	GPIO7
14	GPIO8	I/O	VDD_IOA	GPIO8
15	GPIO9	I/O	VDD_IOA	GPIO9
16	GPIO10	I/O	VDD_IOA	GPIO10
17	GPIO11	I/O	VDD_IOA	GPIO11
18	GPIO12	I/O	VDD_IOA	GPIO12
19	GPIO13	I/O	VDD_IOA	GPIO13
21	GPIO14	I/O	VDD_IOA	GPIO14
22	GPIO15	I/O	VDD_IOA	GPIO15
23	GPIO16	I/O	VDD_IOA	GPIO16
24	GPIO17	I/O	VDD_IOA	GPIO17
25	GPIO18	I/O	VDD_IOA	GPIO18
26	GPIO19	I/O	VDD_IOA	GPIO19
27	GPIO20	I/O	VDD_IOA	GPIO20
28	GPIO21	I/O	VDD_IOA	GPIO21
30	GPIO22	I/O	VDD_IOA	GPIO22
31	GPIO23	I/O	VDD_IOA	GPIO23
32	GPIO24	I/O	VDD_IOA	GPIO24
34	GPIO25	I/O	VDD_IOA	GPIO25
35	GPIO26	I/O	VDD_IOA	GPIO26
36	GPIO27	I/O	VDD_IOA	GPIO27
37	GPIO28	I/O	VDD_IOA	GPIO28
38	GPIO29	I/O	VDD_IOA	GPIO29
39	GPIO30	I/O	VDD_IOA	GPIO30

Pin(s) No.	Symbol	Attribute	Power	Description
55	GPIO31	I/O	VDD_IOB	GPIO31
56	GPIO32	I/O	VDD_IOB	GPIO32
57	GPIO33	I/O	VDD_IOB	GPIO33
58	GPIO34	I/O	VDD_IOB	GPIO34
59	GPIO35	I/O	VDD_IOB	GPIO35
60	GPIO36	I/O	VDD_IOB	GPIO36
62	GPIO37	I/O	VDD_IOB	GPIO37
63	GPIO38	I/O	VDD_IOB	GPIO38
65	GPIO39	I/O	VDD_IOB	GPIO39
67	GPIO40	I/O	VDD_IOB	GPIO40
68	GPIO41	I/O	VDD_IOB	GPIO41
69	GPIO42	I/O	VDD_IOB	GPIO42
70	GPIO43	I/O	VDD_IOB	GPIO43
71	GPIO44	I/O	VDD_IOB	GPIO44
72	GPIO45	I/O	VDD_IOB	GPIO45
74	GPIO46	I/O	VDD_IOB	GPIO46 (BOOT_CFG0)
75	GPIO47	I/O	VDD_IOB	GPIO47 (BOOT_CFG1)
76	GPIO48	I/O	VDD_IOB	GPIO48 (HOST_CFG0)
77	GPIO49	I/O	VDD_IOB	GPIO49 (HOST_CFG1)
78	GPIO50	I/O	VDD_IOB	GPIO50 (PLL_CFG)
79	GPIO51	I/O	VDD_IOB	GPIO51 (DCXO_CFG)
81	GPIO52	I/O	VDD_IOB	GPIO52
82	GPIO53	I/O	VDD_IOB	GPIO53
83	GPIO54	I/O	VDD_IOB	GPIO54
84	GPIO55	I/O	VDD_IOB	GPIO55
85	GPIO56	I/O	VDD_IOB	GPIO56
86	GPIO57	I/O	VDD_IOB	GPIO57
87	GPIO58	I/O	VDD_IOB	GPIO58
88	GPIO59	I/O	VDD_IOB	GPIO59
89	GPIO60	I/O	VDD_IOB	GPIO60
90	GPIO61	I/O	VDD_IOB	GPIO61
91	GPIO62	I/O	VDD_IOB	GPIO62
94	GPIO63	I/O	VDD_IOB	GPIO63
95	GPIO64	I/O	VDD_IOB	GPIO64
96	GPIO65	I/O	VDD_IOB	GPIO65
98	GPIO66	I/O	VDD_IOB	GPIO66
99	GPIO67	I/O	VDD_IOB	GPIO67
100	GPIO68	I/O	VDD_IOB	GPIO68
101	GPIO69	I/O	VDD_IOB	GPIO69
102	GPIO70	I/O	VDD_IOB	GPIO70
103	GPIO71	I/O	VDD_IOB	GPIO71
104	GPIO72	I/O	VDD_IOB	GPIO72
105	GPIO73	I/O	VDD_IOB	GPIO73
106	GPIO74	I/O	VDD_IOB	GPIO74
107	GPIO75	I/O	VDD_IOB	GPIO75
108	GPIO76	I/O	VDD_IOB	GPIO76
109	GPIO77	I/O	VDD_IOB	GPIO77
112	GPIO78	I/O	VDD_IOB	GPIO78
113	GPIO79	I/O	VDD_IOB	GPIO79
114	GPIO80	I/O	VDD_IOB	GPIO80
115	GPIO81	I/O	VDD_IOB	GPIO81
3	GPIO98	I/O	VDD_IOA	GPIO98
4	GPIO99	I/O	VDD_IOA	GPIO99

Table 4-6. Pin Description of Misc Signals

Pin(s) No.	Symbol	Attribute	Power	Description
1	ENTEST	I	VDD_IOA	Test Enable
46	MOVREF	I	VDD_MEM	Memory OVREF
118	XIN	I	VDD_RTC	Crystal 12MHz Input

Pin(s) No.	Symbol	Attribute	Power	Description
120	OSCO	O	VDD_PLL	RTC Crystal 32.768KHz Output
121	OSCI	I	VDD_PLL	RTC Crystal 32.768KHz Input
127	RSTN	I	VDD_IOA	Reset

4.3 IT9856TE/IT9866TE Pin Location

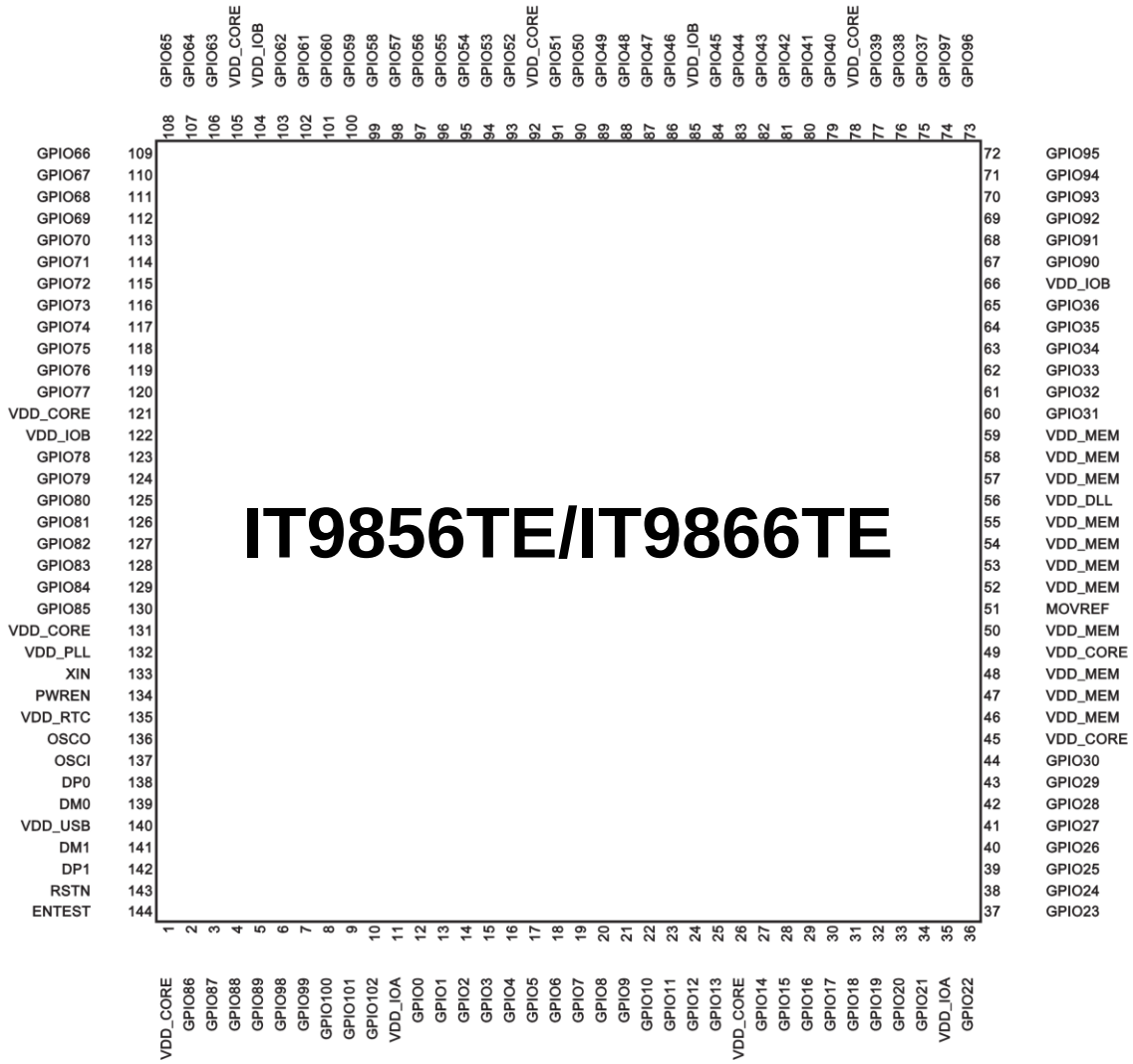

Table 4-7. IT9856TE/IT9866TE Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VDD_CORE	37	GPIO23	73	GPIO96	109	GPIO66
2	GPIO86	38	GPIO24	74	GPIO97	110	GPIO67
3	GPIO87	39	GPIO25	75	GPIO37	111	GPIO68
4	GPIO88	40	GPIO26	76	GPIO38	112	GPIO69
5	GPIO89	41	GPIO27	77	GPIO39	113	GPIO70
6	GPIO98	42	GPIO28	78	VDD_CORE	114	GPIO71
7	GPIO99	43	GPIO29	79	GPIO40	115	GPIO72
8	GPIO100	44	GPIO30	80	GPIO41	116	GPIO73
9	GPIO101	45	VDD_CORE	81	GPIO42	117	GPIO74
10	GPIO102	46	VDD_MEM	82	GPIO43	118	GPIO75
11	VDD_IOA	47	VDD_MEM	83	GPIO44	119	GPIO76
12	GPIO0	48	VDD_MEM	84	GPIO45	120	GPIO77
13	GPIO1	49	VDD_CORE	85	VDD_IOB	121	VDD_CORE
14	GPIO2	50	VDD_MEM	86	GPIO46	122	VDD_IOB
15	GPIO3	51	MOVREF	87	GPIO47	123	GPIO78
16	GPIO4	52	VDD_MEM	88	GPIO48	124	GPIO79
17	GPIO5	53	VDD_MEM	89	GPIO49	125	GPIO80
18	GPIO6	54	VDD_MEM	90	GPIO50	126	GPIO81
19	GPIO7	55	VDD_MEM	91	GPIO51	127	GPIO82
20	GPIO8	56	VDD_DLL	92	VDD_CORE	128	GPIO83
21	GPIO9	57	VDD_MEM	93	GPIO52	129	GPIO84
22	GPIO10	58	VDD_MEM	94	GPIO53	130	GPIO85
23	GPIO11	59	VDD_MEM	95	GPIO54	131	VDD_CORE
24	GPIO12	60	GPIO31	96	GPIO55	132	VDD_PLL
25	GPIO13	61	GPIO32	97	GPIO56	133	XIN
26	VDD_CORE	62	GPIO33	98	GPIO57	134	PWREN
27	GPIO14	63	GPIO34	99	GPIO58	135	VDD_RTC
28	GPIO15	64	GPIO35	100	GPIO59	136	OSCO
29	GPIO16	65	GPIO36	101	GPIO60	137	OSCI
30	GPIO17	66	VDD_IOB	102	GPIO61	138	DP0
31	GPIO18	67	GPIO90	103	GPIO62	139	DM0
32	GPIO19	68	GPIO91	104	VDD_IOB	140	VDD_USB
33	GPIO20	69	GPIO92	105	VDD_CORE	141	DM1
34	GPIO21	70	GPIO93	106	GPIO63	142	DP1
35	VDD_IOA	71	GPIO94	107	GPIO64	143	RSTN
36	GPIO22	72	GPIO95	108	GPIO65	144	ENTEST

Table 4-8. IT9856TE/IT9866TE Pins Listed in Alphabetical Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
DM0	139	GPIO31	60	GPIO67	110	MOVREF	51
DM1	141	GPIO32	61	GPIO68	111	OSCI	137
DP0	138	GPIO33	62	GPIO69	112	OSCO	136
DP1	142	GPIO34	63	GPIO70	113	PWREN	134
ENTEST	144	GPIO35	64	GPIO71	114	RSTN	143
GPIO0	12	GPIO36	65	GPIO72	115	VDD_CORE	1
GPIO1	13	GPIO37	75	GPIO73	116	VDD_CORE	26
GPIO2	14	GPIO38	76	GPIO74	117	VDD_CORE	45
GPIO3	15	GPIO39	77	GPIO75	118	VDD_CORE	49
GPIO4	16	GPIO40	79	GPIO76	119	VDD_CORE	78
GPIO5	17	GPIO41	80	GPIO77	120	VDD_CORE	92
GPIO6	18	GPIO42	81	GPIO78	123	VDD_CORE	105
GPIO7	19	GPIO43	82	GPIO79	124	VDD_CORE	121
GPIO8	20	GPIO44	83	GPIO80	125	VDD_CORE	131
GPIO9	21	GPIO45	84	GPIO81	126	VDD_DLL	56
GPIO10	22	GPIO46	86	GPIO82	127	VDD_IOA	11
GPIO11	23	GPIO47	87	GPIO83	128	VDD_IOA	35
GPIO12	24	GPIO48	88	GPIO84	129	VDD_IOB	66
GPIO13	25	GPIO49	89	GPIO85	130	VDD_IOB	85
GPIO14	27	GPIO50	90	GPIO86	2	VDD_IOB	104
GPIO15	28	GPIO51	91	GPIO87	3	VDD_IOB	122
GPIO16	29	GPIO52	93	GPIO88	4	VDD_MEM	46
GPIO17	30	GPIO53	94	GPIO89	5	VDD_MEM	47
GPIO18	31	GPIO54	95	GPIO90	67	VDD_MEM	48
GPIO19	32	GPIO55	96	GPIO91	68	VDD_MEM	50
GPIO20	33	GPIO56	97	GPIO92	69	VDD_MEM	52
GPIO21	34	GPIO57	98	GPIO93	70	VDD_MEM	53
GPIO22	36	GPIO58	99	GPIO94	71	VDD_MEM	54
GPIO23	37	GPIO59	100	GPIO95	72	VDD_MEM	55
GPIO24	38	GPIO60	101	GPIO96	73	VDD_MEM	57
GPIO25	39	GPIO61	102	GPIO97	74	VDD_MEM	58
GPIO26	40	GPIO62	103	GPIO98	6	VDD_MEM	59
GPIO27	41	GPIO63	106	GPIO99	7	VDD_PLL	132
GPIO28	42	GPIO64	107	GPIO100	8	VDD_RTC	135
GPIO29	43	GPIO65	108	GPIO101	9	VDD_USB	140
GPIO30	44	GPIO66	109	GPIO102	10	XIN	133

4.4 IT9856TE/IT9866TE Pin Description

Table 4-9. Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
1, 26, 45, 49, 78, 92, 105, 121, 131	VDD_CORE	Power	-	Digital Core Supply 1.2V
56	VDD_DLL	Power	-	Memory DLL Supply 1.2V
11, 35	VDD_IOA	Power	-	I/O Supply 3.3V
66, 85, 104, 122	VDD_IOB	Power	-	I/O Supply 3.3V
46, 47, 48, 50, 52, 53, 54, 55, 57, 58, 59	VDD_MEM	Power	-	Memory Chip Supply 1.8V
132	VDD_PLL	Power	-	PLL Supply 1.2V
135	VDD_RTC	Power	-	RTC Supply 3.3V
140	VDD_USB	Power	-	USB Supply 3.3V

Table 4-10. Pin Description of USB Signals

Pin(s) No.	Symbol	Attribute	Power	Description
139	DM0	Analog	VDD_USB	USB data in data negative pin terminal
138	DP0	Analog	VDD_USB	USB data in data positive pin terminal
141	DM1	Analog	VDD_USB	USB data in data negative pin terminal
142	DP1	Analog	VDD_USB	USB data in data positive pin terminal

Table 4-11. Pin Description of GPIO Signals

Pin(s) No.	Symbol	Attribute	Power	Description
12	GPIO0	I/O	VDD_IOA	GPIO0
13	GPIO1	I/O	VDD_IOA	GPIO1
14	GPIO2	I/O	VDD_IOA	GPIO2
15	GPIO3	I/O	VDD_IOA	GPIO3
16	GPIO4	I/O	VDD_IOA	GPIO4
17	GPIO5	I/O	VDD_IOA	GPIO5
18	GPIO6	I/O	VDD_IOA	GPIO6
19	GPIO7	I/O	VDD_IOA	GPIO7
20	GPIO8	I/O	VDD_IOA	GPIO8
21	GPIO9	I/O	VDD_IOA	GPIO9
22	GPIO10	I/O	VDD_IOA	GPIO10
23	GPIO11	I/O	VDD_IOA	GPIO11
24	GPIO12	I/O	VDD_IOA	GPIO12
25	GPIO13	I/O	VDD_IOA	GPIO13
27	GPIO14	I/O	VDD_IOA	GPIO14
28	GPIO15	I/O	VDD_IOA	GPIO15
29	GPIO16	I/O	VDD_IOA	GPIO16
30	GPIO17	I/O	VDD_IOA	GPIO17
31	GPIO18	I/O	VDD_IOA	GPIO18
32	GPIO19	I/O	VDD_IOA	GPIO19
33	GPIO20	I/O	VDD_IOA	GPIO20
34	GPIO21	I/O	VDD_IOA	GPIO21
36	GPIO22	I/O	VDD_IOA	GPIO22
37	GPIO23	I/O	VDD_IOA	GPIO23
38	GPIO24	I/O	VDD_IOA	GPIO24
39	GPIO25	I/O	VDD_IOA	GPIO25
40	GPIO26	I/O	VDD_IOA	GPIO26
41	GPIO27	I/O	VDD_IOA	GPIO27
42	GPIO28	I/O	VDD_IOA	GPIO28
43	GPIO29	I/O	VDD_IOA	GPIO29
44	GPIO30	I/O	VDD_IOA	GPIO30
60	GPIO31	I/O	VDD_IOB	GPIO31

Pin(s) No.	Symbol	Attribute	Power	Description
61	GPIO32	I/O	VDD_IOB	GPIO32
62	GPIO33	I/O	VDD_IOB	GPIO33
63	GPIO34	I/O	VDD_IOB	GPIO34
64	GPIO35	I/O	VDD_IOB	GPIO35
65	GPIO36	I/O	VDD_IOB	GPIO36
75	GPIO37	I/O	VDD_IOB	GPIO37
76	GPIO38	I/O	VDD_IOB	GPIO38
77	GPIO39	I/O	VDD_IOB	GPIO39
79	GPIO40	I/O	VDD_IOB	GPIO40
80	GPIO41	I/O	VDD_IOB	GPIO41
81	GPIO42	I/O	VDD_IOB	GPIO42
82	GPIO43	I/O	VDD_IOB	GPIO43
83	GPIO44	I/O	VDD_IOB	GPIO44
84	GPIO45	I/O	VDD_IOB	GPIO45
86	GPIO46	I/O	VDD_IOB	GPIO46 (BOOT_CFG0)
87	GPIO47	I/O	VDD_IOB	GPIO47 (BOOT_CFG1)
88	GPIO48	I/O	VDD_IOB	GPIO48 (HOST_CFG0)
89	GPIO49	I/O	VDD_IOB	GPIO49 (HOST_CFG1)
90	GPIO50	I/O	VDD_IOB	GPIO50 (PLL_CFG)
91	GPIO51	I/O	VDD_IOB	GPIO51 (DCXO_CFG)
93	GPIO52	I/O	VDD_IOB	GPIO52
94	GPIO53	I/O	VDD_IOB	GPIO53
95	GPIO54	I/O	VDD_IOB	GPIO54
96	GPIO55	I/O	VDD_IOB	GPIO55
97	GPIO56	I/O	VDD_IOB	GPIO56
98	GPIO57	I/O	VDD_IOB	GPIO57
99	GPIO58	I/O	VDD_IOB	GPIO58
100	GPIO59	I/O	VDD_IOB	GPIO59
101	GPIO60	I/O	VDD_IOB	GPIO60
102	GPIO61	I/O	VDD_IOB	GPIO61
103	GPIO62	I/O	VDD_IOB	GPIO62
106	GPIO63	I/O	VDD_IOB	GPIO63
107	GPIO64	I/O	VDD_IOB	GPIO64
108	GPIO65	I/O	VDD_IOB	GPIO65
109	GPIO66	I/O	VDD_IOB	GPIO66
110	GPIO67	I/O	VDD_IOB	GPIO67
111	GPIO68	I/O	VDD_IOB	GPIO68
112	GPIO69	I/O	VDD_IOB	GPIO69
113	GPIO70	I/O	VDD_IOB	GPIO70
114	GPIO71	I/O	VDD_IOB	GPIO71
115	GPIO72	I/O	VDD_IOB	GPIO72
116	GPIO73	I/O	VDD_IOB	GPIO73
117	GPIO74	I/O	VDD_IOB	GPIO74
118	GPIO75	I/O	VDD_IOB	GPIO75
119	GPIO76	I/O	VDD_IOB	GPIO76
120	GPIO77	I/O	VDD_IOB	GPIO77
123	GPIO78	I/O	VDD_IOB	GPIO78
124	GPIO79	I/O	VDD_IOB	GPIO79
125	GPIO80	I/O	VDD_IOB	GPIO80
126	GPIO81	I/O	VDD_IOB	GPIO81
127	GPIO82	I/O	VDD_IOB	GPIO82
128	GPIO83	I/O	VDD_IOB	GPIO83
129	GPIO84	I/O	VDD_IOB	GPIO84
130	GPIO85	I/O	VDD_IOB	GPIO85
2	GPIO86	I/O	VDD_IOA	GPIO86
3	GPIO87	I/O	VDD_IOA	GPIO87
4	GPIO88	I/O	VDD_IOA	GPIO88
5	GPIO89	I/O	VDD_IOA	GPIO89
67	GPIO90	I/O	VDD_IOB	GPIO90

Pin(s) No.	Symbol	Attribute	Power	Description
68	GPIO91	I/O	VDD_IOB	GPIO91
69	GPIO92	I/O	VDD_IOB	GPIO92
70	GPIO93	I/O	VDD_IOB	GPIO93
71	GPIO94	I/O	VDD_IOB	GPIO94
72	GPIO95	I/O	VDD_IOB	GPIO95
73	GPIO96	I/O	VDD_IOB	GPIO96
74	GPIO97	I/O	VDD_IOB	GPIO97
6	GPIO98	I/O	VDD_IOA	GPIO98
7	GPIO99	I/O	VDD_IOA	GPIO99
8	GPIO100	I/O	VDD_IOA	GPIO100
9	GPIO101	I/O	VDD_IOA	GPIO101
10	GPIO102	I/O	VDD_IOA	GPIO102

Table 4-12. Pin Description of Misc Signals

Pin(s) No.	Symbol	Attribute	Power	Description
144	ENTEST	I	VDD_IOA	Test Enable
51	MOVREF	I	VDD_MEM	Memory OVREF
133	XIN	I	VDD_RTC	Crystal 12MHz Input
136	OSCO	O	VDD_PLL	RTC Crystal 32.768KHz Output
137	OSCI	I	VDD_PLL	RTC Crystal 32.768KHz Input
143	RSTN	I	VDD_IOA	Reset

4.5 GPIO Pin Share

Table 4-13. GPIO Pin Share Table

Pin Name	Mode 0	Mode 1	Mode 2	Mode 3
GPIO0	GPIO0	UART0 DCD	IIC_0 SDA	PWM5
GPIO1	GPIO1	UART0 RTS	IIC_0 SCL	PWM6
GPIO2	GPIO2	IrDA_RXL	IIC_1 SDA	IIC_0 SDA
GPIO3	GPIO3	IrDA_TX	IIC_1 SCL	IIC_0 SCL
GPIO4	GPIO4	UART0 RI	Remote IR Out	PWM1
GPIO5	GPIO5	Remote IR Out	IIS ZDO	PWM2
GPIO6	GPIO6	UART0 CTS / RXH	IIS ZDI	PWM3
GPIO7	GPIO7	Remote IR Out	IIS AMCLK	PWM4
GPIO8	GPIO8	Remote IR Out	PWM5	SDCLK2
GPIO9	GPIO9	Remote IR Out	IIS ZWS	UART1 CTS
GPIO10	GPIO10	SPI0 CS# 2	IIS ZCLK	UART1 RTS
GPIO11	GPIO11	SPI1 CS# 2	IIS AMCLK	IIC_0 SDA
GPIO12	GPIO12	UART0 DSR	IIS ZDI	IIC_0 SCL
GPIO13	GPIO13	UART0 DTR	IIS ZDO	SDCLK2
GPIO14	GPIO14	PWM2	-	SPI0 CS# 1
GPIO15	GPIO15	PWM1	SPI0 CS# 3	SPI1 CS# 1
GPIO16	GPIO16	SDCLK1	SPI1 CS# 3	SPDIF OUT
GPIO17	GPIO17	SDCMD	-	PWM3
GPIO18	GPIO18	SD0	-	SPI0 DIN
GPIO19	GPIO19	SD1	-	SPI0 DOUT
GPIO20	GPIO20	SD2	-	SPI0 CLK
GPIO21	GPIO21	SD3	-	PWM6
GPIO22	GPIO22	SD4	-	PWM1
GPIO23	GPIO23	SD5	-	IIC_0 SDA
GPIO24	GPIO24	SD6	-	IIC_0 SCL
GPIO25	GPIO25	SD7	-	IIC_1 SDA
GPIO26	GPIO26	PWM2	-	IIC_1 SCL
GPIO27	GPIO27	PWM3	-	REFCLK
GPIO28	GPIO28	Remote IR Out	-	TXEN
GPIO29	GPIO29	SPI1 DIN	-	TXD1
GPIO30	GPIO30	SPI1 DOUT	-	TXD0
GPIO31	GPIO31	SPI1 CLK	-	RXD1
GPIO32	GPIO32	IIS AMCLK	-	RXD0
GPIO33	GPIO33	IIS ZWS	-	RX_CRS_DV
GPIO34	GPIO34	IIS ZDO	-	MDIO
GPIO35	GPIO35	IIS ZCLK	-	MDC
GPIO36	GPIO36	IIS ZDI	Remote IR In	RX_ER
GPIO37	GPIO37	LSCK	SPI0 CS# 4	REF_25MHZ
GPIO38	GPIO38	LSA0	SPI1 CS# 4	REF_25MHZ
GPIO39	GPIO39	LD23	PWM1	TXEN
GPIO40	GPIO40	LD22	PWM2	TXD1
GPIO41	GPIO41	LD21	PWM3	TXD0
GPIO42	GPIO42	LD20	PWM4	REFCLK
GPIO43	GPIO43	LD19	PWM5	RXD1
GPIO44	GPIO44	LD18	PWM6	RXD0
GPIO45	GPIO45	LD17	-	RX_CRS_DV
GPIO46	GPIO46	LD16	-	PWM1
GPIO47	GPIO47	LD15	-	PWM2
GPIO48	GPIO48	LD14	-	PWM3
GPIO49	GPIO49	LD13	-	PWM4
GPIO50	GPIO50	LD12	-	PWM5
GPIO51	GPIO51	LD11	-	PWM6
GPIO52	GPIO52	LD10	-	-
GPIO53	GPIO53	LD9	-	-
GPIO54	GPIO54	LD8	-	-
GPIO55	GPIO55	LD7	-	-
GPIO56	GPIO56	LD6	-	-
GPIO57	GPIO57	LD5	-	-

Pin Name	Mode 0	Mode 1	Mode 2	Mode 3
GPIO58	GPIO58	LD4	-	TSOCLK
GPIO59	GPIO59	LD3	-	TSOCSN
GPIO60	GPIO60	LD2	-	TSOSTR
GPIO61	GPIO61	LD1	-	TSODATA0
GPIO62	GPIO62	LD0	-	TSODATA1
GPIO63	GPIO63	LSDA	PWM6	TSODATA2
GPIO64	GPIO64	LCSN	PWM5	TSODATA3
GPIO65	GPIO65	LDEN	PWM4	TSODATA4
GPIO66	GPIO66	LDCLK	PWM3	TSODATA5
GPIO67	GPIO67	LHSYNC	PWM2	TSODATA6
GPIO68	GPIO68	LVSYNC	PWM1	TSODATA7
GPIO69	GPIO69	CAP_MCLK	IIC_0 SDA	IIC_1 SDA
GPIO70	GPIO70	CAP_DE	IIC_0 SCL	IIC_1 SCL
GPIO71	GPIO71	CAP_PCLK	-	TSICLK
GPIO72	GPIO72	CAP_HSYNC	-	TSICSN
GPIO73	GPIO73	CAP_VSYNC	-	TSISTR
GPIO74	GPIO74	CAP_D0	-	TSIDATA0
GPIO75	GPIO75	CAP_D1	-	TSIDATA1
GPIO76	GPIO76	CAP_D2	PWM6	TSIDATA2
GPIO77	GPIO77	CAP_D3	PWM5	TSIDATA3
GPIO78	GPIO78	CAP_D4	PWM4	TSIDATA4
GPIO79	GPIO79	CAP_D5	PWM3	TSIDATA5
GPIO80	GPIO80	CAP_D6	PWM2	TSIDATA6
GPIO81	GPIO81	CAP_D7	PWM1	TSIDATA7
GPIO82	GPIO82	SPI0 CLK	SPI1 CLK	PWM1
GPIO83	GPIO83	SPI0 DIN	SPI1 DIN	PWM2
GPIO84	GPIO84	SPI0 DOUT	SPI1 DOUT	PWM3
GPIO85	GPIO85	SPI0 CS# 5	SPI1 CS# 5	PWM4
GPIO86	GPIO86	IIC_0 SDA	IIC_1 SDA	PWM5
GPIO87	GPIO87	IIC_0 SCL	IIC_1 SCL	PWM6
GPIO88	GPIO88	IIC_0 SDA	IIC_1 SDA	-
GPIO89	GPIO89	IIC_0 SCL	IIC_1 SCL	-
GPIO90	GPIO90	-	-	TXEN
GPIO91	GPIO91	-	-	TXD1
GPIO92	GPIO92	-	-	TXD0
GPIO93	GPIO93	-	-	REFCLK
GPIO94	GPIO94	-	-	RXD1
GPIO95	GPIO95	-	-	RXD0
GPIO96	GPIO96	PWM2	-	RX_CRS_DV
GPIO97	GPIO97	-	-	-
GPIO98	GPIO98	IIC_0 SDA	IIC_1 SDA	-
GPIO99	GPIO99	IIC_0 SCL	IIC_1 SCL	-
GPIO100	GPIO100	IIC_0 SDA	IIC_1 SDA	-
GPIO101	GPIO101	IIC_0 SCL	IIC_1 SCL	-
GPIO102	GPIO102	-	-	-

Note: UART0_RX, UART0_TX, UART1_RX, UART1_TX, UART2_RX, UART2_TX, UART3_RX, UART3_TX, Weigand0, Weigand1, USB_ID, and RemoteIR_In can be selected from GPIO0 to GPIO102.
Note: For IT9852E and IT9854E, they have GPIO0 to GPIO81, GPIO98, and GPIO99 pins.
Note: For IT9856TE and IT9866TE, they have GPIO0 to GPIO102 pins.

Table 4-14. GPIO Pin Description

Pin Name	Type	Default (reset)	Power	Description
GPIO0	I/O	HighZ	VDD_IOA	-
GPIO1	I/O	HighZ	VDD_IOA	-
GPIO2	I/O	HighZ	VDD_IOA	-
GPIO3	I/O	HighZ / Output0	VDD_IOA	Default value is: HighZ: if HOST_CFG[1:0] != 01 Output0: if HOST_CFG[1:0] == 01

Pin Name	Type	Default (reset)	Power	Description
GPIO4	I/O	HighZ	VDD_IOA	-
GPIO5	I/O	HighZ	VDD_IOA	-
GPIO6	I/O	HighZ	VDD_IOA	-
GPIO7	I/O	HighZ	VDD_IOA	-
GPIO8	I/O	HighZ	VDD_IOA	-
GPIO9	I/O	HighZ	VDD_IOA	-
GPIO10	I/O	HighZ	VDD_IOA	-
GPIO11	I/O	HighZ	VDD_IOA	-
GPIO12	I/O	HighZ	VDD_IOA	-
GPIO13	I/O	HighZ	VDD_IOA	-
GPIO14	I/O	HighZ	VDD_IOA	-
GPIO15	I/O	HighZ	VDD_IOA	-
GPIO16	I/O	HighZ	VDD_IOA	-
GPIO17	I/O	HighZ	VDD_IOA	-
GPIO18	I/O	HighZ	VDD_IOA	-
GPIO19	I/O	HighZ	VDD_IOA	-
GPIO20	I/O	HighZ	VDD_IOA	-
GPIO21	I/O	HighZ	VDD_IOA	-
GPIO22	I/O	HighZ	VDD_IOA	-
GPIO23	I/O	HighZ	VDD_IOA	-
GPIO24	I/O	HighZ	VDD_IOA	-
GPIO25	I/O	HighZ	VDD_IOA	-
GPIO26	I/O	HighZ	VDD_IOA	-
GPIO27	I/O	HighZ	VDD_IOA	-
GPIO28	I/O	HighZ	VDD_IOA	-
GPIO29	I/O	HighZ	VDD_IOA	-
GPIO30	I/O	HighZ	VDD_IOA	-
GPIO31	I/O	HighZ	VDD_IOB	-
GPIO32	I/O	HighZ	VDD_IOB	-
GPIO33	I/O	HighZ	VDD_IOB	-
GPIO34	I/O	HighZ	VDD_IOB	-
GPIO35	I/O	HighZ	VDD_IOB	-
GPIO36	I/O	HighZ	VDD_IOB	-
GPIO37	I/O	HighZ	VDD_IOB	-
GPIO38	I/O	HighZ	VDD_IOB	-
GPIO39	I/O	HighZ	VDD_IOB	-
GPIO40	I/O	HighZ	VDD_IOB	-
GPIO41	I/O	HighZ	VDD_IOB	-
GPIO42	I/O	HighZ	VDD_IOB	-
GPIO43	I/O	HighZ	VDD_IOB	-
GPIO44	I/O	HighZ	VDD_IOB	-
GPIO45	I/O	HighZ	VDD_IOB	-
GPIO46	I/O	HighZ	VDD_IOB	BOOT_CFG0
GPIO47	I/O	HighZ	VDD_IOB	BOOT_CFG1
GPIO48	I/O	HighZ	VDD_IOB	HOST_CFG0
GPIO49	I/O	HighZ	VDD_IOB	HOST_CFG1
GPIO50	I/O	HighZ	VDD_IOB	PLL_CFG
GPIO51	I/O	HighZ	VDD_IOB	DCXO_CFG
GPIO52	I/O	HighZ	VDD_IOB	-
GPIO53	I/O	HighZ	VDD_IOB	-
GPIO54	I/O	HighZ	VDD_IOB	-
GPIO55	I/O	HighZ	VDD_IOB	-
GPIO56	I/O	HighZ	VDD_IOB	-
GPIO57	I/O	HighZ	VDD_IOB	-
GPIO58	I/O	HighZ	VDD_IOB	-
GPIO59	I/O	HighZ	VDD_IOB	-
GPIO60	I/O	HighZ	VDD_IOB	-
GPIO61	I/O	HighZ	VDD_IOB	-
GPIO62	I/O	HighZ	VDD_IOB	-
GPIO63	I/O	HighZ	VDD_IOB	-

Pin Name	Type	Default (reset)	Power	Description
GPIO64	I/O	HighZ	VDD_IOB	-
GPIO65	I/O	HighZ	VDD_IOB	-
GPIO66	I/O	HighZ	VDD_IOB	-
GPIO67	I/O	HighZ	VDD_IOB	-
GPIO68	I/O	HighZ	VDD_IOB	-
GPIO69	I/O	HighZ	VDD_IOB	-
GPIO70	I/O	HighZ	VDD_IOB	-
GPIO71	I/O	HighZ	VDD_IOB	-
GPIO72	I/O	HighZ	VDD_IOB	-
GPIO73	I/O	HighZ	VDD_IOB	-
GPIO74	I/O	HighZ	VDD_IOB	-
GPIO75	I/O	HighZ	VDD_IOB	-
GPIO76	I/O	HighZ	VDD_IOB	-
GPIO77	I/O	HighZ	VDD_IOB	-
GPIO78	I/O	HighZ	VDD_IOB	-
GPIO79	I/O	HighZ	VDD_IOB	-
GPIO80	I/O	HighZ	VDD_IOB	-
GPIO81	I/O	HighZ	VDD_IOB	-
GPIO82	I/O	HighZ	VDD_IOB	-
GPIO83	I/O	HighZ	VDD_IOB	-
GPIO84	I/O	HighZ	VDD_IOB	-
GPIO85	I/O	HighZ	VDD_IOB	-
GPIO86	I/O	HighZ	VDD_IOA	-
GPIO87	I/O	HighZ	VDD_IOA	-
GPIO88	I/O	HighZ	VDD_IOA	-
GPIO89	I/O	HighZ	VDD_IOA	-
GPIO90	I/O	HighZ	VDD_IOB	-
GPIO91	I/O	HighZ	VDD_IOB	-
GPIO92	I/O	HighZ	VDD_IOB	-
GPIO93	I/O	HighZ	VDD_IOB	-
GPIO94	I/O	HighZ	VDD_IOB	-
GPIO95	I/O	HighZ	VDD_IOB	-
GPIO96	I/O	HighZ	VDD_IOB	-
GPIO97	I/O	HighZ	VDD_IOB	-
GPIO98	I/O	HighZ	VDD_IOA	-
GPIO99	I/O	HighZ	VDD_IOA	-
GPIO100	I/O	HighZ	VDD_IOA	-
GPIO101	I/O	HighZ	VDD_IOA	-
GPIO102	I/O	HighZ	VDD_IOA	-

Notes: GPIO46~GPIP51 are for the hardware trap. There is pull-high/low resistance on I/O. It cannot drive the value on the external device when the system is resetting.

Table 4-15. SPI Host Interface when HOST_CFG == 01

Pin Name	Type	Default	Description
GPIO0	Input	HighZ	SPI Slave CLK
GPIO1	Input	HighZ	SPI Slave CS#
GPIO2	Input	HighZ	SPI Slave DIN
GPIO3	Output	0	SPI Slave DOUT

Table 4-16. IIC Host Interface when HOST_CFG == 10

Pin Name	Type	Default	Description
GPIO0	I/O	HighZ	IIC SCL
GPIO1	I/O	HighZ	IIC SDA

4.6 Hardware Trapping

Table 4-17. Hardware Trapping

Pin Name	Symbol	Description
GPIO46	BOOT_CFG0	Boot Configuration 00: booting from SD/MMC 01: booting from NOR 10: booting from SPI NAND 11: co-operative mode
GPIO47	BOOT_CFG1	
GPIO48	HOST_CFG0	Host Configuration 00: select JTAG interface 01: select SPI interface 10: select IIC interface 11: uses as DGPIO[0-3]
GPIO49	HOST_CFG1	
GPIO50	PLL_CFG	PLL Configuration 0: normal 1: bypass PLL
GPIO51	DCXO_CFG	PLL DCXO Configuration 0: normal 1: bypass DCXO

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5. Function Description

5.1 Overview

The IT9852E/IT9854E/IT9856TE/IT9866TE supports 8/9/16/18/24 bits CPU interface, with 6/9/16/18/24 bits RGB interface, CCIR601, digital T-CON mode. The IT9852E/IT9854E/IT9856TE/IT9866TE supports both that with memory and that without memory LCD modules (LCM). The programmable interface timing is designed to fit most LCMs. Hereunder is the pin share mapping on each different mode.

Table 5-1. LCD Interface General Pin Mapping

Pin Name	RGB I/F	CPU I/F	CCIR 601/656	Digital T-CON
LVSYNC	VSYNC	XWR	VSYNC	STV / CTG1
LHSYNC	HSYNC	XRS	HSYNC	DIO / CTG0
LDCLK	DCLK		DCLK	DCLK
LDEN	DEN		DEN	DE / CTG2
LD0	D0	D0	D0	D0
LD1	D1	D1	D1	D1
LD2	D2	D2	D2	D2
LD3	D3	D3	D3	D3
LD4	D4	D4	D4	D4
LD5	D5	D5	D5	D5
LD6	D6	D6	D6	D6
LD7	D7	D7	D7	D7
LD8	D8	D8	D8	D8
LD9	D9	D9	D9	D9
LD10	D10	D10	D10	D10
LD11	D11	D11	D11	D11
LD12	D12	D12	D12	D12
LD13	D13	D13	D13	D13
LD14	D14	D14	D14	D14
LD15	D15	D15	D15	D15
LD16	D16	D16		D16
LD17	D17	D17		D17
LD18	D18	D18		D18
LD19	D19	D19		D19
LD20	D20	D20		D20
LD21	D21	D21		D21
LD22	D22 / CTG4	D22	CTG4	D22 / POL
LD23	D23 / CTG5	D23	CTG5	D23 / REV
LCSN	CS0 / CTG7	CS0	CS0 / CTG7	CS0 / LD
LSA0	A0 / CTG6		A0 / CTG6	A0 / CKV
LSDA	SDA		SDA	SDA
LSCK	SCK / CTG3		SCK / CTG3	SCK / OEV

Table 5-2. LCD with RGB Interface Pin Mapping for RGB565 and RGB666

Color Mode	RGB565	RGB666					
Panel Interface	16bits	6-bits			9-bits		18-bits
Timing Sequence	t/pixel	t1/pixel	t2/pixel	t3/pixel	t1/pixel	t2/pixel	t/pixel
LD0	B0	R0	G0	B0	G3	B0	B0
LD1	B1	R1	G1	B1	G4	B1	B1
LD2	B2	R2	G2	B2	G5	B2	B2
LD3	B3	R3	G3	B3	R0	B3	B3
LD4	B4	R4	G4	B4	R1	B4	B4
LD5	G0	R5	G5	B5	R2	B5	B5
LD6	G1				R3	G0	G0

LD7	G2				R4	G1	G1
LD8	G3				R5	G2	G2
LD9	G4						G3
LD10	G5						G4
LD11	R0						G5
LD12	R1						R0
LD13	R2						R1
LD14	R3						R2
LD15	R4						R3
LD16							R4
LD17							R5

Table 5-3. LCD with RGB Interface Pin Mapping for RGB888

Color Mode	RGB888								
Panel Interface	9-bits/mode 1			9-bits/mode 2			18-bits		24-bits
Timing Sequence	t1/pixel	t2/pixel	t3/pixel	t1/pixel	t2/pixel	t3/pixel	t1/pixel	t2/pixel	t/pixel
LD0	R0	G0	B0	GND	GND	GND	R0	B0	B0
LD1	R1	G1	B1	R0	G0	B0	R1	B1	B1
LD2	R2	G2	B2	R1	G1	B1	R2	B2	B2
LD3	R3	G3	B3	R2	G2	B2	R3	B3	B3
LD4	R4	G4	B4	R3	G3	B3	R4	B4	B4
LD5	R5	G5	B5	R4	G4	B4	R5	B5	B5
LD6	R6	G6	B6	R5	G5	B5	R6	B6	B6
LD7	R7	G7	B7	R6	G6	B6	R7	B7	B7
LD8	GND	GND	GND	R7	G7	B7	GND	G0	G0
LD9							GND	G1	G1
LD10							GND	G2	G2
LD11							GND	G3	G3
LD12							GND	G4	G4
LD13							GND	G5	G5
LD14							GND	G6	G6
LD15							GND	G7	G7
LD16							GND	GND	R0
LD17							GND	GND	R1
LD18									R2
LD19									R3
LD20									R4
LD21									R5
LD22									R6
LD23									R7

Table 5-4. LCD Pin Share with GPIO Table

Pin	Mode 0	Mode 1	Mode 2	Mode 3
GPIO37	GPIO37	LSCK		
GPIO38	GPIO38	LSA0		
GPIO39	GPIO39	LD23		
GPIO40	GPIO40	LD22		
GPIO41	GPIO41	LD21		
GPIO42	GPIO42	LD20		
GPIO43	GPIO43	LD19		
GPIO44	GPIO44	LD18		
GPIO45	GPIO45	LD17		
GPIO46	GPIO46	LD16		

Pin	Mode 0	Mode 1	Mode 2	Mode 3
GPIO47	GPIO47	LD15		
GPIO48	GPIO48	LD14		
GPIO49	GPIO49	LD13		
GPIO50	GPIO50	LD12		
GPIO51	GPIO51	LD11		
GPIO52	GPIO52	LD10		
GPIO53	GPIO53	LD9		
GPIO54	GPIO54	LD8		
GPIO55	GPIO55	LD7		
GPIO56	GPIO56	LD6		
GPIO57	GPIO57	LD5		
GPIO58	GPIO58	LD4		
GPIO59	GPIO59	LD3		
GPIO60	GPIO60	LD2		
GPIO61	GPIO61	LD1		
GPIO62	GPIO62	LD0		
GPIO63	GPIO63	LSDA		
GPIO64	GPIO64	LCSN		
GPIO65	GPIO65	LDEN		
GPIO66	GPIO66	LDCLK		
GPIO67	GPIO67	LHSYNC		
GPIO68	GPIO68	LVSYNC		

5.1.1 General Description

- 80-type CPU interface
- 68-type CPU interface
- RGB with serial interface
- RGB with direct control interface
- CCIR601/CCIR656 output interface
- LCD common timing generator

5.1.2 80-Type CPU Interface

The figure below illustrates the implementation for interfacing the IT9852E/IT9854E/IT9856TE/IT9866TE to an 80-type CPU interface LCM. IT9852E/IT9854E/IT9856TE/IT9866TE can support dual display for this interface.

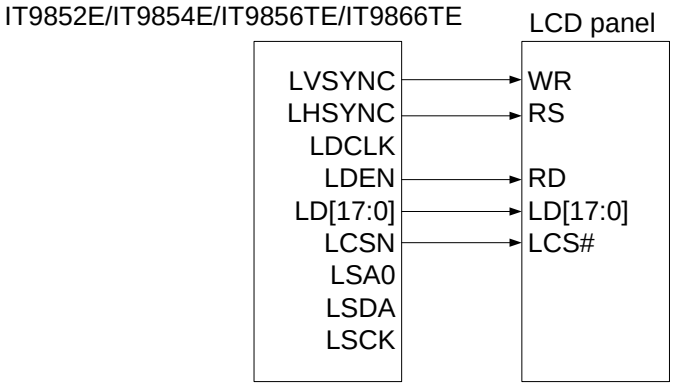


Figure 5-1. Connection of IT9852E/IT9854E/IT9856TE/IT9866TE to 80-Type CPU Interface LCM

The timing for 80-type CPU interface is shown in the following figure. There is an internal clock DHCLK. By adjusting the timing parameters T_1 ~ T_8, which are relative to DHCLK, it can satisfy the timing requirement of LCD panels.

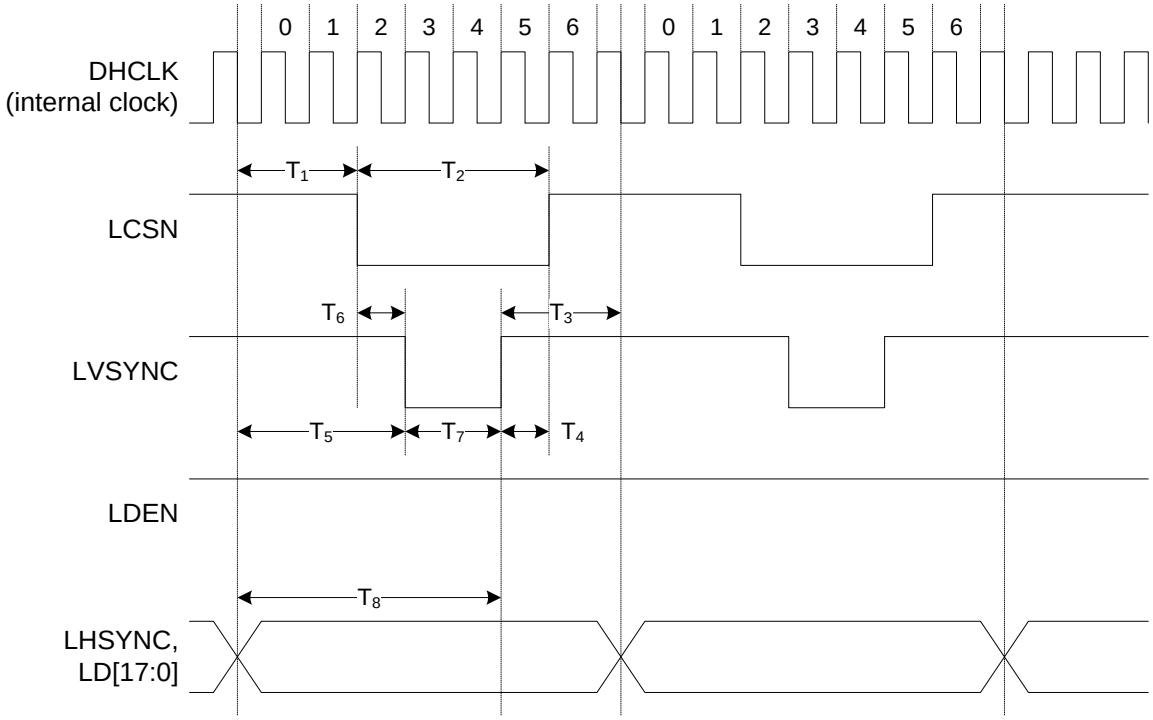


Figure 5-2. 80-Type CPU Interface Timing

5.1.3 68-Type CPU Interface

The figure below illustrates the implementation for interfacing the IT9852E/IT9854E/IT9856TE/IT9866TE to a 68-type CPU interface LCM. IT9852E/IT9854E/IT9856TE/IT9866TE can support dual display for this interface.

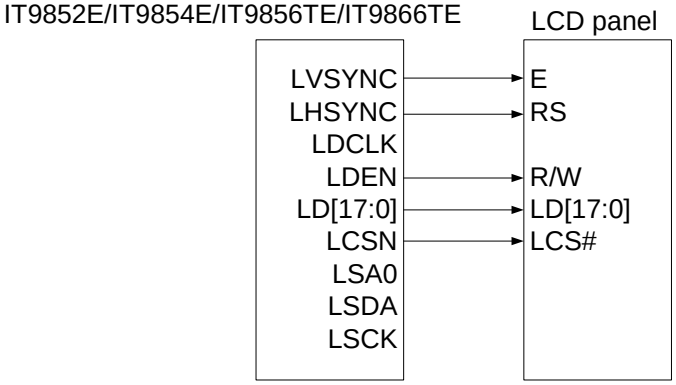


Figure 5-3. Connection of IT9852E/IT9854E/IT9856TE/IT9866TE to 68-Type CPU Interface LCM

The timing for 68-type CPU interface is shown in the following figure. There is an internal clock DHCLK. By adjusting the timing parameters T_1 ~ T_8, which are relative to DHCLK, it can satisfy the timing requirement of LCD panels.

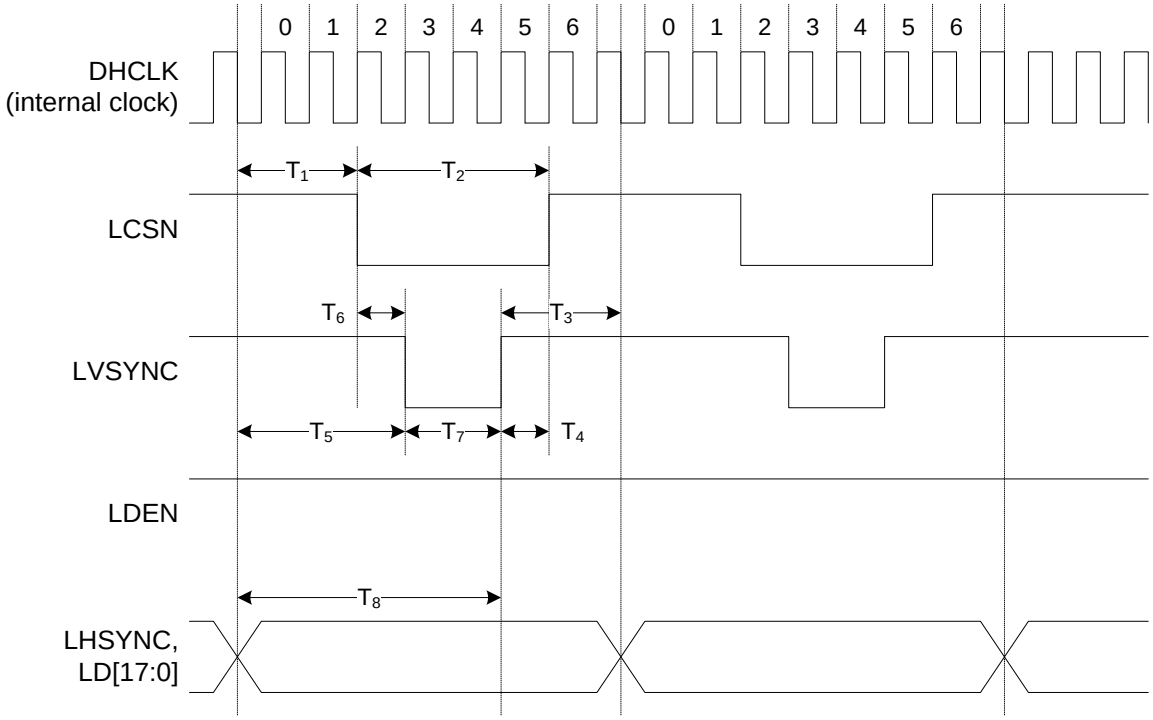


Figure 5-4. 68-Type CPU Interface Timing

5.1.4 RGB with Serial Interface

The figure below illustrates the implementation for interfacing the IT9852E/IT9854E/IT9856TE/IT9866TE to an RGB with serial interface LCM. IT9852E/IT9854E/IT9856TE/IT9866TE only supports one display for this interface.

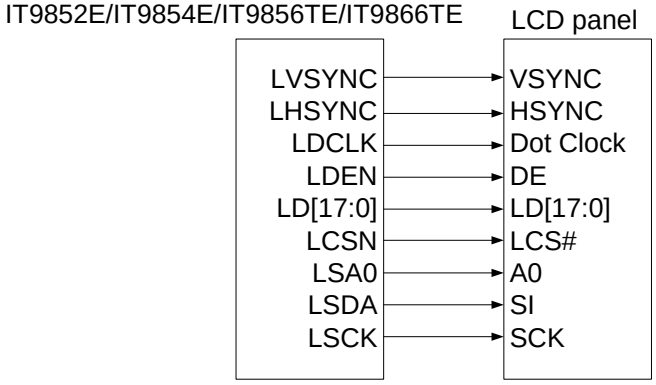


Figure 5-5. Connection of IT9852E/IT9854E/IT9856TE/IT9866TE to RGB with Serial Interface LCM

IT9852E/IT9854E/IT9856TE/IT9866TE supports 8/9/24 bits serial interface to send LCM command and uses 6/9/16/18 bits parallel RGB interface to send display data. The timing for RGB with serial interface is shown in the following figure.

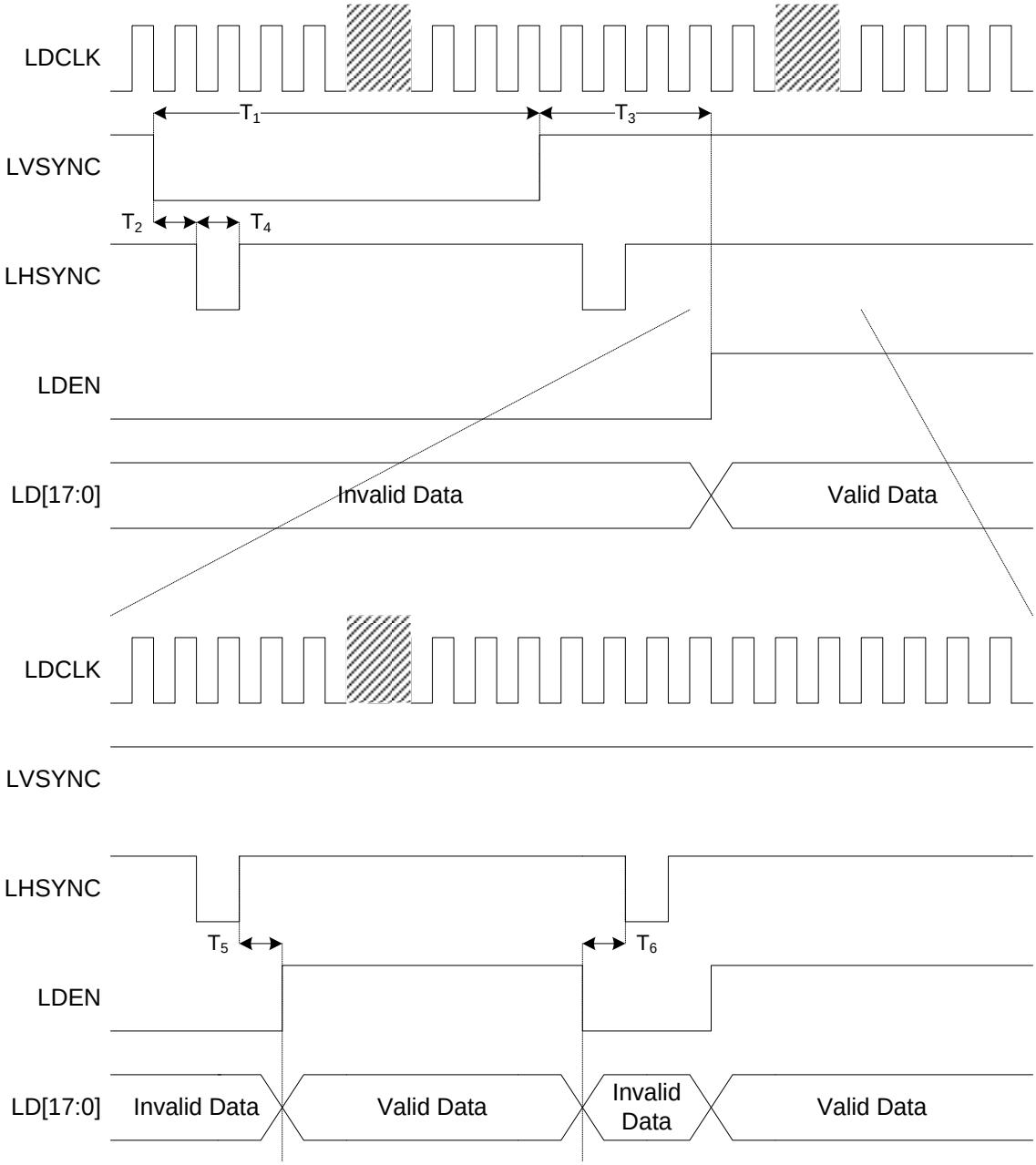


Figure 5-6. RGB Timing (for data)

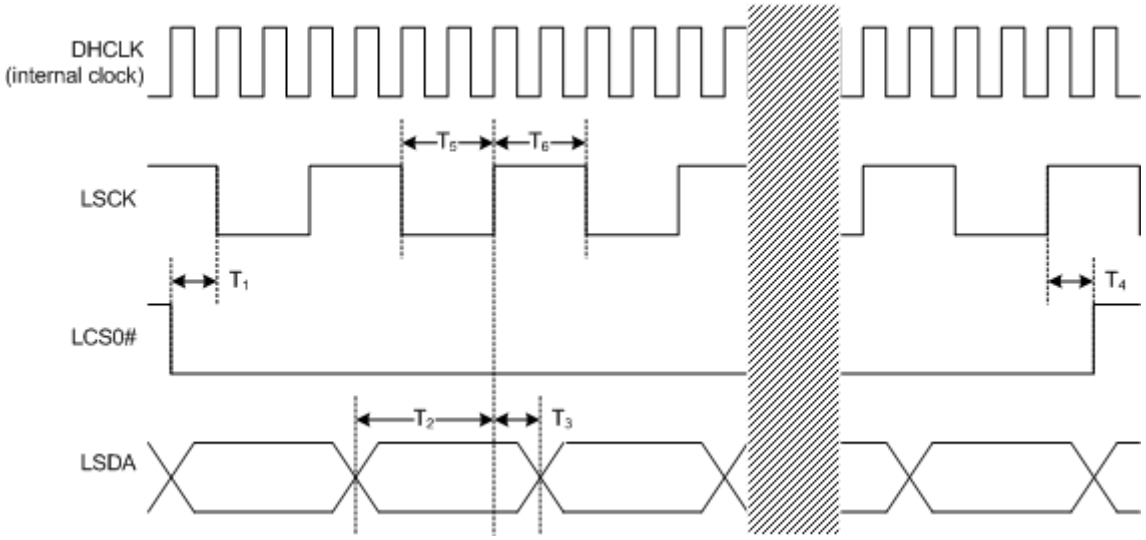


Figure 5-7. RGB Timing (for command)

5.1.5 RGB with Direct Control Interface

The figure below illustrates the implementation for interfacing the IT9852E/IT9854E/IT9856TE/IT9866TE to a RGB with direct control interface LCM. IT9852E/IT9854E/IT9856TE/IT9866TE only supports one display with this interface

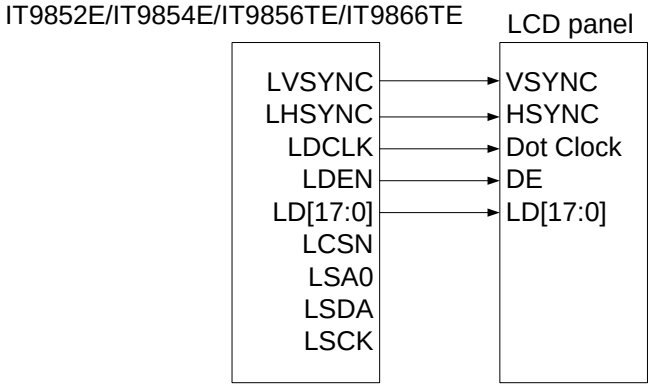


Figure 5-8. Connection of IT9852E/IT9854E/IT9856TE/IT9866TE to RGB with Direct Control Interface LCM

Some LCMs do not have any serial interface, but only have parallel RGB interface. In this case, the unused pins LCSN can be defined as GPIO. See Table 5-4 for detail. The timing for RGB parallel interface is shown in the following figure.

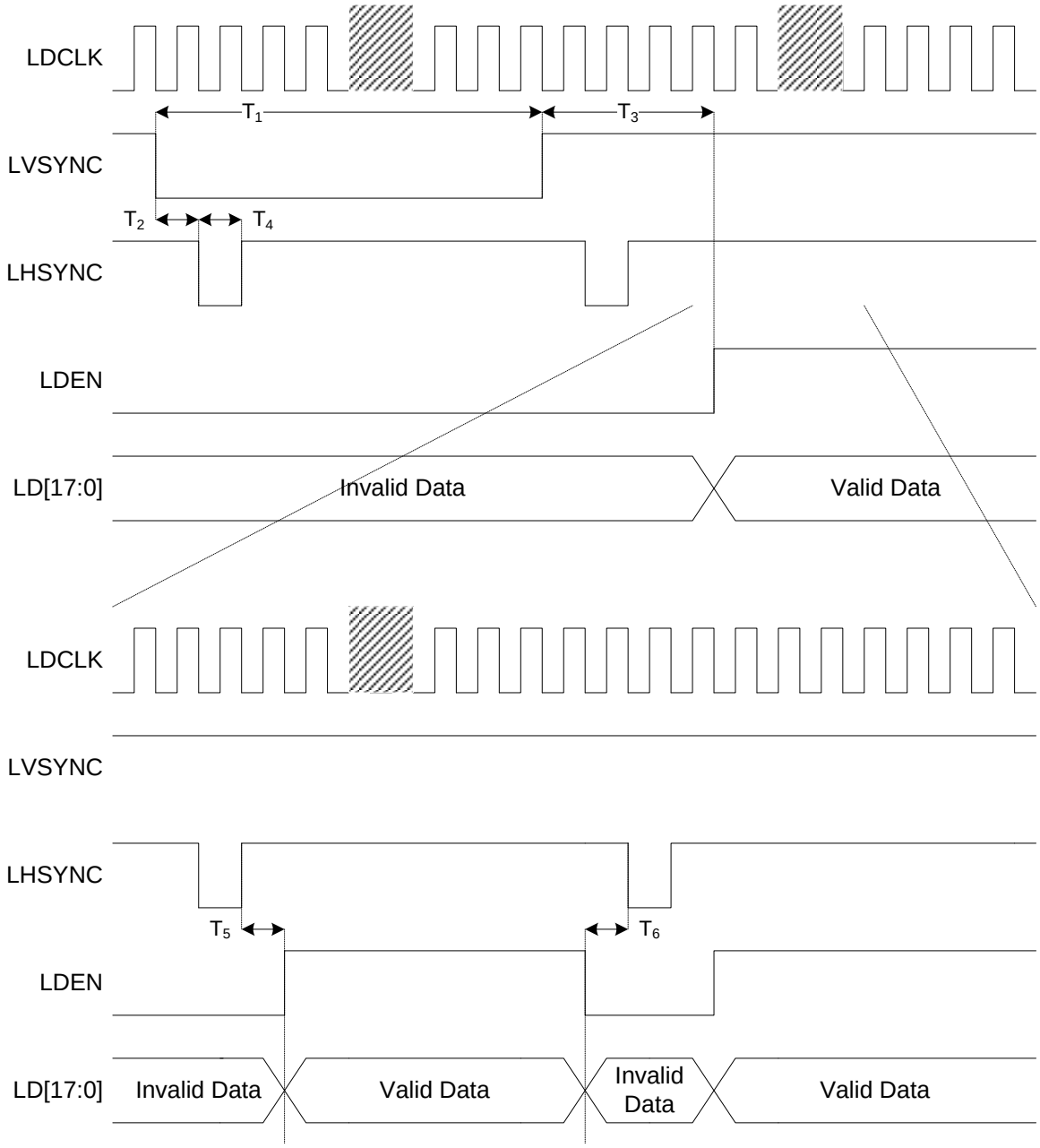


Figure 5-9. RGB with Direct Control Interface Timing (for data)

5.1.6 CCIR601/656 Output Interface

IT9852E/IT9854E/IT9856TE/IT9866TE supports CCIR601/656 output interface. It can be connected to any device which has CCIR601/656 input interface. The figure below illustrates the implementation. The CCIR601/656 output video resolution and timing are programmable. It can be set to meet the system requirement. The general output resolutions are 800x480, 640x480, 480x272, 320x240 and 240x320.

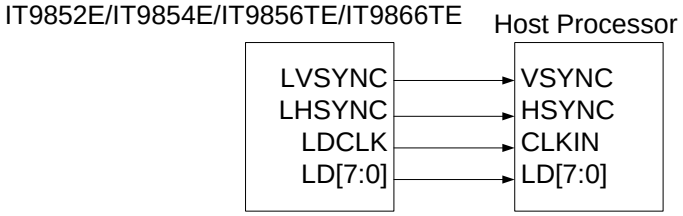


Figure 5-10. Connection of IT9852E/IT9854E/IT9856TE/IT9866TE to a Host Processor with CCIR601 Interface

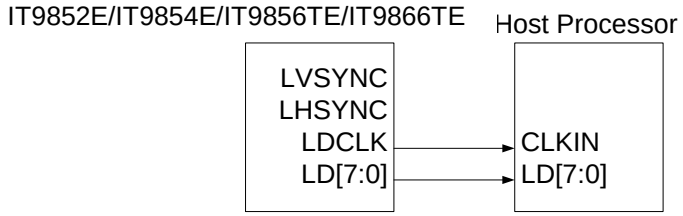


Figure 5-11. Connection of IT9852E/IT9854E/IT9856TE/IT9866TE to a Host Processor with CCIR656 Interface

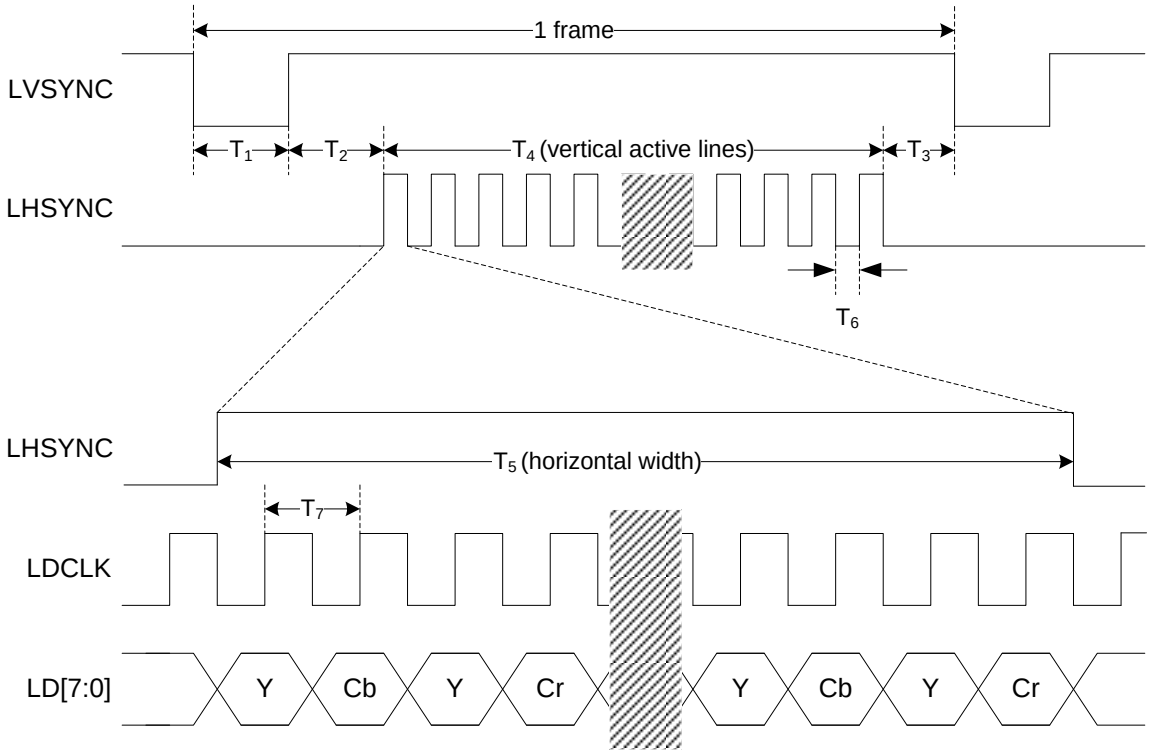


Figure 5-12. CCIR601 Output Interface Timing

Table 5-5. CCIR601 Output Interface Timing Table

Symbol	Parameter	30 frame/sec	25 frame/sec	Unit
800x480 progressive video				
T_1	Vertical sync pulse width	8	8	line
T_2	Vertical back porch	6	6	line

T_3	Vertical front porch	6	6	line
T_4	Vertical active lines	480	480	line
T_5	Horizontal width of one active line	1600	1600	T (1)
T_6	Horizontal sync pulse width	200	560	T
T_7	Clock period	37 (2)	37	ns
640x480 progressive video				
T_1	Vertical sync pulse width	8	8	line
T_2	Vertical back porch	6	6	line
T_3	Vertical front porch	6	6	line
T_4	Vertical active lines	480	480	line
T_5	Horizontal width of one active line	1280	1280	T
T_6	Horizontal sync pulse width	520	880	T
T_7	Clock period	37	37	ns
480x272 progressive video				
T_1	Vertical sync pulse width	8	8	line
T_2	Vertical back porch	10	10	line
T_3	Vertical front porch	10	10	line
T_4	Vertical active lines	272	272	line
T_5	Horizontal width of one active line	960	960	T
T_6	Horizontal sync pulse width	40	240	T
T_7	Clock period	111(3)	111	ns
320x240 progressive video				
T_1	Vertical sync pulse width	20	20	line
T_2	Vertical back porch	20	20	line
T_3	Vertical front porch	20	20	line
T_4	Vertical active lines	240	240	line
T_5	Horizontal width of one active line	640	640	T
T_6	Horizontal sync pulse width	110	260	T
T_7	Clock period	148 (4)	148	ns
240x320 progressive video				
T_1	Vertical sync pulse width	15	15	line
T_2	Vertical back porch	20	20	line
T_3	Vertical front porch	20	20	line
T_4	Vertical active lines	320	320	line
T_5	Horizontal width of one active line	480	480	T
T_6	Horizontal sync pulse width	120	240	T

T_7	Clock period	148	148	ns

Notes:

1. T represents the clock period.
2. The clock frequency is 27.0 MHz.
3. The clock frequency is 9.0 MHz.
4. The clock frequency is 6.75 MHz.

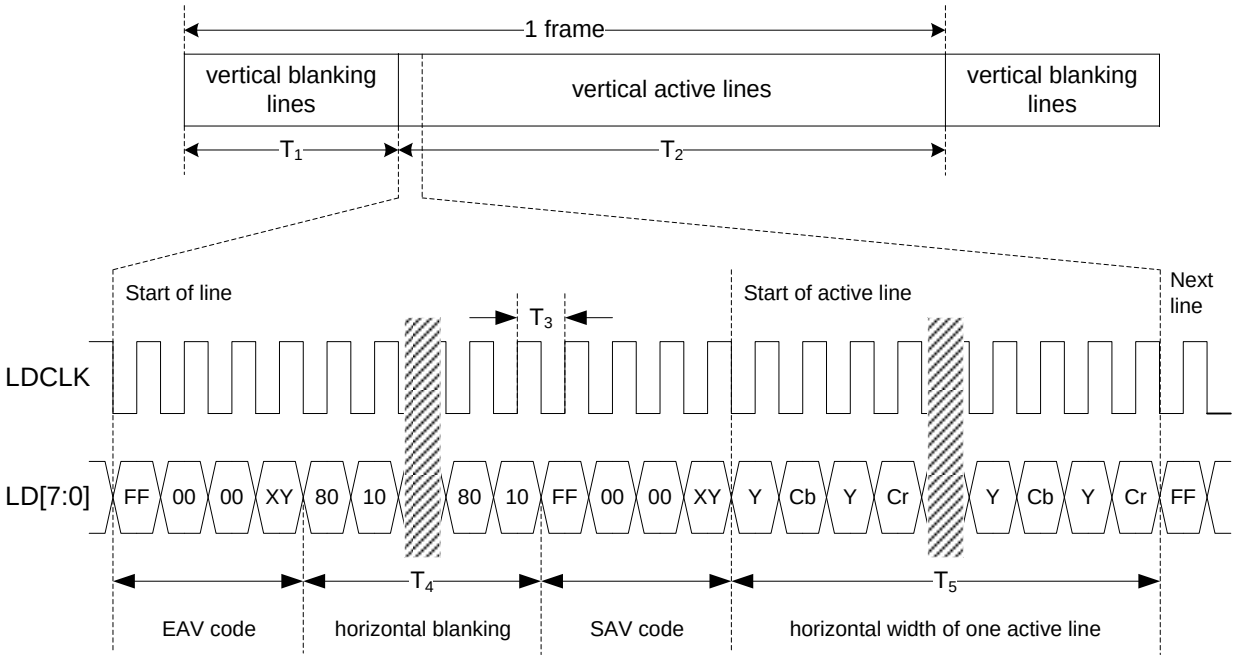


Figure 5-13. CCIR656 Output Interface Timing

The SAV (start of active video) code and EAV (end of active video) code are embedded within the video data stream. They replace the vertical sync and horizontal sync signals. The definitions of SAV and EAV codes are shown in the following table.

Table 5-6. SAV Code and EAV Code

Bit Number	The 1st word	The 2nd word	The 3rd word	The 4th word
7 (MSB)	1	0	0	1
6	1	0	0	F(1)
5	1	0	0	V(2)
4	1	0	0	H(3)
3	1	0	0	P3(4)
2	1	0	0	P2
1	1	0	0	P1
0	1	0	0	P0

Notes:

1. When interleaved video: F = 0 for field 1 and F = 1 for field 2. When progressive video: F = 0.
2. V = 1 during vertical blanking, and V = 0 elsewhere.
3. H = 0 in SAV, H = 1 in EAV.
4. P3 ~ P0 are protection bits. Where P3 = V xor H, P2 = F xor H, P1 = F xor V, P0 = F xor V xor H.

Table 5-7. CCIR656 Output Interface Timing Table

Symbol	Parameter	30 frame/sec	25 frame/sec	Unit
800x480 progressive video				
T_1	Vertical blanking lines	20	20	line
T_2	Vertical active lines	480	480	line
T_3	Clock period	37 (2)	37	ns
T_4	Horizontal blanking	192	552	T (1)
T_5	Horizontal width of one active line	1600	1600	T
640x480 progressive video				
T_1	Vertical blanking lines	20	20	line
T_2	Vertical active lines	480	480	line
T_3	Clock period	37	37	ns
T_4	Horizontal blanking	512	872	T
T_5	Horizontal width of one active line	1280	1280	T
480x272 progressive video				
T_1	Vertical blanking lines	28	28	line
T_2	Vertical active lines	272	272	line
T_3	Clock period	111(3)	111	ns
T_4	Horizontal blanking	32	232	T
T_5	Horizontal width of one active line	960	960	T
320x240 progressive video				
T_1	Vertical blanking lines	60	60	line
T_2	Vertical active lines	240	240	line
T_3	Clock period	148 (4)	148	ns
T_4	Horizontal blanking	102	252	T
T_5	Horizontal width of one active line	640	640	T
240x320 progressive video				

T_1	Vertical blanking lines	55	55	line
T_2	Vertical active lines	320	320	line
T_3	Clock period	148	148	ns
T_4	Horizontal blanking	112	232	T
T_5	Horizontal width of one active line	480	480	T

Notes:

1. T represents the clock period.
2. The clock frequency is 27.0 MHz.
3. The clock frequency is 9.0 MHz.
4. The clock frequency is 6.75 MHz.

5.1.7 LCD Common Timing Generator

There are 8 configurable timing generator signals for driving LCD module which is without Timing Controller (TCON) inside. One type of configurable timing generator signals (CTG0 ~ CTG3) has 2 pairs of control points, while the other type of configurable timing generator signals (CTG4 ~ CTG7) has 1 pair of control points. Two control points define one operation window. The start point is in the top-left corner and the end point is in the bottom-right corner.

The operation window can be in frame mode or line mode. In frame mode, the signal only changes in the top-left and bottom-right corner of each operation window. In line mode, the signal changes every line at the left boundary and the right boundary of the operation window.

When the signal meets the change condition, one action will be assigned. Here are 4 possible actions:

1. Hold the same value
2. Set the value to be 1
3. Set the value to be 0
4. Inverse of the previous value

By setting proper parameters of the configurable timing generator signals, we can generate every control signal for LCD module which is without Timing Controller (TCON) inside.

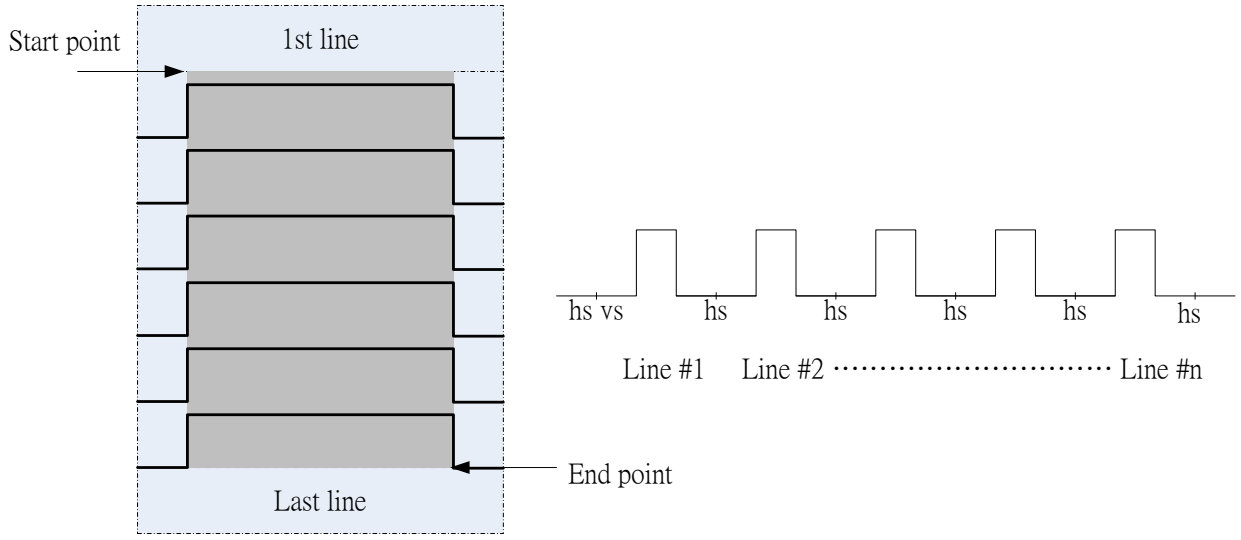


Figure 5-14. Line Mode

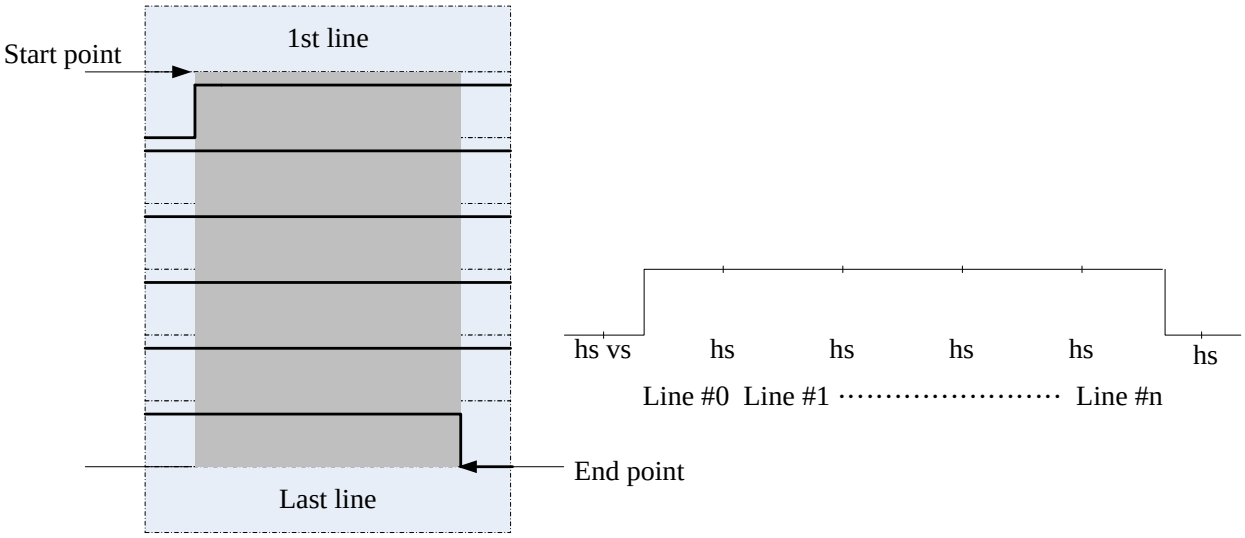


Figure 5-15. Frame Mode

The following two figures are the examples of the controller signal for digital TCON. The related CTG timing parameters are shown on the next table.

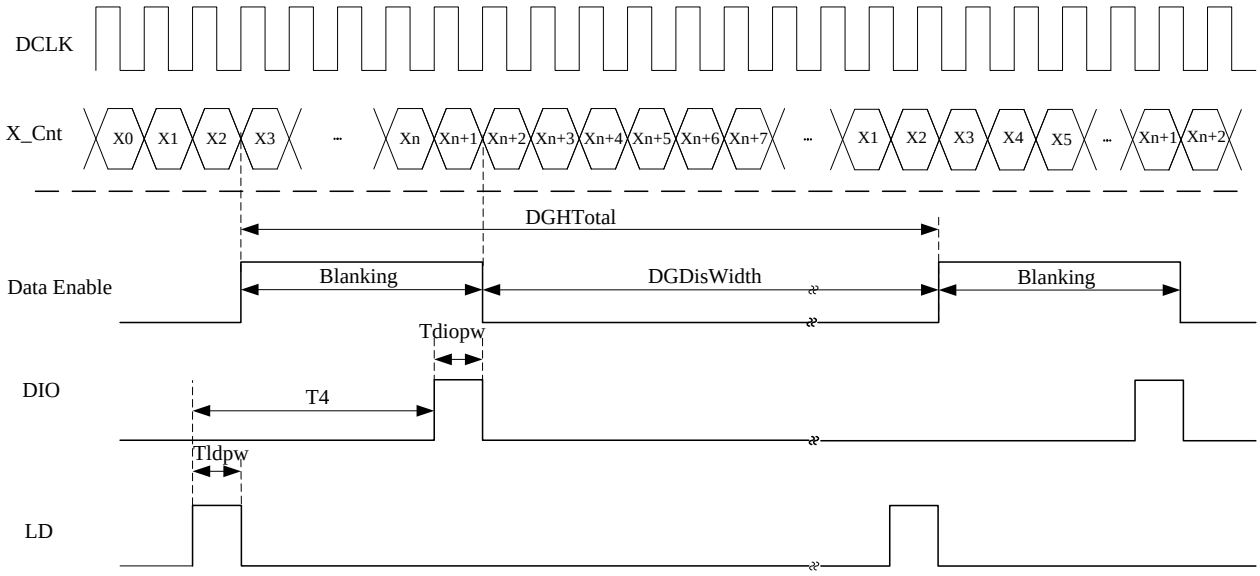


Figure 5-16. Horizontal Control Timing Waveform for Digital T-CON

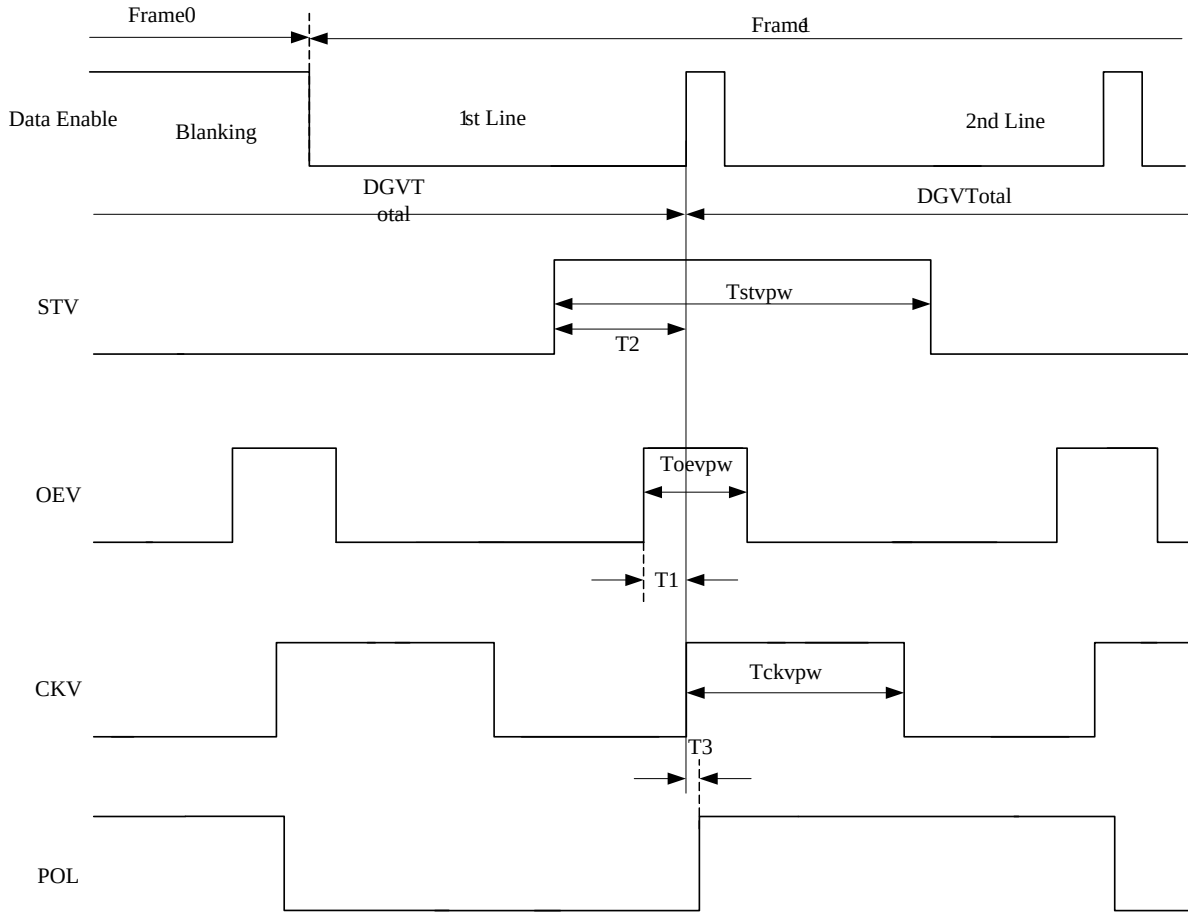


Figure 5-17. Vertical Control Timing Waveform for Digital T-CON

Table 5-8. The timing parameters for Digital T-CON

Symbol	Related CTG Control Signal	Unit
Tstvpw	CTG1 P2X – CTG1 P1X	Pix
T2	CTG1 P1X – CTG6 P1X	Pix
Toevpw	CTG3 P2X – CTG0 P1X	Pix
T1	CTG3 P1X – CTG6 P1X	Pix
Tckvpw	CTG6 P2X – CTG6 P1X	Pix
T3	CTG6 P1X – CTG4 P1X	Pix
Tdiopw	CTG0 P2X – CTG0 P1X	Pix
T4	CTG0 P1X – CTG7 P1X	Pix
Tldpw	CTG7 P2X – CTG7 P1X	Pix

5.2 Host/Device USB 2.0 Interface

This is a universal serial bus (USB) 2.0 On-The-Go (OTG) controller, which can play a dual role, either as a host or as a peripheral controller. There are two USB controllers. One is Host/Device selectable, and the other is host only. For the Host/Device selectable controller, it controls with USB_ID pin which it can be selected by any GPIO pins. When it acts as a host, it contains a USB host controller that supports all-speed transactions. Without the software intervention, the host controller can deal with a transaction-based data structure to offload the CPU and automatically transmit and receive data on the USB bus. When it acts as a peripheral controller, each

endpoint, except endpoint 0, accepts programmable HS/FS transfer types to provide flexibility to suit all applications. In addition, complying with OTG standards means both the Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) are supported. The system bus can be a PVCI or AHB 32-bit bus interface. The transceiver interface is UTMI+ level 3, which supports the HS/FS/LS transfers and a HS/FS hub.

Table 5-9. Dynamic Characteristics of DP/DM

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
USB 2.0 transceiver (HS)						
Input levels (Differential receiver)						
V_{HSDIFF}	High-speed differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$ Measured at the connection as an application circuit	300	-	-	mV
V_{HSCM}	Voltage range of high-speed data signaling in the common mode		-50	-	500	mV
V_{HSSQ}	High-speed squelch detection threshold	Squelch is detected.	-	-	100	mV
		Squelch is not detected.	150	-	-	mV
V_{HSDSC}	High-speed disconnection detection threshold	Disconnection is detected.	625	-	-	mV
		Disconnection is not detected.	-	-	525	mV
Output levels						
V_{HSOI}	High-speed idle-level output voltage (Differential)		-10	-	10	mV
V_{HSOL}	High-speed low-level output voltage (Differential)		-10	-	10	mV
V_{HSOH}	High-speed high-level output voltage (Differential)		-360	-	400	mV
V_{CHIRPJ}	Chirp-J output voltage (Differential)		700	-	1100	mV
V_{CHIRPK}	Chirp-K output voltage (Differential)		-900	-	-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as the internal chip	40.5	45	49.5	Ω
Termination						
V_{TERM}	Termination voltage of the pull-up resistor on the RPU pin.		3.0	-	3.6	V
USB 1.1 transceiver (FS/LS)						
Input levels (Differential receiver)						
V_{DI}	Differential input voltage sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$	0.2	-	-	V
V_{CM}	Differential common-mode voltage		0.8	-	2.5	V
Input levels (single-ended receivers)						
V_{SE}	Single-ended receiver threshold		0.8	-	2.0	V
Output levels						

V_{OL}	Low-level output voltage		0	-	0.3	V
V_{HL}	High-level output voltage		2.8	-	3.6	V

Table 5-10. Static Characteristics of DP/DM

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics						
High-speed mode						
t_{HSR}	High-speed differential rise time		500	-	-	ps
t_{HSF}	High-speed differential fall time		500	-	-	ps
Full-speed mode						
t_{FR}	Rise time of DP/DM	C_L = 50 pF; 10% ~ 90% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	Fall time of DP/DM	C_L = 50 pF; 90% ~ 10% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FRMA}	Differential rise/fall time matching (t_{FR} / t_{FF})	Excluding the first transition from the idle mode	90	-	110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from the idle mode	1.3	-	2.0	V
Low-speed mode						
t_{LR}	Rise time of DP/DM	CL = 200 pF ~ 600 pF; 10% ~ 90% of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LF}	Fall time of DP/DM	CL = 200 pF ~ 600 pF; 90% ~ 10% of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LRMA}	Differential rise/fall time matching (t_{LR}/t_{LF})	Excluding the first transition from the idle mode	80	-	125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from the idle mode	1.3	-	2.0	V
Driver timing						
High-speed mode						
	Driver waveform requirement	Please refer to the eye pattern of template 1 described in USB specification, Rev. 2.0.	Follow template 1			
Full-speed mode						
	Propagation delay (VI, FSE 0, OE to DP, DN)	For the detailed description of VI, FSE 0, and OE, please refer to the USB specification, Rev. 1.1.	-	-	15	ns
Low-speed mode						
Not specified: The low-speed delay time is dominated by the slow t_{LR} and t_{LF}.						

Receiver timing						
High-speed mode (Template 4, USB 2.0 spec.)						
	Data source jitter and receiver jitter tolerance	Please refer to the eye pattern of template 4 described in the USB rev 2.0 specification.	Follow template 4			
Full-speed mode						
$t_{PLH(rcv)}$ $t_{PHL(rcv)}$	Receiver propagation delay (DP; DM to RCV)	For the detailed description of RCV, please refer to the USB 1.1 specification.	-	-	15	ns
$t_{PLH(single)}$ $t_{PHL(single)}$	Receiver propagation delay (DP; DM to VOP, VON)		-	-	15	ns

5.3 MMC/SD Interface

5.3.1 General Description

The IT9852E/IT9854E/IT9856TE/IT9866TE supports the MMC/SD card for users to store the audio files, JPEG image and MPEG-4 movies. It is convenient for users to put these data to the computer or download data from the computer. The IT9852E/IT9854E/IT9856TE/IT9866TE is fully compliant with MMCA v3.3, low-voltage support, and 4-bit data of MMCA v4.0.

5.3.2 MMC/SD Interface Timing Diagram

The MMC/SD Interface Timing diagram is shown in Figure 5-18. The detailed timing description is shown in Table 5-11.

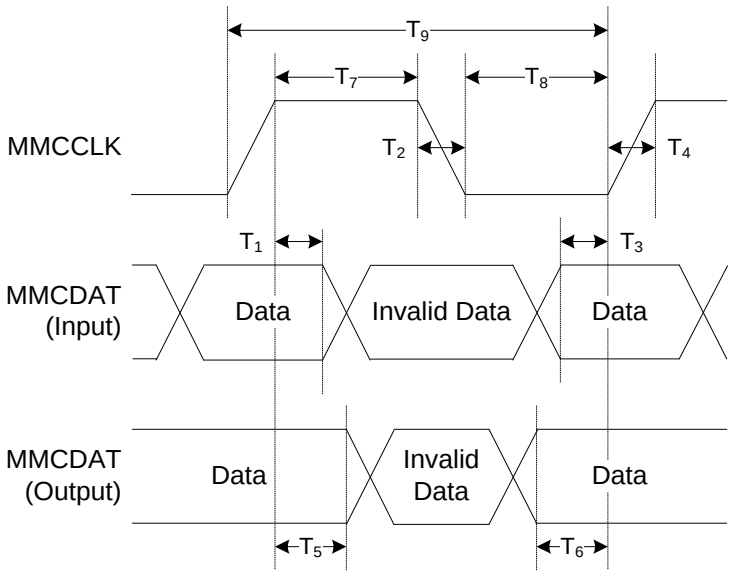


Figure 5-18. MMC/SD Interface Timing Diagram

Table 5-11. MMC/SD Interface Timing Table

Symbol	Parameter	Min	Max	Units
T1	Input Hold Time	5	-	ns
T2	Clock fall time	-	10	ns

T3	Input Setup Time	5	-	ns
T4	Clock Rise Time	-	10	ns
T5	Output Hold Time	3	-	ns
T6	Output Setup Time	3	-	ns
T7	Clock High Time	10	-	ns
T8	Clock Low Time	10	-	ns
T9	Clock Cycle Time	40	-	ns

5.4 SPI Interface

Table 5-12. NOR Interface AC Timing

Symbol	Alt	Parameter	Min	Typ	Max	Units
F_{clk}		Serial Clock Frequency	D.C.		20	MHz
t_{CH}		Serial Clock High Time	25			ns
t_{CL}		Serial Clock Low Time	25			ns
t_{CLCH}		Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}		Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time	5			ns
t_{CHSH}		CS# Active Hold Time	5			ns
t_{SHSL}	t_{CSH}	CS# High Time	50			ns
t_{CLQX}	t_{HO}	Input Hold Time	5			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	4			ns
t_{CHDX}	t_{DH}	Data In Hold Time	4			ns
t_{CLQV}		t_V Output Valid from SCK			12.5	ns

Notes: $t_{CLH} + t_{CLL}$ must greater than $1 / F_{CLK}$

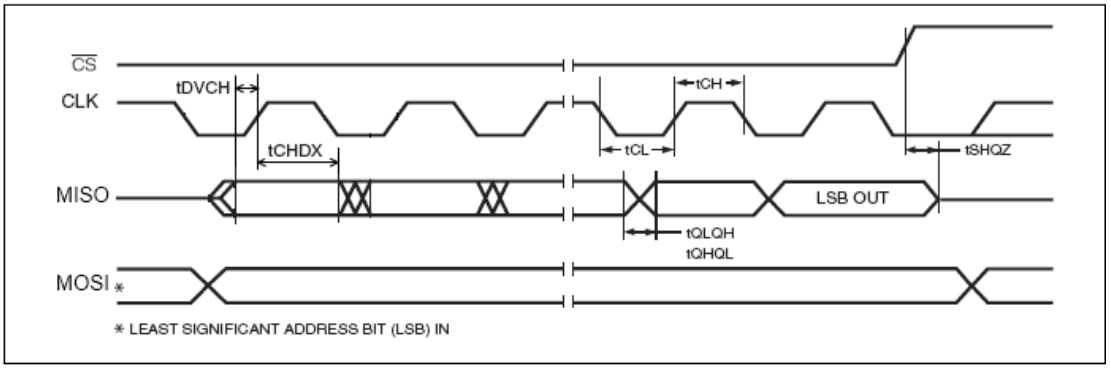


Figure 5-19. Serial Input Timing

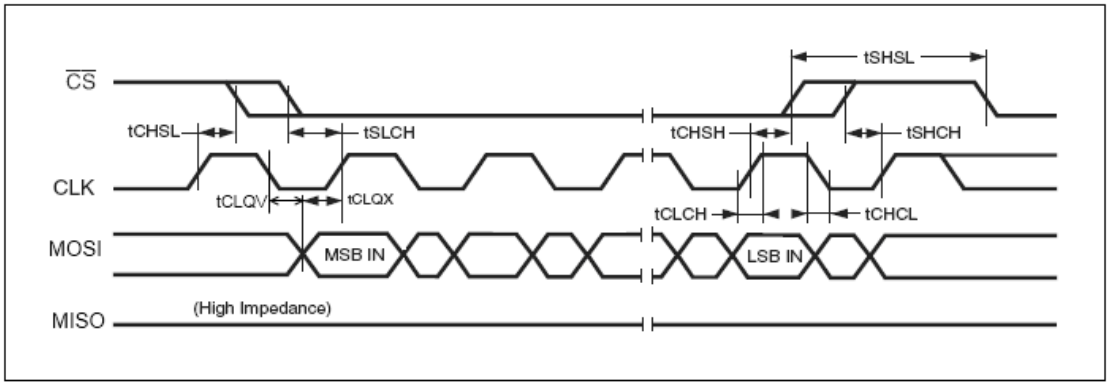


Figure 5-20. Serial Output Timing

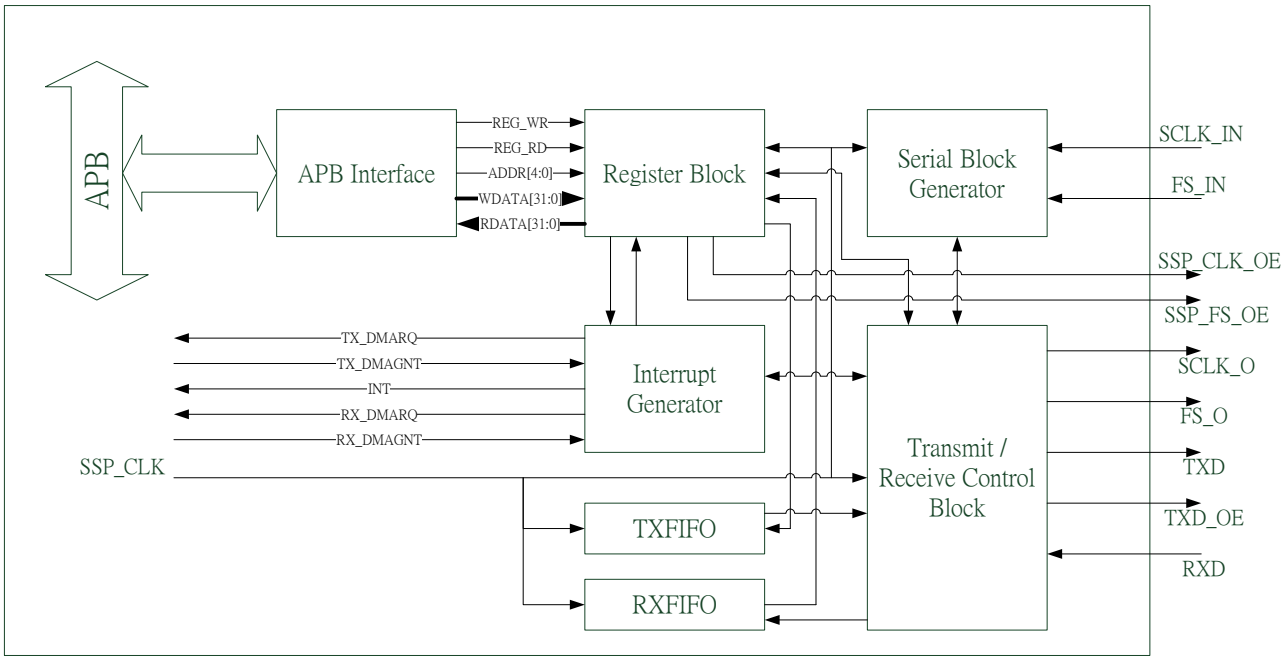
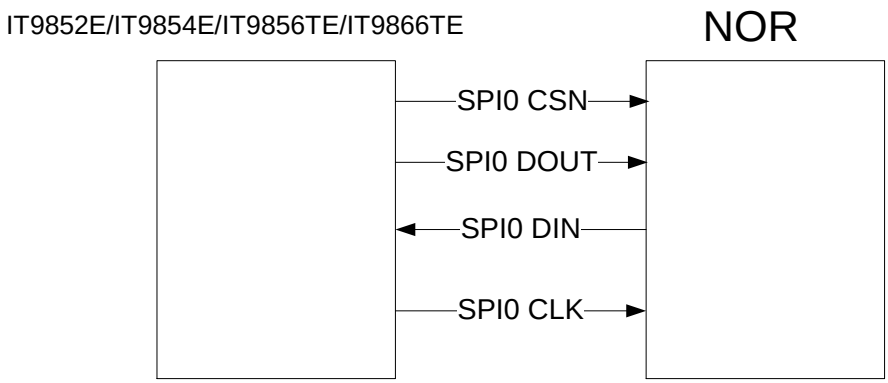


Figure 5-21. Block Diagram of NOR Interface

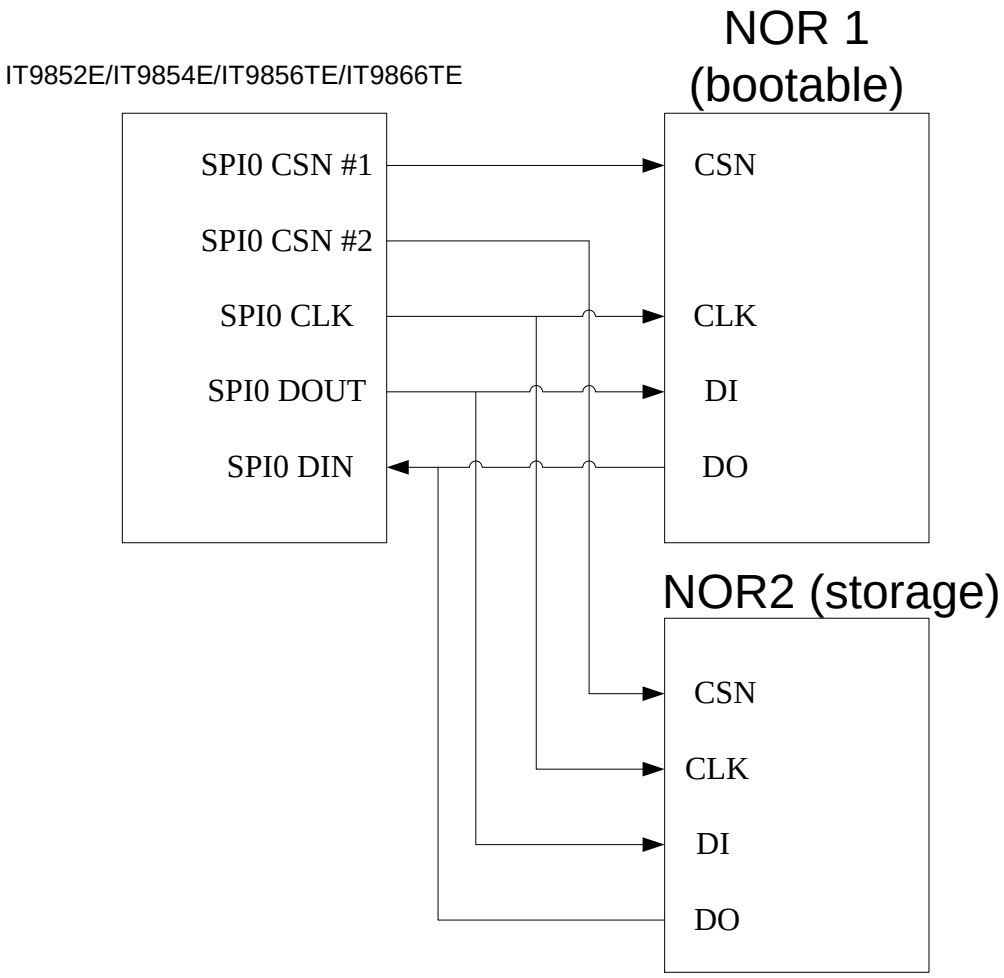
Table 5-13. Pin Share for SPI Interface

Pin Name	Mode 0	Mode 1	Mode 2	Mode 3
GPIO10	GPIO10	SPI0 CS# 2		
GPIO11	GPIO11	SPI1 CS# 2		
GPIO14	GPIO14			SPI0 CS# 1
GPIO15	GPIO15		SPI0 CS# 3	SPI1 CS# 1
GPIO16	GPIO16		SPI1 CS# 3	
GPIO18	GPIO18			SPI0 DIN
GPIO19	GPIO19			SPI0 DOUT
GPIO20	GPIO20			SPI0 CLK
GPIO29	GPIO29	SPI1 DIN		
GPIO30	GPIO30	SPI1 DOUT		
GPIO31	GPIO31	SPI1 CLK		
GPIO37	GPIO37		SPI0 CS# 4	
GPIO38	GPIO38		SPI1 CS# 4	
GPIO82	GPIO82	SPI0 CLK	SPI1 CLK	
GPIO83	GPIO83	SPI0 DIN	SPI1 DIN	
GPIO84	GPIO84	SPI0 DOUT	SPI1 DOUT	
GPIO85	GPIO85	SPI0 CS# 5	SPI1 CS# 5	

For the NOR booting, it only can connect GPIO14, GPIO18, GPIO19, and GPIO20 to the NOR device. The other pins are storage devices, which have no booting capability.



Hereunder is multi-chips connection to support two NORs. NOR1 is for the boot device while NOR2 is for the storage device.



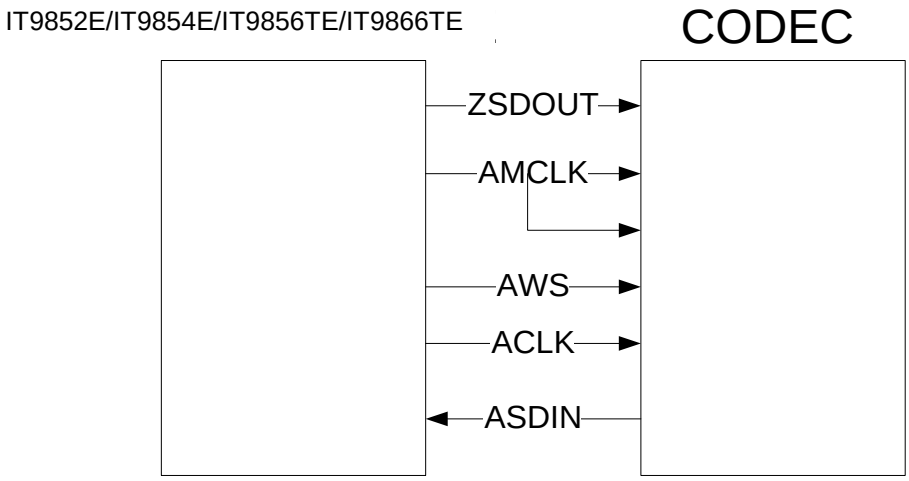
5.5 Digital Audio Interface

5.5.1 General Description

IT9852E/IT9854E/IT9856TE/IT9866TE features a standard audio interface to support the transmission of mono or stereo data to and from the DAC or ADC. The standard audio IT9852E/IT9854E /IT9856TE supports two data formats. One is standard IIS data format and the other is left justified data format. IT9852E/IT9854E /IT9856TE audio interface may be configured as either master or slave. As a master interface mode, IT9852E/IT9854E /IT9856TE/IT9866TE generates the ACLK (ZCLK) and AWS (ZWS) and controls sequencing of the data transfer. In the slave mode, DAC or ADC generates the ACLK (ZCLK) and AWS (ZWS) and controls the sequencing of data transfer.

5.5.2 Digital Audio Interface Implementation

The audio interface in IT9852E/IT9854E/IT9856TE/IT9866TE has seven pins to support all the application implementation. The IT9852E/IT9854E/IT9856TE/IT9866TE can connect one DAC and one ADC. IT9852E/IT9854E/IT9856TE/IT9866TE can be connected to CODAC as well, which depends on the application's purpose. There are three kinds of interface implementations, all of which can be configured as either master or slave mode.



5.5.3 Audio Interface Data Formats

IT9852E/IT9854E/IT9856TE/IT9866TE supports IIS and left justified audio interface data formats.

In IIS mode, The MSB is available on the second rising edge of ACLK following the AWS transition. The other bits up to LSB are then transmitted in order. The figure below illustrates the IIS interface.

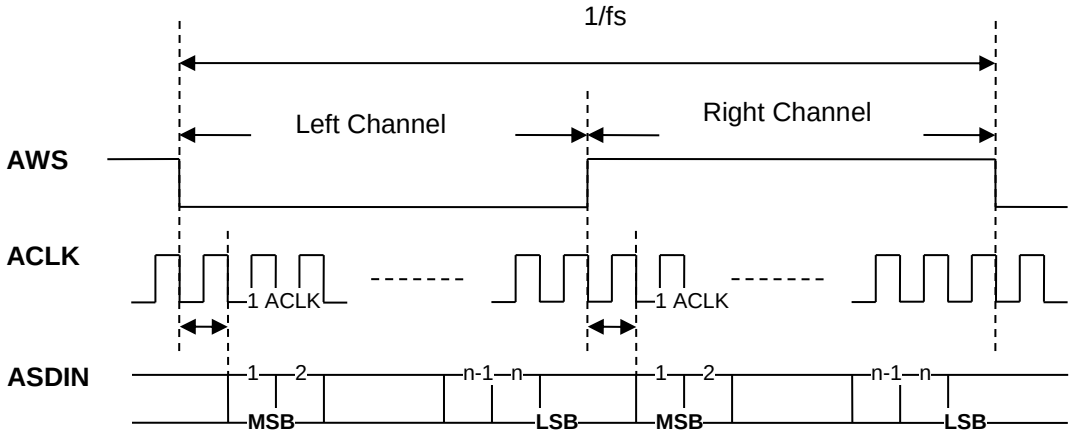


Figure 5-22. IIS Audio Interface

In Left justified mode, The MSB is available on the first rising edge of ACLK following the AWS transition. The other bits up to LSB are then transmitted in order. The figure below illustrates the IIS interface.

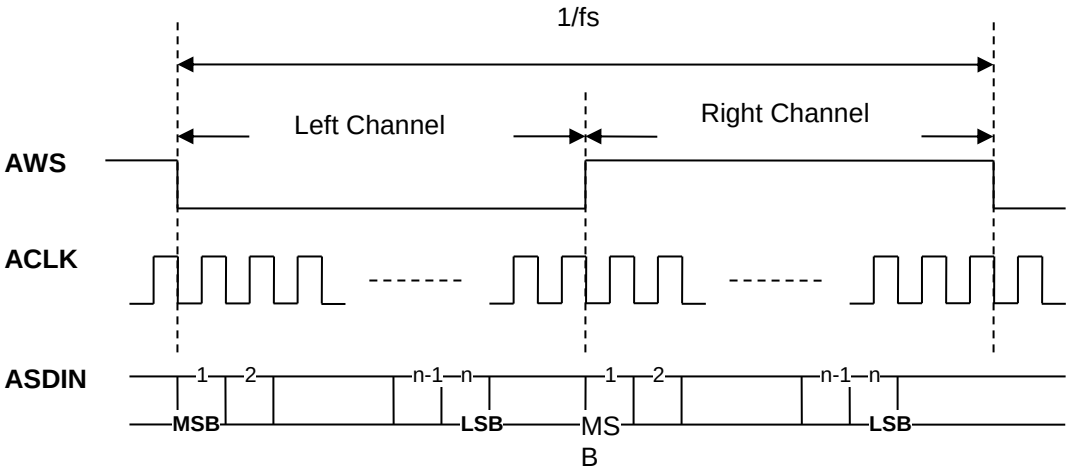


Figure 5-23. MSB Left Justified Interface

Table 5-14. Pin Share for IIS Interface

Pin Name	Mode 0	Mode 1	Mode 2	Mode 3
GPIO5	GPIO5		IIS ZDO	
GPIO6	GPIO6		IIS ZDI	
GPIO7	GPIO7		IIS AMCLK	
GPIO9	GPIO9		IIS ZWS	
GPIO10	GPIO10		IIS ZCLK	
GPIO11	GPIO11		IIS AMCLK	
GPIO12	GPIO12		IIS ZDI	
GPIO13	GPIO13		IIS ZDO	
GPIO32	GPIO32	IIS AMCLK		
GPIO33	GPIO33	IIS ZWS		
GPIO34	GPIO34	IIS ZDO		
GPIO35	GPIO35	IIS ZCLK		
GPIO36	GPIO36	IIS ZDI		

5.6 UART and IrDA Interface

The UART and IrDA controller is a serial communication element that implements the most common infrared communication protocols. In addition to the infrared modes, the device also provides a UART mode of operation that is backward compatible to 16550 to support the existing communication software. It provides the following features:

- Firmware compatible with the high-speed NS 16C550A UART
- IrDA 1.3 SIR with up to 115.2 kbps data rate
- SIR pulse width programmable as 1.6 µs or 3/16 of the baud-rate pulse width
- Supports IrDA 1.3 FIR
- Multi-frame transmission and reception in FIR mode
- Back-to-back infrared frame transmission and reception in FIR mode
- 32-bit IEEE 802 CRC32 hardware CRC generators and checkers for FIR communications
- Break, parity, overrun, and framing error simulations in UART mode
- CRC error and physical error simulation in FIR mode

5.7 DMA Controller

IT9852E/IT9854E/IT9856TE/IT9866TE Direct Memory Access Controller is designed to enhance system performance and reduce processor-interrupt generation. System efficiency is improved by employing high-speed data transfer between the system and device. The DMA controller provides 8 channels for memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfer with a shared buffer. Here is the main feature:

- An AHB slave port for DMA controller configuration
- 2 AHB master interfaces for data transfer
- 8 configurable DMA channels
- Supports chain transfer
- Memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfers
- Group round-robin arbitration scheme with 4 priority levels
- Supports 8-, 16-, and 32-bit wide data transaction
- Supports big-endian and little-endian

5.8 Ethernet MAC Interface

The IT9852E/IT9854E/IT9856TE/IT9866TE provides a high-quality 10/100 Ethernet controller with DMA function. It includes an AHB wrapper, DMA engine, on-chip memories (TX FIFO and RX FIFO), MAC, and RMII interface. It is an Ethernet controller that provides AHB master capability and is fully compliant with the IEEE 802.3 100 Mbps and 10 Mbps specifications. The MAC DMA controller handles all data transfers between system memory and on-chip memories. The DMA engine supports the zero-copy data transfer that drastically improves the system performance. The DMA engine can be used to reduce the CPU loading, maximize the performance, and minimize the FIFO size. It has on-chip memories for buffering, which requires no external local buffer memory. The RMII interface can support two specific data rates, 10 Mbps and 100 Mbps. The functionality is identical at both data rates, and so is the signal timing relationship. The only difference between the 10 Mbps and 100 Mbps operations is the nominal clock frequency.

Table 5-15. Pin share for Ethernet MAC Interface

Pin Name	Mode 0	Mode 1	Mode 2	Mode 3
GPIO27	GPIO27			REFCLK
GPIO28	GPIO28			TXEN
GPIO29	GPIO29			TXD1
GPIO30	GPIO30			TXD0
GPIO31	GPIO31			RXD1
GPIO32	GPIO32			RXD0
GPIO33	GPIO33			RX_CRS_DV
GPIO34	GPIO34			MDIO
GPIO35	GPIO35			MDC
GPIO36	GPIO36			RX_ER
GPIO37	GPIO37			REF_25MHZ
GPIO38	GPIO38			REF_25MHZ
GPIO39	GPIO39			TXEN
GPIO40	GPIO40			TXD1
GPIO41	GPIO41			TXD0
GPIO42	GPIO42			REFCLK
GPIO43	GPIO43			RXD1
GPIO44	GPIO44			RXD0
GPIO45	GPIO45			RX_CRS_DV
GPIO90	GPIO90			TXEN
GPIO91	GPIO91			TXD1
GPIO92	GPIO92			TXD0
GPIO93	GPIO93			REFCLK
GPIO94	GPIO94			RXD1
GPIO95	GPIO95			RXD0
GPIO96	GPIO96			RX_CRS_DV

5.9 PLL Interface

IT9852E/IT9854E/IT9856TE/IT9866TE has three clock synthesizers to generate all of the internal clocks. The clock synthesizer can generate wide range of programmable frequencies up to 400MHz. The clock synthesizer accepts 12 MHz or 30MHz reference clock input. Moreover, system can even stop the reference clock after the PLL locks the target frequency and phase for power saving.

5.10 2D Graphice Engine

The 2D Graphics Accelerator supports the following functions:

- Bit Block Transfer (BitBlt) with ROP3 operation
- Supports mask plane with 1bpp, 2bpp, 4bpp, and 8bpp format
- Supports color expansion with 1bpp, 2bpp, 4bpp and 8bpp format
- Constant/Variable global alpha blending
- Coordinate transform
- Gradient (horizontal / vertical) fill with dithering / solid color fill
- Clipping window
- Supports following color formats
  - 32-bit ARGB8888, ABGR8888, RGBA8888, BGRA8888,
  - 16-bit ARGB4444, ABGR4444, RGBA4444, BGRA4444, ARGB1555, ABGR1555, RGBA1555, BGRA1555
  - 16-bit RGB565, BGR565
  - Alpha A_8, A_4, A_2, and 1-bit black and white BW_1
- Color depth conversion from any to any RGB format with dithering
- Supports interrupt output
- 64-bit memory interface with maximum 4-pixel pipelined engine
- Up to 4096x4096 pixels display resolution
- Automatic clock gating

5.11 JPEG

The IT9852E/IT9854E/IT9856TE/IT9866TE JPEG codec is based on the JPEG baseline standard and the arithmetic accuracy satisfies the requirement of the compatibility test of JPEG Part-2 (ISO/IEC10918-2). The maximum image size is 256M pixels (16376x16376). The parameters of luminance and chrominance quantization table are fully programmable. The Huffman tables is the default ones suggested by the specification. The decoding process supports YUV 4:4:4, 4:2:2, 4:1:1 and 4:2:0 with the interleaved format, but the encoding process only supports the YUV 4:2:2 interleaved formats. The progressive mode is not supported, but sequential mode. The following diagram shows the definition of each formation.

5.12 Video

Supports H.264 decode on high/main profile level 3.1. It real time decodes for 720p@30fps (1280x720).

5.13 General-Purpose I/O

The GPIO controller is a user programmable general-purpose I/O controller. It is used to input/output data from the system and device. Each GPIO can be programmed as the input or output and pulled high or pulled low.

This GPIO can also be an interrupt input. It supports the rising edge, falling edge, both edge, and high/low level interrupt sense types. Each port can choose the pre-scale APB clock source as an interrupt source.

All the inputs are set to input upon the hardware reset.

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6. DC Characteristics

Absolute Maximum Ratings*

Core Power (VDD_CORE).....-0.3V to 2.0V

IO Power (VDD_IO) ..... -0.3V to 4.0V

Input Voltage (Vi)..... -0.3V to VDD_IO + 10%

Output Voltage (Vo)..... -0.3V to VDD_IO + 10%

Operation Temperature (Topt) ..... -25°C to +85°C

Storage Temperature ..... -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Normal Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD_CORE	Core Power (IVDD) – CPU < 380MHz	1.1	1.2	1.3	V
	Core Power (IVDD) – CPU ≥ 380MHz	1.2	1.3	1.4	V
VDD_MEM	DDR2 Memory Power – CPU < 380MHz	1.7	1.8	1.9	V
	DDR2 Memory Power – CPU ≥ 380MHz	1.8	1.9	2.0	V
VDD_IOA VDD_IOB	I/O Power	3.0	3.3	3.6	V
VDD_RTC	RTC Power	2.0	3.3	3.6	V
VDD_DLL	DDR2 DLL Power	1.1	1.2	1.3	V
VDD_PLL	OSC Power	1.1	1.2	1.3	V
VDD_USB	USB Power	2.0	3.3	3.6	V
-	Operating Temperature	-25	-	+85	^{0}C

DC Electrical Characteristics

Symbol	Parameter	Condition.	Min.	Max.	Unit
V_{OL}	Output low voltage	Refer to I_{OL}	GND	GND+0.4	V
V_{OH}	Output high voltage	Refer to I_{OH}	VDD_IO-0.4	VDD_IO	V
I_{OH_S}	Output high current (with maximum driving strength)	VDD_IO = 3.3V V_{OH}= 2.9V	3.03	5.58	mA
I_{OL_S}	Output low current (with maximum driving strength)	VDD_IO = 3.3V V_{OL}= 0.4V	3.60	5.59	mA
I_{OH_W}	Output high current (with minimum driving strength)	VDD_IO = 3.3V V_{OH}= 2.9V	1.20	2.23	mA
I_{OL_W}	Output Low Current (with minimum driving strength)	VDD_IO = 3.3V V_{OL}= 0.4V	1.44	2.23	mA
I_{OZ}	Tri-state Leakage Current	-	-	± 10	uA
V_{IL}	Input Low Voltage	VDD_IO=3.3V	-	1.35	V
V_{IH}	Input High Voltage	VDD_IO=3.3V	1.95	-	V
I_{IN}	Input Leakage Current	-	-	± 10	uA

C_{IN}	Input Capacitance	-	-	3	pF

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7. AC Characteristics

7.1 Reset Timing

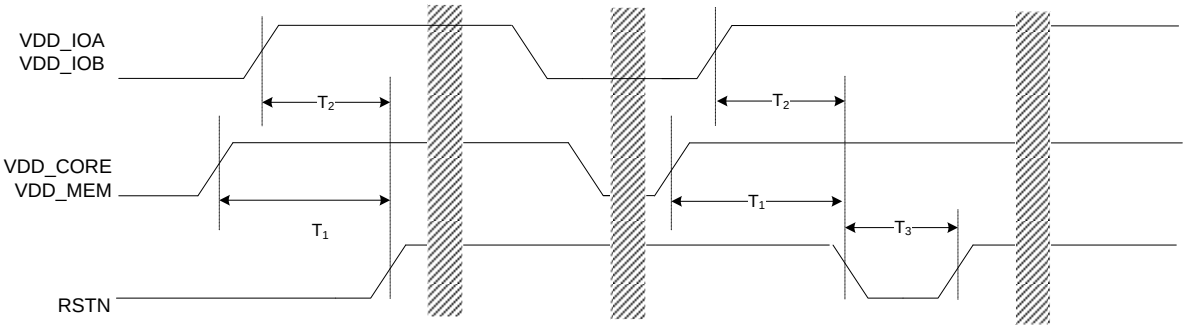

Figure 7-1. Reset Timing

Table 7-1. Reset Timing Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_1	Core Power (memory power) valid to reset inactive	-	50	-	ms
T_2	I/O Power valid to reset inactive	-	40	-	ms
T_3	Minimum reset pulse width	1	-	-	ms

Notes: The registers can be accessed 4 ms after the reset process is finished.

7.2 Power Sequence

Specific sequencing requirements shall be followed for all I/O power and core power.

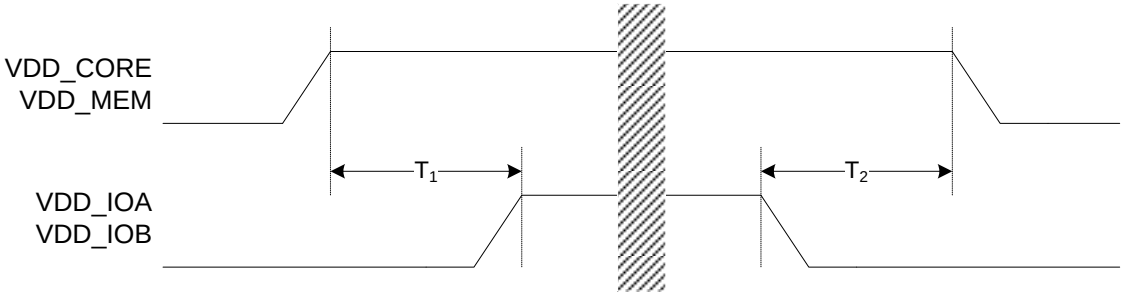

Figure 7-2. Power Sequence Timing

Table 7-2. Power Sequence Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_1	Core power (memory power) valid to I/O power valid	10	-	-	us
T_2	I/O power invalid to core power (memory power) invalid	10	-	-	us

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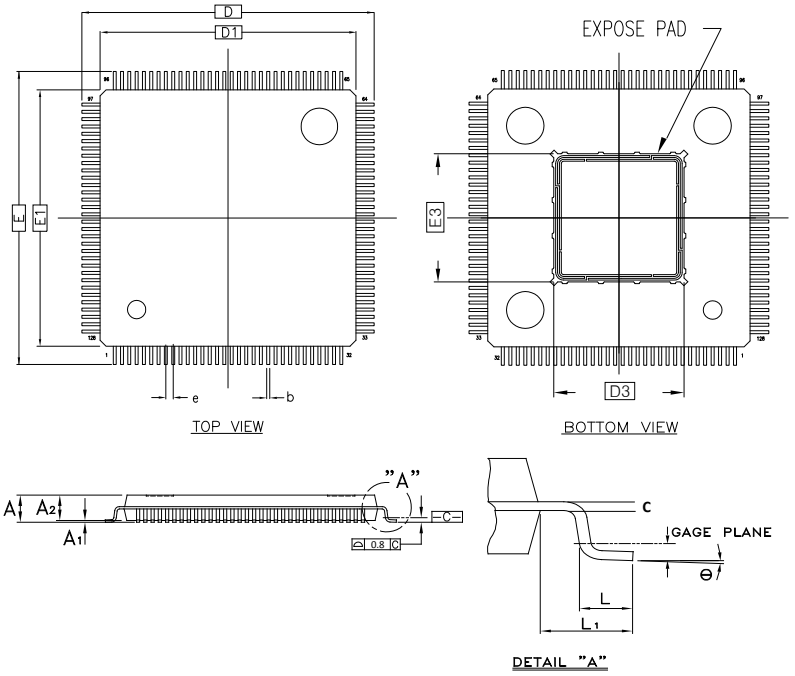
8. Package Information

8.1 IT9852E/IT9854E Package Information

LQFP 128(14*14) Outline Dimensions unit: inches/mm



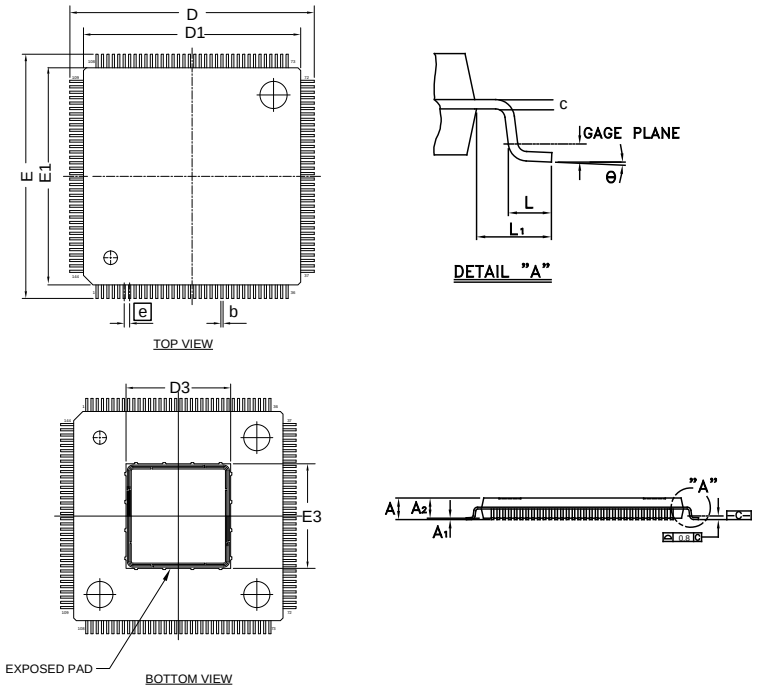
Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.063	-	-	1.60
A1	0.002	-	0.006	0.05	-	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.005	0.006	0.009	0.13	0.16	0.23
c	0.004	-	0.008	0.09	-	0.20
D / E	0.630 BSC			16.00 BSC		
D_1 / E_1	0.551 BSC			14.00 BSC		
D_3 / E_3	0.270	0.274	0.278	6.86	6.96	7.06
e	0.016 BSC			0.40 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	0.039 REF.			1.0 REF.		
θ	0°	-	7°	0°	-	7°

Notes:
1. Dimensions D1 and E1 do not include mold protrusion, but mold mismatch is included.
2. Dimensions b does not include dambar protrusion.
3. Controlling dimensions: Millimeter

DI-E(274*274MIL)-LQFP128(14*14)v0

8.2 IT9856TE/IT9866TE Package Information

TQFP 144(16*16) Outline Dimensions **unit: inches/mm**



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.047	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.005	0.006	0.009	0.13	0.16	0.23
c	0.004	-	0.008	0.09	-	0.20
D/E	0.709 BSC			18.00 BSC		
D_1/E_1	0.630 BSC			16.00 BSC		
D_3/ E_3	0.315 BSC			8.00 BSC		
e	0.016 BSC			0.40 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	0.039 REF.			1.0 REF.		
θ	0°	-	7°	0°	-	7°

Notes:
4. Dimensions D1 and E1 do not include mold protrusion. But mold mismatch is included.
5. Dimensions b does not include dambar protrusion.
6. Controlling dimensions: Millimeter

DI-E(315*315MIL)-TQFP144(16*16)v0

9. Ordering Information

Part Number	Description	Package	Body Size
IT9852E	Smart control and display SoC for networked home appliance	128 pins LQFP/EPAD	14*14 mm
IT9854E	Smart control and display SoC with H.264 decoder for networked home appliance	128 pins LQFP/EPAD	14*14 mm
IT9856TE	HD media SoC with H.264 decoder for video door phone appliance	144 pins TQFP/EPAD	16*16 mm
IT9866TE	HD media SoC with H.264 decoder for Biometrics Application	144 pins TQFP/EPAD	16*16 mm

All green components provided are in compliance with RoHS, and Halogen-Free.

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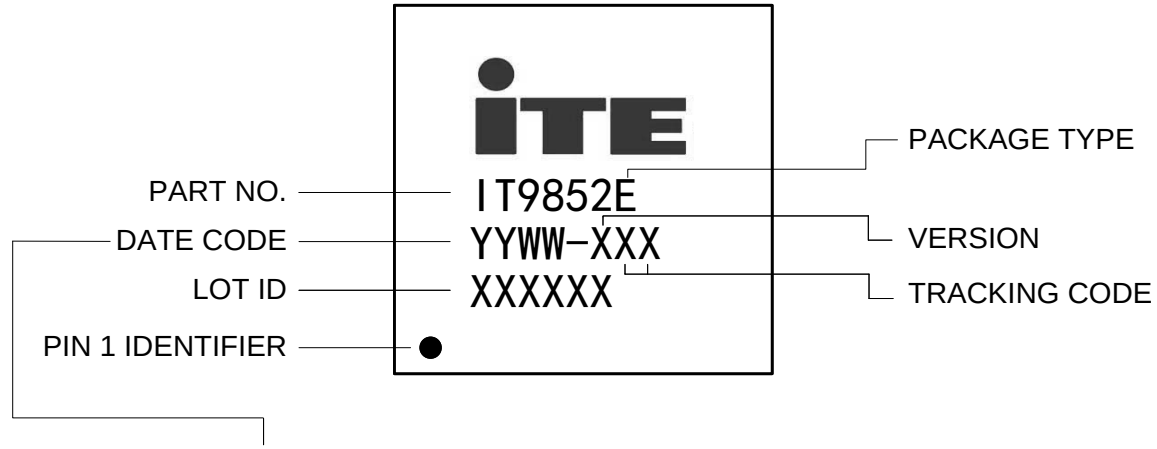
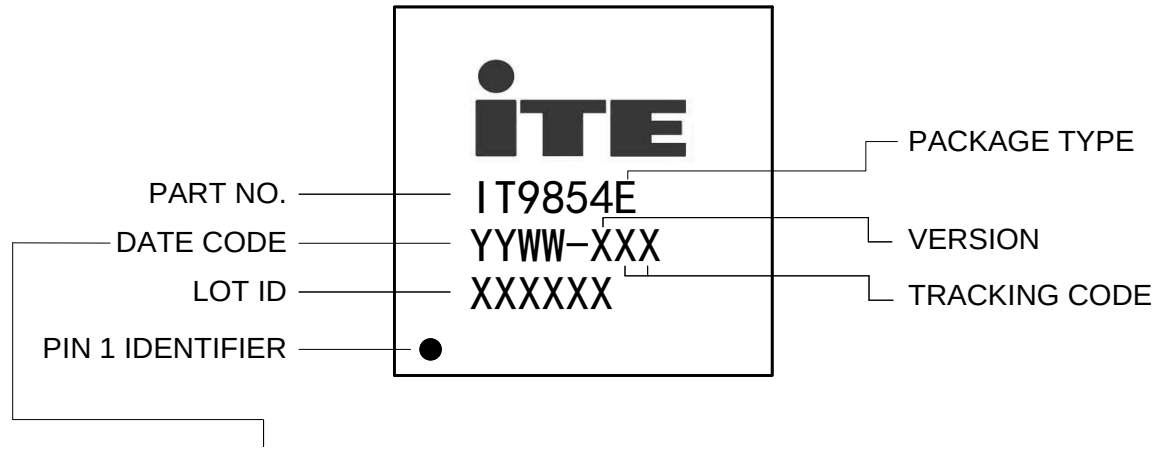
10. Top Marking Information

IT9852E



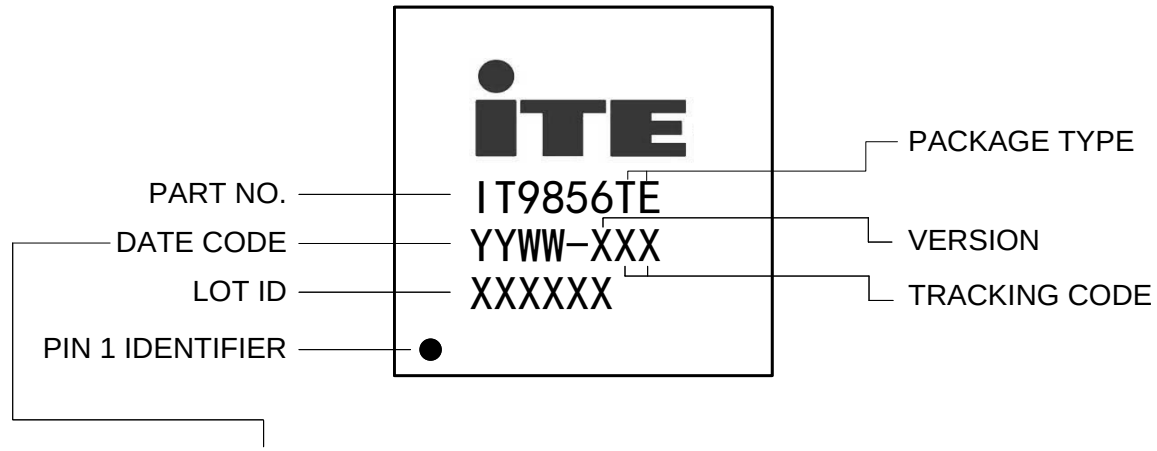
(YY: Year WW: Week)
e.g. YYWW = 1507 → The seventh week of the year 2015

IT9854E



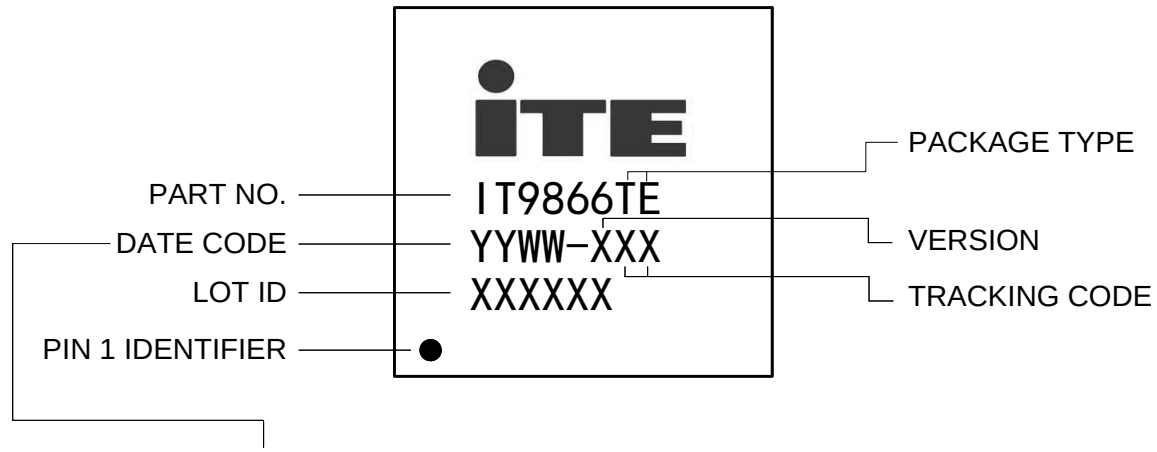
(YY: Year WW: Week)
e.g. YYWW = 1507 → The seventh week of the year 2015

IT9856TE



(YY: Year WW: Week)
e.g. YYWW = 1507 → The seventh week of the year 2015

IT9866TE



(YY: Year WW: Week)
e.g. YYWW = 1507 → The seventh week of the year 2015

ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2013)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc.

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Otherwise specified in the order agreed by Seller, delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.
(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.
(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and by its conditions Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.
(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.
(c) Buyer will not return any goods without first obtaining a customer return order number.
(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.
(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.