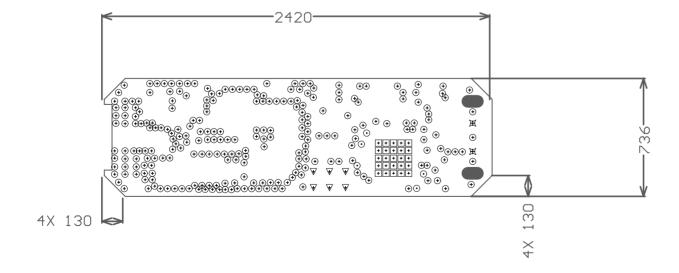
	Symbol	Hit	Count	Tool	Size	Physical	Length	Rout	Path	Length	Plated	Hole Typ	e e
		25		12.99	2mil (0.33mm)						PTH	Round	
	0	254		15mil	(O.381mm)	1					PTH	Round	
	∇	6		35.43	3mil (0.9mm)	1					PTH	Round	
	Ħ	2		59.05	5mil (1.5mm)	1					NPTH	Round	
	*	2		39.37	mil (1mm)	98.425mil	(2.5mm)	59.05	5mil (1	(.5mm)	PTH	Slot	
1		200	T-4-1										

289 Total

Slot definitions: Rout Path Length = Calculated from tool start centre position to tool end centre position.

Physical Length = Rout Path Length + Tool Size = Slot length as defined in the PCB layout



Layer Name	Gerber Document	Copper Thickness	Dielectric Height	Dielectric Material	Dielectric Constant	Dielectric Type
Top Solder Mask	(.GTS)		O.4mil	Solder Resist	3.50	
Top Layer	(.GTL)	1.4mil				
0 1 -1	(OD()	4 4	20mil	FR-4 High Tg	4.80	Core
Ground plane	(.GP1)	1.4 mil	16mil	FR-4 High Tg	4.80	PrePreg
Power plane	(.GP2)	1.4 mil				
			20mil	FR-4 High Tg	4.80	Core
Bottom Layer	(.GBL)	1.4mil				
Bottom Solder Mask	(.GBS)		O.4mil	Solder Resist	3,50	

NOTES: UNLESS OTHERWISE SPECIFIED

- 1. PRINTED CIRCUIT BOARD SHALL BE FABRICATED TO THE MOST RECENT REVISION OF IPC-6011 AND IPC-6012, CLASS 2.
- 2. BOARD MATERIAL:
- 2.1 SHALL BE CONSTRUCTED AS SPECIFIED IN STACKUP
- 3. FINISH:

 - 3.1 BOARD FINISH SHALL BE ROHS-COMPLIANT HASL ON BOTH SIDES.
 3.2 SOLDER MASK TO BE LIQUID PHOTO IMAGEABLE MATTE FINISH,
 BOTH SIDES OF BOARD, COLOR GREEN, CLASS T, PER IPC-SM-840
 - 3.3 ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF .001 COPPER PLATING.
 3.4 ALL HOLE SIZES ARE FINISHED SIZE, TOLERANCE TO BE +/- .003
- 3.5 VIAS SHALL BE TENTED AS INDICATED IN SOLDER MASK LAYERS GERBER DATA
- 4. FABRICATION TOLERANCES:
 - 4.1 WARP AND TWIST SHALL NOT EXCEED 0.75% AS MEASURED PER IPC-TM-650 2.4.22.
 4.2 CONDUCTOR WIDTH AND SPACING SHALL CONFORM SUPPLIED GERBER DATA.
 4.3 LAYER TO LAYER REGISTRATION SHALL BE WITHIN .002. POSITION.
- 4.5 MINIMUM ANNULAR RING TO BE .005 EXTERNAL LAYERS , .003 INTERNAL LAYERS.
- 5.1 SILKSCREEN WITH PERMANENT NON CONDUCTIVE WHITE EPOXY
- BASED INK. THERE SHALL BE NO MARKINGS ON ANY SOLDERABLE COMPONENT LANDS.
- 6. DIMENSIONS ARE IN MILS

Open ADSB P	roject	www.openadsb.com Sunnyvale, CA USA					
TITLE FAB DRAWING							
APPROVALS DATE					.1.		
DWN B Kuschak	04/14/12	OpenADSB USB Stick					
CKD		SIZE	DWG NO.	REV	SHEET		
APVR		Α		Α	1 OF 1		