

# TSM36CA Bidirectional Surge Protection Device in SOT-23

## 1 Features

- IEC 61000-4-2 ESD protection:
  - $\pm 30\text{kV}$  contact discharge
  - $\pm 30\text{kV}$  air gap discharge
- IEC61000-4-5 surge protection:
  - 20A (8/20 $\mu\text{s}$ )
  - Clamping voltage: 55V at 20A (8/20 $\mu\text{s}$ )
- IO capacitance: 15pF (typical)
- Low leakage current of 100nA (maximum)
- Industrial temperature range:  $-55^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$
- SOT-23 (DBZ) leaded package to minimize board space and allow for automatic optical inspection (AOI)

## 2 Applications

- Industrial sensors
- 4/20mA loops
- [Lighting](#)
- [Field transmitter & sensor](#)

## 3 Description

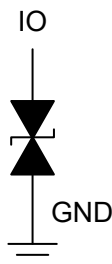
The TSM36CA is a 36V, bidirectional TVS protection diode designed for clamping harmful transients such as ESD and surge. The TSM36CA robustly shunts up to 20A of IEC 61000-4-5 fault current to protect systems from high power transients or lightning strikes. The TSM36CA device is rated to dissipate ESD strikes up to  $\pm 30\text{kV}$  (contact and air gap discharge) which exceeds the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

Additionally, the TSM36CA is available in a small leaded SOT-23 (DBZ) package which is reduced in size by approximately 50 percent compared to the industry standard SMA package. The extremely low device leakage and capacitance ensures a minimal effect on the protected line.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE
TSM36CA	DBZ (SOT-23, 3)	2.92mm $\times$ 2.37mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



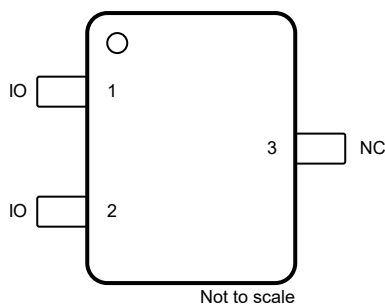
Functional Block Diagram



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## 4 Pin Configuration and Functions



**Figure 4-1. DBZ Package,  
3-Pin SOT-23  
(Top View)**

**Table 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
IO	1,2	I/O	Surge and ESD protected IO. Connect other pin to ground.
NC	3	NC	Leave this pin floating for proper performance.

(1) I = Input, O = Output, I/O = Input or Output, NC = No connect

## 5 Specifications

### 5.1 Absolute Maximum Ratings

T<sub>A</sub> = 25°C (unless otherwise noted) <sup>(1)</sup>

Parameter		MIN	MAX	UNIT
P <sub>PPM</sub>	IEC 61000-4-5 Power (t <sub>p</sub> - 8/20 μs) Peak Pulse Power at 25°C		1400	W
I <sub>PPM</sub>	IEC 61000-4-5 Current (t <sub>p</sub> - 8/20 μs) Peak Pulse Current at 25°C		20	A
T <sub>A</sub>	Operating free-air temperature	-55	150	°C
T <sub>stg</sub>	Storage temperature	-65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 5.2 ESD Ratings—JEDEC Specification

Parameter			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002	± 1000	

### 5.3 ESD Ratings—IEC Specification

T<sub>A</sub> = 25°C (unless otherwise noted)

Parameter			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	±30000	

## 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input voltage	–36		36	V
T <sub>A</sub>	Operating free-air temperature	–55		150	°C

## 5.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TSM36CA	UNIT
		DBZ (SOT-23)	
		3 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	204.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	96.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	39.9	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	7.1	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	39.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.6 Electrical Characteristics

T<sub>A</sub> = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>RWM</sub>	Reverse stand-off voltage		–36		36	V
V <sub>BR</sub>	Breakdown voltage <sup>(1)</sup>	I <sub>IO</sub> = 10 mA, IO to GND and GND to IO	37.8		44.2	V
V <sub>CLAMP</sub>	Surge clamping voltage, t <sub>p</sub> = 8/20 μs <sup>(2)</sup>	I <sub>PP</sub> = 10A, IO to GND		47	58	V
		I <sub>PP</sub> = 20A, IO to GND		55	71	
I <sub>LEAK</sub>	Leakage current	V <sub>IO</sub> = +36 V		25	100	nA
R <sub>DYN</sub>	Dynamic resistance	t <sub>p</sub> = 8/20 μs, from IO to GND		1.0		Ω
C <sub>LINE</sub>	Line capacitance	V <sub>IO</sub> = 0 V, f = 1 MHz, V <sub>p-p</sub> = 30 mV		15	20	pF

(1) V<sub>BR</sub> is defined as the voltage when ±10 mA is applied in the positive-going direction.

(2) Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

## 5.7 Typical Characteristics

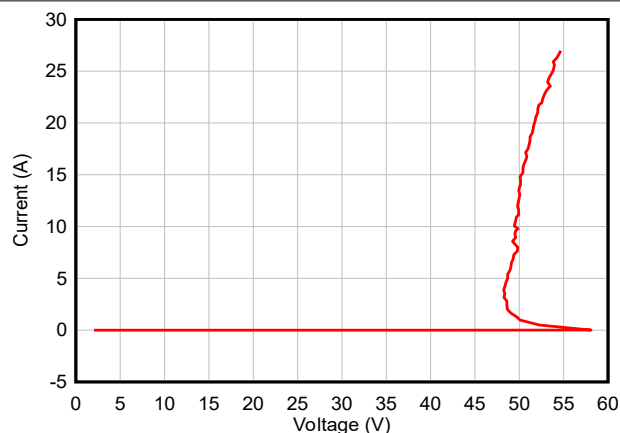


Figure 5-1. Positive TLP Curve

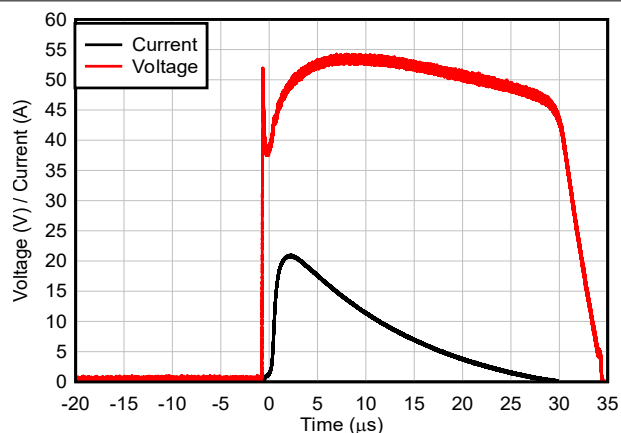


Figure 5-2. 8/20 $\mu$ s Surge Response

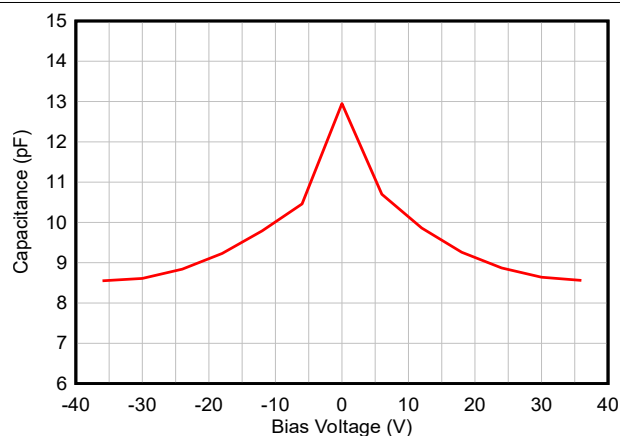


Figure 5-3. Capacitance vs Bias Voltage

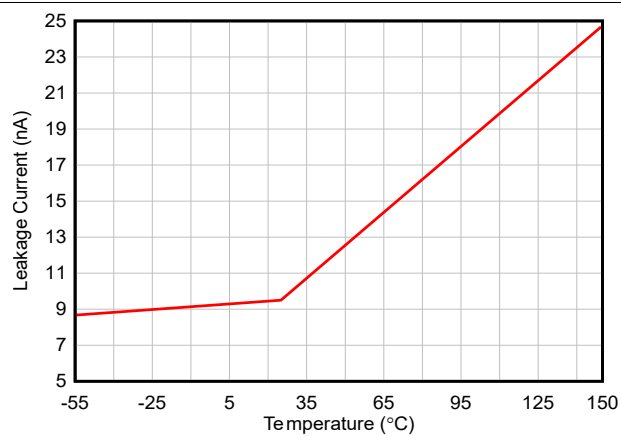


Figure 5-4. Leakage Current vs Temperature

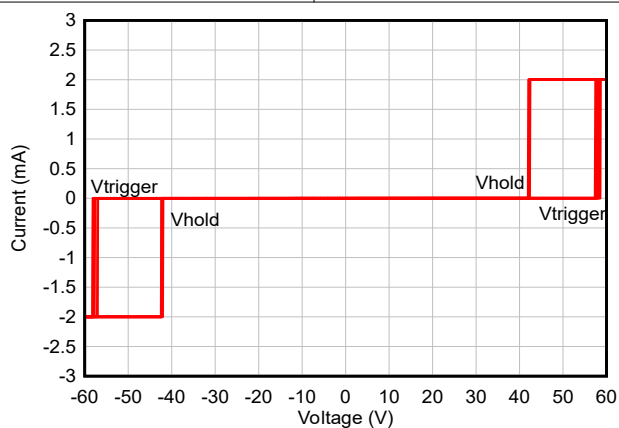


Figure 5-5. DC Voltage Sweep I-V Curve

## 6 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 6.1 Application Information

TSM36CA is a diode type TVS that provides a path to ground for dissipating transient voltage spikes, such as ESD or surge, on signal lines and power lines. Connect the device in parallel to the down stream circuitry for protection. As the current from the transient passes through the device, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low  $R_{DYN}$  of the triggered TVS holds this voltage ( $V_{CLAMP}$ ) to a safe level for the protected IC. For more information on how to properly use this device, refer to the [ESD Packaging and Layout Guide](#) for details.

One common example of implementing TSM36CA is to protect both sides of a PLC module and a sensor transmitter, as shown in the figure below.

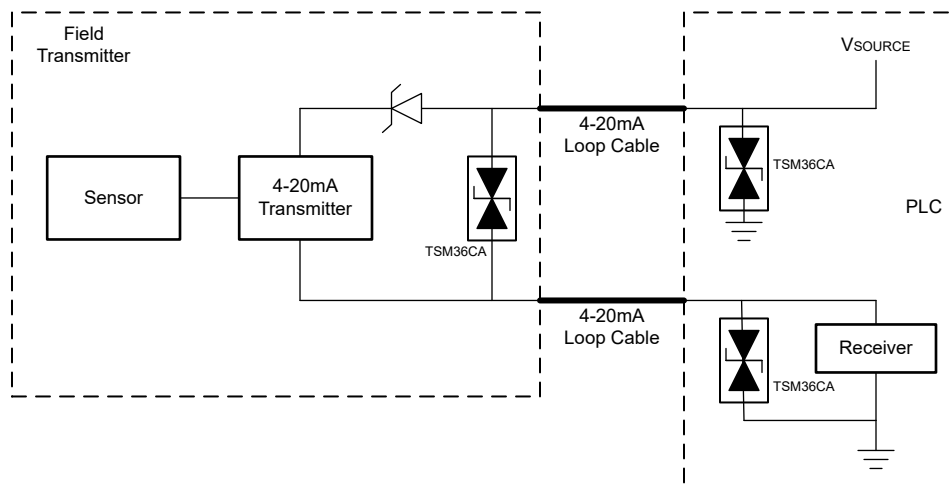


Figure 6-1. Typical Application Diagram

## 7 Device and Documentation Support

### 7.1 Documentation Support

#### 7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [TI's IEC 61000-4-x Testing application note](#)
- Texas Instruments, [ESD Layout Guide user's guide](#)
- Texas Instruments, [ESD Protection Diodes EVM user's guide](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Reading and Understanding an ESD Protection Data Sheet user's guide](#)

### 7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 7.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 7.4 Trademarks

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## 7.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2024	*	Initial Release

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TSM36CADBZR</a>	Active	Production	SOT-23 (DBZ)   3	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 150	(3IIG, 3LC8)
TSM36CADBZR.Z	Active	Production	SOT-23 (DBZ)   3	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	(3IIG, 3LC8)

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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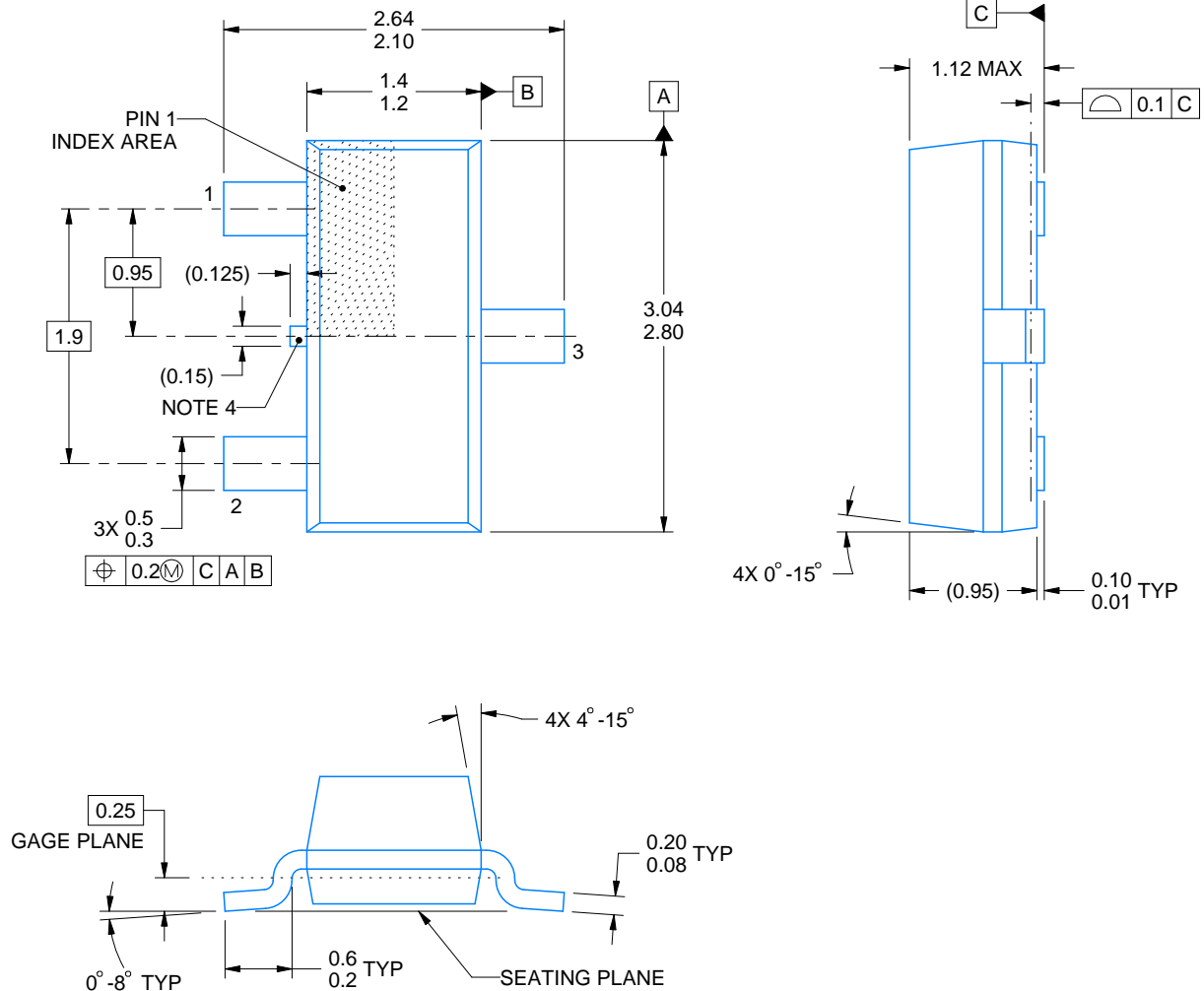
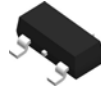
### OTHER QUALIFIED VERSIONS OF TSM36CA :

- Automotive : [TSM36CA-Q1](#)



NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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## NOTES:

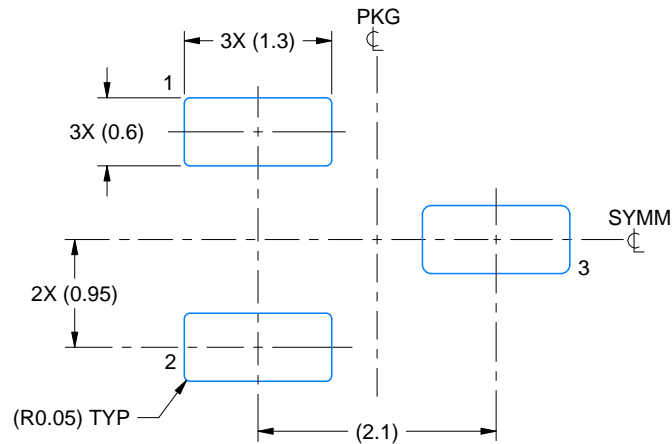
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side.

# EXAMPLE BOARD LAYOUT

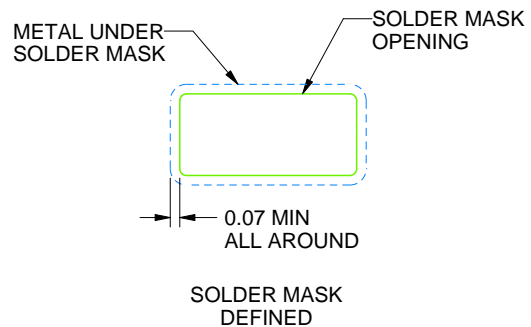
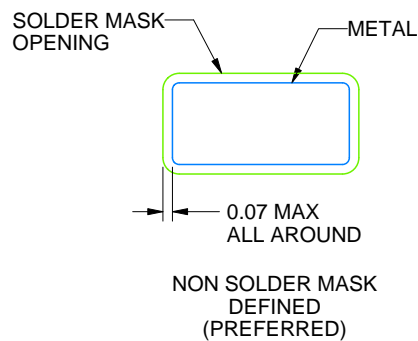
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

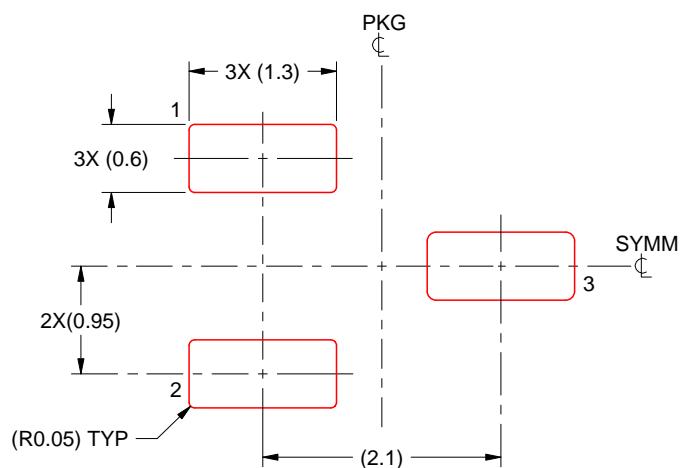
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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