MANCHESTER 1824
The University of Manchester

Research Proposal

Validation of Data-Driven Circuit Simulation Framework for Power Electronics: A Case Study Using Instantaneous Dynamic Phasor Analysis

Name: Doyun Gu
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1. Executive Summary

This research project aims to validate a data-driven circuit simulation framework by faithfully reproducing experimentally verified results from published power electronics research. Using the RLC resonant circuit with full-bridge inverter from Rim et al. (IEEE TPEL 2025) as a benchmark, we will investigate the accurate simulation of switching dynamics in phasor-domain representation.

The key contribution is addressing the challenge of simulating switching events in RLC circuits using instantaneous dynamic phasor methods, which currently produces anomalous results. By systematically investigating this issue and comparing with validated experimental data, we will establish best practices for reproducible power electronics simulation.

2. Background and Motivation

2.1 Problem Statement

Current challenges in power electronics circuit simulation include:

- **Time-varying Dynamics:** Complex behaviours (like dynamic phasors with FM signals) are difficult to model accurately.
- **Limitation of Circuit Simulation:** When there's a switching sequence in the RLC circuit, phasor representation produces unexpected or non-physical results.
- **Phasor-based Simulation Anomalies:** When switching events occur in RLC circuits, traditional phasor methods produce discontinuities or artefacts because:
  - Instantaneous switching creates high-frequency harmonics
  - Phasor transformation assumes slowly-varying envelopes
  - The real part operator Re[·] may not properly capture switching transients
  - Time-varying reactance becomes undefined or numerically unstable during switching
- **Need for Validation:** Unclear whether simulation artefacts are due to: (1) numerical implementation issues, (2) fundamental limitations of phasor representation during switching, or (3) missing physics in the model (parasitics, dead-time, etc.).
- **Reproducibility Crisis:** Published research often lacks sufficient implementation details for exact replication, making it difficult to validate simulation frameworks.

2.2 Opportunity

The paper *"General Instantaneous Dynamic Phasor"* (Rim et al., IEEE TPEL 2025) provides an ideal benchmark because it includes:

- Complete experimental setup documentation (Figure 7)
- Detailed circuit parameters (Table II)
- Both simulation (Figures 5-6) and experimental results (Figures 8-9)
- Multiple operating frequencies (580 krad/s and 650 krad/s)
- Complex time-varying dynamics (frequency modulation cases)

The paper's experimental setup includes a full-bridge inverter with actual switching behaviour, yet the reported simulation and experimental results show good agreement. This suggests that the instantaneous dynamic phasor CAN handle switching if implemented correctly. By comparing our simulation artefacts with the paper's successful implementation, we can identify what's missing in our current approach and establish best practices.

3. Research Objectives

3.1 Primary Objective

Validate a data-driven circuit simulation framework by faithfully reproducing experimentally verified results from published power electronics research without simplification, with specific focus on accurately handling switching dynamics in phasor-domain representation.

3.2 Core Research Question

Can a data-driven simulation framework accurately reproduce the dynamics of switching RLC resonant converters using instantaneous dynamic phasor representation, including during switching transients?

Specific Investigations:

1. Does the simulation artefact stem from implementation issues or fundamental phasor theory limitations?
2. Can the framework distinguish between physical switching effects, numerical artifacts, and phasor representation limitations?
3. What modifications or enhancements are needed for accurate switching representation?

3.3 Specific Objectives

1. **Faithful Reproduction**
   - Implement the RLC resonant circuit with full-bridge inverter exactly as described
   - Achieve <3% accuracy matching reported experimental results
   - Validate across multiple operating frequencies (580 krad/s and 650 krad/s)
2. **Framework Validation**
   - Demonstrate handling of time-varying reactance without approximation
   - Show multi-physics integration (switching dynamics, parasitics)
   - Verify computational efficiency vs. traditional methods
3. **Extended Analysis**
   - Perform parameter sensitivity studies
   - Analyse frequency modulation cases
   - Quantify uncertainty propagation
4. **Switching Dynamics Investigation**
   - Identify root cause of simulation artefacts during switching
   - Compare multiple switching representation methods
   - Validate against experimental waveforms during transients
   - Establish guidelines for phasor simulation of switching circuits

4. Technical Approach

4.1 Circuit Under Test

From Rim et al. (2025), implement the following circuit:

Circuit: Series RLC resonant tank with full-bridge inverter

Parameters (from Table II):

- **Inductance (L):** 100.04 µH
- **Capacitance (C):** 30.07 nF
- **Series Resistance (Rs): 3.0 Ω (includes inverter internal resistance)**
- **Load Resistance (Ro):** 2.00 kΩ
- **Operating Frequencies:** 580 krad/s and 650 krad/s

Inverter Switching Specifications:

- **Topology:** H-bridge (4 switches)
- **Switching frequency:** Equal to operating frequency
- **Dead-time:** To be determined from experimental setup (typical ~100 ns)
- **Switch model:** Ideal with finite rise/fall times

Measurement Points (matching Figure 7):

- $i_s(t)$**:** Source current
- $v_o(t)$**:** Output voltage
- $v_s(t)$**:** Input voltage

Operating Conditions:

- **Input:** Step voltage envelope (matching Figures 8-9)
- **Initial conditions:** Zero (cold start)
- **Simulation duration:** 0.2 ms (matching experimental captures)
- **Time resolution:** At least 10 points per switching period

4.2 Validation metrics

Metric	Target
Current amplitude accuracy	<3% error
Voltage amplitude accuracy	<3% error
Envelope matching	Correlation >0.95%
Transient response time	Within 10%
Steady-state ripple	<5% difference
Switching Specific Metrics	
Switching transient duration	Match within 15%
Peak overshoot during switching	<10% deviation
Harmonic content (up to 5th)	<20% difference
Absence of non-physical artefacts	Visual Inspection

Artefact Detection Criteria:

- No negative inductance/capacitance values during transients
- Energy conservation maintained (±5%) across switching events
- No oscillations faster than circuit natural frequency
- Phasor magnitude remains non-negative

4.3 Switching Dynamics Handling

Challenge: The full-bridge inverter creates discontinuous switching events that interact with the phasor transformation. Current implementation produces anomalous results that need investigation.

Approach 1: Time-Domain Switching with Phasor Post-Processing

- Model switches as ideal on/off with finite rise/fall times
- Compute instantaneous voltages/currents
- Apply phasor transformation (Eq. 1) to extract envelope
- Compare with analytical phasor equations (Eq. 37a-b)

Approach 2: Phasor-Space Switching Model

- Represent switching as time-varying source in phasor domain
- Use switching function $s(t) = \pm 1$ for bridge states
- Transform s(t) to phasor space: $\tilde{s}(t) = \sqrt{m} \cdot s(t) \cdot e^{-j\theta(t)}$
- Validate against time-domain results

Approach 3: Hybrid Method (Proposed)

- Use time-domain near switching instants (high-resolution)
- Use phasor-domain between switching events (efficient)

- Smooth transition between representations
- Validate seamless integration

Investigation Plan:

1. Implement all three approaches
2. Compare accuracy, computational cost, and artefacts
3. Identify source of anomalous results in current phasor simulation
4. Propose best-practice methodology for switching RLC circuits

4.4 Systematic Troubleshooting Strategy

Step 1: Artefact Characterisation

- Document exact nature of simulation anomalies
- Classify: discontinuity / non-physical value / oscillation / divergence
- Identify: occurs during switching / steady-state / transient

Step 2: Isolation Testing

Test Case A: No Switching (DC source)

- If artefacts remain: phasor transformation implementation issue
- If artefacts gone: switching-related problem

Test Case B: Slow Switching (frequency << resonant frequency)

- If artefacts appear: phasor envelope assumption violated
- If artefacts gone: high-frequency switching interaction

Test Case C: Ideal Switches vs. Real Switches

- Compare with/without dead-time, rise/fall times, parasitics
- Identify which non-ideality causes artefacts

Step 3: Reference Comparison

- Implement circuit exactly as in Rim et al. equations (37a-b)
- Compare term-by-term with our implementation
- Identify discrepancies in time-varying reactance, phasor transformation, real part operator, or switching function representation

Step 4: Validation Hierarchy

- **Level 1:** Match analytical equations for simple cases (no switching)
- **Level 2:** Match paper's simulation results (Figures 5-6)
- **Level 3:** Match experimental results (Figures 8-9)

5. Expected Contributions

5.1 To Power Electronics Community

1. **Validated Simulation Framework:** Demonstrated accuracy against real experimental data from published research
2. **Reproducibility Benchmark:** Establishes methodology for validating simulation tools
3. **Switching Dynamics Guidelines:** Best practices for simulating switching circuits in phasor domain

5.2 To simulation methodology

1. **No-Simplification Approach:** Handles complex time-varying dynamics exactly
2. **Data-Driven Validation:** Systematic comparison with published experimental results
3. **Artefact Resolution:** Clear identification and mitigation of switching-related simulation artefacts

5.3. Novel Aspects

- First systematic validation of data-driven simulation against instantaneous dynamic phasor analysis with switching
- Demonstrates framework applicability to time-varying frequency cases (FM signals)
- Provides computational efficiency analysis for high-frequency resonant converters
- Bridges gap between dynamic phasor theory and practical implementation

6. Risk Assessment and Mitigation

Risk	Impact	Probabilty	Mitigation
Cannot achieve <3% accuracy	High	Medium	Start with <5% tolerance, document differences
Switching artefacts unresolved	High	Medium	Document findings, contact paper authors for clarification
Missing circuit details	Medium	Low	Make reasonable assumptions, document clearly
Computational time too long	Medium	Medium	Optimise code, use variable time-step, parallel processing
Timeline delays	Medium	Medium	Built-in 2 week buffer, prioritise core validation

7. Key References

1. *C. T. Rim et al., "General Instantaneous Dynamic Phasor,"* IEEE Transactions on Power Electronics, vol. 40, no. 11, pp. 16953-16962, November 2025.
2. C. T. Rim and G. H. Cho, "Phasor transformation and its application to the dc/ac analyses of frequency phase-controlled series resonant converters (SRC)," IEEE Trans. Power Electron., vol. 5, no. 2, pp. 201–211, Apr. 1990.
3. S. R. Sanders, J. M. Noworolski, X. Z. Liu, and G. C. Verghese, "Generalized averaging method for power conversion circuits," IEEE Trans. Power Electron., vol. 6, no. 2, pp. 251–259, Apr. 1991.

8. Conclusion

This research proposal outlines a comprehensive plan to validate a data-driven circuit simulation framework using real experimental data from published power electronics research. By focusing on the challenging case of switching dynamics in RLC resonant circuits, we aim to bridge the gap between dynamic phasor theory and practical implementation.

The systematic investigation of switching-related simulation artifacts represents a significant contribution to the power electronics community, as many practitioners face similar challenges. The validation against the Rim et al. benchmark provides a rigorous foundation for establishing best practices in reproducible power electronics simulation.

Upon successful completion, this work will not only produce a validated simulation framework but also establish methodologies for future research in data-driven circuit analysis, contributing to more reliable and reproducible power electronics research.