Florida Polytechnic University
Electrical and Computer Engineering
EEL4242 POWER ELECTRONICS CIRCUITS, SPRING 2018

Final Design Assignment Points: 90

Design a Boost regulator to meet the following specifications.

- Input DC voltage $V_s = 12$ V
- Average output voltage $V_a = 48$ V
- Peak-to-peak ripple on the output ripple $\Delta V \leq 5\%$ of the average output voltage
- Peak-to-peak ripple on the inductor (L) current $\Delta I \leq 5\%$ of the average inductor current
- Average load current $I_a = 0.5$ A
- Switching frequency $f_s = 20$ kHz.

Use a Power MOSFET as a switch for PSpice (or Multisim or LTspice) simulation (Note the gate voltage must be between the base and the emitter terminals).

1. Design objectives and specifications (5 points)
2. Select the circuit topology (5 points)
3. Give the complete design including the current ratings and values of each component. (20 points)
4. Verify your design specifications by simulating your circuit using PSpice or Multisim ot LTspice. Plot the transient response of the output voltage and show that output voltage specification is met. (20 points)
5. Design modifications to meet the specifications (5 points)
6. Compute the performance parameters in Table D-1. In order to calculate the average load current Ia, the average supply current Is and the rms load current Io, you can assume that instantaneous load current io rises (or falls) linearly from I_1 to I_2. (30 points)

Table D-1: Performance parameters of a Boost regulator

	Min current of L		**Max current of L**		**Ripple current of L**		**Average load current**	
Duty cycle	**Calculated**	**Simulated**	**Calculated**	**Simulated**	**Calculated**	**Simulated**	**Calculated**	**Simulated**
k	I_1	I_1	I_2	I_2	ΔI	ΔI	I_a	I_a
.75	1.5 A	= .8 A	2.5 A	= 2.0 A	1 A	= 1.2 A	.5 A	= .355 A
	Average supply current		**RMS supply current**		**Average load voltage**			
Duty cycle	= 2 A **Calculated**	= 1.36 A **Simulated**	= 1.41 A **Calculated**	= 1.39 A **Simulated**	= 48 V **Calculated**	= 34.1 V **Simulated**	= .5 A **Calculated**	= .355 A **Simulated**
k	I_s	I_s	I_o	I_o	Va	Va		

Hint: PSpice Function: You can use PSpice functions to plot the average, rms values of a waveform, e.g. AVG(I(R)), RMS(I(R)).

6. Components and costs (5 points)
7. Flowchart of the design process (5 points)
9. Conclusions (5 points)

By submitting this assignment on the Canvas drop-box, I certify that this assignment is the result of my own efforts.

DUE ON: 10:00 AM ON MAY 2, 2018

Boost Regulator Design

EEL 4242.01, Power Electronics
Spring 2018
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The design of the boost regulator given the required constraints demanded the following calculations (the design flow is inherent within the order of calculations):

Input DC: 12V ; Avg. Output (V_a): 48V ;

$\Delta V < 5\%$ of V_a ; $\Delta I_L < 5\%$ of I_a ; $I_a = .5A$; $f_s = 20kHz$

$$\Delta I = \frac{V_s(V_a - V_s)}{f L V_a} \Rightarrow \frac{12(48-12)}{(20kHz)(L)(48)} = .05$$

$$\therefore L = \frac{12(36)}{(20000)(48)(.05)} \Rightarrow \boxed{9mH}$$

$$\Delta V = .05 = \frac{I_a(V_a - V_s)}{f V_a C} \quad \therefore \quad C = \frac{(.5)(36)}{(20000)(48)(.05)} \Rightarrow \boxed{375 \mu F}$$

$$R = \frac{V_a}{I_a} = \frac{48v}{.5A} \Rightarrow \boxed{96 \Omega}$$

Duty cycle (k): $V_a = V_s \frac{T}{t_2} \Rightarrow \frac{V_s}{1-k} \Rightarrow 48 = \frac{12}{1-k}$

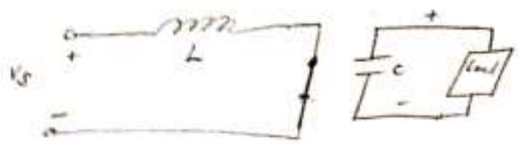
$$\therefore 48 - 48k = 12 \Rightarrow 36 = 48k \therefore \boxed{k = 75\%}$$

$$\therefore \boxed{1-k = 25\%}$$

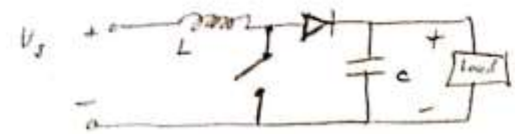
$$\therefore L_c = \frac{(1-k)kR}{2f} = \frac{(1-.75).75(96)}{2(20000)} \Rightarrow \boxed{450 \mu H}$$

$$\therefore C_c = \frac{k}{2fR} \Rightarrow \frac{.75}{2(20000)(96)} \Rightarrow \boxed{.195 \mu F}$$

$\therefore$ mode 1 :



Mode 2 :



P-P Ripple Current $\Delta I = \frac{V_s k}{fL} = \frac{(12)(36)}{(2000)(450\mu H)(48)} \Rightarrow \boxed{1A}$

Peak Current of Inductor $I_2 = I_s + \frac{\Delta I}{2}$ where $I_s = \frac{.5A}{(1-.75)} = 2A.$

$\therefore I_2 = 2 + .5 = \boxed{2.5A}$ ← max I_L

$\because \Delta I = I_2 - I_1 \therefore 1A = 2.5 - 1.5 \therefore \boxed{I_1 = 1.5A}$ ← min I_L

$\therefore I_s = \frac{I_a}{1-k} \Rightarrow \frac{.5}{.25} \Rightarrow \boxed{2A}$ $\quad \therefore I_{s(RMS)} = \frac{2A}{\sqrt{2}} = \boxed{1.41A}$

$V_{o(rms)} = \frac{V_o}{\sqrt{2}} = \frac{48}{\sqrt{2}} \approx \boxed{33.94V}$ ← RMS VOLTAGE (OUT)

$\therefore I_{o(rms)} = \frac{33.94V}{96\Omega} = \boxed{.354A}$ ← RMS CURRENT (OUT)

Given these calculations, the circuit topology should closely resemble the following in order to obtain an average of 48 V output from 12 Volts DC input:

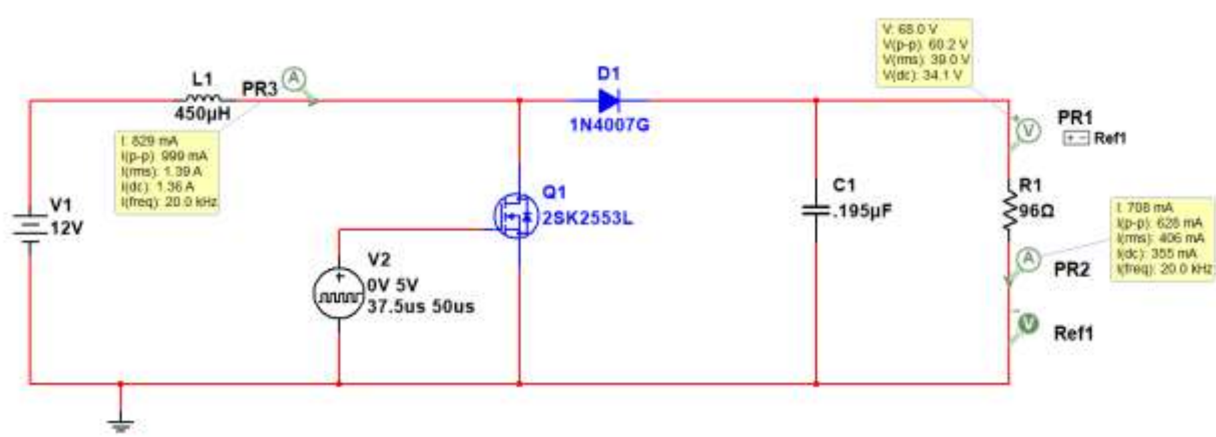


Figure 1. Boost Regulator Topology and Simulation.

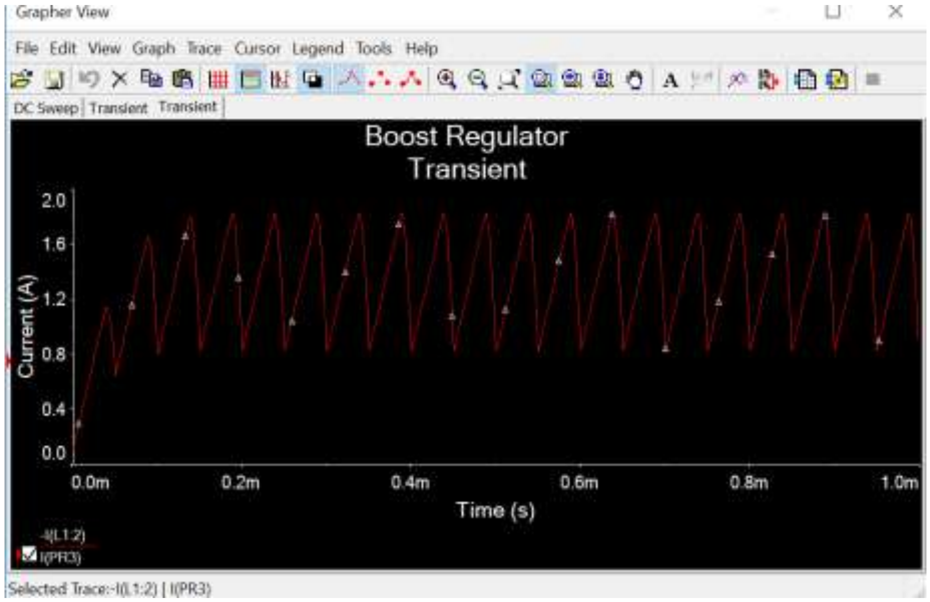


Figure 2. Transient Inductor Current.

From the given topology and Multisim circuit, it is obvious that adjustments were necessary. Specifically, the simulated average output voltage of 34.1 Volts fell short of the desired average output voltage of 48 Volts. In order to rectify this, I increased the 75% duty cycle in order to capture more of the stored voltage to be augmented to the output from the calculated 37.5 microseconds (us) to 41.25 us (a duty cycle of 82.5%). This enabled me to obtain an exact average output voltage of 48.1 volts. However, after replacing the components used in Multisim with values that are more readily available at reasonable prices per unit, the average output voltage was measured at 49.6 volts, which is approximately 3% more than the desired average output voltage. However, I felt this was an acceptable result, especially as the resulting output voltage fell within the limits of the chosen components.

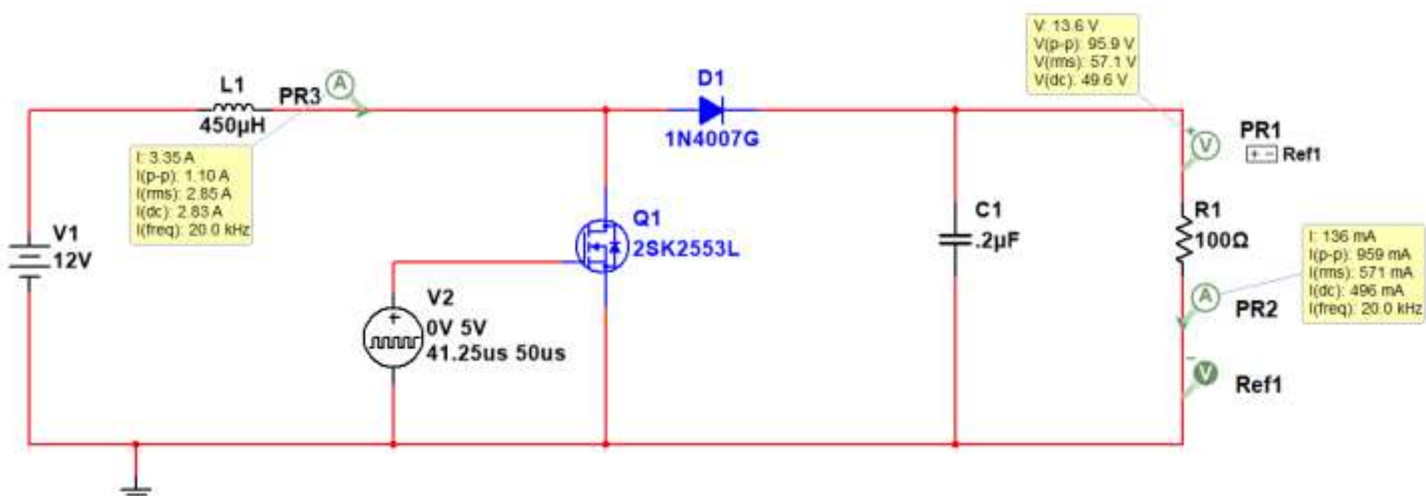


Figure 3. Modified Boost Regulator Simulation.

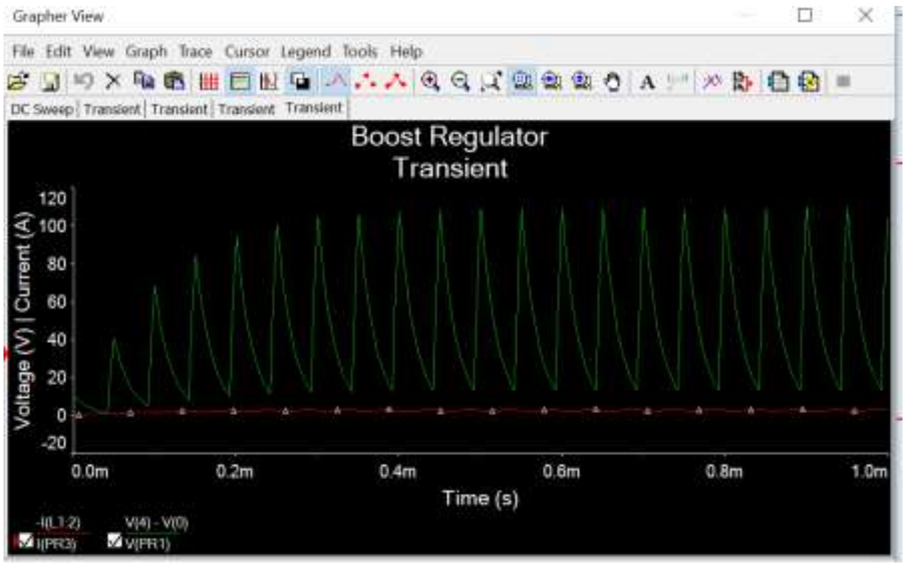


Figure 4. Output Voltage (peak to peak), Modified Circuit.

Component Table

Part (hyperlinked)	Cost per item
5705-RC 450 uH inductor	$3.50
NTE2996 N-channel MOSFET	$2.56
1N4007-T Diode	$0.12
12065C204KAT4A .2 uF, 50 V capacitor	$0.11
100 Ohm, 2-Watt carbon film resistor	$0.25
Total Cost:	**$6.54**

Conclusions

Although the desired results can be calculated on paper and closely simulated via Multisim or another simulation tool, the actual results will vary based on several factors, from operating environment to actual component parameters that are often too numerous or too troublesome to adjust due to time, resource, or physical restraints. In addition, components sold in the real world reflecting desired values may either be too expensive for use, or simply not available and, thus, the designer must often settle for components possessing values and tolerances closest to those desired as the most viable solution. This inevitably impacts performance of the designed circuit, so these variations should be taken into account and simulated yet again to ensure proper working condition and desired outcome within acceptable limits.