# Buck Converter: Design Project

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## Introduction

As a follow-on to my Power Electronics course final project (a step-up, or "boost" converter), I set out to design an asynchronous step-down ("buck") converter. In order to keep things simple, I am aiming to use a 12 VDC source as the input, with a desired output voltage of approximately 5 VDC and amperage of approximately 20 mA over a resistive load, $R_L$. I also wish to use a switching frequency of 1 kHz. Although the preliminary design will endeavor to produce the desired output, I will also attempt to design a circuit that can be practically implemented via a pulsed voltage source on the gate of a metal-oxide semi-conductor field effect transistor (MOSFET) serving as a switch. As I may wish to actually build a working model, I will include a list of real-world components, similar to what was accomplished in the boost converter project. Of critical import, I will be assuming continuous conduction mode (CCM) and steady-state (SS) operations for this project. This is important because it makes certain calculations and assumptions much less complicated, as we will see. Finally, we will need to ensure we avoid any undesirable harmonics within the circuit due to the requirement of working with switching frequencies.

## Analysis

The first step for this project will be to mathematically examine all variables, based on the given constraints and parameters. For these calculations, M. Rashid's book, *Power Electronics: Circuits, Devices, and Applications,* will be referenced. As we are assuming CCM and SS operation, average current, $I_A$, is considered constant. Thus, our first equation to determine the load resistance $R_L$ is a simple application of Ohm's Law:

$$V_O \;=\; (I_A)(R_L),\ thus \tag{1}$$

$$R_L \;=\; \frac{V_O}{I_A} \;=\; \frac{5V}{.020A},\ which\ yields\ \underline{250\ \Omega}. \tag{2}$$

Next, we should endeavor to determine the duty cycle of the input signal, which will determine the average level of current flowing through the inductor and to the load over time. This equation can be derived from

$$V_A \;=\; \frac{1}{T}\int_0^{t_1} V_O\ dt, \tag{3}$$

where the period from 0 to $t_1$ is the time or mode in which the switch is closed. Thus, this simplifies to

$$\frac{t_1}{T}V_S \;=\; ft_1V_S \;=\; kV_S\ (since\ duty\ cycle\ k \;=\; ft_1). \tag{4}$$

We also know that the duty cycle multiplied by the input voltage $V_S$ should be equivalent to the output voltage $V_O$. Since we also know that our desired current at the output is 20 mA, we can solve for k as follows:

$$I_A \;=\; \frac{V_A}{R_L} \;=\; \frac{kV_S}{R_L},\; thus \tag{5}$$

$$k \;=\; I_A\,\frac{R_L}{V_S} \;=\; .020A\,\frac{250\Omega}{12V} \;=\; \underline{.4167}. \tag{6}$$

Of note, the astute reader will notice that the previous equation simplifies to k = $\frac{V_O}{V_S}$, which is very useful for future reference.

As the current in our circuit will be fairly low (i.e., <1A), we may use a Zener diode for the flyback function of the buck converter, which we place in parallel with the load but between the inductor and the voltage source. Specifically, the Zener diode will maintain a constant DC output voltage across the load regardless of variations in the input voltage or changes in the load current. Since it operates in the reverse bias mode, it will conduct current once its breakdown voltage value has been reached. However, a resistor ($R_Z$) should be used in series with this diode. To find the desired value of $R_Z$, we assume a generous 2W power rating and use the following:

$$I_S \;=\; \frac{P}{V_O} \;=\; \frac{2W}{5V} \;=\; .4A \tag{7}$$

We know that the total Zener diode current, $I_Z$, should be equal to the source current minus the load current, thus

$$I_Z \;=\; I_S - I_L \;=\; .4A - .020A = \; .380A. \tag{8}$$

Now we can solve for $R_Z$:

$$R_Z \;=\; \frac{V_S - V_Z}{I_Z} \;=\; \frac{(12-5)V}{.380A} \;=\; \underline{18.42\ \Omega}. \tag{9}$$

Next, we will need a capacitor in parallel with the load, which will help smooth the output signal. To find an appropriate capacitance value, we will use the fact that Q = C$V_C$. From this, we know that

$$\Delta Q \;=\; C\Delta V_C \;=\; C\Delta V_O. \tag{10}$$

Assuming a desired voltage ripple $V_R$ of about 5 percent, we can solve for ΔQ:

$$\Delta Q_C \;=\; (\frac{1}{2})(\frac{T}{2})(\frac{V_R}{2}) \;=\; (.5)(.001)(.025) \;=\; 1.25E-5. \tag{11}$$

Now we can solve for C:

$$C \;=\; \frac{1.25E-5}{.05} \;=\; 2.5E-4 \;=\; \underline{250\ uF}. \tag{12}$$

Last, but not least, of the passive components for our design purposes is the inductor. As noted previously, the fact that this circuit is CCM and steady-state, we can assume $I_L$ is constant and, thus, the peak current $I_P = 2I_L = .040$ A. To solve for the critical value of the inductor, $L_C$, we use

$$V_L \;=\; L_C\frac{\Delta I}{\Delta t}, \tag{13}$$

and

$$V_S - V_O = L_C \frac{2I_O}{kT}, \tag{14}$$

thus,

$$L_C = \frac{(V_S - V_O)(kT)}{2I_O} = \frac{[(12-5)(.4167)(.001)]\ V \cdot s}{.040\ A} = .0729\ H,\ or\ \underline{73\ mH}. \tag{15}$$

# Design

## Initial Model

We begin by modeling the buck converter in Multisim using ideal passive components and simulate the switching through a function generator operating at a frequency of 1000 Hz, per the given parameters. It is important to note there are two methods of achieving a range of output voltages from 0 to $V_S$. Specifically, the switching frequency may be held constant, while only adjusting the pulse width or switch "on" time; this method is known as pulse width modulation (PWM). The second method involves varying the frequency while maintaining either a constant on or off time for the switch. As you might predict, this method is called frequency modulation. As you might also predict, varying the switching frequencies over a wide range will inevitably provoke undesirable and unpredictable harmonics in our circuit; thus, we will use PWM to determine the length of time for which the input voltage $V_S$ appears across the load. The proposed model is seen in Fig. 1.

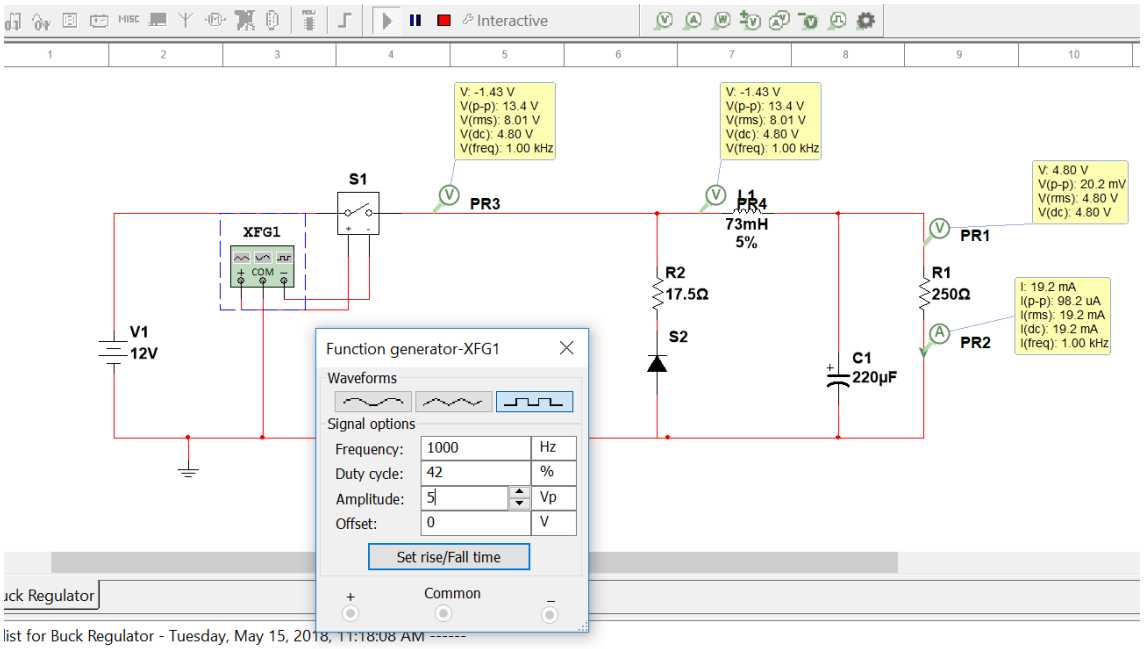



Figure 1: Initial Circuit Design, Multisim.

The resulting transient analysis as seen in Fig. 2 confirms the output voltage and current are fairly close to our desired results, with an output voltage of 4.8 V and a load current of 19.2 mA. However, an obvious voltage spike can be seen at the initial stages of the circuit simulation. This, combined with other potential issues, demands a modified approach.

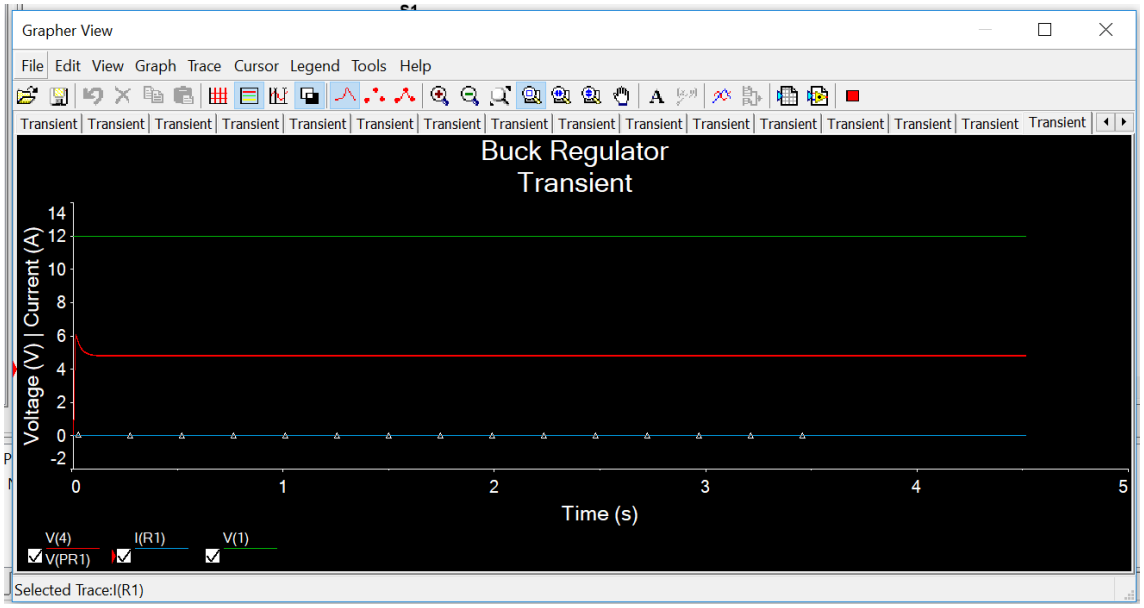



Figure 2: Transient Analysis, Initial Circuit, Multisim.

## Modified Model

In order to obtain a circuit that is more practical, we replace the ideal switch with a transistor and use a pulsed voltage source instead of a function generator to achieve the desired output voltage. The proposed circuit schematic can be seen in Fig. 3, while the resulting characteristics can be seen in the transient analyses in Figures 4 through 9. Of note, the output voltage is approximately 4.91 V while the current is approximately 19.6 mA; these results are closer than our initial model and certainly within an acceptable range. Further, the output current and voltage ripples are seen in Figures 6 and 8, respectively. The ripple current is approximately .25 mA, while the ripple voltage is approximately 60 mV; these values are considered acceptable for nearly all applications. For example, many central processing units (CPUs) use approximately 1V and have an acceptable voltage ripple of about .010 V, or about 1%. Our output voltage ripple is approximately 1.2%, so we are within an acceptable range for common electronic applications.

However, we can reduce the output voltage ripple at the expense of an increased initial spike in output voltage. Specifically, the higher the filter capacitor value, the less ripple we see; however, the higher the initial spike in output voltage due to a decreased impedance in the filter, per our impedance equation for capacitors:

$$X_C = \frac{1}{2\pi f C} \tag{16}$$

Thus, if ripple is an issue, and we are not concerned with a small spike in voltage, we may alter our capacitor value to achieve the desired affect. We can calculate the output ripple current and output ripple voltage, respectively, with the following equations:

$$\Delta I = \frac{V_O(v_S - V_O)}{V_S f L} \tag{17}$$

and

$$\Delta V = \frac{\Delta I}{8 f C} \tag{18}$$

There are some additional key notes for this design. First, we used a capacitor in parallel with the input voltage for stability purposes (i.e., to remove as much noise from the input DC signal as possible). Second, we replaced the Zener diode with a Schottky diode, as this is more commonly used with voltage regulator circuits.

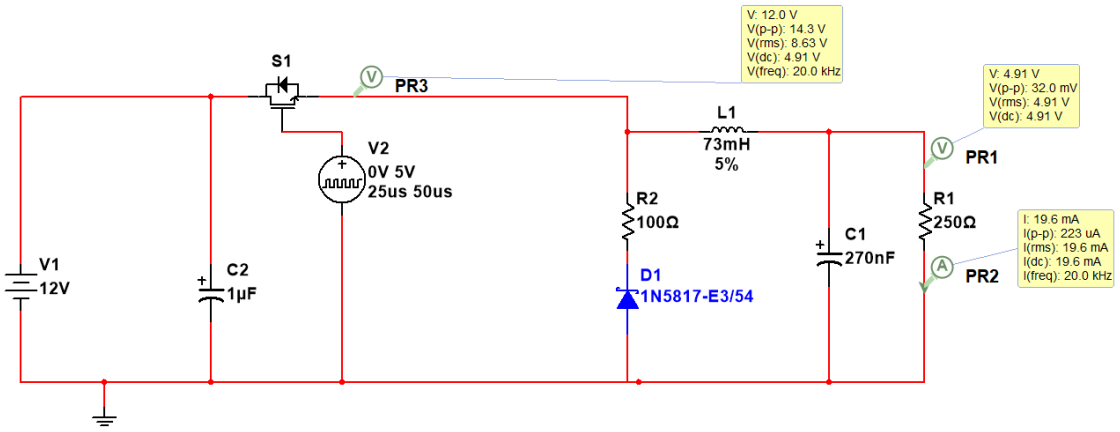



Figure 3: Modified Circuit, Multisim.

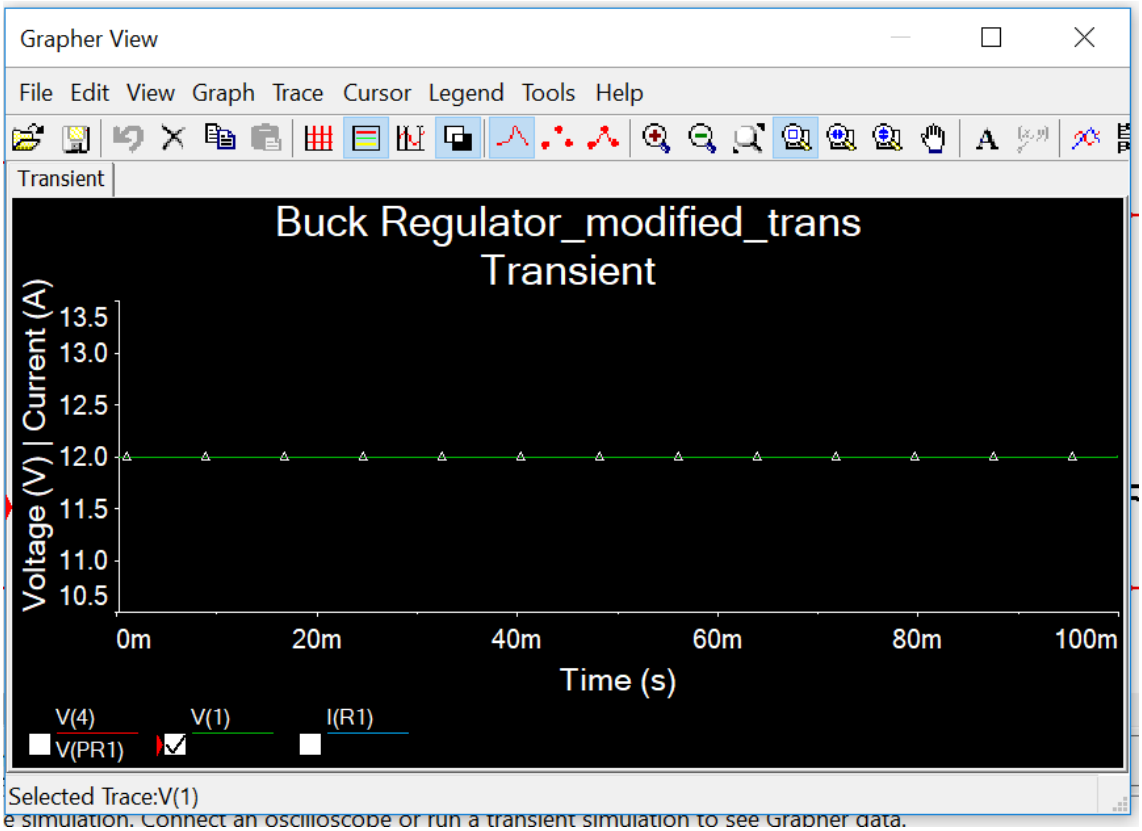



Figure 4: Input Voltage, Modified Circuit, Multisim.

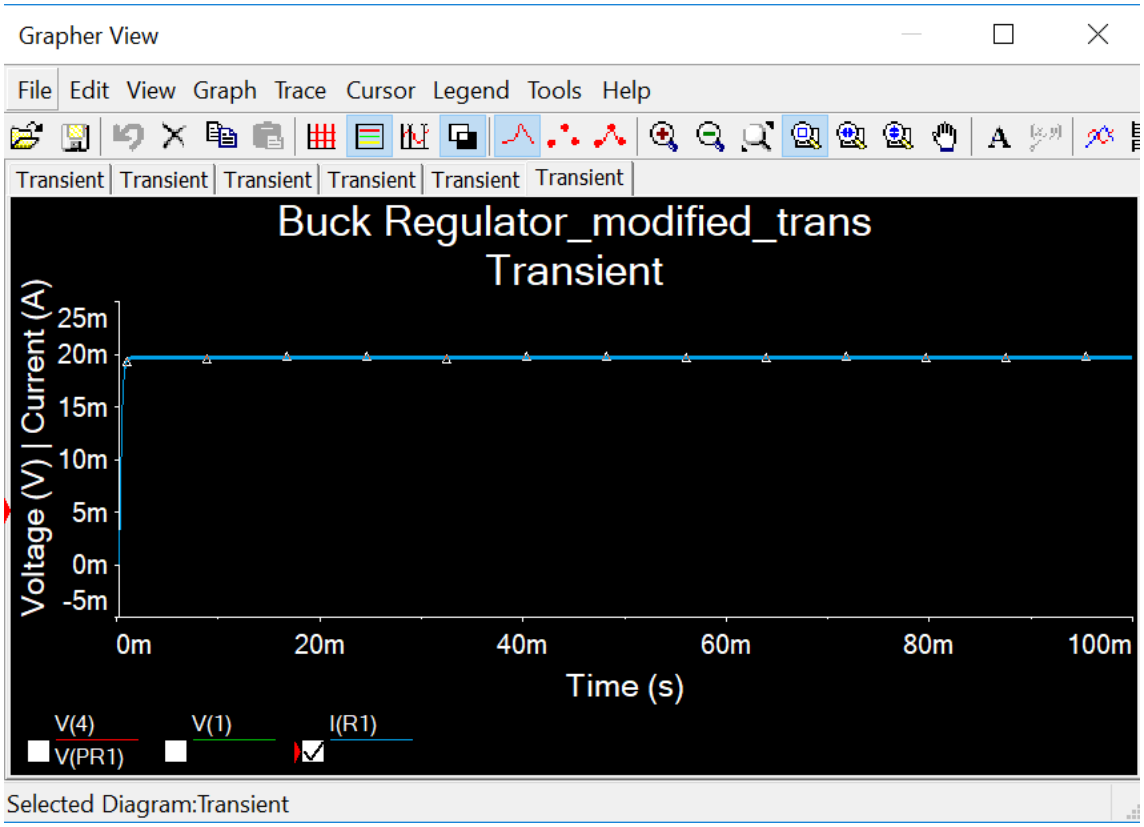



Figure 5: Output Current, Modified Circuit, Multisim.

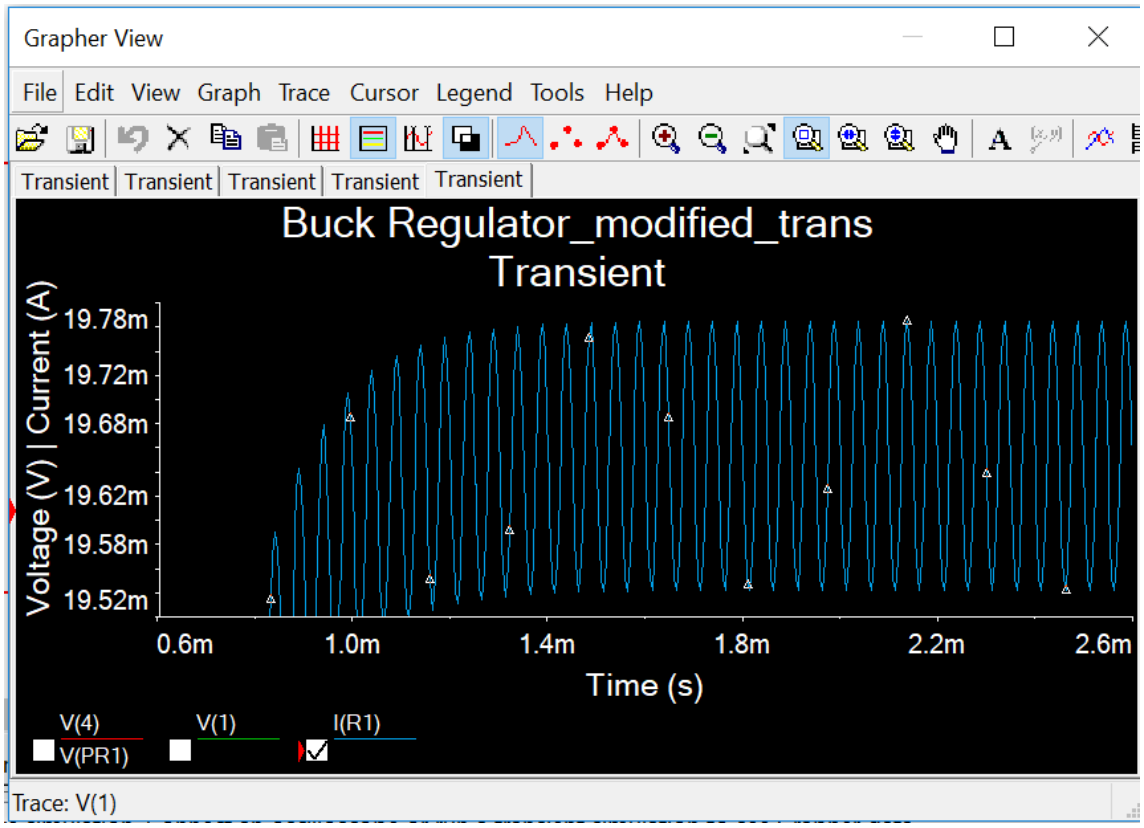



Figure 6: Output Current Ripple, Modified Circuit, Multisim.

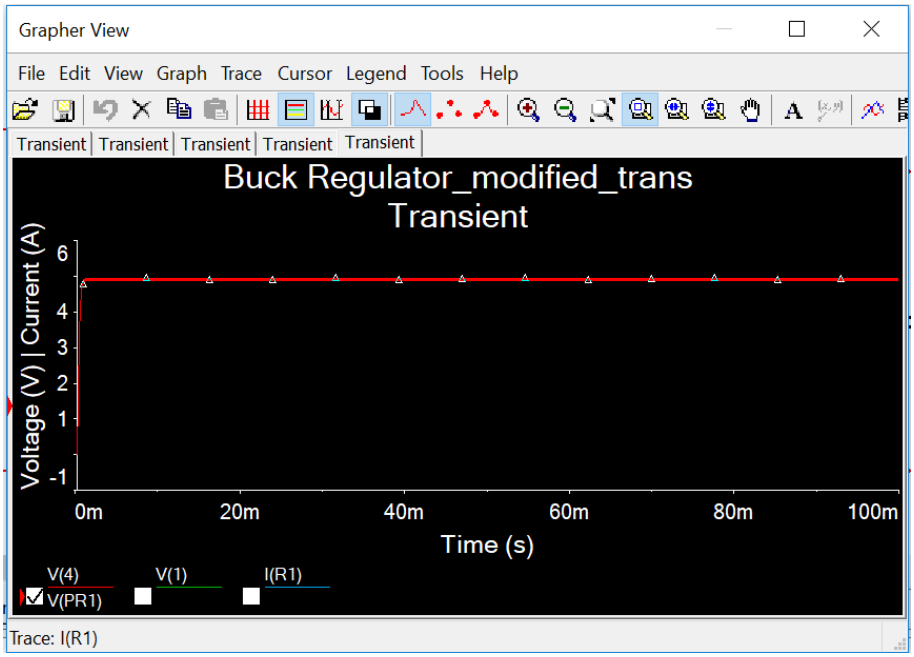



Figure 7: Output Voltage, Modified Circuit, Multisim.

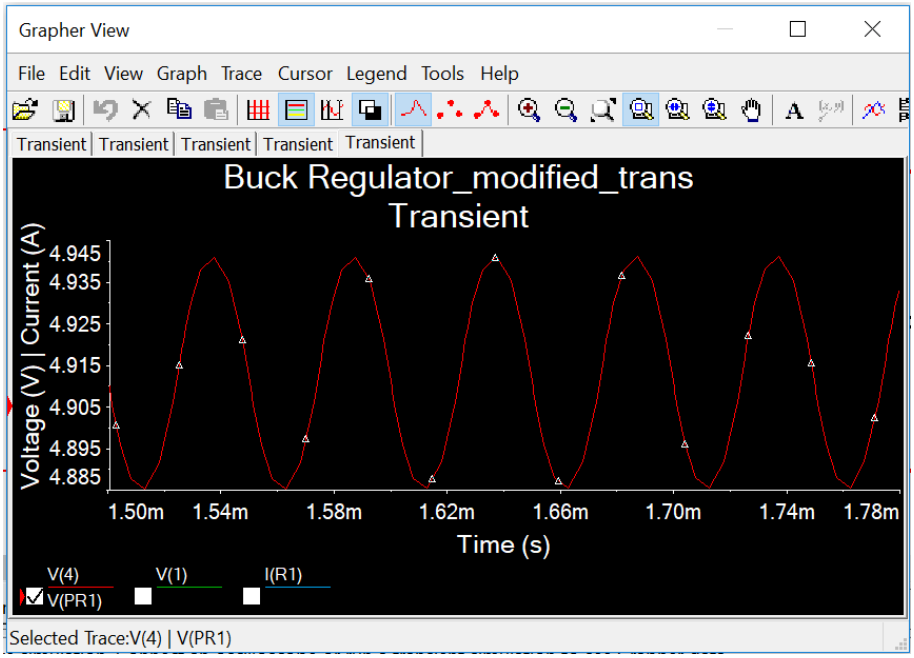



Figure 8: Output Voltage Ripple, Modified Circuit, Multisim.

## Output Ripples

Let us examine more closely the effects of changing the capacitance values in the output filter portion of this circuit (i.e., the capacitor in parallel with the output voltage load). It is important to note that, from equation (18), we may either vary the capacitance or frequency values to achieve a desired output ripple voltage. However, as noted previously, we desire to keep the frequency at 1 kHz for this design; thus, we will only examine the effects on varying the output filter capacitance.

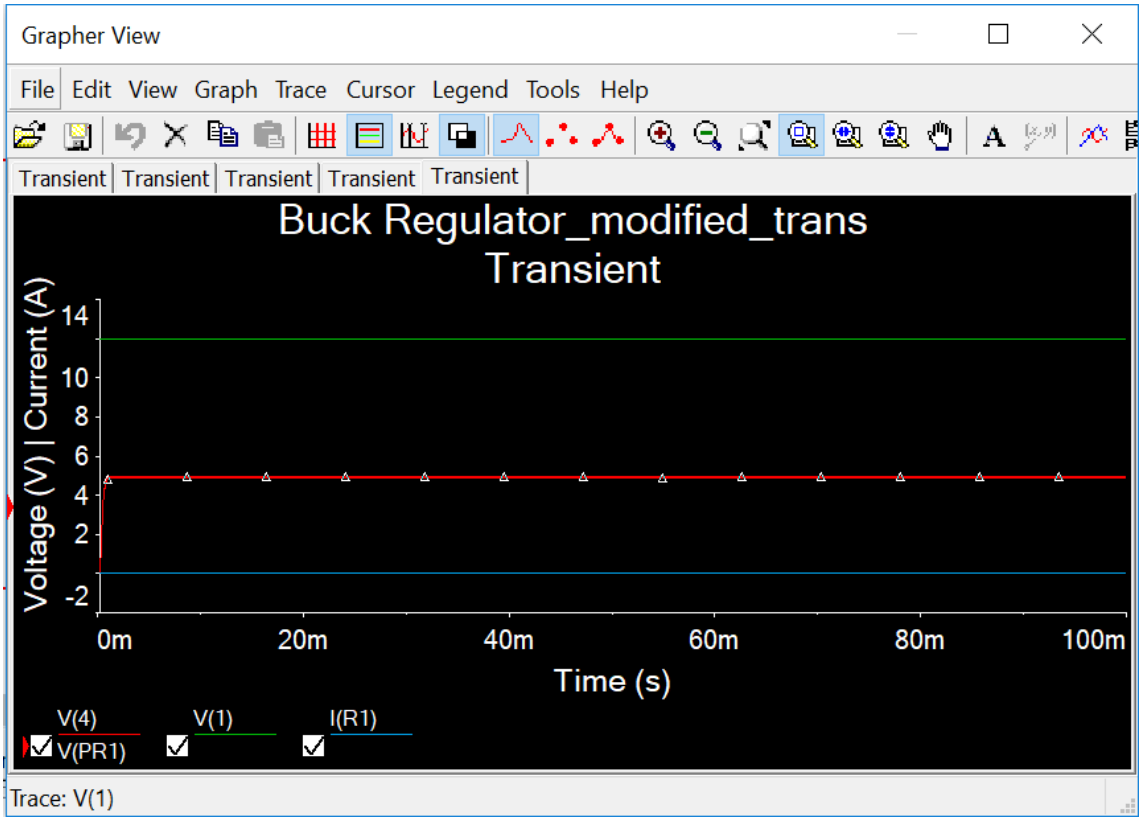
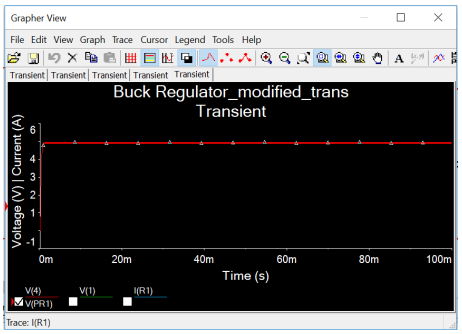
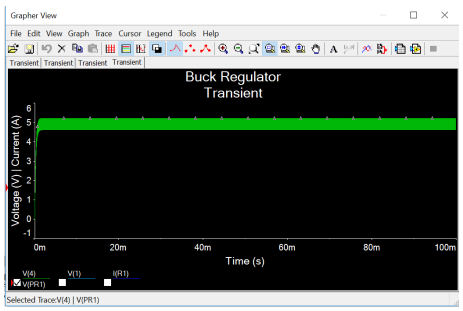



Figure 9: Comprehensive Transient Analysis, Modified Circuit, Multisim.

We can begin by first removing the output capacitor and examining the effect on output voltage ripple. The negative effect can be clearly seen in Fig. 10, where we compare the output voltage of the modified circuit without a filter with that of our filtered modified circuit (Fig. 7). For a close examination, Fig. 11 shows the unfiltered output voltage ripple is approximately 600 mV, which is 10 times that of our filtered modified circuit! Also, we see in the same figure that the output voltage exceeds our desired goal of 5 V by 200 mV; this could be a serious issue for sensitive applications.




(a) Output Voltage with Filter




(b) Output Voltage without Filter

Figure 10: Comparison of Output Voltages with and without Filters....

It is clear from this exercise that a filtering capacitor inserted in parallel with the load is highly effective and desirable. But what value? To demonstrate the effect of various capacitance values, we inserted different capacitors increasing in increments of standard values; these results are documented in Table 1.

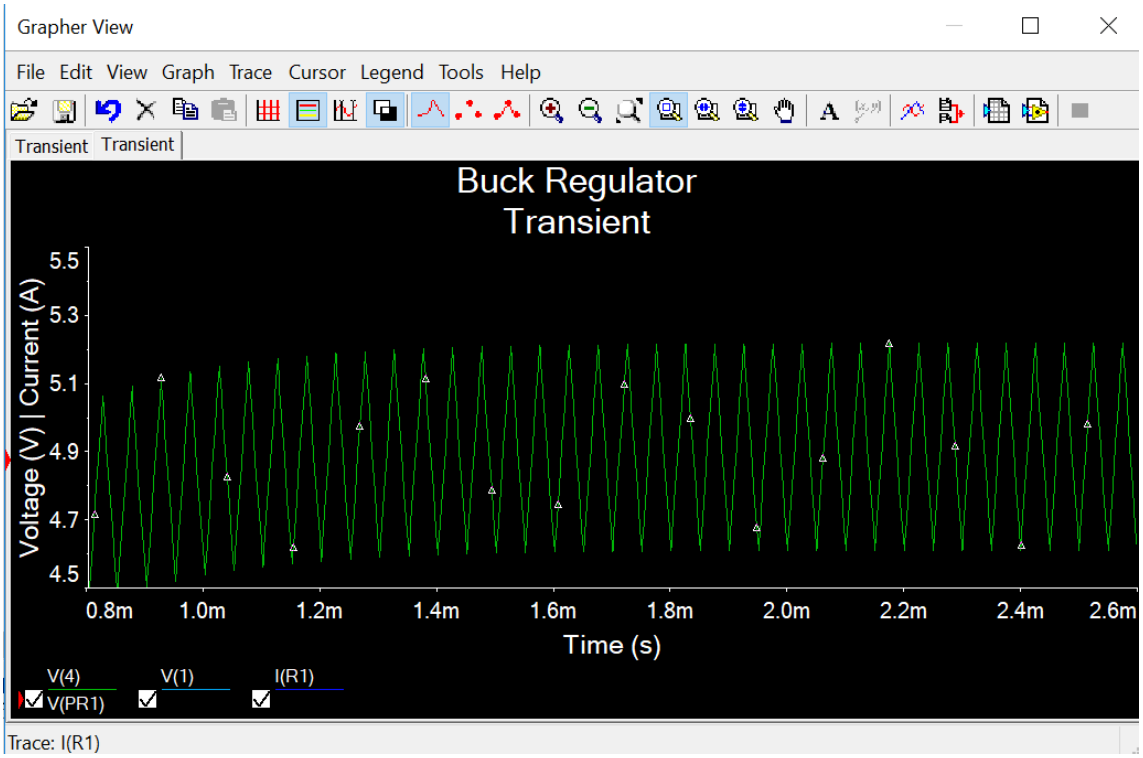



Figure 11: Output Voltage Ripple, Modified Circuit without Filter, Multisim.

We began with the calculated capacitor value of 270 nF, and increased by standard values until we observed a clear spike in the initial output voltage. This initially occurred at a capacitor value of 390 nF, and can be seen in Fig. 12. This spike was only about 4.97 V; since this did not exceed our desired $V_O$ of 5 V, we proceeded to test the next highest value of 470 nF. At this point, we observed a spike of about 5.04 V, or 40 mV (reference Fig. 13). Although this was not sustained and the output voltage fell back to below 5 V at approximately 1 ms, we felt this was sufficient to demonstrate the trade-off experienced. Thus, to obtain both a minimal output voltage spike and ripple, we may consider a 390 nF capacitor optimal for this particular design.

| Capacitor Value | $V_O$ Ripple | Initial Spike |
|---|---|---|
| 270 nF | 60 mV | None |
| 330 nF | 50 mV | None |
| 390 nF | 40 mV | 4.97 V |
| 470 nF | 35 mV | 5.04 V |

Table 1: Effects of Varying Capacitor Values on $V_O$

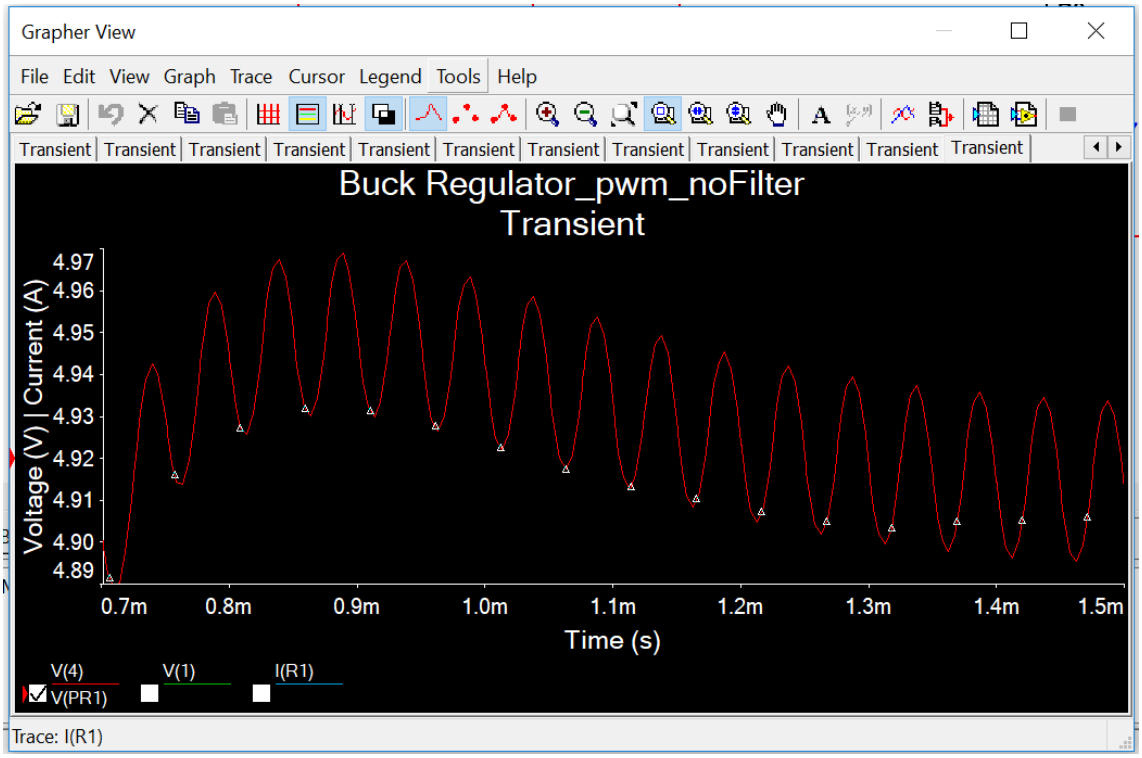



Figure 12: Output Voltage Spike, 390 nF Filter Capacitor, Modified Circuit, Multisim

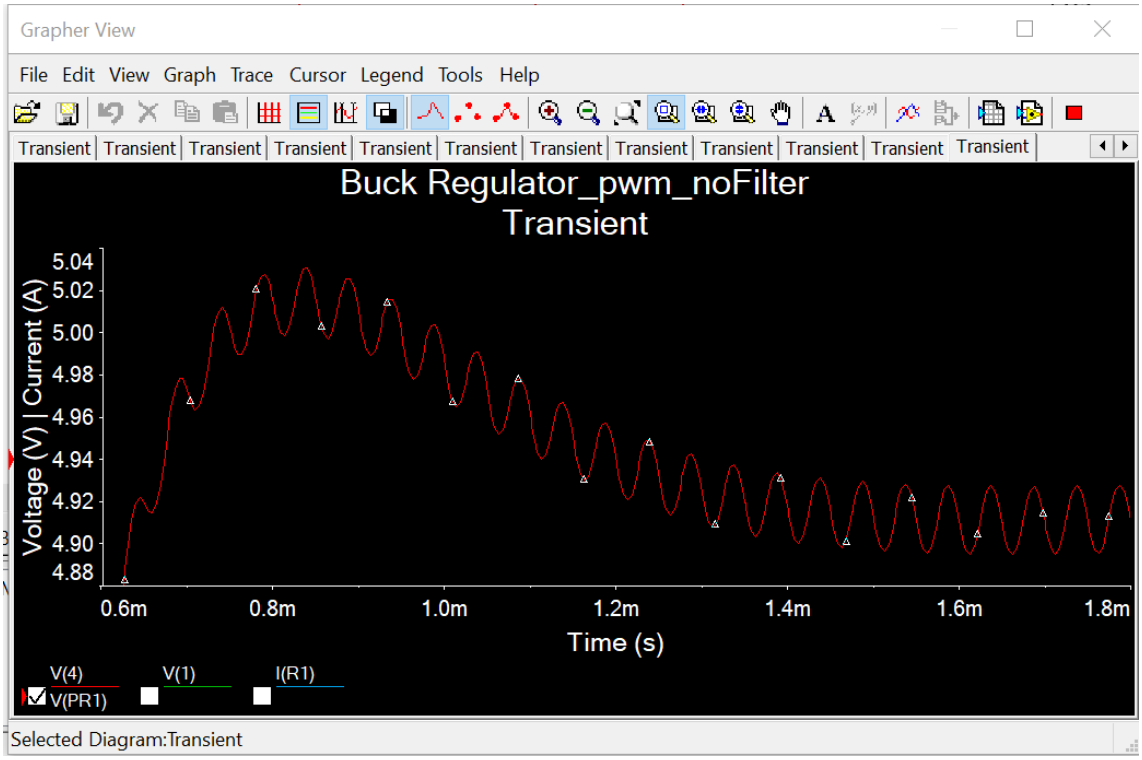



Figure 13: Output Voltage Spike, 470 nF Filter Capacitor, Modified Circuit, Multisim.

# Conclusion

In this project, we set out to design and simulate a simple step-down, or "buck," converter. The first step was to identify the conditions and assumptions made regarding the operating mode and state, in addition to the values of both input and desired output voltages, output current, and switching frequency, as these would drive our design. Choosing to operate in CCM and SS conditions simplified the analysis and modeling of this circuit greatly. Further, as operating with a variable frequency requires a wide range to obtain the full output voltage range, achieving the step-down output voltage through this method ("frequency modulation") would generate unpredictable harmonics, imposing even more complexity on the design of our circuit. Thus, we chose to achieve a "chopped" output voltage through pulse width modulation, which essentially just varies the on and off times of the switch while maintaining a constant frequency.

Once our mathematical analysis was complete, we placed the components in an order that enabled a controlled transfer of voltage, based on a calculated duty cycle, from the higher input voltage source to the lower load, or output, voltage. Although we initially designed the circuit with ideal switches and a function generator providing the switching frequency and duty cycle, we modified the design to include a more realistic MOSFET instead of the switch, with a pulsed voltage source (which can be implemented through a micro-controller, for example) supplying the gate voltage.

Finally, although we included filter capacitors in both our initial and modified designs, we examined the effects of omitting the output filter capacitor as an exercise. We observed that doing so increased our output ripple voltage ten-fold. Further, we examined the effects of increasing the capacitance value from the initial, calculated value of 270 nF in standard increments and found that, although the output ripple voltage decreased, we encountered a spike in potentially harmful initial output voltage. Thus, as in every circuit, there are a multitude of important trade-offs which need to be considered in the design process, from the obvious factors of component values, tolerances, and cost to less intuitive factors such as frequency-induced undesirable harmonics, output voltage spikes, and ripples, to name only a few.