

David J. Palframan

CONTACT	<i>Email:</i> dpalframan@gmail.com	<i>Phone:</i> 608-770-0134
EDUCATION	Ph.D. in Computer Engineering , University of Wisconsin–Madison, May 2015 Advisors: Mikko Lipasti, Nam Sung Kim M.S. in Computer Engineering , University of Wisconsin–Madison, May 2011 B.S. in Electrical Engineering , <i>Summa Cum Laude</i> , Bucknell Univ., May 2009	
EXPERIENCE	AMD , Austin, TX <i>Member of Technical Staff</i> March 2019 – present <ul style="list-style-type: none">• Created a flexible model for cache hierarchy studies and workload analysis.• Evaluated accuracy of abstract CPU modeling for high core/thread counts.• Responsible for running server SOC studies. Also created SOC model regression.• Misc: optimized simulator smoke build (2X speedup), improved job monitor tool, implemented smart pool pointers, implemented experimental Git/Jenkins workflow. Qualcomm Research , Raleigh, NC <i>Senior Engineer</i> November 2016 – February 2019 <ul style="list-style-type: none">• Research on novel prefetch and memory system optimizations. Modeled, evaluated, and designed new prefetch algorithms for next generation CPUs.• Contributed to an instruction set emulator and toolkit, including compressed check-point format and system call emulation.• Developed cycle-accurate model on top of emulation framework, including configurable OoO structures and modeling primitives. ARM Research , Austin, TX <i>Senior Research Engineer</i> July 2015 – October 2016 <ul style="list-style-type: none">• Research on hardware optimizations for machine learning and speech recognition.• Modified and simulated machine learning routines to evaluate new instructions.• Developed and trained a keyword spotting algorithm for workload characterization. Created optimizations for the Cortex-M DSP library (40-50% speedup). Qualcomm Research , Raleigh, NC <i>Intern</i> May 2013 – August 2013 <p>Evaluated custom cache replacement policies, one of which was implemented in silicon. Developed a stand-alone cache hierarchy model to supplement experiments in cycle-accurate simulator. Also investigated prefetch throttling to reduce cache pollution.</p> IBM , Raleigh, NC <i>Intern</i> May 2012 – April 2013 <p>Examined the benefits of power gating individual cores. Evaluated the AIX dynamic “core folding” policy on POWER7+ hardware. Created a tool for visualization of power data traces. (Tool generates HTML pages with Gnuplot graphs.)</p> NVIDIA , Santa Clara, CA <i>Intern</i> May 2011 – August 2011 <p>Configured verification infrastructure for bringup and executed full-chip functional test plan. Also wrote Perl scripts to automate performance tuning experiments.</p>	

SKILLS

- Languages: C++, C, Python, Perl, some Ruby, Java, Verilog, HTML, \LaTeX
- Tools: Git, Gdb, Valgrind, Simpoint, Make, CMake, Perf, Gnuplot, MATLAB

PATENTS

- Rami Al Sheikh, Shivam Priyadarshi, Brandon Dwiell, **David Palframan**, Derek Hower, Muntaquim Chowdhury, “Method and Apparatus for Intelligent Data Prefetching using Address-Delta Prediction,” patent pending, filed August 2017.
- Rami Al Sheikh, Shivam Priyadarshi, Brandon Dwiell, **David Palframan**, Derek Hower, “Method and Apparatus for Expediting Cache Misses through Cache Hit Prediction,” patent pending, filed August 2017.
- Jiecao Yu, Andrew Lukefahr, **David Palframan**, Reetuparnda Das, Scott Mahlke, “Systems and Devices for Compressing Neural Network Parameters,” patent pending, filed June 2017.
- Jiecao Yu, Andrew Lukefahr, **David Palframan**, Reetuparnda Das, Scott Mahlke, “Systems and Devices for Formatting Neural Network Parameters,” patent pending, filed June 2017.
- **David Palframan**, Nam Sung Kim, and Mikko Lipasti, “Memory Fault Patching Using Pre-Existing Memory Structures,” U.S. patent number 9,626,297, issued April 18, 2017.
- Harold W. Cain III and **David J. Palframan**, “Adaptive Cache Prefetching Based on Competing Dedicated Prefetch Policies in Dedicated Cache Sets to Reduce Cache Pollution,” patent pending, filed April 2014.
- **David Palframan**, Nam Sung Kim, and Mikko Lipasti, “Method and Apparatus for Soft Error Mitigation in Computers,” U.S. patent number 9,235,461, issued January 12, 2016.
- Malcolm S. Allen-Ware, Heather L. Hanson, **David J. Palframan**, Srinivasan Ramani, and Ken V. Vu, “Energy Efficient Optimization in Multicore Processors Under Quality of Service (QoS) / Performance Constraints,” U.S. patent number 9,541,985, issued January 10, 2017.

PUBLICATIONS

- Jiecao Yu, Andrew Lukefahr, **David Palframan**, Ganesh Dasika, Reetuparna Das, Scott Mahlke, “Scalpel: Customizing DNN Pruning to the Underlying Hardware Parallelism,” in *Proceedings of the 44th International Symposium on Computer Architecture (ISCA 2017)*, Toronto, ON, June 2017.
- **David J. Palframan**, Nam Sung Kim, and Mikko H. Lipasti, “COP: To Compress and Protect Main Memory,” in *Proceedings of the 42nd International Symposium on Computer Architecture (ISCA 2015)*, Portland, OR, June 2015.
- Amir Yazdanbakhsh, **David Palframan**, Azadeh Davoodi, Nam Sung Kim, Mikko Lipasti, “Online and Operand-Aware Detection of Failures by Utilizing False Alarm Vectors,” in *Proceedings of the 25th Great Lakes Symposium on VLSI (GLSVLSI 2015)*, Pittsburgh, PA, May 2015.
- **David J. Palframan**, Nam Sung Kim, and Mikko H. Lipasti, “iPatch: Intelligent Fault Patching to Improve Energy Efficiency,” in *Proceedings of the 21st IEEE International Symposium on High Performance Computer Architecture (HPCA 2015)*, Bay Area, CA, February 2015.

- **David J. Palframan**, Nam Sung Kim, and Mikko H. Lipasti, “Precision-Aware Soft Error Protection for GPUs,” in *Proceedings of the 20th IEEE International Symposium on High Performance Computer Architecture (HPCA 2014)*, Orlando, FL, February 2014.
- **David J. Palframan**, Nam Sung Kim, and Mikko H. Lipasti, “Resilient High-Performance Processors with Spare RIBs,” *IEEE MICRO*, vol. 33, no. 4, July-Aug 2013 (special issue on reliability).
- **David J. Palframan**, Nam Sung Kim, and Mikko H. Lipasti, “Mitigating Random Variation with Spare RIBs: Redundant Intermediate Bitslices,” in *Proceedings of the 42nd Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN 2012)*, Boston, MA, June 2012.
- Vignyan R. K. Naresh, **David J. Palframan**, and Mikko H. Lipasti, “CRAM: Coded Registers for Amplified Multiporting,” in *Proceedings of the 44th Int’l Symposium on Microarchitecture (MICRO-44)*, Porto Alegre, Brazil, December 2011.
- **David J. Palframan**, Nam Sung Kim, and Mikko H. Lipasti, “Time Redundant Parity for Low-Cost Transient Error Detection,” in *Proceedings of Design, Automation, and Test in Europe (DATE 2011)*, Grenoble, France, March 2011.

AWARDS

- AMD spotlight award for speeding up debug/smoke simulations by 2X.
- IBM PhD Fellowship
- Peter Schneider Fellowship, University of Wisconsin–Madison
- George Allison Irland Prize for achievement in electrical engineering, Bucknell U.
- Jeffrey James Harold Prize for first-year EE with highest standing, Bucknell U.
- Alpha Lambda Delta Honor Society
- Tau Beta Pi Engineering Honor Society
- Sigma Pi Sigma Physics Honor Society
- Eagle Scout