Dhyan Patell

Laredo, Texas & Princeton, New Jersey 956-319-6330
dpatell@princeton.edu www.linkedin.com/in/dhyan-patell

EDUCATION

Princeton University, Princeton, NJ *May 2022*

B.S.E., Electrical and Computer Engineering; *Minor:* Computer Science
Cumulative GPA: 3.558 **Major GPA:** 3.635
Awards: Honors, Sigma Xi, Sigma Xi Award for Outstanding Research

CS Coursework: Computer Vision, Operating Systems, Distributed Systems, Stochastic Processes, Robotics
EE Coursework: Computer Arch., Embedded Systems, Digital Logic Design, Wireless Comms., Power Electronics

SKILLS

Software: *(proficient):* Python, C *(familiar):* Golang, Java, SQLite, MATLAB, R, Verilog
Hardware: Arduino, PSoC, ATMEL, UART/I2C/XBee, SWD/JTAG, CPLD, Cadence OrCAD/Virtuoso

WORK EXPERIENCES

Researcher, SWAN Lab (Eavesdropping on Underwater Communication from Air) *Dec 2021/-*

- Research focused on eavesdropping on underwater communications only using a narrowband THz radar.
- Implemented a FSK modulated communication chain on hardware for real-time underwater acoustic communication.
- Designed eavesdropping technique to log underwater communications via μ-meter ripples of the air-water interface
- Leveraged knowledge: Designed and implemented a FSK underwater audio communication schema operable on hardware; implemented signal processing blocks to clean, decode, ensure the received underwater and eavesdropped signals are resilient to multi-path ISI and hardware non-linearities; programmed in Python.

Researcher, SWAN Lab (THz Object Localization and Velocity Estimation) *Sept 2021/Dec 2021*

- Research focused on developing an object tracking and velocity classification technique for a THz leaky-wave antenna.
- Designed non-coherent radar perception pipeline to fingerprint and classify each object using wideband-doppler shift.
- Developed a virtual radar simulator in Python to track and log radar's velocity classification accuracy using to non-trivial trajectories.

Hardware-Firmware Engineering Intern, Amazon (Health-Wearables) *June 2021/Aug 2021*

- Owned schematic design, firmware development, and functional verification for a battery powered wearable.
- Implemented C/C++ API to bootstrap associated IC drivers, tune IC modes, update status via I2C, and log error and bus communication via UART on a bare-metal MCU.
- Scripted a MCU driver to automate software validation and published functional verification and board bring up plan.
- Worked with a mechanical intern to balance cross-functional goals and successfully conducted a user-study.
- Leveraged knowledge: Developed device drivers in C on a bare-metal 32-bit MCU; debugged firmware using Oscilloscope; performed board bring up and validation; performed concurrent HW/SW co-design of wearable.

Undergraduate Assistant Instructor, Princeton University *Aug 2020/May 2021*

- Taught ELE203 (Electronic Circuit Design) and ELE206 (Digital Logic Design) in the Fall and Spring, respectively.
- ELE206: Taught Verilog and RTL design and helped students debug projects.
- ELE203: Led weekly small group recitations, homework-help sessions, and contributed to the class's online forum.

Researcher, Integrated Microsystems Lab (Dual-Band Phased Array Generation) *June 2020/Feb 2021*

- Research focused on developing a dual-band antenna array for efficient transmission at 5/10 and 28/56 GHz.
- Designed an array spacing heuristic and modified particle swarm optimization algorithm using multiple virtualized arrays to perform tune inter-element spacings to avoid local optima, reduce grating lobes, and minimize side lobes.
- Sped up array generation convergence time by 5% compared to prior methods.
- Leveraged knowledge: Used machine learning, stochastic processes, and optimization on a sparse data to improve convergence time; batched jobs on HPC cluster; programmed in MATLAB and Python.

PROJECTS

Personal Website: https://dpatell22.github.io/ (for additional projects and information)

Zero-Shot Recognition on Animals with Attributes dataset (Pytorch)

- Used a non-pretrained ResNet18 model to embed image into 85 attributes and compared class attribute vector.
- Tested model on unseen set of obtained 35% accuracy compared to 65% accuracy seen in state-of-the-art models.

MIPS ISA Cycle-Accurate Simulator (C/C++) (3-person group)

- Designed a 5-stage pipelined MIPS simulator with flexible L1 cache API using OOP to abstract processor and cache.
- Directly responsible for implementing the 5-stage pipeline simulator that supports forwarding and bypassing, single branch delay slot, multi-cycle halts for cache misses, and one-cycle load-use stalls.

Fault-Tolerant Distributed Key-Value Storage Service (Golang)

- Implemented RAFT leader election and log consensus API without membership change and log compaction support.
- Designed fault-tolerant server backend using the RAFT API to log and respond to unique client RPCs.