Implementation of the IEEE 1149.1 Test Access Port Standard   
(TAP Controller)

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1. **Introduction**

The IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture standard is a standard defining a four- or five-pin interface on integrated circuits used for device testing. The Test Access Port (TAP) accepts serial inputs Test Mode Select (TMS), Test Clock (TCK), Test Data In (TDI), Test Data Out (TDO), and an optional dedicated reset. TDI and TDO are shifted in and out respectively to one of two sets of registers, one instruction register (IR) and other data registers (DR). Each of these registers can be interfaced parallel with a shadow register. The contents of these registers provide an easy, standard method of feeding instructions and data for test purposes. This report models the TAP controller and thus only deals with TMS and TCK but outputs a variety of signals that could be used to control the registers.

1. **FSM Block Diagram**

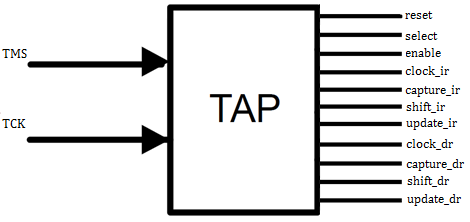


Figure 1: TAP Finite State Machine

1. **Module/Test Bench Connection**

Figure 2 models the connection between the TAP module and the test bench.

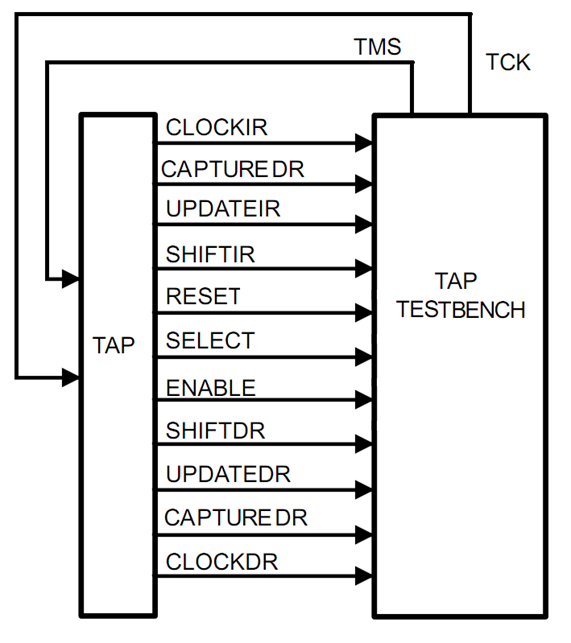
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Figure 2: Module/Test Bench Connection\*

\*Note: Test Bench Diagram drawn from IEEE 1149.1 documentation <http://focus.ti.com/lit/an/ssya002c/ssya002c.pdf>

**4.0 Planned Implementation of Registers (Not Implemented)**

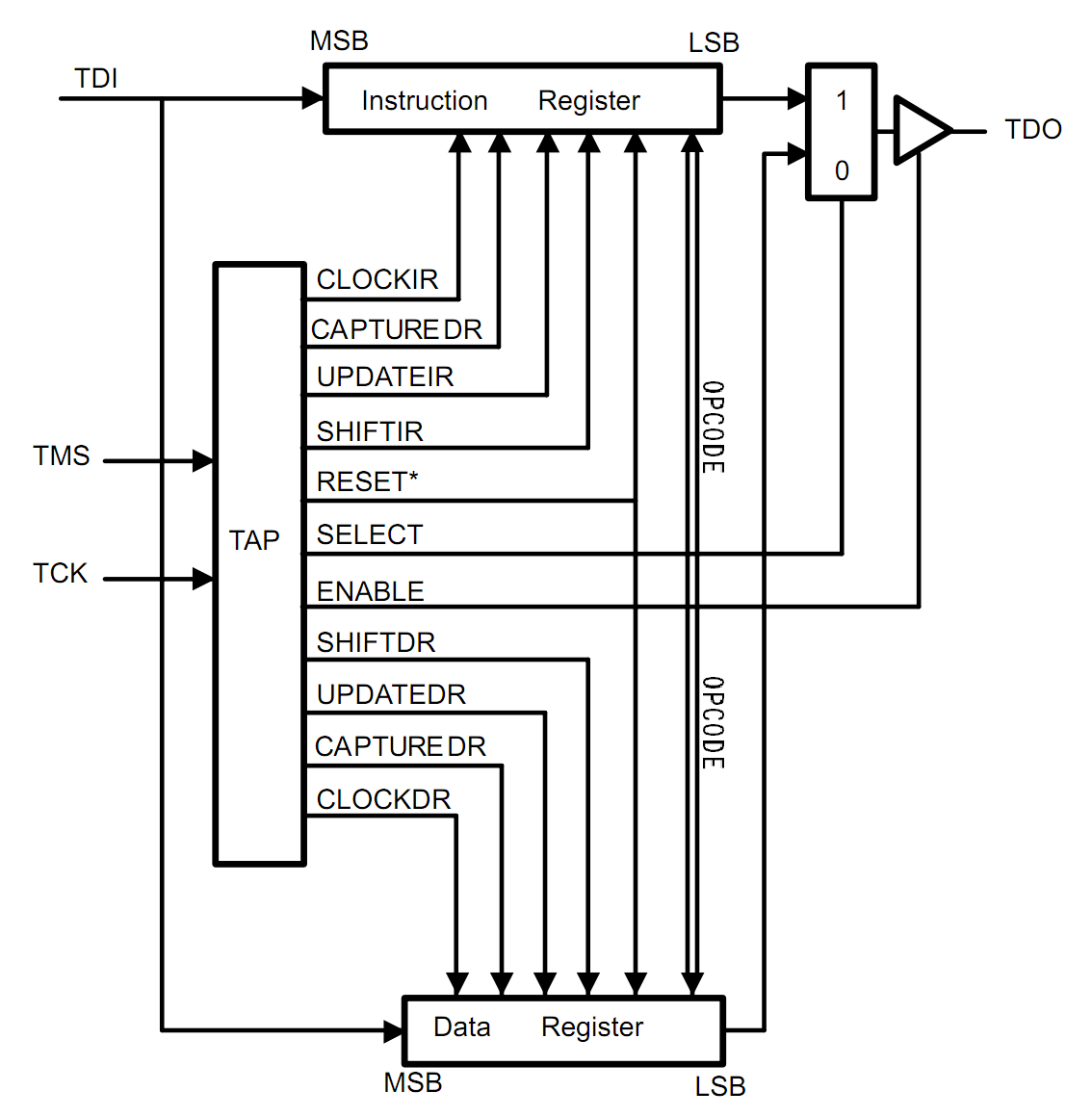
Figure 3 is a block diagram for how the TAP will interact with the registers. Note that this is projected and not yet implemented.

Figure 3: TAP with Registers\*

\*Note: Adapted from the IEEE 1149.1 documentation <http://focus.ti.com/lit/an/ssya002c/ssya002c.pdf>

1. **State Diagram**

Figure 4 is the state diagram for the TAP controller FSM. Refer to Table 1 and Table 2 for more information regarding the flow of data.

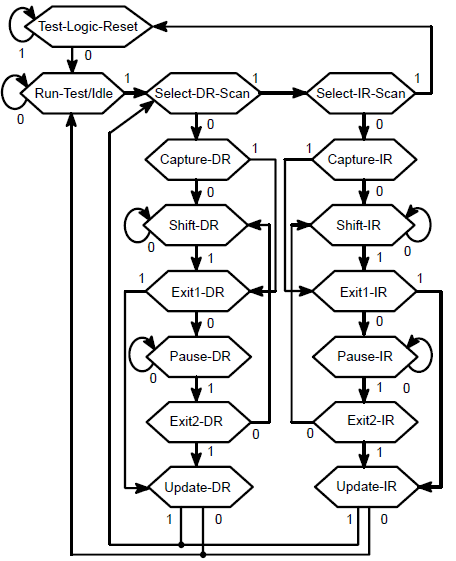


Figure 4: TAP State Diagram\*

\*Note: State Diagram drawn from IEEE 1149.1 documentation <http://focus.ti.com/lit/an/ssya002c/ssya002c.pdf>

|  |  |  |  |
| --- | --- | --- | --- |
| **State Details** | | **State Transition Details** | |
| Alpha Assignment | Description | On TMS "0" | On TMS "1" |
| A | Run-Test/Idle | A | B |
| B | Select-DR-Scan | C | I |
| C | Capture-DR | D | E |
| D | Shift-DR | D | E |
| E | Exit1--DR | F | H |
| F | Pause-DR | F | G |
| G | Exit2-DR | D | H |
| H | Update-DR | A | B |
| I | Select-IR-Scan | J | P |
| J | Capture-IR | K | L |
| K | Shift-IR | K | L |
| L | Exit1-IR | M | O |
| M | Pause-IR | M | N |
| N | Exit2-IR | J | O |
| O | Update-IR | A | B |
| P | Test-Logic-Reset | A | P |

Table 1: State Details



Table 2: Output Wire Behavior (Alpha from Table 1)

**6.0 Simulation Waveform Results**

The waveform produced by simulation can be seen in Figure 5. Table 3 conveniently maps the test bench testing order and subsequent results.

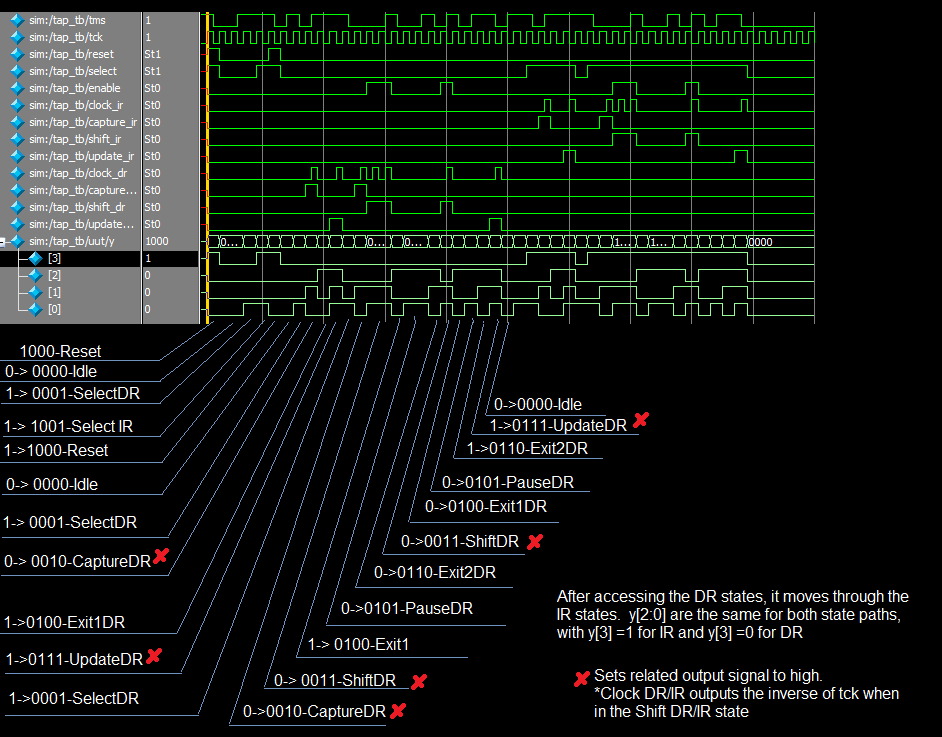
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Figure 5: Test Bench Waveform

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Cycle | Test Bench Test Pattern | Alpha | Pass/Fail |  | Cycle | Test Bench Test Pattern | Alpha | Pass/Fail |
| 1 | Test-Logic-Reset | P | Pass |  | 24 | Exit2-DR | G | Pass |
| 2 | Test-Logic-Reset | P | Pass |  | 25 | Update-DR | H | Pass |
| 3 | Run-Test/Idle | A | Pass |  | 26 | Run-Test/Idle | A | Pass |
| 4 | Run-Test/Idle | A | Pass |  | 27 | Select-DR-Scan | B | Pass |
| 5 | Select-DR-Scan | B | Pass |  | 28 | Select-IR-Scan | I | Pass |
| 6 | Select-IR-Scan | I | Pass |  | 29 | Capture-IR | J | Pass |
| 7 | Test-Logic-Reset | P | Pass |  | 30 | Exit1-IR | L | Pass |
| 8 | Run-Test/Idle | A | Pass |  | 31 | Update-IR | O | Pass |
| 9 | Select-DR-Scan | B | Pass |  | 32 | Select-DR-Scan | B | Pass |
| 10 | Capture-DR | C | Pass |  | 33 | Select-IR-Scan | I | Pass |
| 11 | Exit1-DR | E | Pass |  | 34 | Capture-IR | J | Pass |
| 12 | Update-DR | H | Pass |  | 35 | Shift-IR | K | Pass |
| 13 | Select-DR-Scan | B | Pass |  | 36 | Shift-IR | K | Pass |
| 14 | Capture-DR | C | Pass |  | 37 | Exit1\_IR | L | Pass |
| 15 | Shift-DR | D | Pass |  | 38 | Pause-IR | M | Pass |
| 16 | Shift-DR | D | Pass |  | 39 | Pause-IR | M | Pass |
| 17 | Exit1\_DR | E | Pass |  | 40 | Exit2-IR | N | Pass |
| 18 | Pause-DR | F | Pass |  | 41 | Shift-IR | K | Pass |
| 19 | Pause-DR | F | Pass |  | 42 | Exit1\_IR | L | Pass |
| 20 | Exit2-DR | G | Pass |  | 43 | Pause-IR | M | Pass |
| 21 | Shift-DR | D | Pass |  | 44 | Exit2-IR | N | Pass |
| 22 | Exit1\_DR | E | Pass |  | 45 | Update-IR | O | Pass |
| 23 | Pause-DR | F | Pass |  | 46 | Run-Test/Idle | A | Pass |

Table 3: Test Bench Pattern and Results (Alpha from Table 1)

**7.0 Behavioral Verilog and Test Bench Code**

Please see attached files *“****tap.v****”* and *“****tap\_tb.v****”* respectively for the behavioral Verilog and test bench code.