Xilinx SP605 (XC6SLX45) and DDR3 eval design

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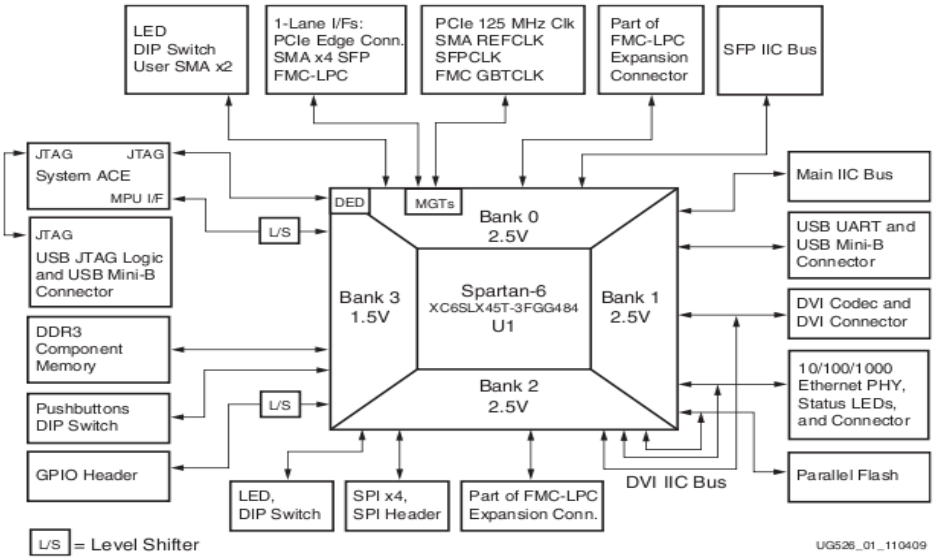
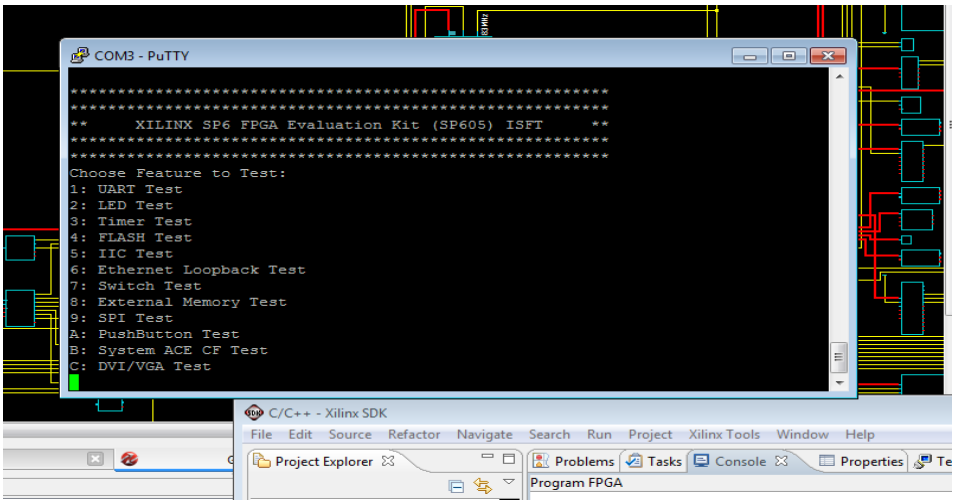
20th June 2011

The Xilinx SP605 evaluation board enables hardware and software developers to create or evaluate designs targeting the Spartan 6 XC6SLX45T FPGA.The SP605 provides board features common to many embedded processing systems. Some commonly used features include DDR3 component memory, x1 PCIe interface, (10/100/1000) Ethernet PHY, general purpose I/O, Flash, SPI, BPI and UART. The following diagram shows the high-level block diagram of the SP605, the peripherals it offers and the I/O bank to which each peripheral is connected.



The purpose of task 1a “Bring up MicroBlaze and DDR3 memory interface on Xilinx's SP605 Spartan 6 reference design” was to gain experience in building the Microblaze soft-core processor with DDR3 memory for the Spartan 6 XC6SLX45T FPGA using version 13.4 of Xilinx's XPS (Xilinx Platform Studio), EDK and SDK. It was felt that the experience gained from this task would be valuable in bringing up CRFS's own Spartan6 baseband board which has the larger XC6LXT150T FPGA and dual MT41J128M16HA-125IT Micron DDR3 SDRAM.

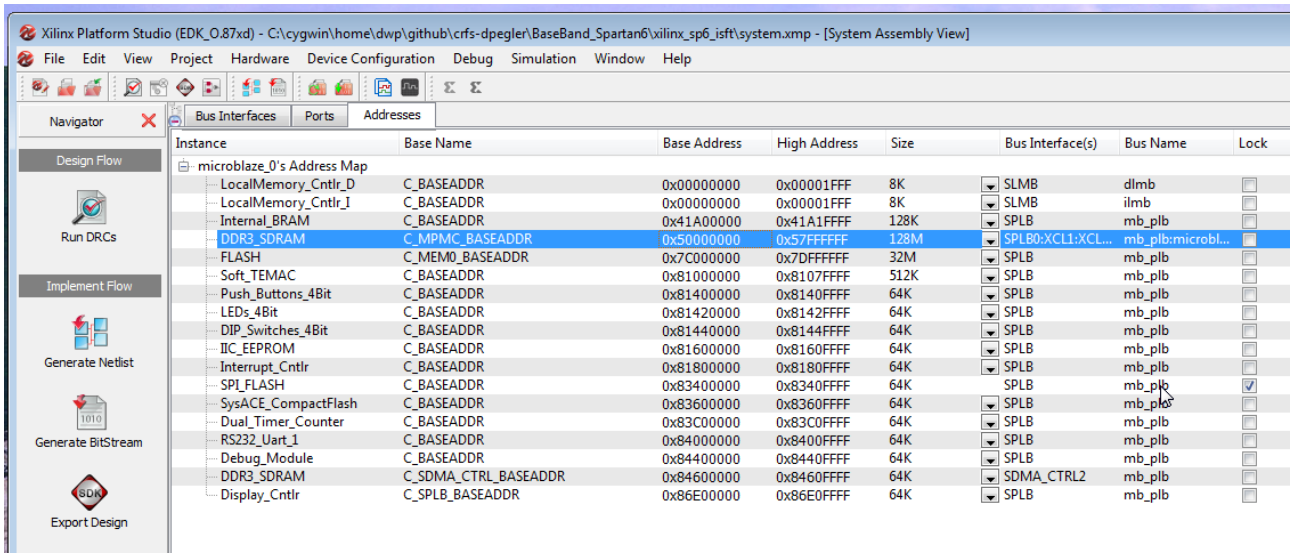
For the SP605 eval board, Xilinx provides numerous example designs, one of which is the BIST. The Built-In System Test (BIST) application uses an EDK MicroBlaze system to verify board functionality through a UART based terminal program which offers users a menu of tests to run. These tests include a UART, LED, Timer, Flash, IIc, Ethernet, Switch, DDR3 external memory, SPI, System ACE CF and DVI/VGA test; as shown below:



The BIST application uses the XPS EDK to build the hardware FPGA bitstream and SDK to build the application software which runs on the MicroBlaze (i.e. that shown in the Putty terminal labelled “Xilinx SP6 FPGA Evaluation Kit (SP605) ISFT” in the

diagram above). The Microblaze executable is split into two components, the bootloader and then numerous standalone test applications. The bootloader is a small application which run out of FPGA Block RAM which then dynamically loads standalone test applications out of the on-board CF (using the SystemACE interface) based on user requests (i.e. test 1 to C) input via the serial interface.

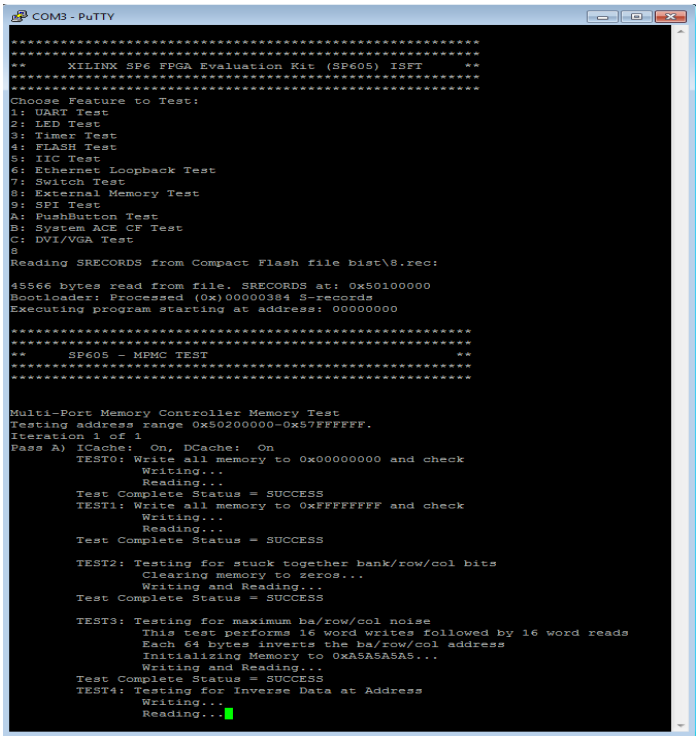
For the purpose of task 1a, test 8 “External Memory Test” proves a good method of verifying the Microblaze and DDR3 interface on the SP605 eval board. As show in the diagram below, the EDK in the BIST example design creates a memory map placing the 1Mbit MT41J64M16LA-187EM DDR3 SDRAM at base address 0x50000000:



The *Microprocessor Hardware Specification (MHS)* file (system.mhs) in the xilinx_sp6_isft project checked into github defines the hardware component of the MicroBlaze system such as Bus architecture, Peripherals, Processor Type, Connectivity, and Address space. As shown in the diagram above, the base address of the DDR3 SDRAM is mapped into the address space of the MicroBlaze at location *0x50000000* and this is defined in the Multi-Port Memory Controller (MPMC) section of the MHS file like so:

> *[dwp@tesla xilinx_sp6_isft]$ egrep -r "C_MPMC_BASEADDR" .*
> *./system.mhs: PARAMETER C_MPMC_BASEADDR = 0x50000000*

The diagram below shows the results of BIST test application 8 “External Memory Test” running on the SP605 testing the 1 Gbit Micron MT41J64M16LA-187EM DDR3 SDRAM.



The following screen shot from the XPS EDK shows Device Utilization Summary for the BIST application built for the XC6SLX45T-FG484 device:

Device Utilization Summary (actual values)				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	9,820	54,576	17%	
Number used as Flip Flops	9,813			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	7			
Number of Slice LUTs	10,062	27,288	36%	
Number used as logic	9,130	27,288	33%	
Number using O6 output only	6,503			
Number using O5 output only	313			
Number using O5 and O6	2,314			
Number used as ROM	0			
Number used as Memory	455	6,408	7%	
Number used as Dual Port RAM	224			
Number using O6 output only	4			

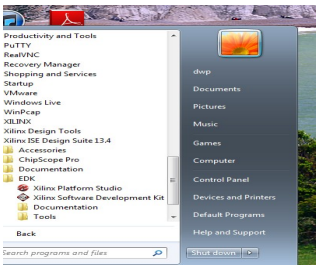
and the following table shows BRAM Utilizaion:

Number of occupied Slices	4,153	6,822	60%	
Nummber of MUXCYs used	1,536	13,644	11%	
Number of LUT Flip Flop pairs used	12,318			
Number with an unused Flip Flop	3,593	12,318	29%	
Number with an unused LUT	2,256	12,318	18%	
Number of fully used LUT-FF pairs	6,469	12,318	52%	
Number of unique control sets	749			
Number of slice register sites lost to control set restrictions	2,858	54,576	5%	
Number of bonded IOBs	181	296	61%	
Number of LOCed IOBs	181	181	100%	
IOB Flip Flops	133			
Number of RAMB16BWERs	77	116	66%	
Number of RAMB8BWERs	2	232	1%	
Number of BUFIO2/BUFIO2_2CLKs	3	32	9%	
Number used as BUFIO2s	3			

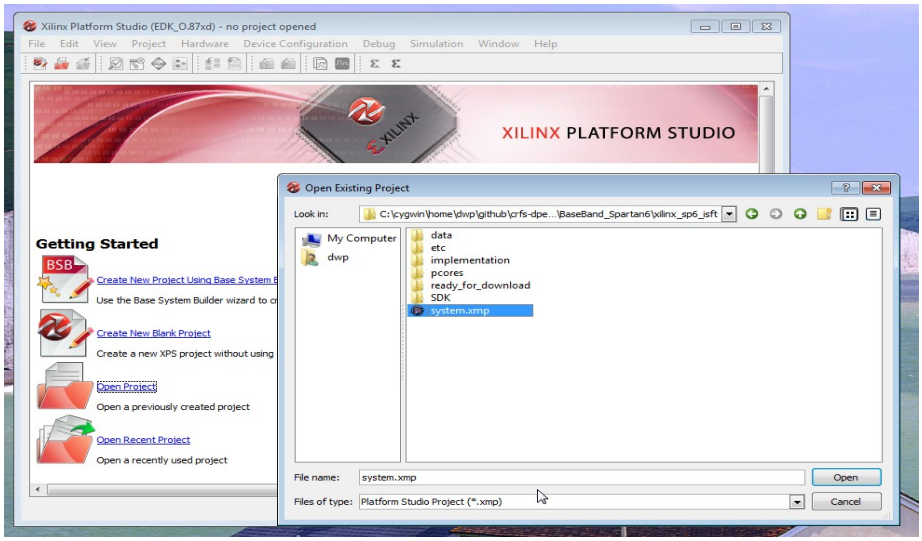
The Xilinx XPS/SDK and EDK project files for the Built-In System Test (BIST) application used to test the MicroBlaze and DDR3 memory interface as described in this document is checked into CRFS' area on git hub. All the BIST project files are stored in directory “xilinx_sp6_isft” under the BaseBand_Spartan6 git repository. The following diagram shows how to clone a copy of the BaseBand_Spartan6 repository, and navigate to the “xilinx_sp6_isft” XPS project directory:

```
~/github/crfs-dpegler/BaseBand_Spartan6/xilinx_sp6_isft

dwp@doppler ~
$ cd github/crfs-dpegler/

dwp@doppler ~/github/crfs-dpegler
$ git clone https://crfs-dpegler@github.com/CRFS/BaseBand_Spartan6.git
Cloning into 'BaseBand_Spartan6'...
Password for 'https://crfs-dpegler@github.com':
remote: Counting objects: 815, done.
remote: Compressing objects: 100% (436/436), done.
remote: Total 815 (delta 287), reused 812 (delta 287)
Receiving objects: 100% (815/815), 8.58 MiB | 412 KiB/s, done.
Resolving deltas: 100% (287/287), done.

dwp@doppler ~/github/crfs-dpegler
$ cd BaseBand_Spartan6/

dwp@doppler ~/github/crfs-dpegler/BaseBand_Spartan6
$ cd xilinx_sp6_isft/

dwp@doppler ~/github/crfs-dpegler/BaseBand_Spartan6/xilinx_sp6_isft
$ ls
data  etc  implementation  pcores  ready_for_download  SDK  system.mhs  system.xmp

dwp@doppler ~/github/crfs-dpegler/BaseBand_Spartan6/xilinx_sp6_isft
$
```

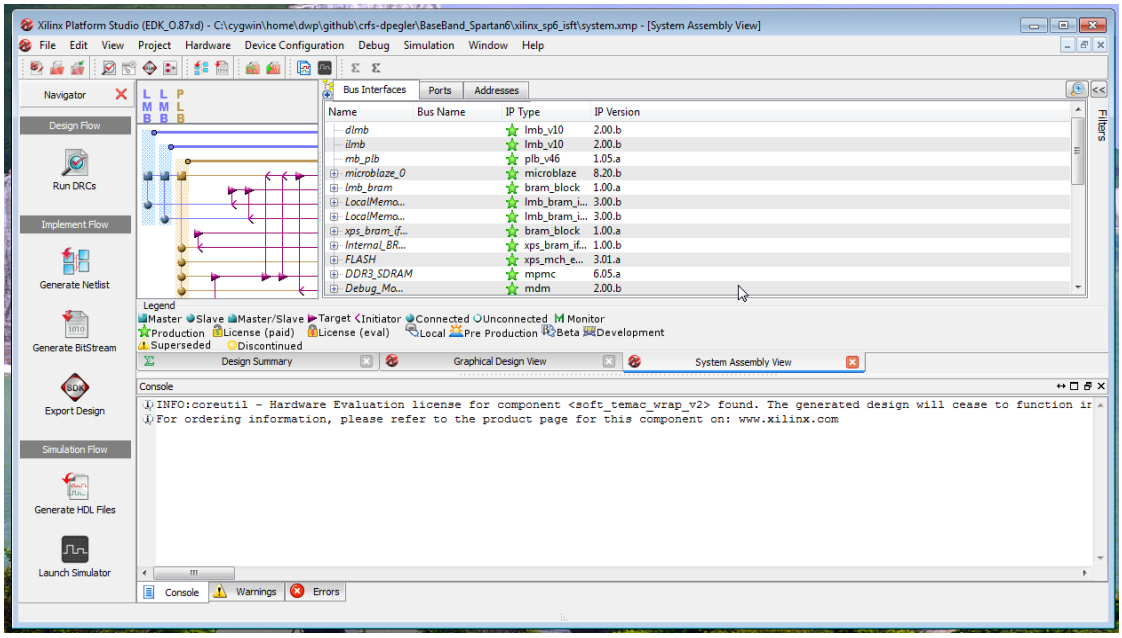
To build the BIST project, start Xilinx Platform Studio from Start -> All Programs -> Xilinx ISE Design Suite 13.4 -> EDK -> Xilinx Platform Studio like so :



From Xilinx Platform Studio, Select “Open Project” and then navigate to BaseBand_Spartan6/xilinx_sp6_isft directory and select “system.xmp” and then Open :

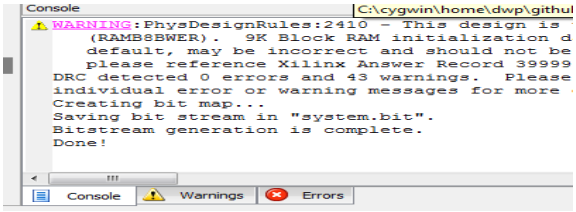


and this will open the EDK :

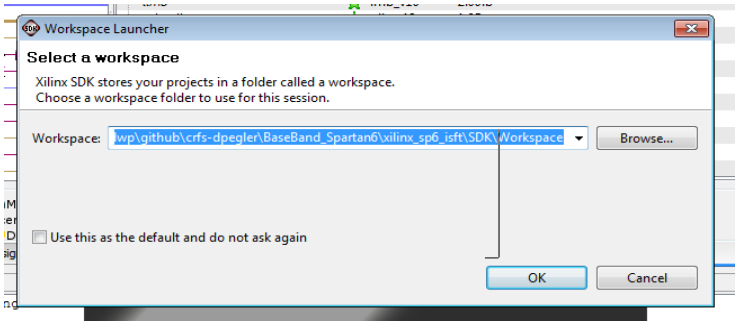


At this stage you have two options. You can either rebuild the MicroBlaze from scratch (i.e. from HDL) by selecting “Generate Bitsteam” in the “Implement Flow” section or skip this (as the MicroBlaze is pre-built) and invoke the SDK to re-build the MicroBlaze software applications by selecting “Export Design”.

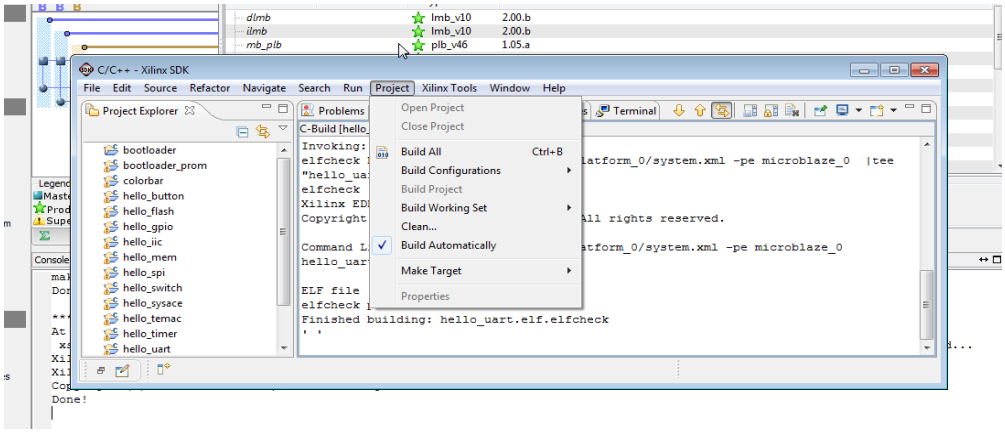
If you select “Generate Bitstream” go and have a coffee, as this takes around 20 minutes (on a Win7 Intel i3 machine) to build the Microblaze. When“Bitstream generation is complete” is displayed in the “Console” window, as show in the diagram below, the MicroBlaze build is complete.



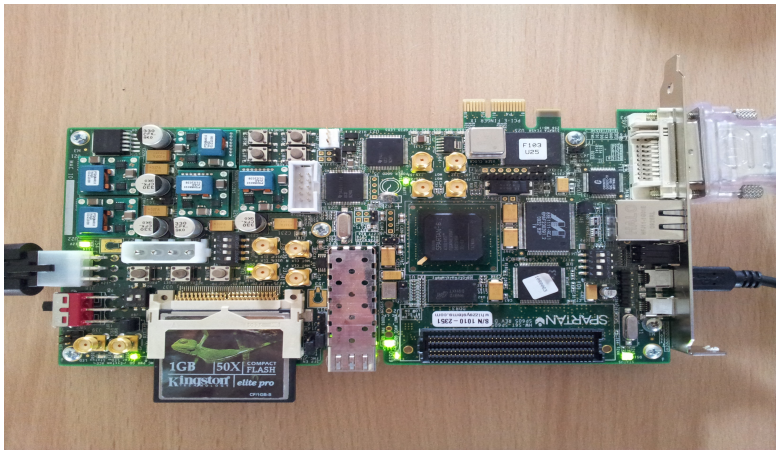
Selecting “Export Design” and then “Export and Launch SDK”, exports the FPGA bit stream image, from the EDK to the SDK and then invokes the SDK so that the FPGA image and the MicroBlaze application binaries (built under the SDK) can be programmed into the XC6SLX45T FPGA at the same time. When the SDK “Workspace Launcher” window appears, navigate to the “Workspace” directory (that you checked out of github repository BaseBand_Spartan6) like so:



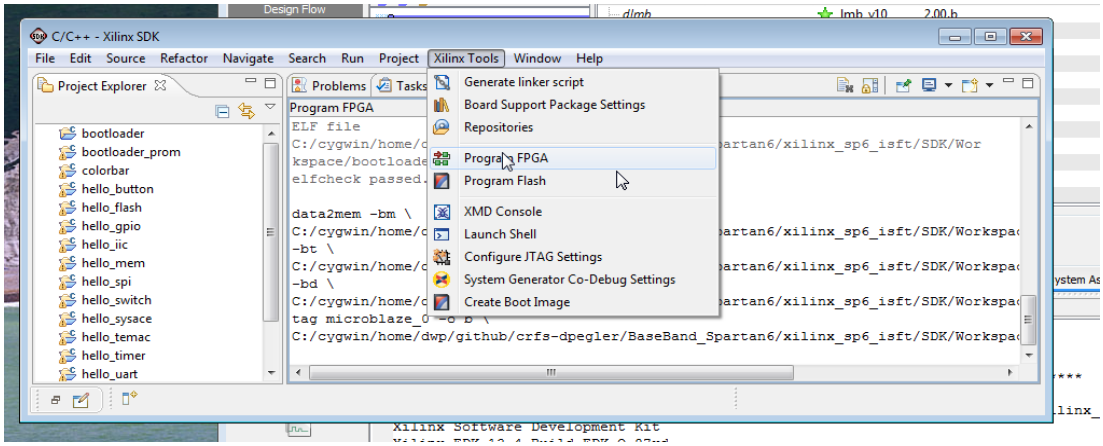
This will invokes the C/C++ Xilinx SDK. As shows in the diagram below, to start building the MicroBlaze BIST applications, select “Project” from the pull down menu and either select “Clean” to clean up the detritus left behind by the previous build (i.e. make clean) , or “Build All” to do a complete, from scratch, build of all the applications.



Once the build is complete, to load the MicroBlaze and BIST applications to the XC6SLX45T FPGA, ensure the SP605 is powered up and the USB JTAG lead is connected between the board and your Win7/XP PC as show below:



Next under the SDK, select “Xilinx Tools” and then Program FPGA like so:



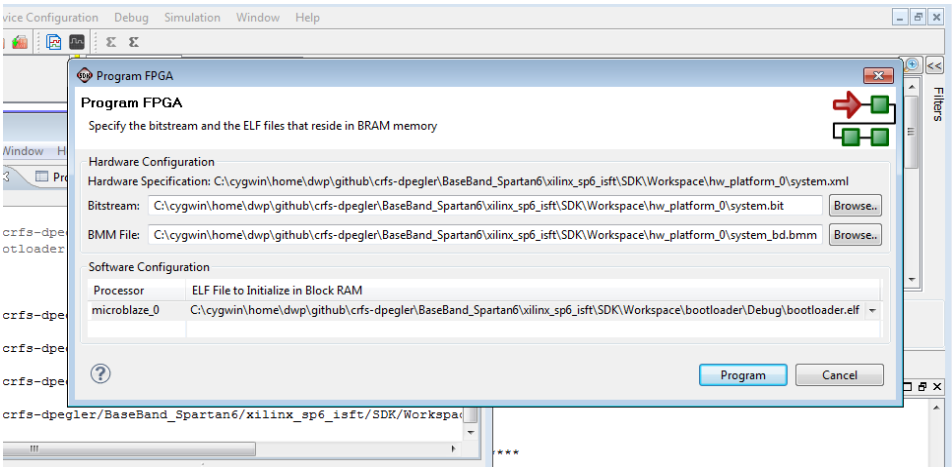
This will open the “Program FPGA” window which allows you specify the FPGA bitstream (image) and MicroBlaze bootloader ELF file that needs to be programmed into BlockRAM. The bitstream (system.bit) file image and BMM (Block RAM Memory Map) file (system_bd.bmm) required for Hardware Configuration can be found under

BaseBand_Spartan6/xilinx_sp6_isft/SDK/Workspace/hw_platform_0

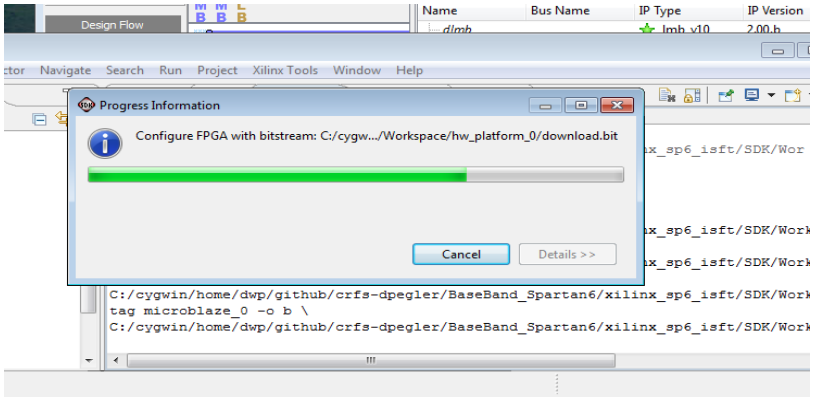
and the ELF bootloader File required by the Software Configuration (to initialise the Block RAM) can be found under

BaseBand_Spartan6/xilinx_sp6_isft/SDK/Workspace/bootloader/Debug/bootloader.elf

as show in the diagram below:



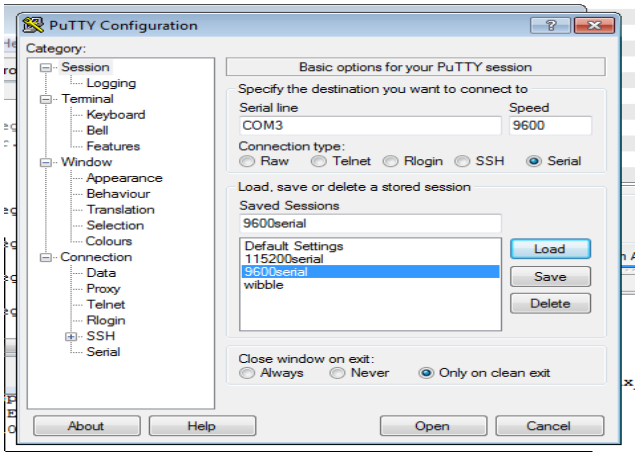
Finally click “Program” and with a some luck the three images should start being downloaded to the XC6SLX45T FPGA via JTAG and you should get a programming window with a green progress bar like so:



To connect to the serial port on the SP605 (to try the BIST utilities), you will need to connect a second USB -> mini USB cable between the board and the Win7/XP machine you are using. On Windows 7, Microsoft in their wisdom have removed HyperTerm so I would recommend installing PuTTy (which is downloadable from the following URL) to act as a serial terminal:

http://the.earth.li/~sgtatham/putty/latest/x86/putty-0.62-installer.exe

To configure PuTTy to act as a serial terminal, select “Serial” under the “Connection type”, set the “Serial line” to COM3 and “Speed” to 9600 as show below:



and then click “Open”. This will invoke a simple terminal emulater connected to the USB -> UART bridge (COM3) on the SP605 to allow access to the BIST test utlity menu from which test 8, “External Memory Test” can be invoked to test the Micron MT41J64M16LA-187EM DDR3 SDRAM which is mapped into the MicroBlaze address space at location 0x5000000.