$$ADD_{32} \coloneqq 15.376 \quad ADD_{64} \coloneqq 15.992 \\ SUB_{64} \coloneqq 15.992 \\ COMP_{64} \coloneqq 16.601 \\ MUX_{64} \coloneqq 15.168 \\ REG_{16} \coloneqq 4.284 REG_{32} \vDash 4.973 \quad REG_{64} \coloneqq 5.832 \\ SHL_{64} \coloneqq 19.817 \\ SHR_{32} \coloneqq 18.330 \quad SHR_{64} \coloneqq 19.817 \\ DIV_{32} \coloneqq 102.831 DIV_{64} \coloneqq 303.02 \\ MOD_{64} \coloneqq 312.498 \\ DIC \coloneqq ADD_{32} \\ IO \coloneqq ADD_{32} \\ IO \coloneqq ADD_{32} \\ IO \coloneqq ADD_{32} + \max(IO2,IO3) \\ I2 \coloneqq ADD_{32} + \max(IO2,IO3) \\ I2 \coloneqq ADD_{32} + \max(IO1,III) \\ I2div2 \coloneqq SHR_{32} + I2 div4 \\ avg \coloneqq REG_{32} + I2div4 \\ avg \coloneqq REG_{32} + I2div4 \\ avg \coloneqq REG_{32} + I2 \\ I4 \coloneqq ADD_{32} + i1 \\ I3 \coloneqq ADD_{32} + i2 \\ I4 \coloneqq ADD_{32} + i5 \\ I7 \coloneqq ADD_{32} + i5 \\ I7 \coloneqq ADD_{32} + i6 \\ I8 \vDash ADD_{32} + i8 \\ I10 \coloneqq ADD_{32} + i9 \\ I11 \coloneqq ADD_{32} + i0 \\ I2 \coloneqq ADD_{32} + i0 \\ I3 \coloneqq ADD_{32} + i1 \\ I3 \coloneqq ADD_{32} + i2 \\ I4 \coloneqq ADD_{32} + i1 \\ I3 \coloneqq ADD_{32} + i2 \\ I2 \coloneqq ADD_{32} + i1 \\ I3 \coloneqq ADD_{32} + i1 \\ I3 \coloneqq ADD_{32} + i2 \\ I11 \coloneqq ADD_{32} + i2 \\ I11 \coloneqq ADD_{32} + i1 \\ I12 \coloneqq ADD_{32} + i1 \\ I13 \coloneqq ADD_{32} + i1 \\ I3 \coloneqq ADD$$

t14 := ADD₃₂ + t13
final := REG₃₂ + t14
final = 220.237

5)
$$d := ADD_{64}$$

$$g := ADD_{64}$$

$$f := SUB_{64}$$

$$dEQe := COMP_{64} + max(d, e)$$

$$dLTe := COMP_{64} + max(dLTe, d, e)$$

$$h := MUX_{64} + max(dLTe, d, e)$$

$$h := MUX_{64} + max(dEQe, g, f)$$

$$greg := REG_{64} + g$$

$$hreg := REG_{64} + h$$

$$xrin := SHL_{64} + hreg$$

$$zrin := SHR_{64} + greg$$

$$x := REG_{64} + xrin$$

$$z := REG_{64} + xrin$$

$$z := REG_{64} + zrin$$

$$x = 94.41$$
6)
$$tl.:= ADD_{32}$$

$$r1 := REG_{32} + t1$$

$$t2 := REG_{32} + t2$$

$$t3 := ADD_{32} + r1$$

$$r2 := REG_{32} + t3$$

$$t4 := ADD_{32} + r2$$

$$r3 := REG_{32} + t3$$

$$t4 := ADD_{32} + r3$$

$$r4 := REG_{32} + t4$$

$$t5 := ADD_{32} + r4$$

$$r5 := REG_{32} + t5$$

$$t6 := ADD_{32} + r5$$

$$r6 := REG_{32} + t6$$

$$t7 := ADD_{32} + r6$$

$$r7 := REG_{32} + t7$$

$$avgwire := DIV_{32} + r7$$

$$avgwire := REG_{16} + avgwire$$