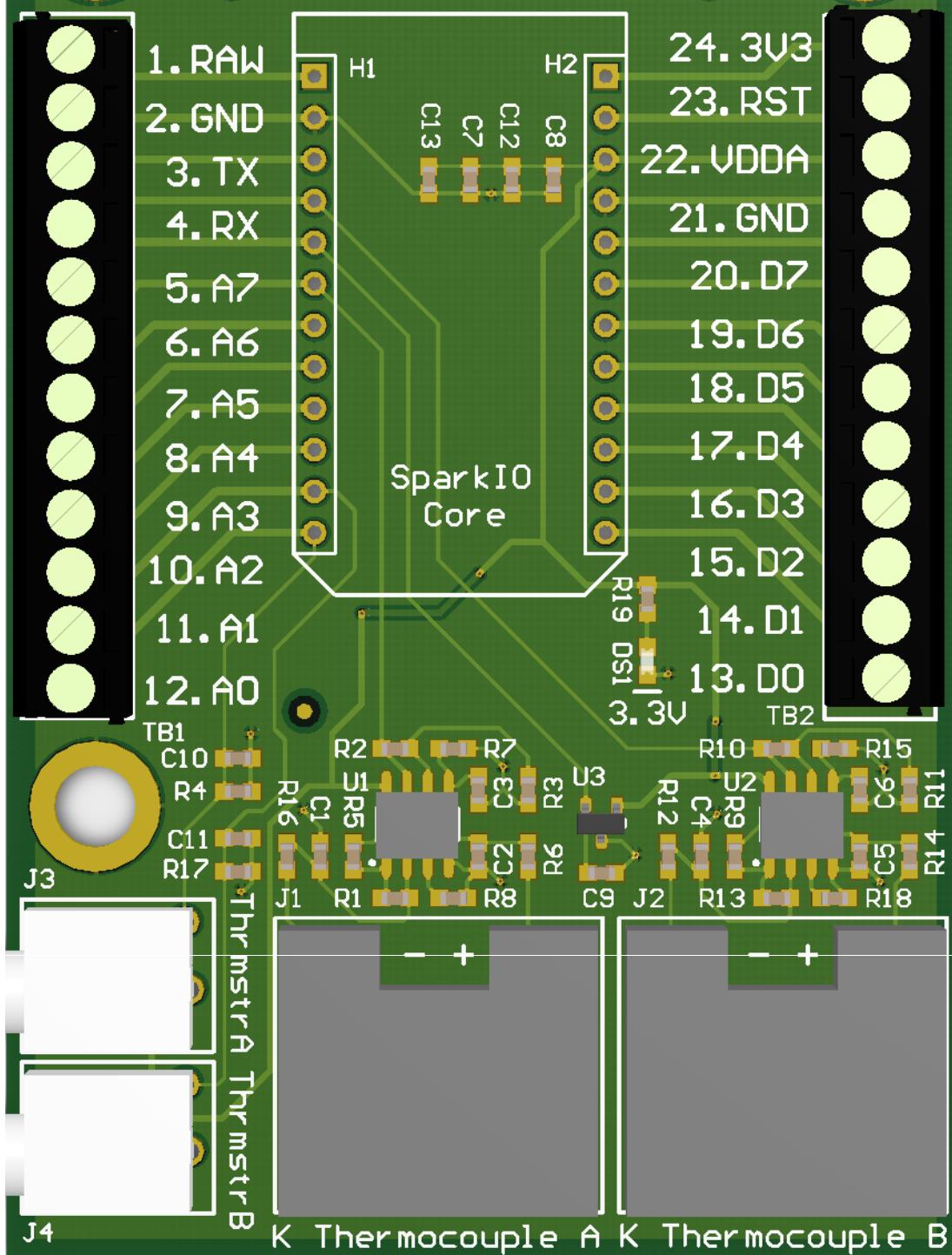
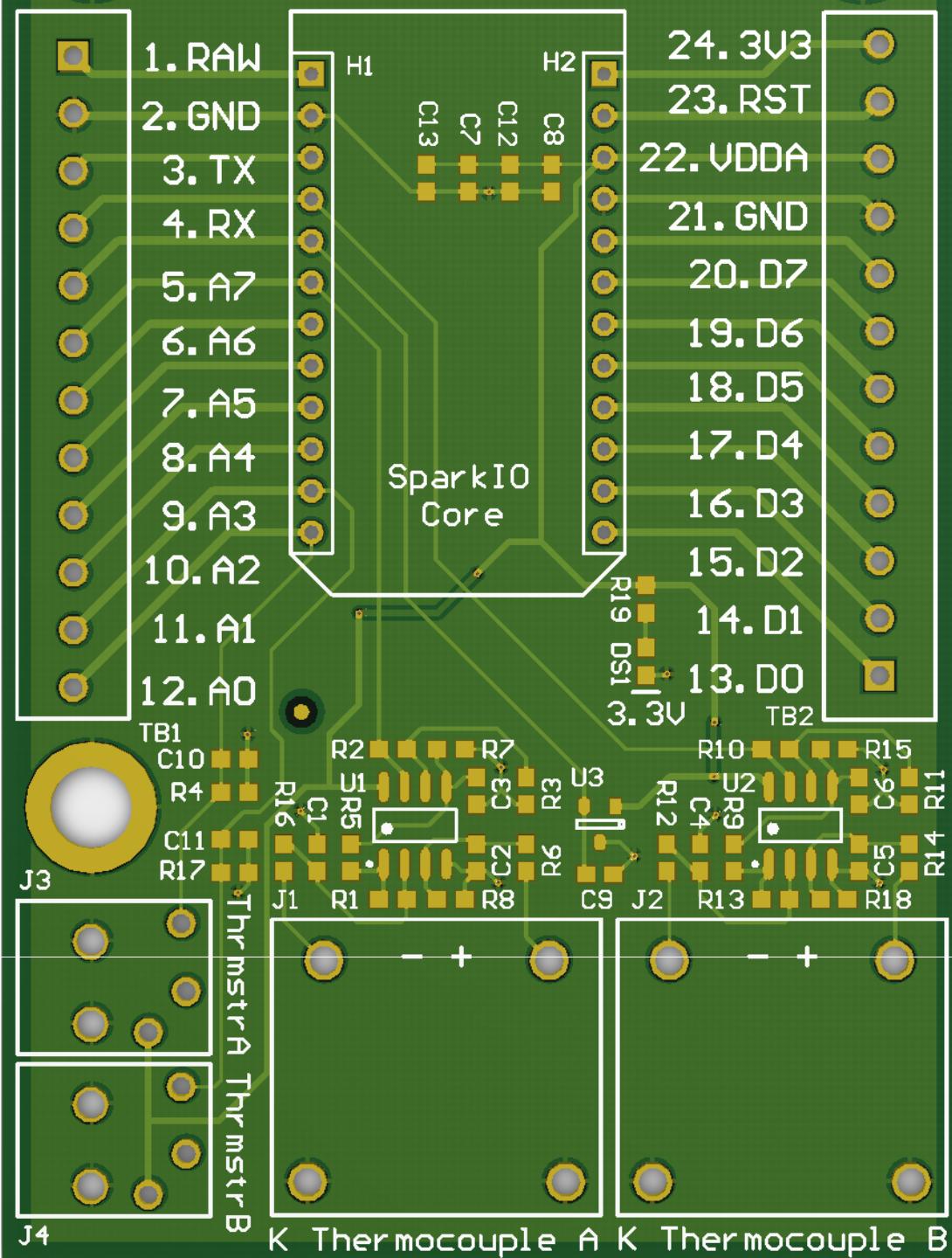
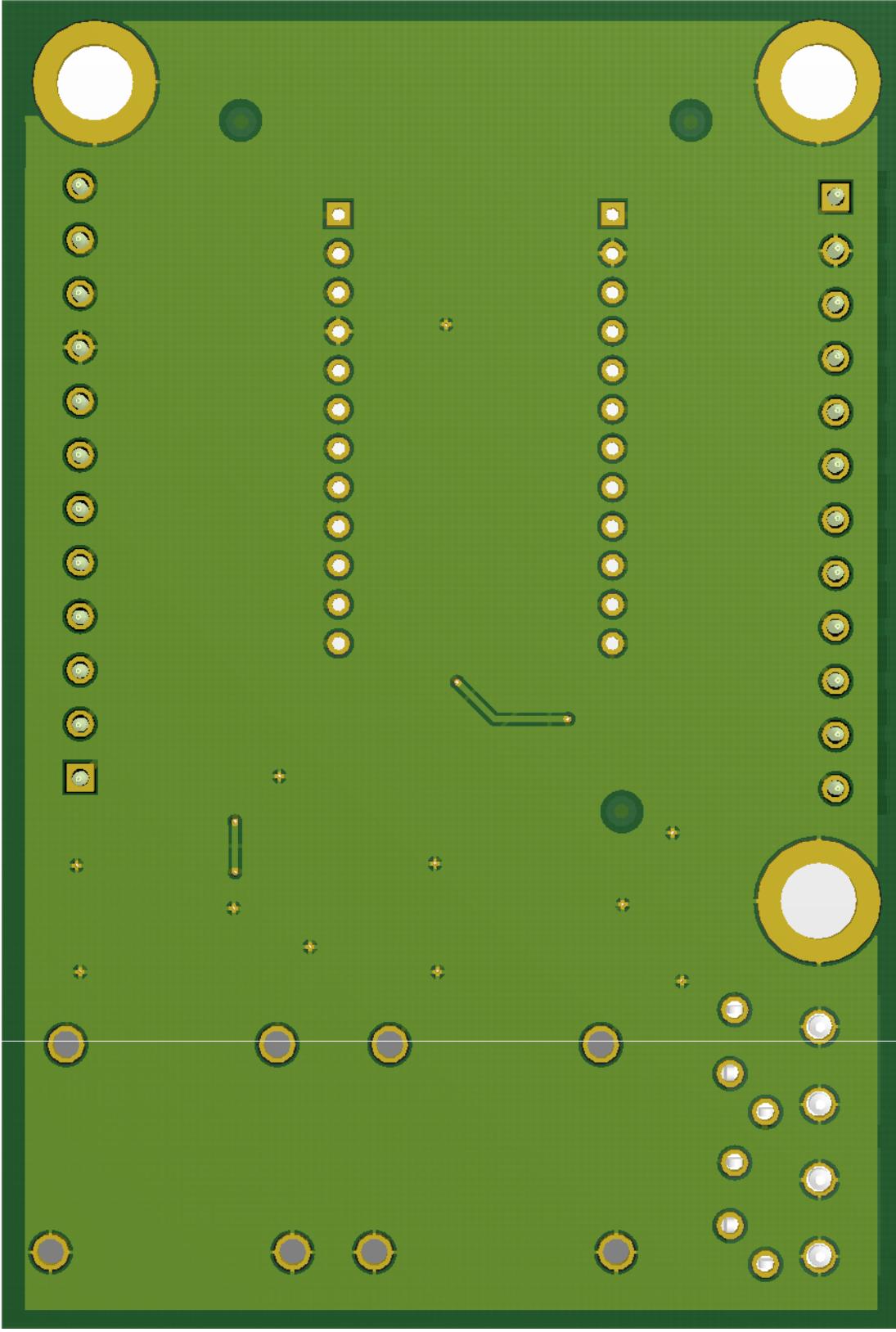


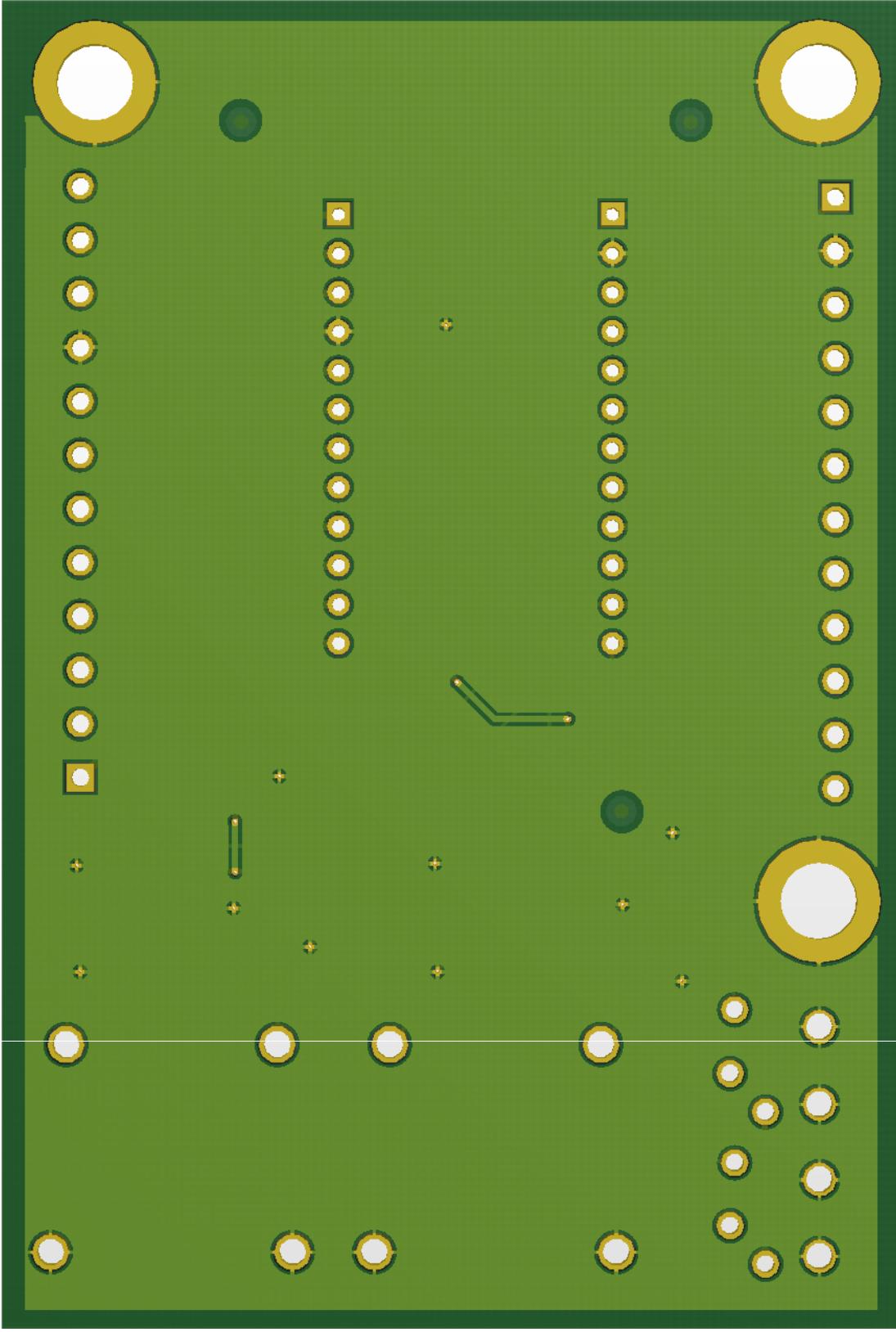
SparkIO Temperature
Sensing Shield
CharPCB Rev A

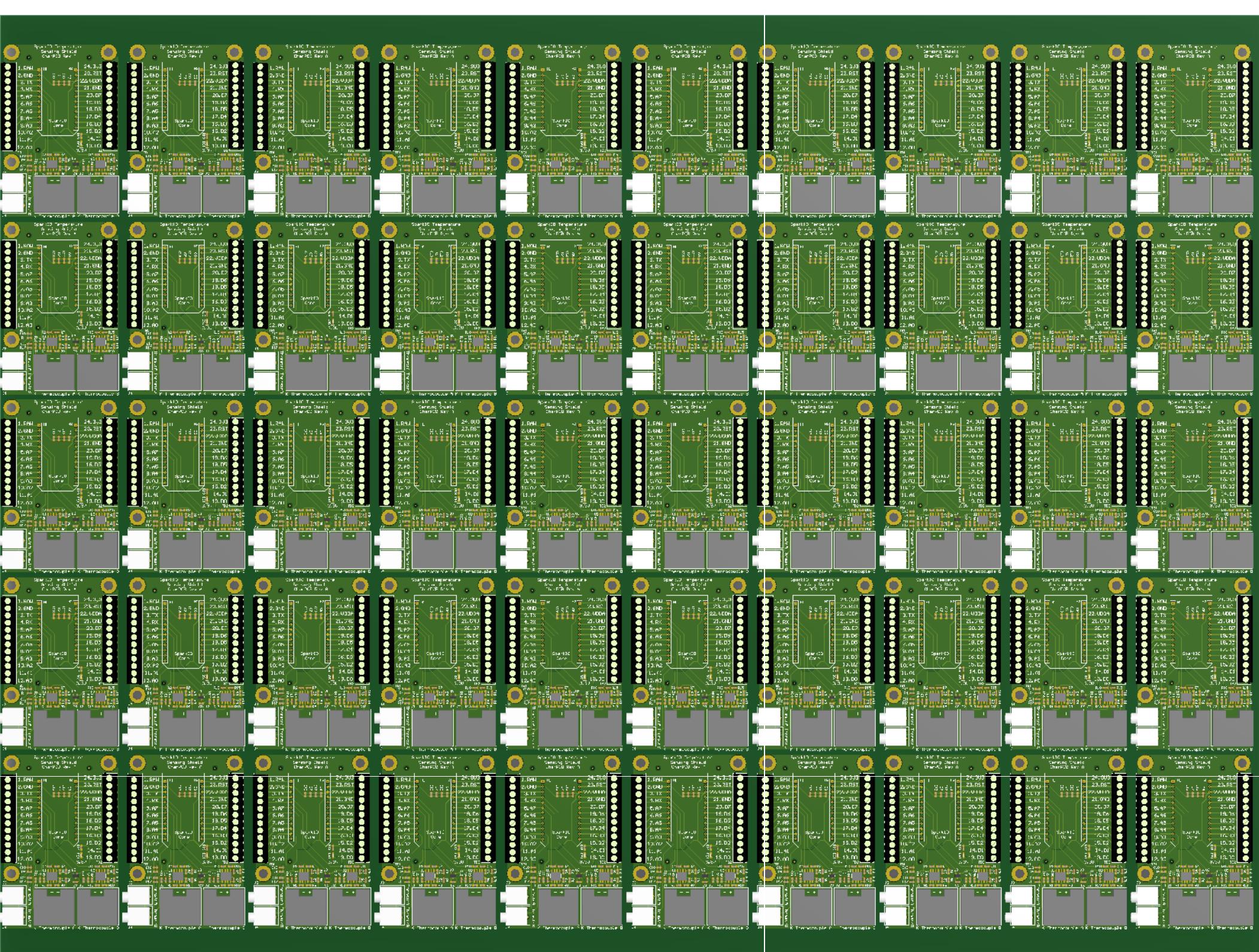


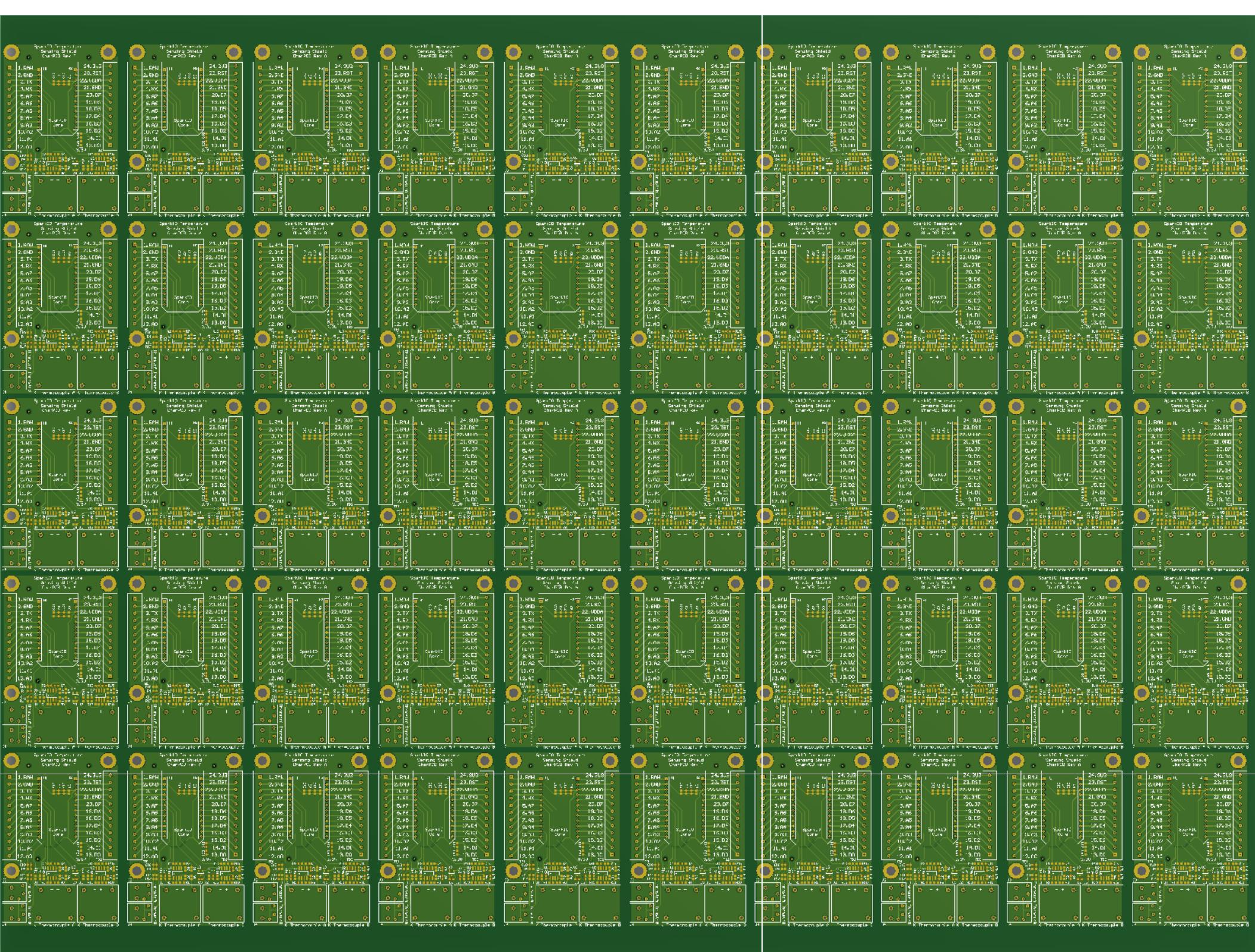
SparkIO Temperature
Sensing Shield
CharPCB Rev A

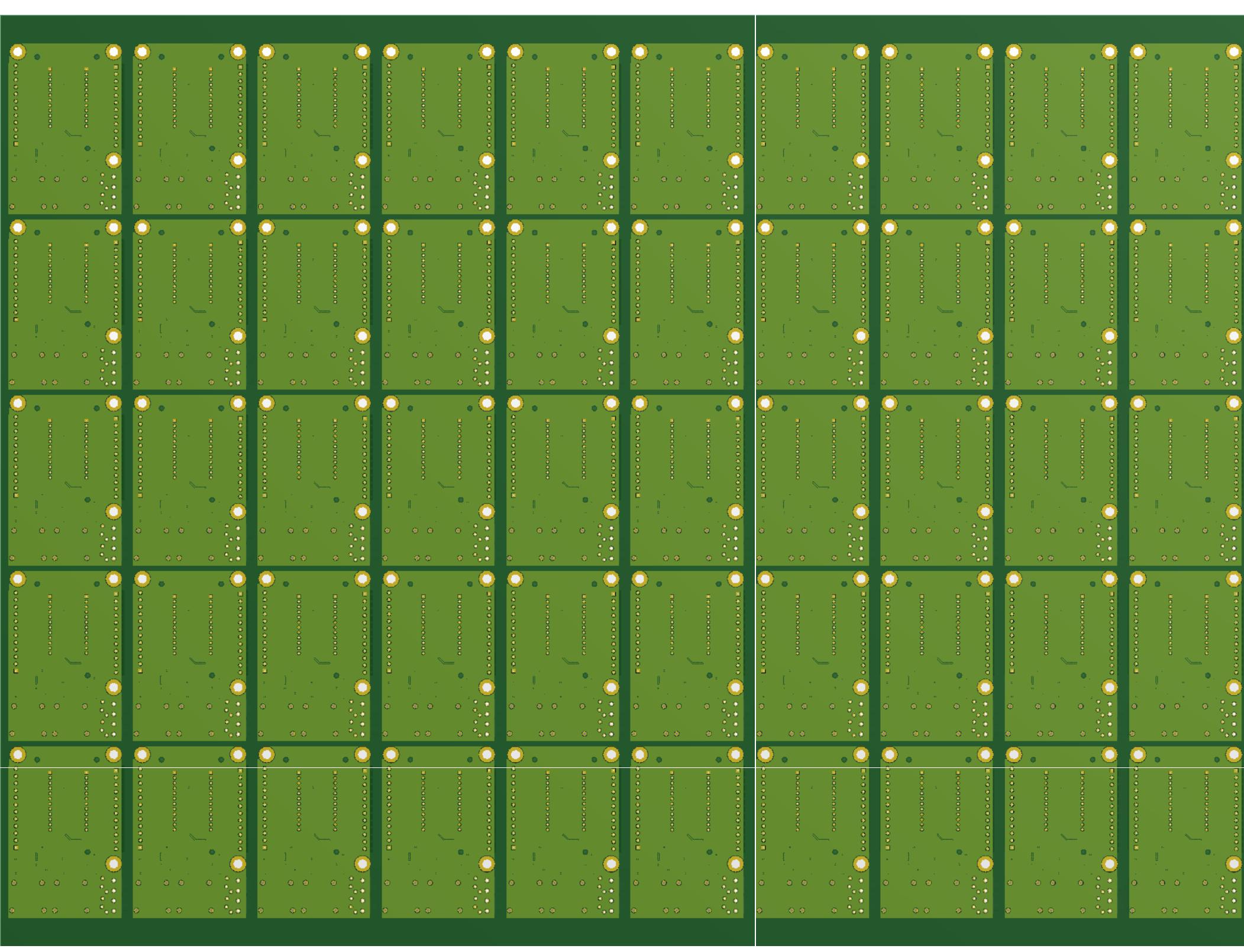


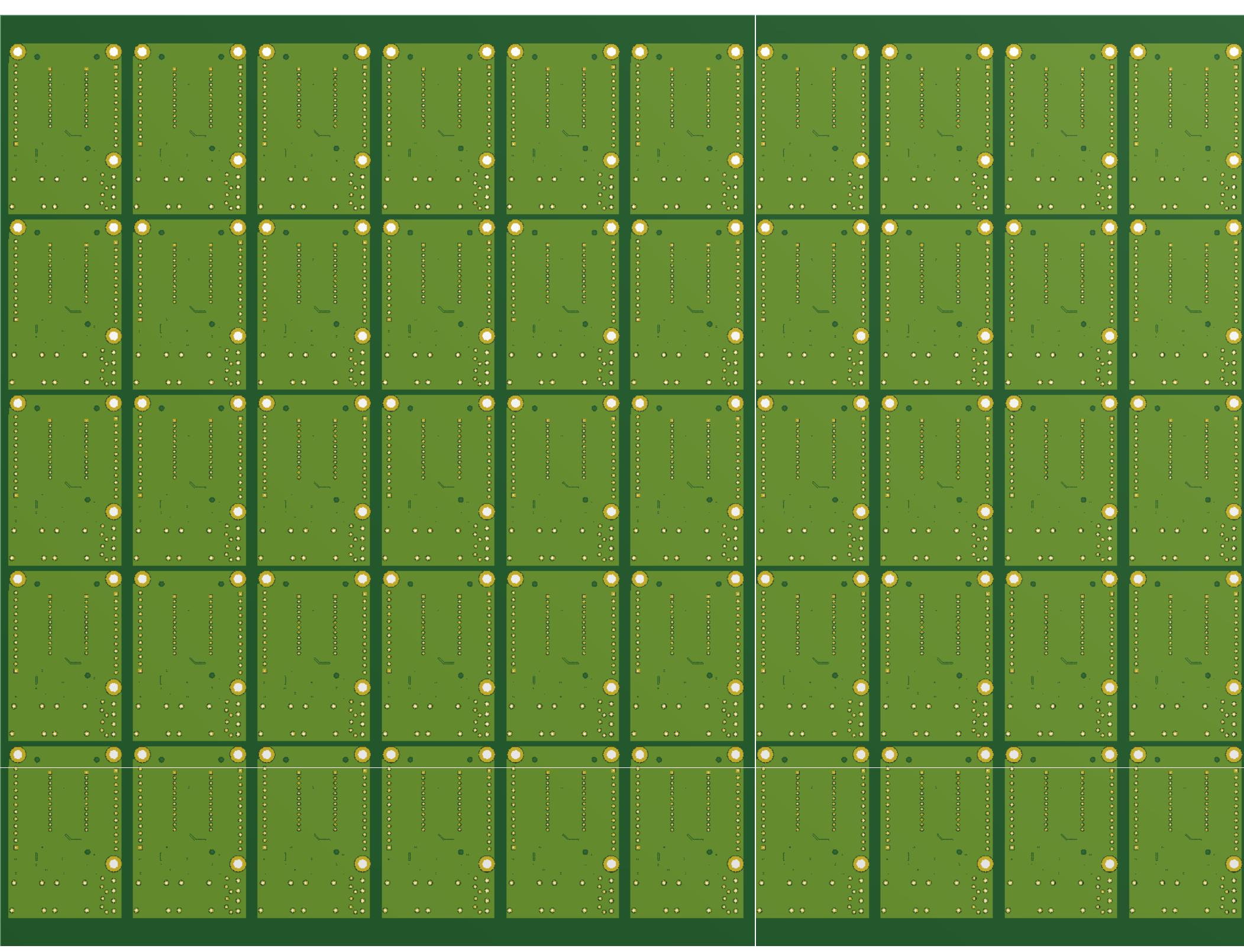


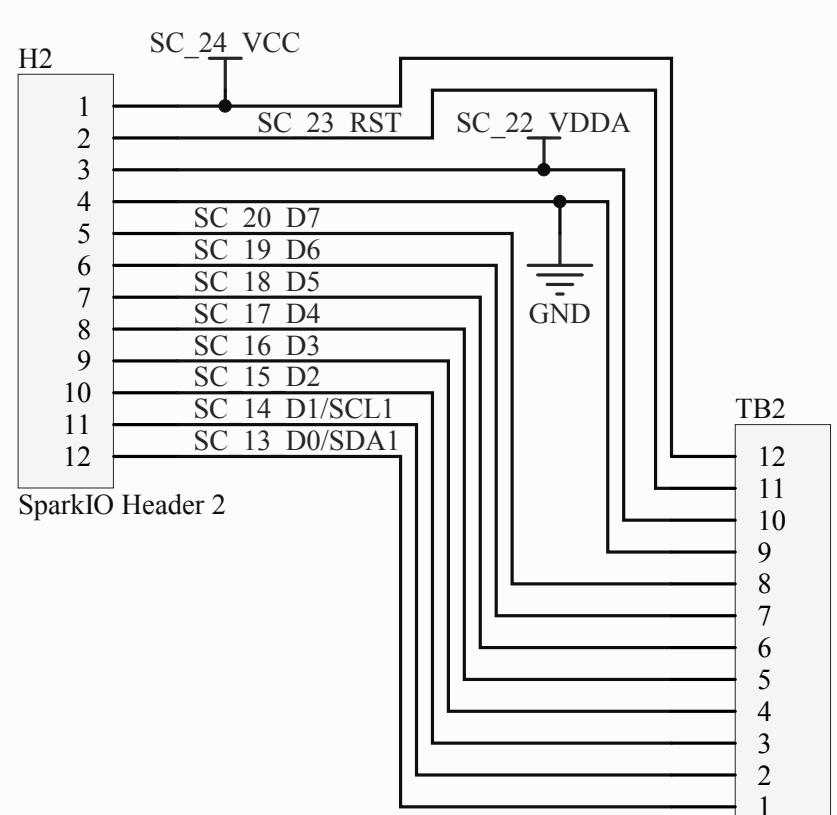
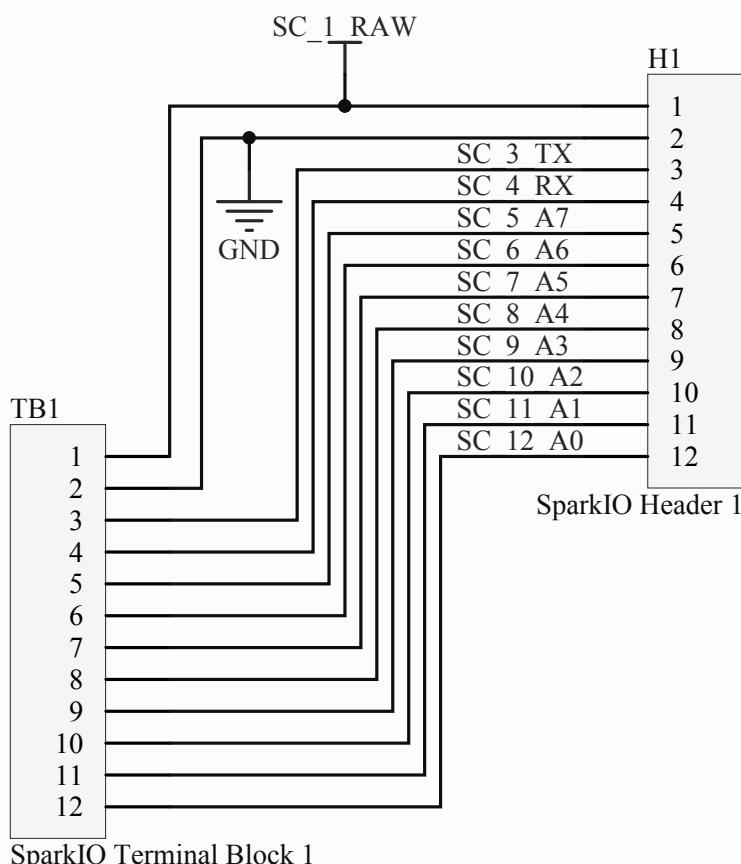












SparkIO Terminal Block 1

*SparkIO Module
RAW = Diode drop down from +5VUSB
VCC = 3.3V, 500mA Max
VDDA = 3.3V through 500mA ferrite, analog VDD
RST = Reset switch on Spark.io Module
Spark Core has male headers - need female headers here

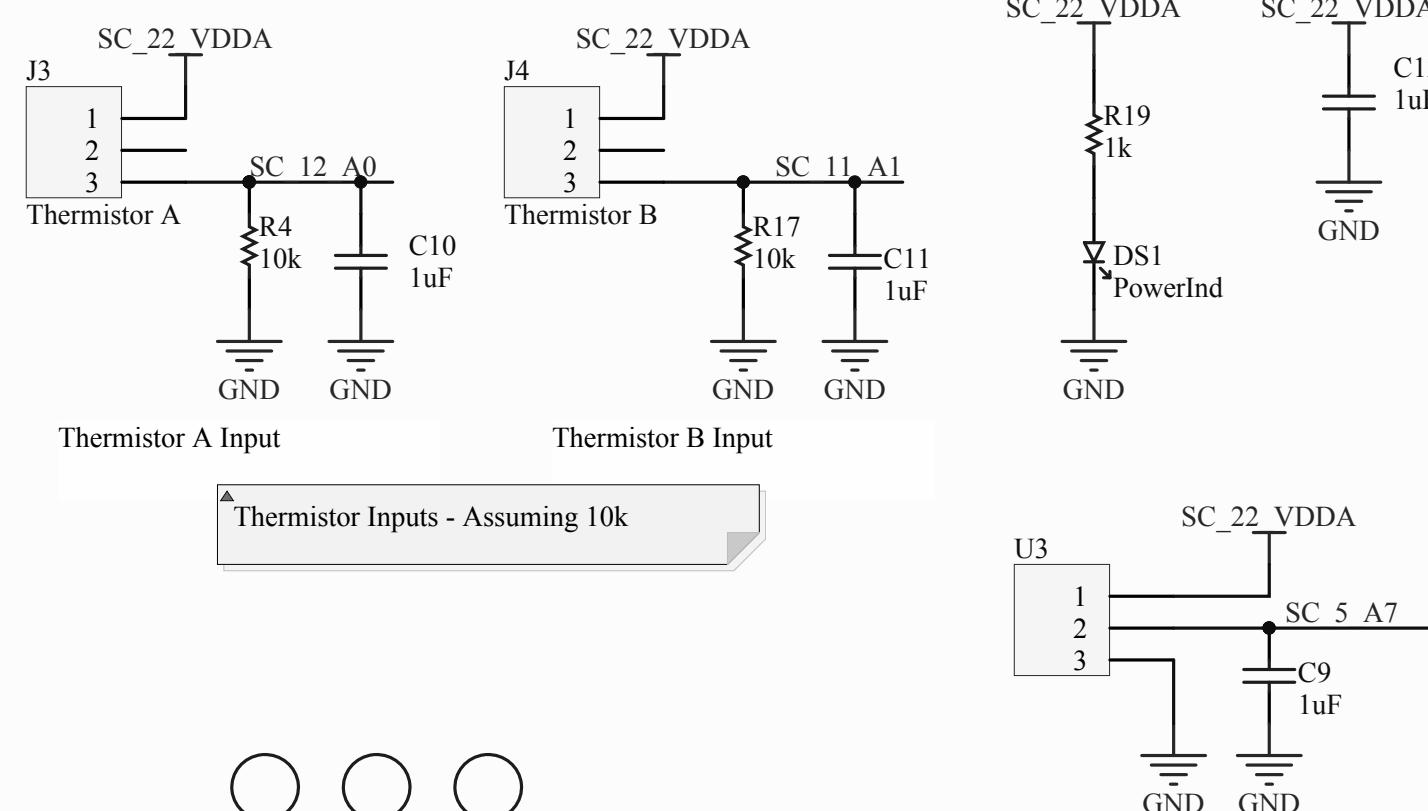
Chose ADC Pins on Core specifically to leave SPI interface and as many timer channels intact as possible.

Op Amp Circuits are a cascaded two stage amplifier:
A Gain = 10 stage followed by a Gain = 22 stage to accomplish overall gain of 220

Linear approximation of a K-type thermocouple is about 40.8uV per degree C from -200C to +1350C
At 25C: V=1020uV = 1.02mV
At 100C, V=4008uV = 4.008mV
At 1000C, V=40.8mV
At 1350C, V=55.08mV

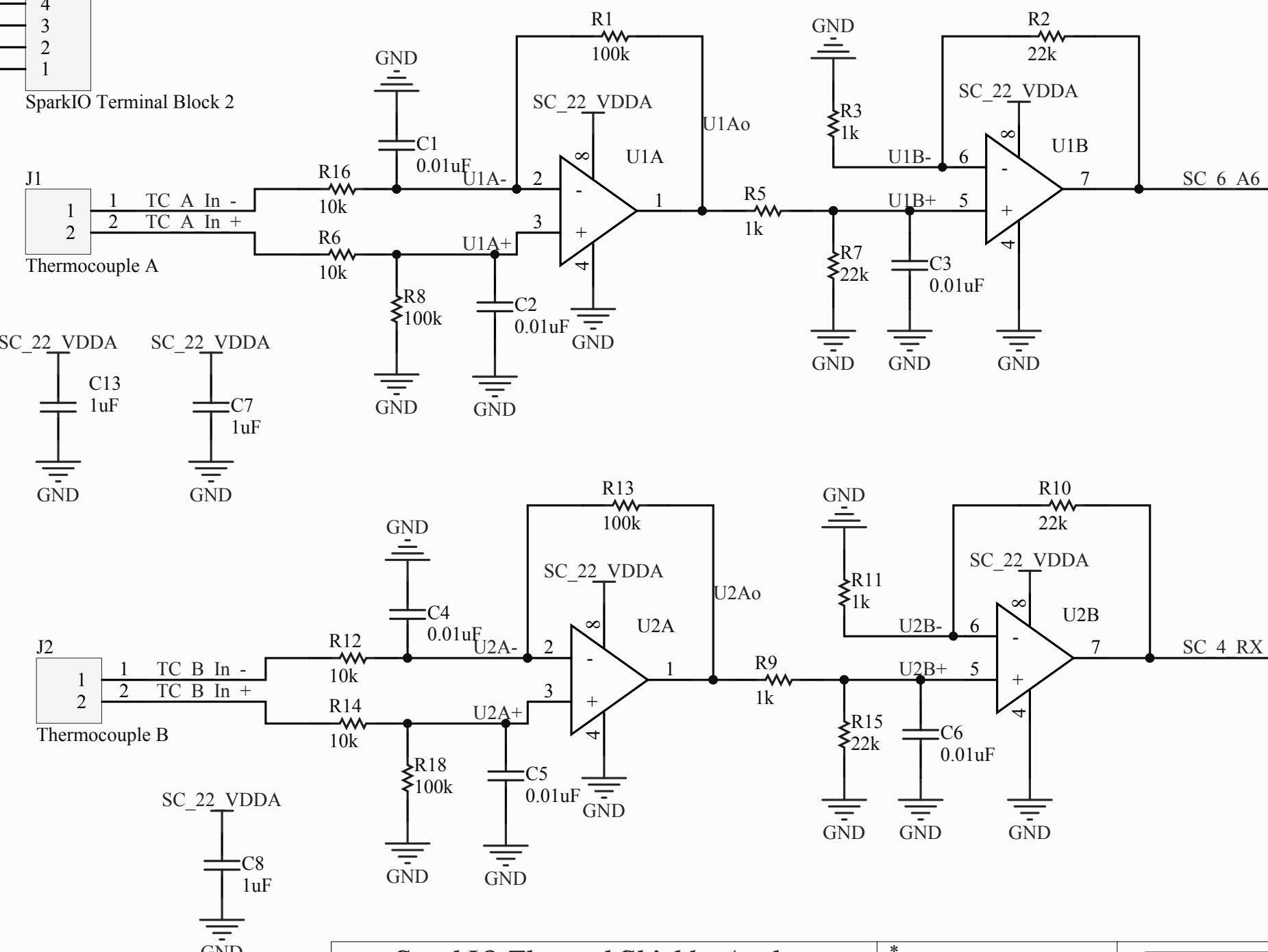
Desired range is roughly up to 600F or 0C to 350C
At 0C: V=0V
At 350C: V=14.28mV

To scale this voltage to 3.2V, gain needed is
 $A = 3.2V/14.28mV = 224$



Cold Junction Temperature Compensation Thermistor
*Must be located very close to thermocouple connectors
U3 is analog thermistor IC

FID1 FID2 FID3



Title **SparkIO Thermal Shield - Analog**

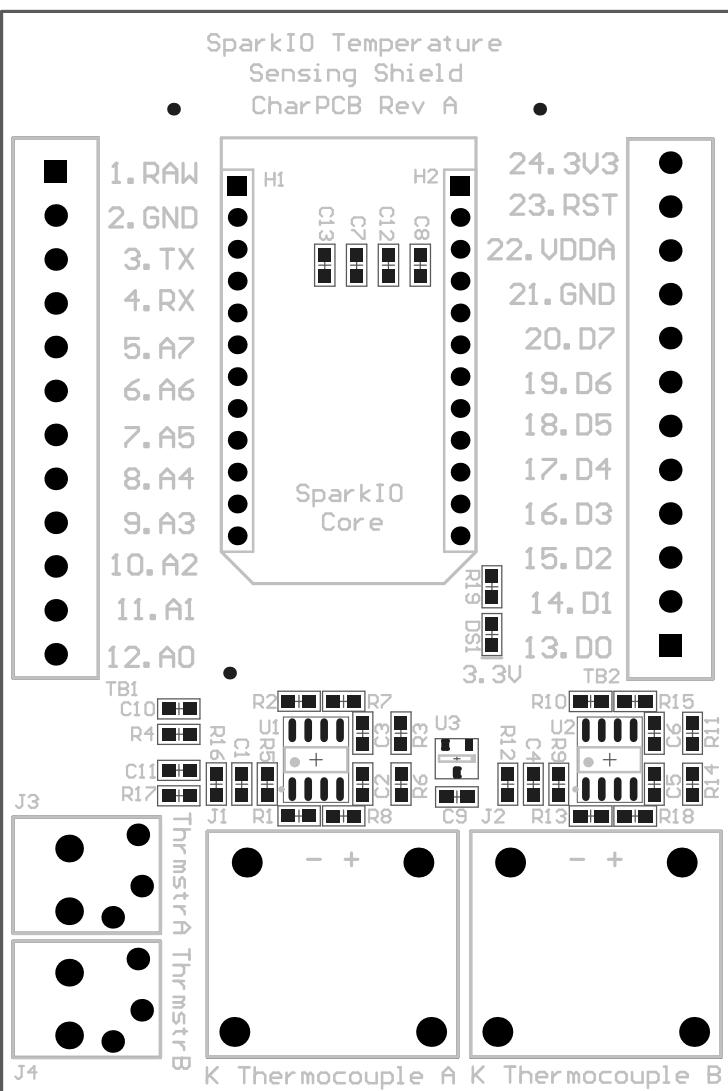
Size: A4 Number: * Revision: A

Date: 7/27/2014 Time: 11:11:42 PM Sheet 1 of 1

File: C:\Users\Jim\Documents\GitHub\probe\SparkIO Thermal Shield\SparkIO Thermal Shield - No Aux ADC.SchDoc

Altium

Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:11:44 PM



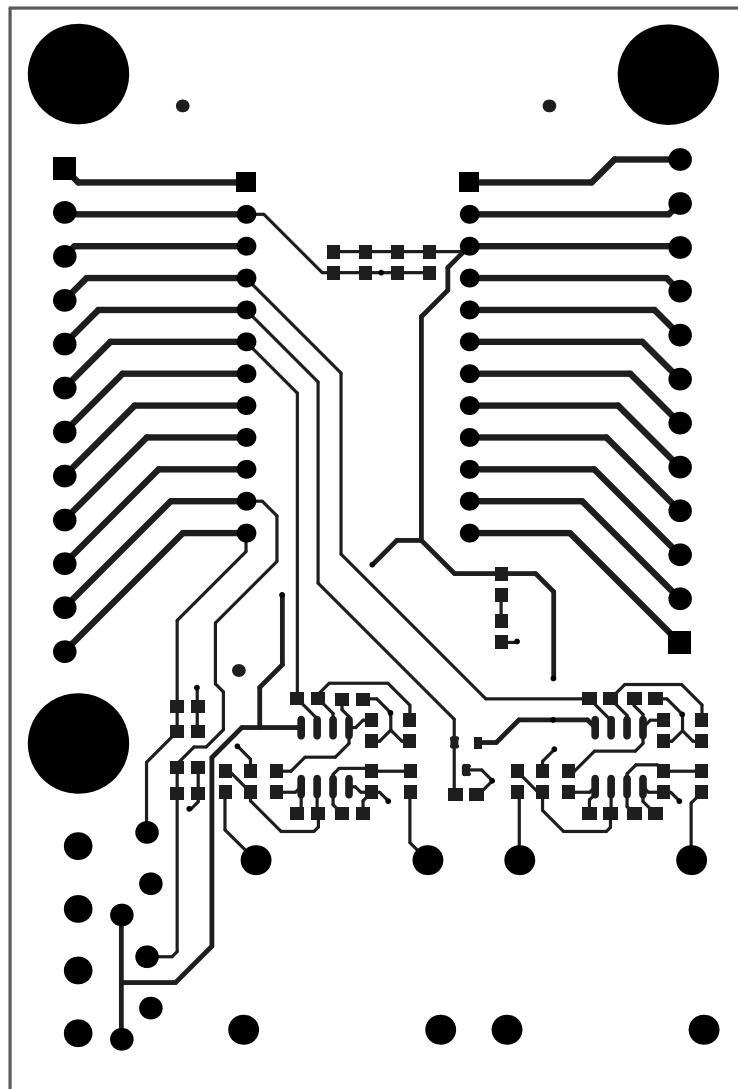
Visible Layer(s)

Top Overlay

[M1] Board Outline

[M15] Top Component Keepout

Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:11:47 PM

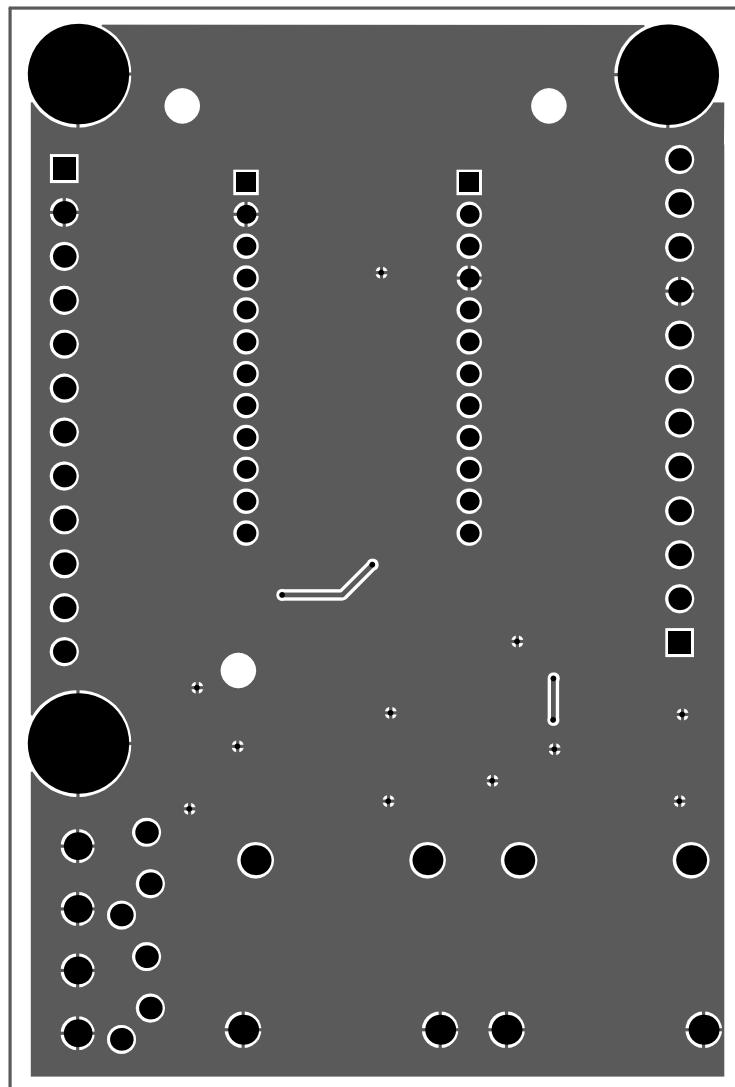


Visible Layer(s)

[1] Top Layer

[M1] Board Outline

Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:11:48 PM

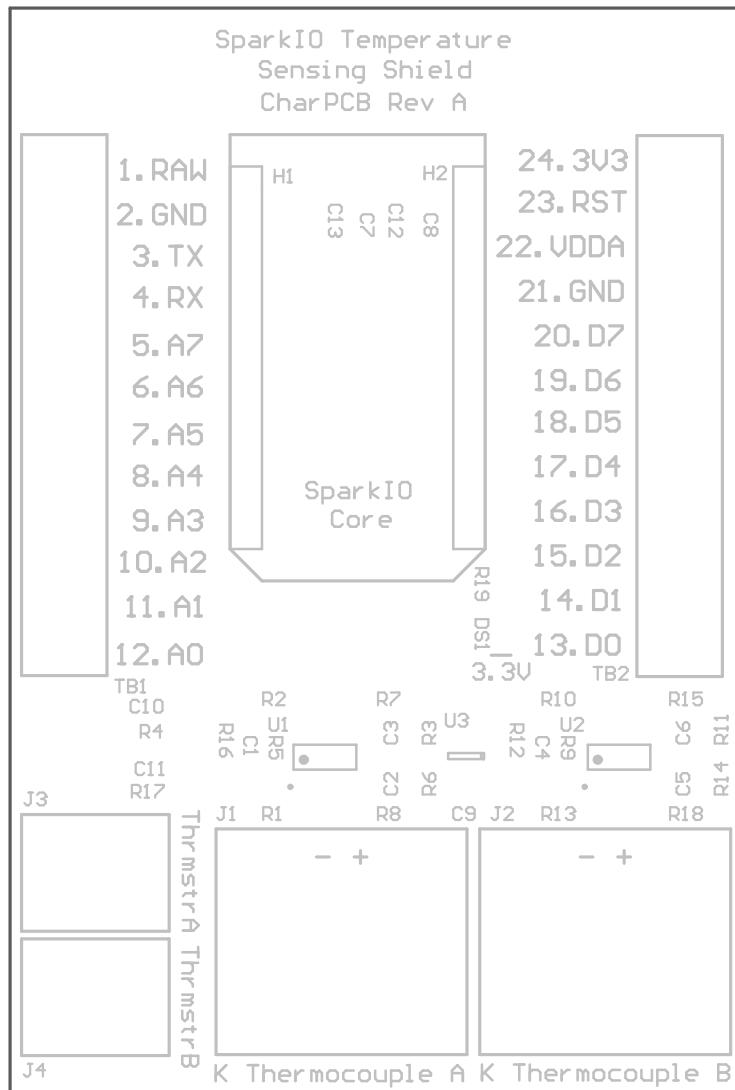


Visible Layer(s)

[2] Bottom Layer

[M1] Board Outline

Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Grissbacher
Date: 7/27/2014
Time: 11:11:48 PM



Visible Layer(s)

Top Overlay

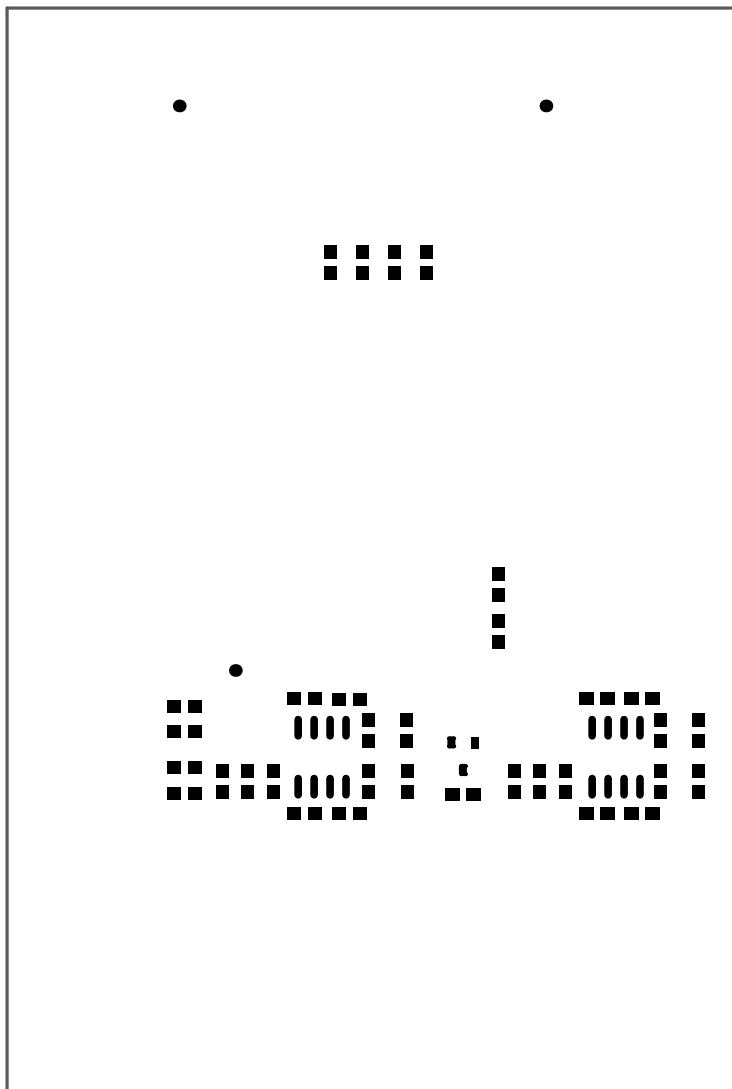
[M1] Board Outline

Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:11:49 PM

Visible Layer(s)

Top Paste

[M1] Board Outline

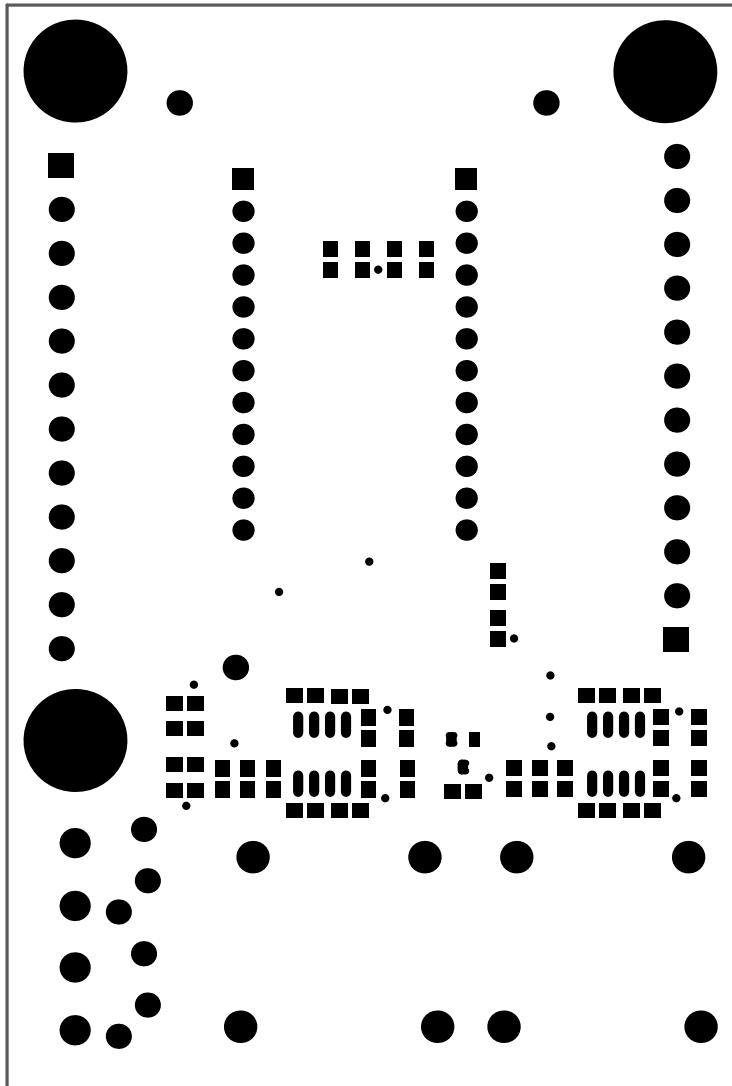


Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:11:49 PM

Visible Layer(s)

Top Solder

[M1] Board Outline

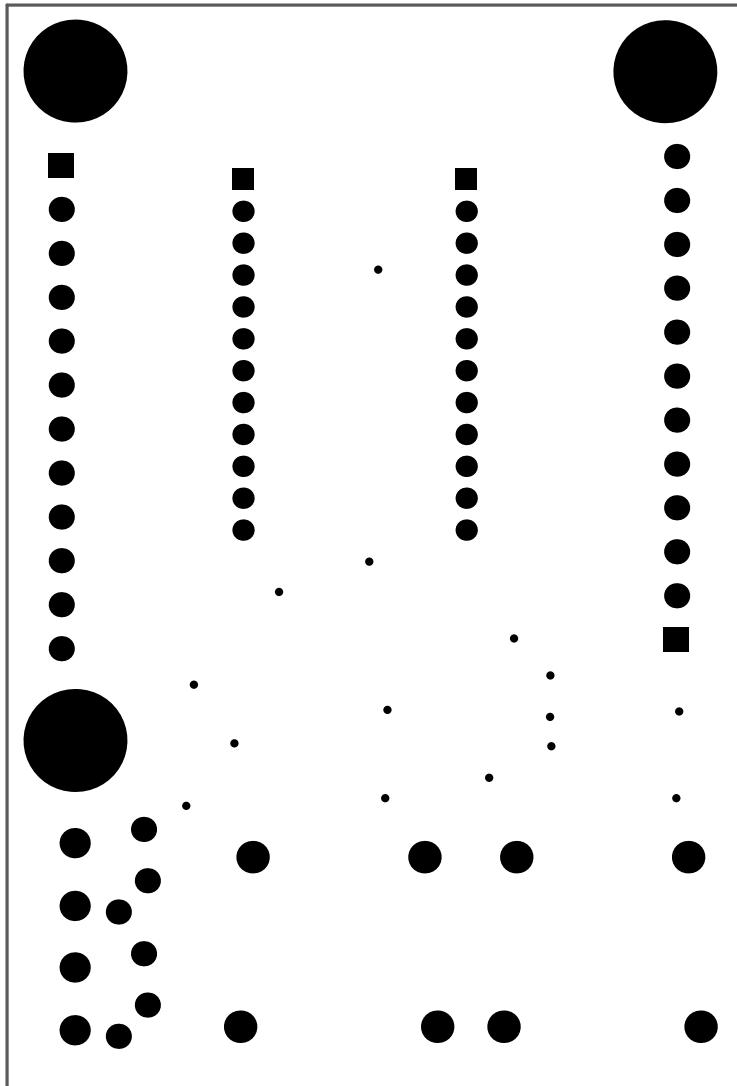


Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:11:50 PM

Visible Layer(s)

Bottom Solder

[M1] Board Outline

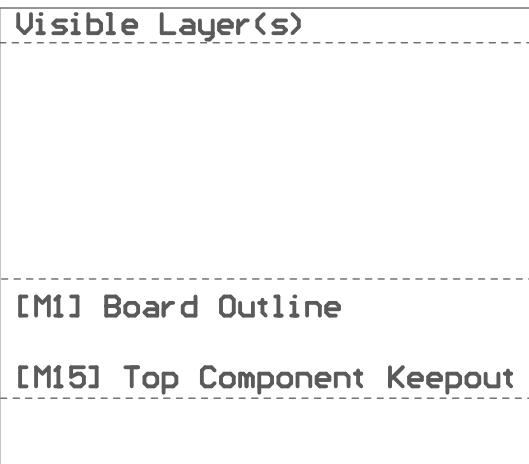
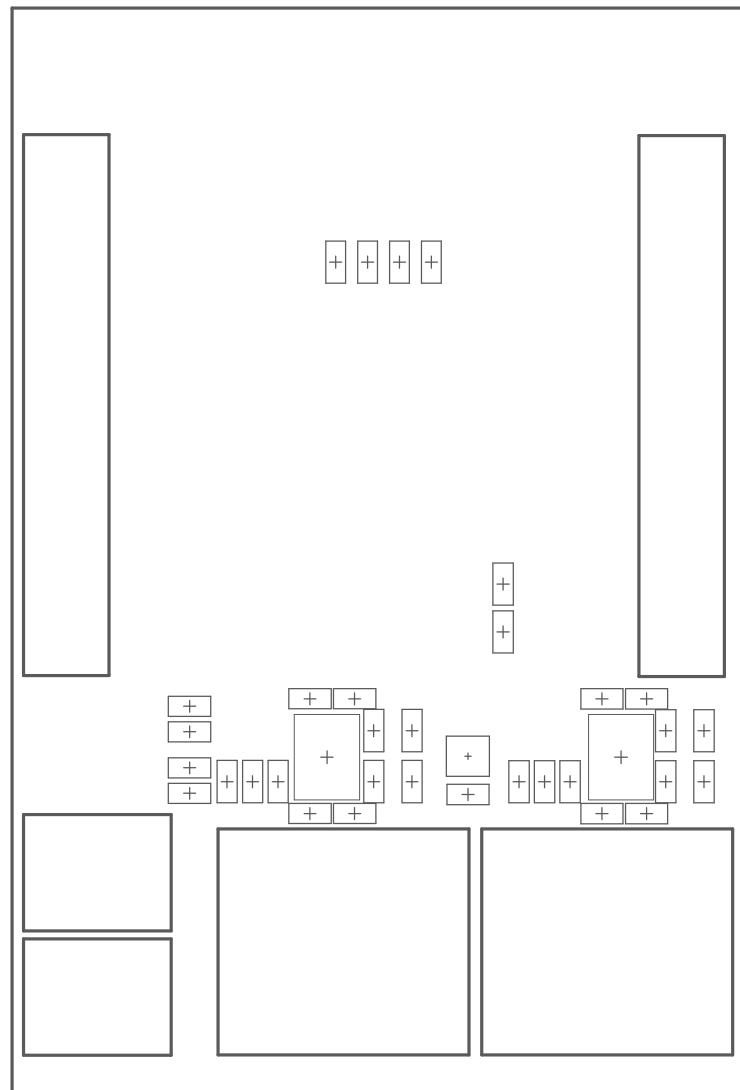


Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:11:50 PM

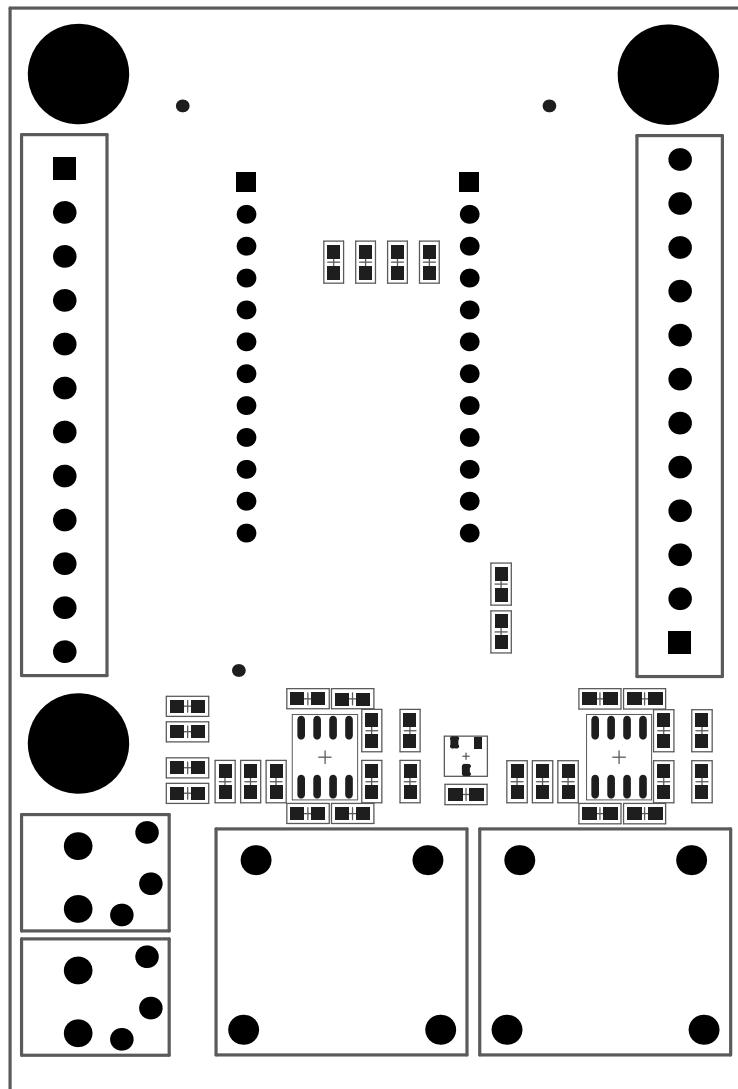
Visible Layer(s)

[M1] Board Outline

Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:11:51 PM



Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:11:51 PM



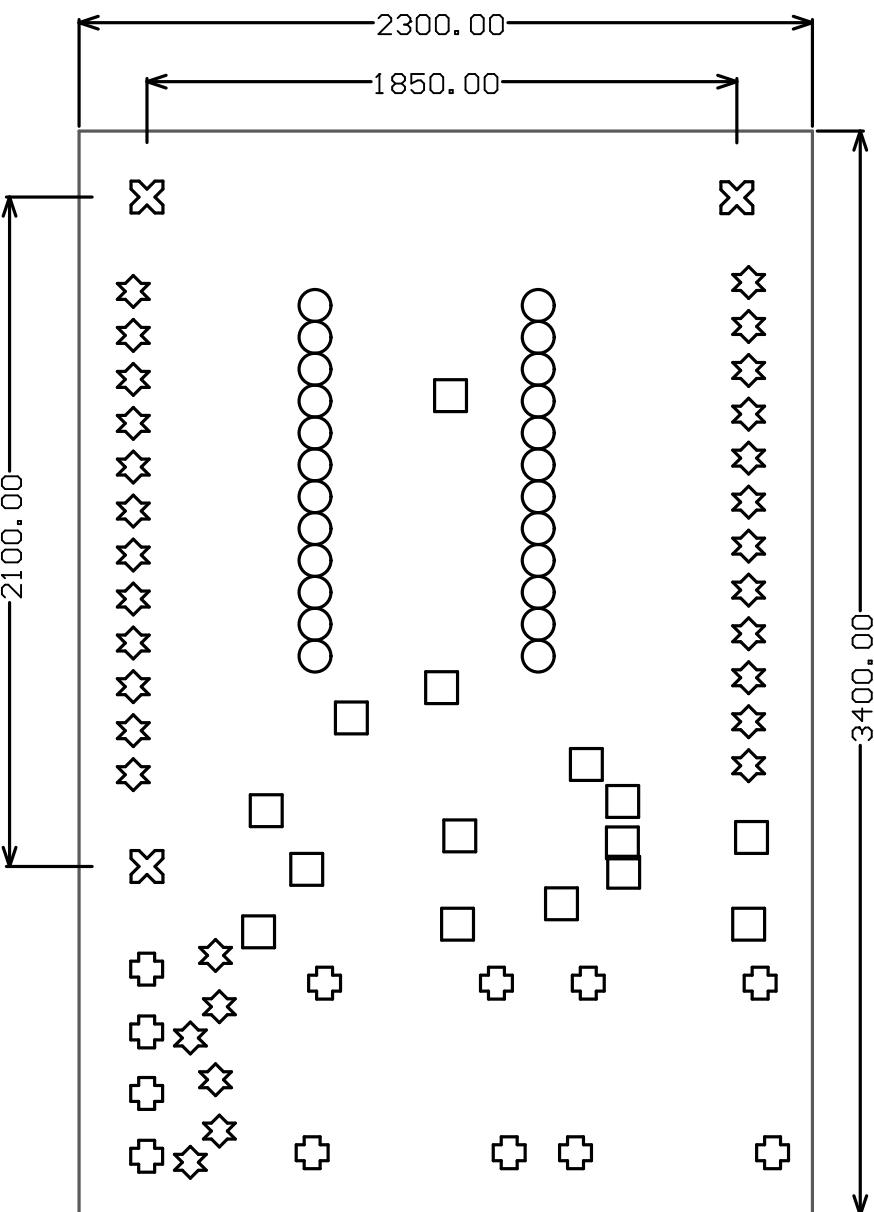
Visible Layer(s)

[M1] Board Outline

[M15] Top Component Keepout

Layer Stack Up Detail: Final PCB Thickness is 62.0mil				
Layer Name	Gerber Document	Copper Thickness (Final Height)	Dielectric Height	Material
Top Solder Mask	(.GTS)	0.5mil	PSR 4000 Taiyo	
Top Layer	(.GTL)	1.4mil (1oz)		
-	-	58.2mil	Lam, 370HR	
Bottom Layer	(.GBL)	1.4mil (1oz)		
Bottom Solder Mask	(.GBS)	0.5mil	PSR 4000 Taiyo	

Project: SparkIO Thermal Shield
 Revision: A
 Drawn By: Jim Griszbacher
 Date: 7/27/2014
 Time: 11:11:52 PM



Visible Layer(s)

[M1] Board Outline

Drill Drawing

Fabrication

- i. Green Solder Mask SMOBC, in accordance to IPC-SM-840
- ii. White Silkscreen on Top Side: No ink shall be on exposed pads
- iii. ENIG Surface Finish
- iv. PCB shall be RoHS material and RoHS process compliant, T_(g) > 170C, T_(d)-288 test >5 minutes
- v. PCB is 10mil min trace/space design
- vi. Drill sizes are finished size after plating
- vii. PCB core is 58.2mil thick 370HR material or equivalent


Assembly

- i. RoHS Clean process, in accordance to IPC-A-600 and IPC-A-610 Class II
- ii. Top Side contains through-hole and surface-mount components
- iii. Bottom Side contains no components, design is single sided
- iv. Only populate the components marked as 'Fitted' in the Bill of Materials
- v. No electrical testing required

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
✗	3	196.85mil (5.000mm)	PTH	Round
○	12	69.69mil (1.770mm)	PTH	Round
✳	30	47.24mil (1.200mm)	PTH	Round
○	24	35.43mil (0.900mm)	PTH	Round
□	15	10.00mil (0.254mm)	PTH	Round
84 Total				


Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:12:08 PM


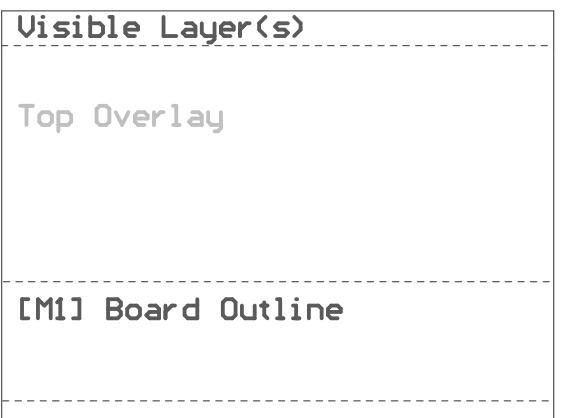
Visible Layer(s):
 Top Layer
 Board Outline



Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:12:47 PM

Visible Layer(s):
[2] Bottom Layer
[M1] Board Outline






Visible Layer(s):
Top Paste

[M1] Board Outline



Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:14:22 PM

Visible Layer(s):
Top Solder
[M1] Board Outline




Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:14:47 PM

Visible Layer(s):

Bottom Solder

[M1] Board Outline




Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:15:06 PM

Visible Layer(s):

[M1] Board Outline



Visible Layer(s):
[M1] Board Outline
[M15] Top Component Keepout




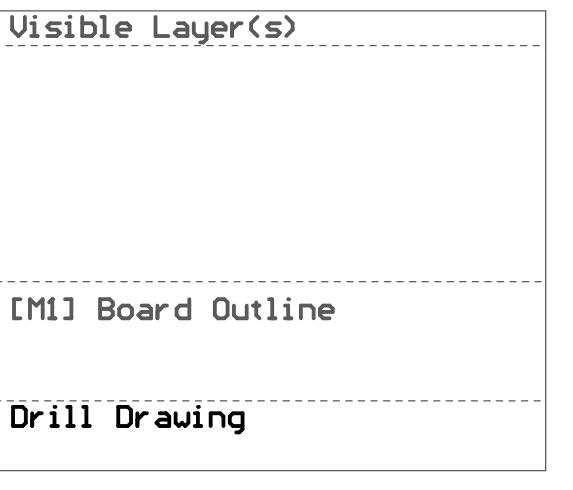
Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:15:49 PM

Visible Layer(s):

[M1] Board Outline

[M15] Top Component Keepout

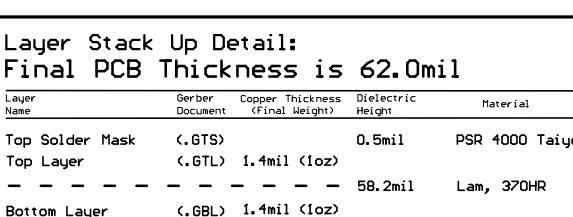
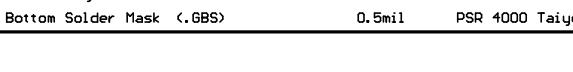
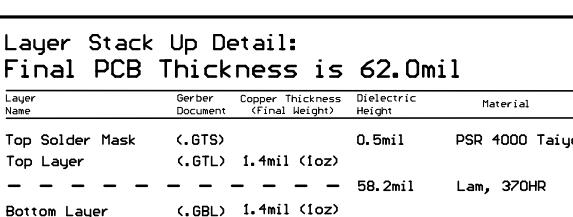




Fabrication
i. Green Solder Mask SH0BC, in accordance to IPC-SM-840
ii. White Silkscreen on Top Side; No ink shall be on exposed pads
iii. Drill sizes are 0.062 mil, 0.075 mil, 0.090 mil, 0.125 mil, 0.150 mil
iv. PCB shall be RoHS material and RoHS process compliant,
v. PCB is 1.0mil thick, 35 mils wide
vi. Drill sizes are finished size after plating
vii. There are 68.2mil thick 3DHR material or equivalent

Panel Design
i. Panel is 18 inches by 24 inches with 500mil width rails
ii. Rous are 5 up with U-Score between each PCB
iii. 10 rows are fitted on the panel, each separated with a 100mil width route

Assembly
i. RoHS Green process, in accordance to IPC-H-600 and IPC-H-610 Class II
ii. Top Side contains through-hole and surface-mount components
iii. Bottom Side contains no components, design is single sided
iv. Only populate the components marked as "Fitted" in the Bill of Materials
v. No electrical testing required



Final PCB Thickness is 62.0mil

Top Solder Paste 0.075mil (0.019mm) LwY 304K Tgyp
Top Layer 0.010mil (0.025mm) LwY 304K
Bottom Layer 0.080mil (0.020mm) LwY 304K
Bottom Solder Paste 0.075mil (0.019mm) LwY 304K Tgyp

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
x	150	196.85mil (.5.000mm)	PTH	Round
o	600	69.69mil (1.770mm)	PTH	Round
□	250	10.00mil (.254mm)	PTH	Round
○	1200	35.43mil (.0.900mm)	PTH	Round
●	1500	47.24mil (.1.200mm)	PTH	Round
	4200 Total			

U-SCORE DETAIL
30 Degrees

16mil ↓ 62mil ↑

Row Routing Detail
100mil ↓ 62mil ↑

(x10)

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

↓

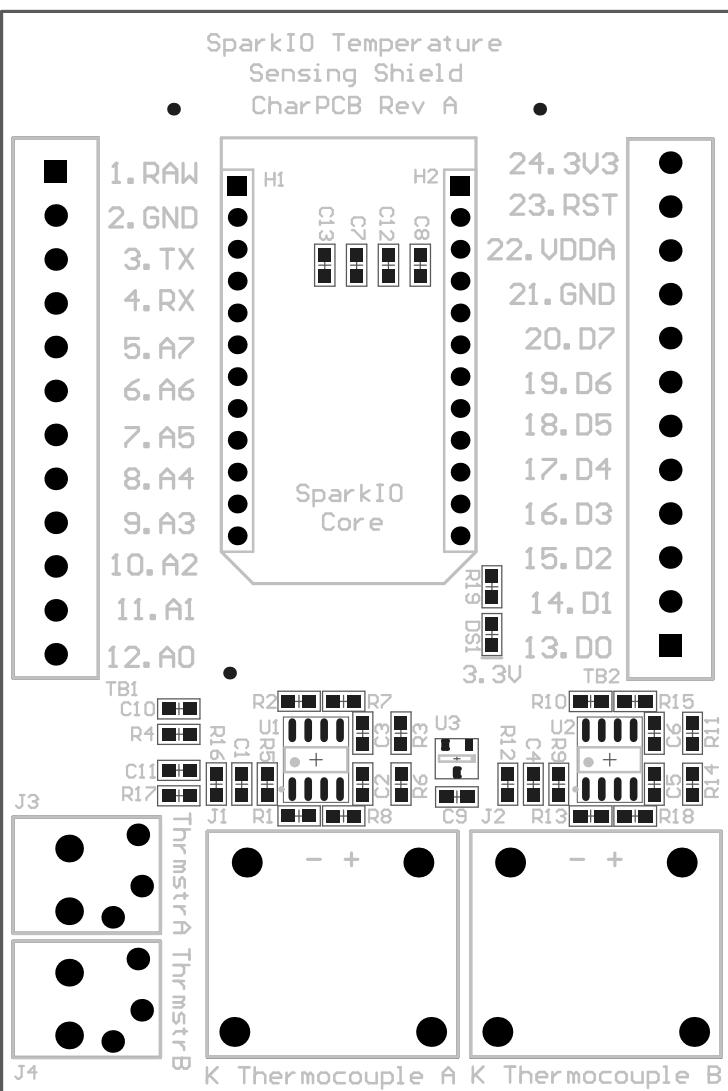
↓

↓

↓

</

Project: SparkIO Thermal Shield
Revision: A
Drawn By: Jim Griszbacher
Date: 7/27/2014
Time: 11:21:11 PM



Visible Layer(s)

Top Overlay

[M1] Board Outline

[M15] Top Component Keepout