# Daniel Ruelas-Petrisko

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## Summary

*I am a full-stack computer engineer with broad experience developing ASIC flows; from architectural specification to RTL, physical design, and EDA tooling. My research explores leveraging open-source tools and IP to minimize iteration time, without sacrificing design quality. I have experience leading multiple tapeouts in TSMC 28nm and GlobalFoundries 12nm, as well as prototyping designs in Skywater 130nm, TSMC 40nm and advanced FPGA prototypes.*

## Education

Ph.D., M.S. **University of Washington, Seattle** Computer Science & Engineering (2025, 2023)
*A Qualitative Approach to Agile Hardware Design*, advised by Professors Michael Taylor, Mark Oskin

M.S., B.S. **University of Illinois at Urbana-Champaign** Electrical & Computer Engineering (2018, 2016)
*Architectural Exploration of Si-IF Many-Die Processors*, advised by Professor Rakesh Kumar

## Experience

**Organization Director** Nov 2022 - present
*Free and Open-Source Silicon (FOSSi) Foundation* London, UK
– Advocates and provides stewardship for various open-source silicon tools, standards, and IP
– Organizes premiere conferences in the open-source silicon community, including LatchUp and ORConf

**ASIC Design Consultant** Jan 2023 - present
*OpenASIC Consulting, LLC* Seattle, WA
– Provides full-stack support for specification, implementation and verification across RTL2GDS flow
– Specializes in open-source IP integration, commercial/open hybrid CAD flows and rapid-design, N=1 test chips

**Research Assistant** Sep 2018 - August 2025
*University of Washington* Seattle, WA
– Collaborated on agile tapeouts of complex, record-breaking 12nm chips, hacking from RTL through GDS
– Created and maintained plethora of IP and tooling across the open-source BaseJump ASIC development ecosystem
– Mentored 20+ masters and undergrad projects, resulting in dozens of contributions to major research projects

**Lead Digital Chip Architect - MaxSDR ASIC** Mar 2021 - Dec 2022
*MaXentric Technologies, LLC* San Diego, CA
– Architected 3 Mgate TSMC 28nm mixed signal design with 192-core manycore and 3 Linux-capable cores
– Oversaw full RTL2GDS flow, including RTL, synthesis, floorplanning, verification, GLS and ECOs
– Pioneered source-synchronous link topology for rapid convergence of blocks, reducing iteration from 1 week to 1 day

**Research Assistant** August 2014 - May 2018
*University of Illinois* Champaign, IL
– Developed novel large-scale parallel simulation framework to approximate waferscale GPU system performance
– Applied novel ILP-based PPA optimization framework for multi-system architectural DSE of chiplets
– Implemented classical and novel ECC schemes in RTL to evaluate EDP tradeoffs for subthreshold operation

**Logic Design Co-op** Spring 2018; Summer 2018
*IBM* Austin, TX
– Designed and implemented VHDL for the POWER10 fetch unit, including branch prediction and issue logic
– Triaged core-level functional failures and power regressions alongside verification and integration teams

**SoC Design Verification Intern** Summer 2017
*Apple* Cupertino, CA
– Developed testbenches and verification flows for large-scale gate-level simulations, reducing build and run times
– Analysed coverage trade-offs between emulation and simulation flows, balancing developer and iteration time

**Device Design Intern; Systems Validation Intern** Summer 2016; Summer 2015
*Intel* Portland, OR
– Converged static timing and electrical quality for structurally designed circuits in embedded DRAM circuits
– Triaged hardware failures on prototype processors in lab, suggesting fix or debug directions to the design team

**Embedded Software Intern; Test Automation Intern** Summer 2014; Summer 2013
*John Deere* Des Moines, IA
– Automated embedded display testing equipment, eliminating costly manual programming and verification
– Created continuous build, test and deployment pipelines for production webapps

## Skills

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| **Hardware** | Synopsys DC, ICC2, Primetime; Cadence Genus, Innovus, Tempus; Yosys, Verilator, Surelog |
| **Software** | SystemVerilog, C, C++, Python, TCL, Make, Git |
| **Other** | Logic Design, VLSI, Continuous Integration (CI), Agile Development, Architectural Simulation |

## Projects

**BlackParrot (Lead Architect)** black-parrot
*Heterogeneously tiled application-class multicore with custom cache coherence for accelerator integration*

**ZynqParrot (Lead Architect)** zynq-parrot
*Cycle-accurate, Scale-Down, FPGA-accelerated co-emulation platform for generic RTL prototyping*

**BSG Pearls (Lead Architect)** bsg_pearls
*Modular RTL and collateral library for hierarchy-insensitive hardware design*

**HammerBlade (Maintainer)** bsg_manycore
*Highly scalable RISC-V manycore fabric for bulk-synchronous parallel workloads*

**BaseJump STL (Maintainer)** basejump_stl
*Standard Template Library for latency-insensitive hardware design*

## Publications

"A 12nm FinFET Implementation of Ruche Networks on a 99mm$^2$ 2048-Core HammerBlade RISC-V Manycore SoC"
P. Gao, D. Jung, S. Davidson, **D. Ruelas-Petrisko**, et al. *TVLSI 2025**

"A Qualitative Approach to Agile Hardware Design"
**D. Ruelas-Petrisko** *PhD Dissertation, ProQuest 2025**

"ZynqParrot: A Scale-Down Approach to Cycle-Accurate, FPGA-Accelerated Co-Emulation"
**D. Ruelas-Petrisko**, et al. *arXiv 2025**

"Scalable, Programmable and Dense: Open-Source RISC-V Manycore with Scalable Resource Organization"
D. Jung, M. Ruttenberg, P. Gao, S. Davidson, **D. Ruelas-Petrisko**, et al. *ISCA 2024*

"Scaling Program Synthesis Based Technology Mapping with Equality Saturation"
G. Smith, C. Knizek, **D. Ruelas-Petrisko**, et al. *WOSET 2024*

"RISE: RISC-V SoC for En/decryption Acceleration on the Edge for Homomorphic Encryption"
Z. Azad, G. Yang, R. Agrawal, **D. Ruelas-Petrisko**, et al. *IEEE TVLSI*

"RACE: RISC-V SoC for En/decryption Acceleration on the Edge for Homomorphic Computation"
Z. Azad, G. Yang, R. Agrawal, **D. Ruelas-Petrisko**, et al. *ISLPED 2022*

"BlackParrot: An Agile Open Source RISC-V Multicore for Accelerator SoCs"
**D. Ruelas-Petrisko**, et al. *IEEE Micro July/August 2020*

"NoC Symbiosis (Invited Paper)"
**D. Ruelas-Petrisko**, et al. *NOCS 2020*

"Architectural Exploration of Si-IF Many-die Processors"
**D. Ruelas-Petrisko** *MS Dissertation, ProQuest 2018*

"Design Space Exploration for Chiplet-Assembly-Based Processors"
S. Pal, **D. Ruelas-Petrisko**, et al. *IEEE VLSI April 2020*

"Rethinking Waferscale Processors - A GPU Case Study"
S. Pal, **D. Ruelas-Petrisko**, et al. *HPCA 2019*

"A Case for Packageless Processors"
S. Pal, **D. Ruelas-Petrisko**, et al. *HPCA 2018*

"Transforming Error Patterns to Enable Deeper Voltage Scaling in On-chip Memories"
H. Duwe, X. Jian, **D. Ruelas-Petrisko**, et al. *ISCA 2016*

## Workshop & Tutorials

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| **FOSSi Latchup 2025** | Introduced BSG Pearls as a modular library for hierarchy-insensitive hardware design |
| **FOSSi LatchUp 2022** | Introduced BSG Tag as an flexible, robust and minimal ASIC configuration bus |
| **RISC-V Summit 2020** | Tutorial to get up and running with BlackParrot and accelerators |
| **Supercomputing 2020** | Described integration BlackParrot into HPC systems |
| **FOSDEM 2020** | Announced the BlackParrot processor to the open-source hardware community |
| **FOSSi LatchUp 2019** | Pitched BaseJump STL as standard library for latency-insensitive hardware design |

## Chip Gallery

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|---|---|---|
| **BP0** | 4-core BlackParrot | GF12 3x3mm |
| **BP1** | 4-core BlackParrot | TSMC40 4x6mm* |
| **BigBlade** | 16 x (2 unicore + CGRA + 128-core manycore) | GF12 10x10mm |
| **MaxSDRv1** | 1 big, 2 little cores, 192-core manycore, high-speed I/O | TSMC28 4x6mm |
| **TT-DLL** | All-digital delay-locked-loop | Sky130 160x100um |
| **MaxSDRv2** | 1 big, 2 little cores, 192-core manycore, high-speed I/O, LPDDR1 | TSMC28 4x6mm |
| **MiniBlade** | DBI testing infrastructure, scalable clock generator | GF12 1x1mm* |