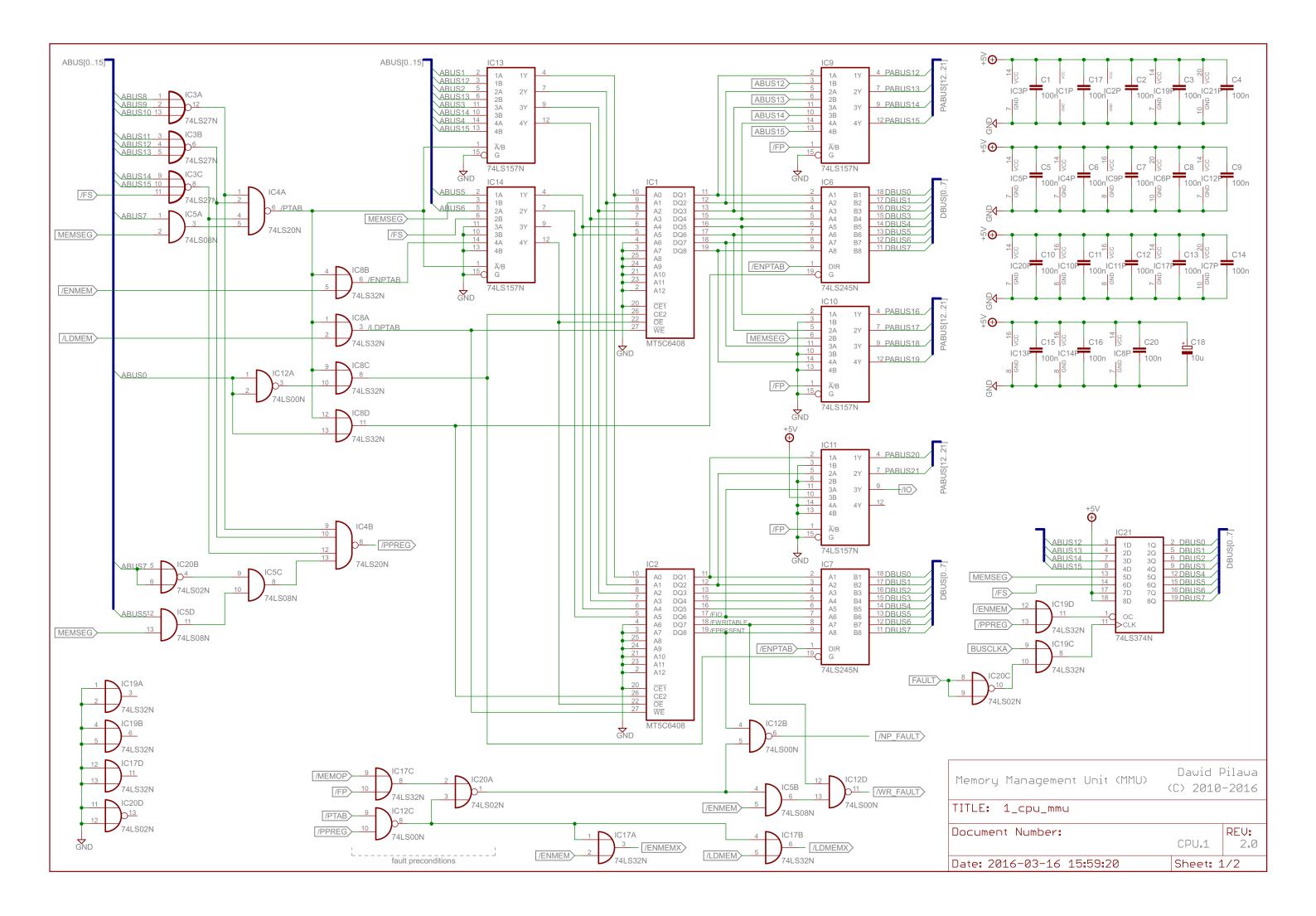
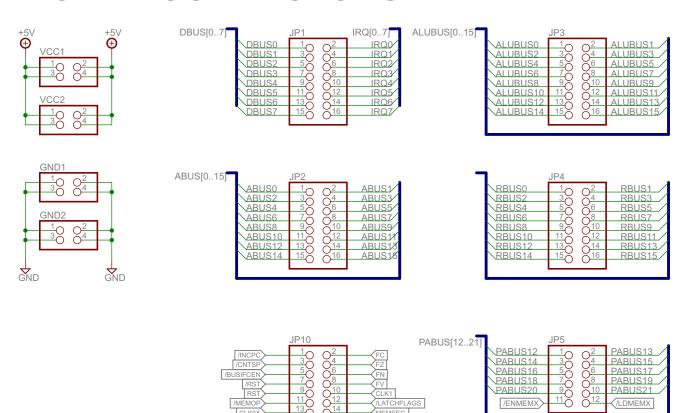


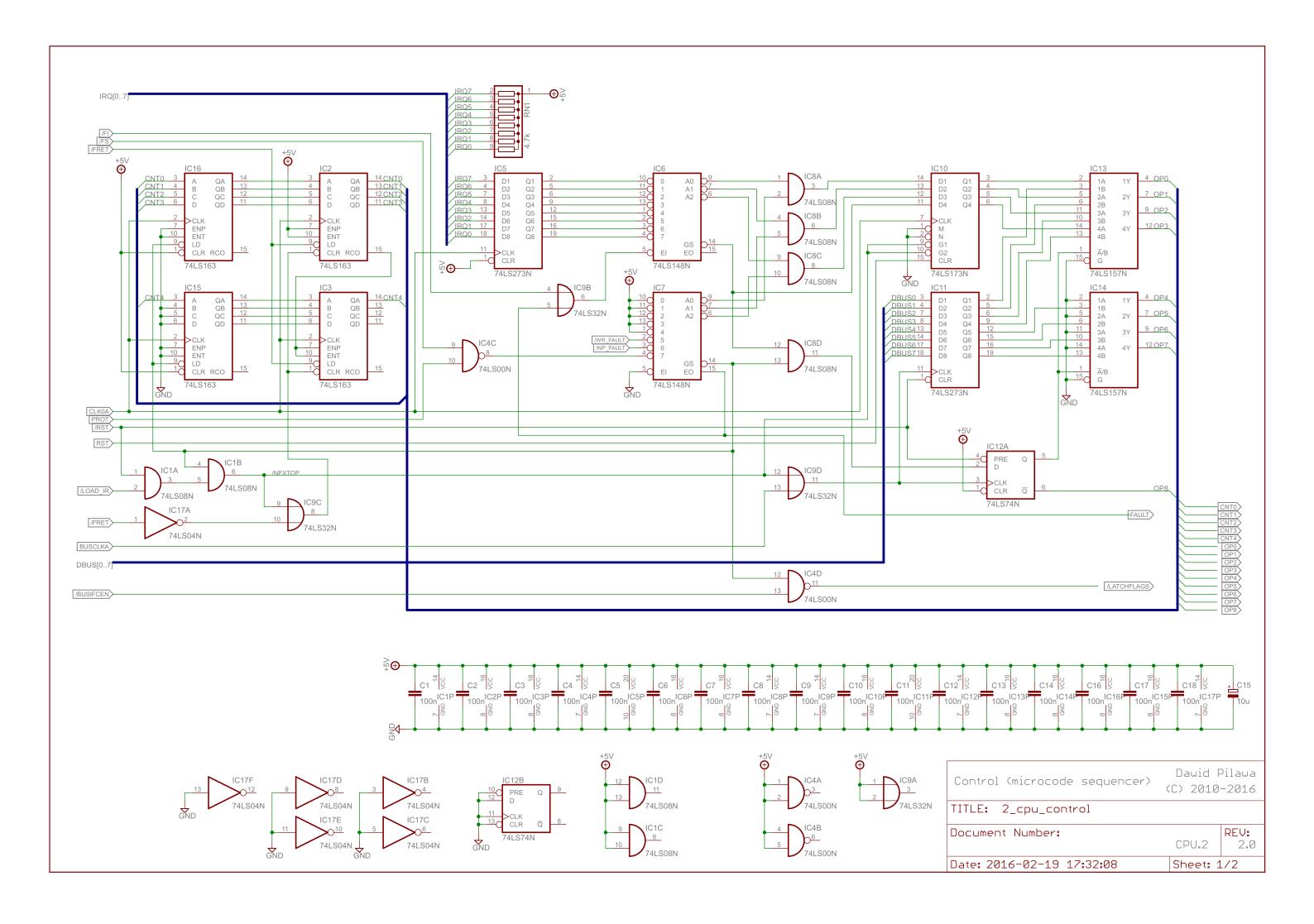
Clocks, reset, bus interface	Dawid (	
	(C) 2010	-2016
TITLE: 0_cpu_interface		
Document Number:	CPU.0	REV: 2.0
Date: 2016-02-12 16:16:01	Sheet: 2	2/2

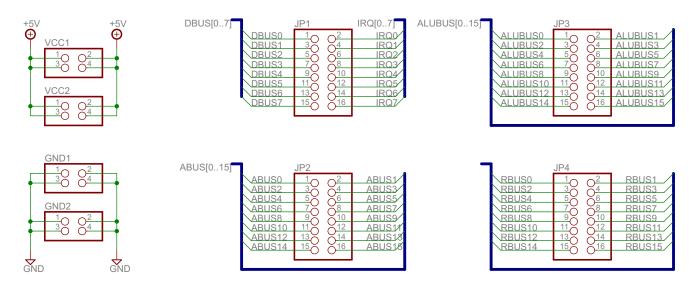


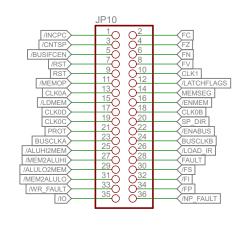


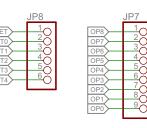
/ENMEMX

Memory Management Unit (MMU)	Dawid F C) 2010	
TITLE: 1_cpu_mmu		
Document Number:	CPU.1	REU: 2.0
Date: 2016-03-16 15:59:20	Sheet: 2	2/2

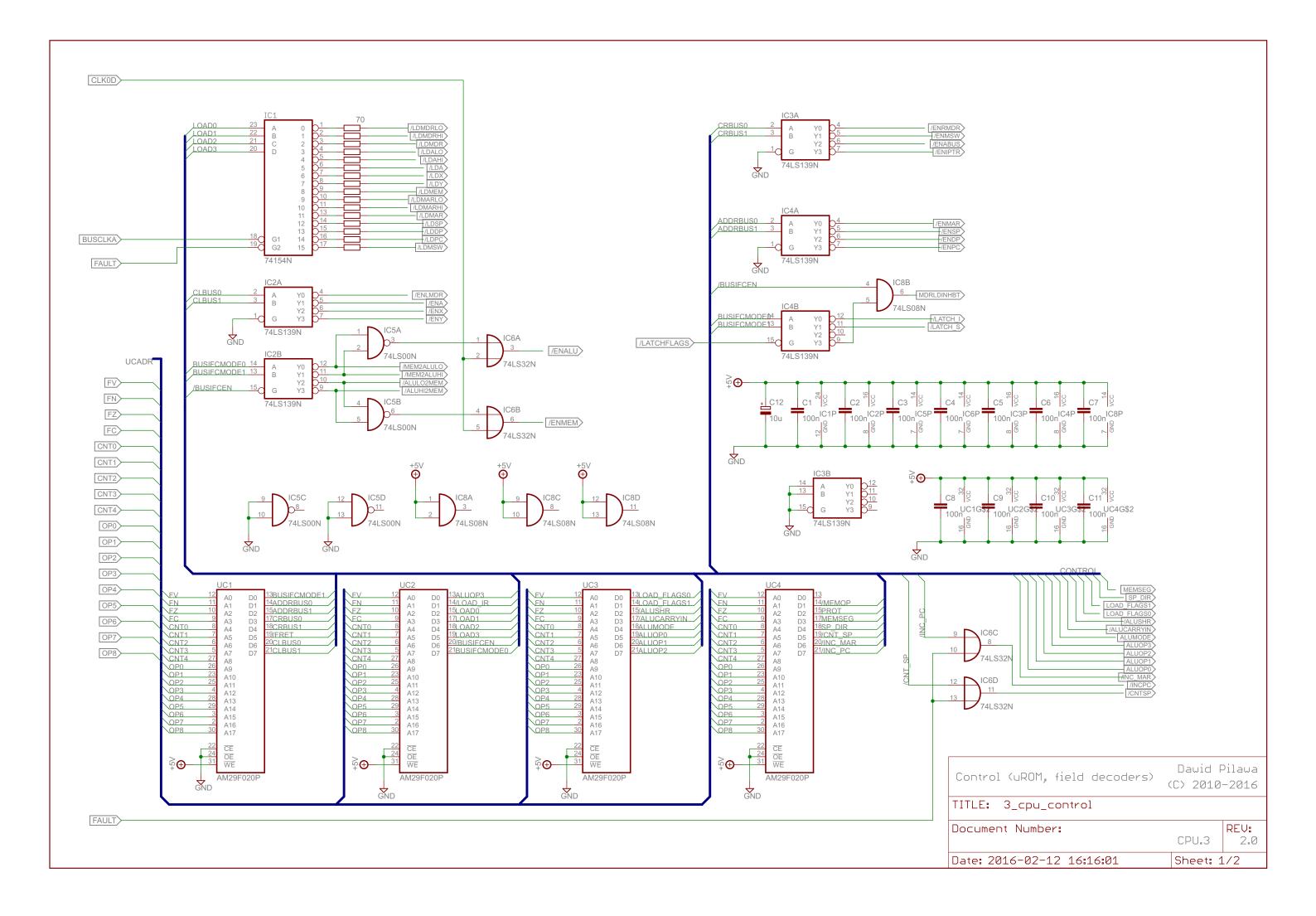


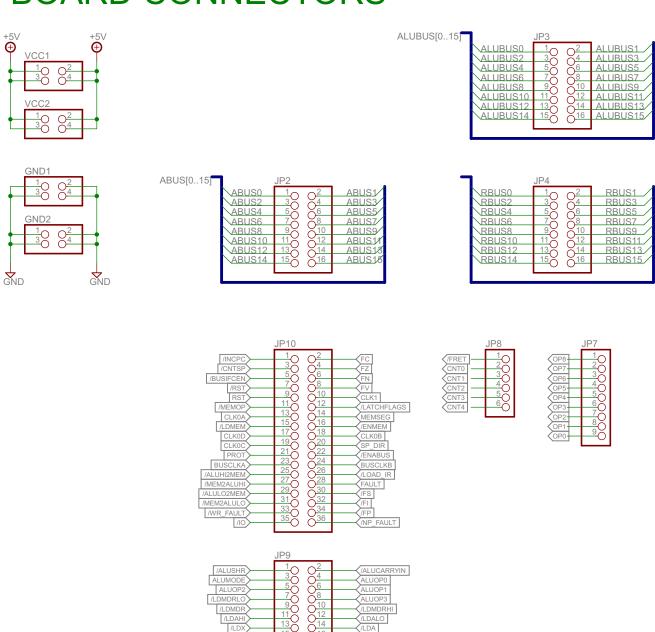




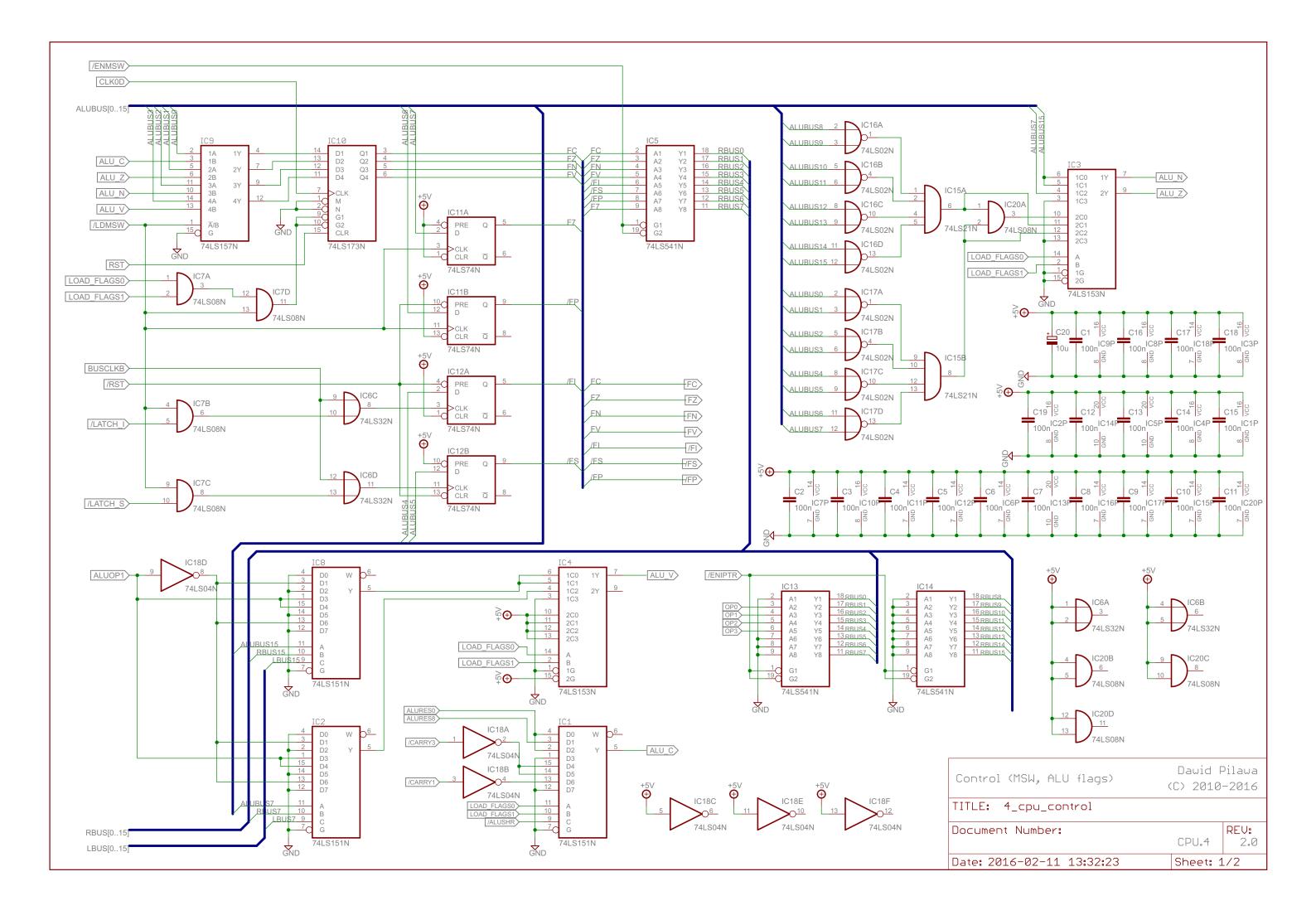


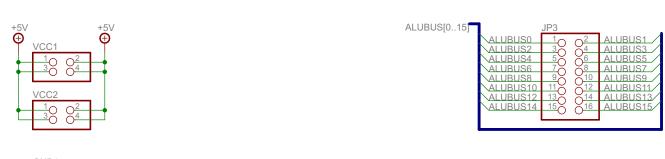
Control (microcode sequencer)	Dawid F (C) 2010	
TITLE: 2_cpu_control		
Document Number:	CPU.2	REU: 2.0
Date: 2016-02-19 17:32:08	Sheet: 2	2/2

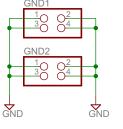


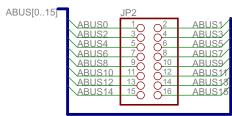


Control (uROM, field decoders)	Dawid ( (C) 2010	
TITLE: 3_cpu_control		
Document Number:	CPU.3	REU: 2.0
Date: 2016-02-12 16:16:01	Sheet: 2	2/2



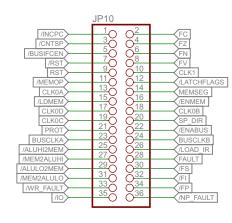


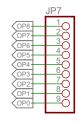




7		JP4		_
RBUS	30	1	$\bigcirc^2$	RBUS1 /
RBUS	32	3	$\sim_4$	RBUS3 /
RBUS	34	5	$\gtrsim_6$	RBUS5 /
RBUS	36	7	$\gtrsim_8$	RBUS7 /
RBUS	88	9	$\simeq 10$	RBUS9 /
RBUS	310	11	<u></u>	RBUS11
RBUS	312	13	<u>14</u>	RBUS13/
RBUS	314	15	<u> 16</u>	RBUS15/
		$\Box$	0	

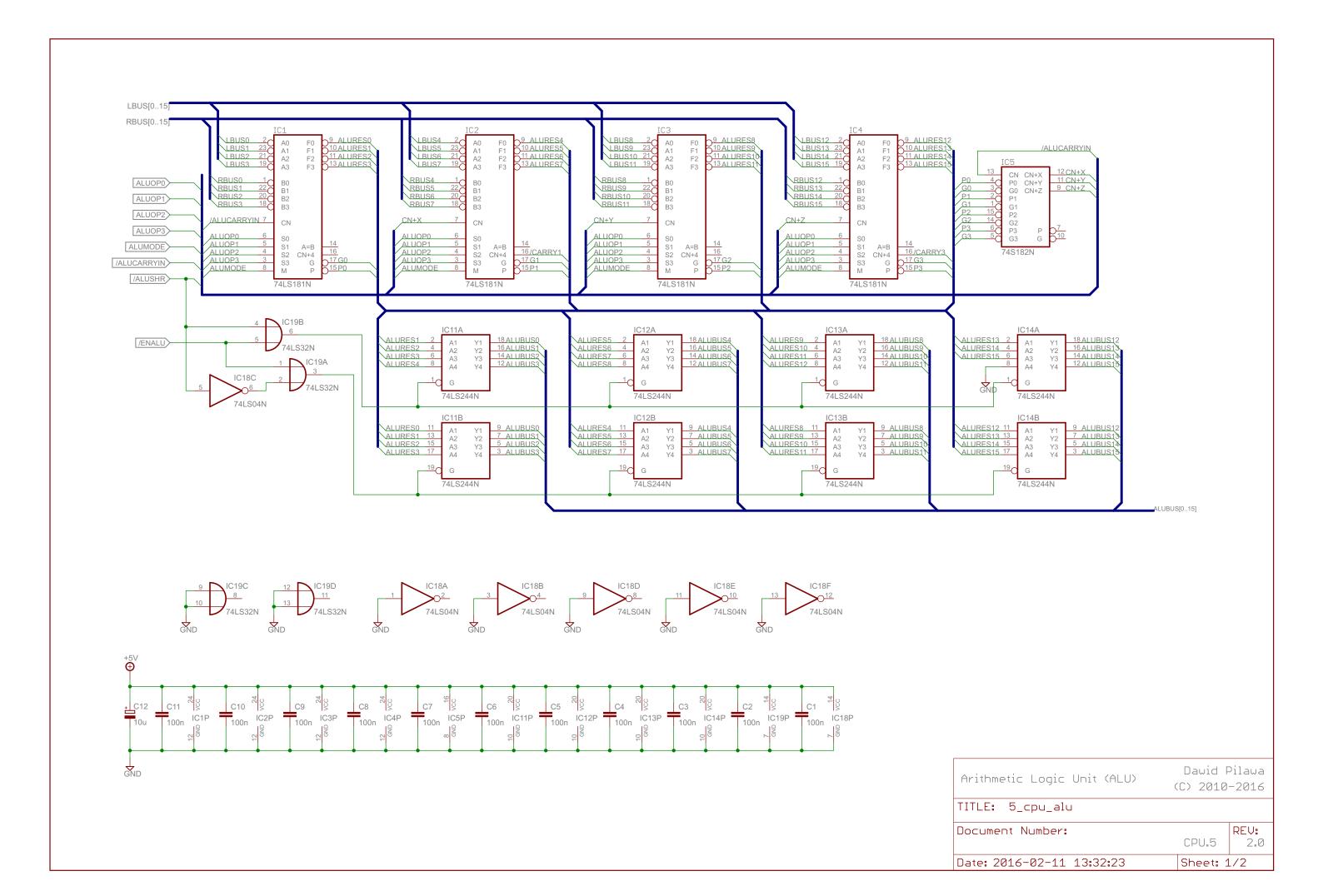
1	JP5	_
LBUS14 LBUS12 LBUS10 LBUS8 LBUS6 LBUS4 LBUS2	1 0 2 3 0 4 5 0 6 7 0 8 9 0 10 11 0 12 13 0 14	LBUS15 LBUS13 LBUS11 LBUS9 LBUS7 LBUS5 LBUS3
LBUS0	15 0 16	LBUS1

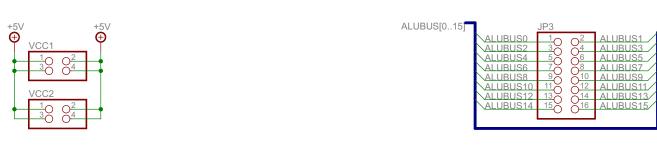


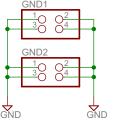


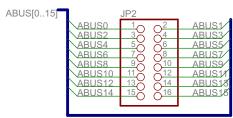
	JP9	
I/ALUSHR ALUMODE   ALUOP2   ALUOP2   /LDMDRLO   /LDMDR   /LDAH    /LDX   /LDMARH    /LDX   /LDMARH    /LDX   /LDMARH    /LDX   /LDMARH    /LDX   /LDX	1 0 2 3 0 04 5 0 6 7 0 8 9 0 10 11 0 14 15 0 16 17 0 18 19 0 20 21 0 22 23 0 24 25 0 26 27 0 28 29 0 30 31 0 32 27 0 28 29 0 30 31 0 32 33 0 34 35 0 36 37 0 38 39 0 40 41 0 42 43 0 44 45 0 44 47 0 48	/ALUCARRYIN ALUOPO ALUOPO ALUOPT ALUOPS Aluo

Control (MSW, ALU flags)	Dawid F (C) 2010	
TITLE: 4_cpu_control		
Document Number:	CPU.4	REV: 2.0
Date: 2016-02-11 13:32:23	Sheet: 2	2/2



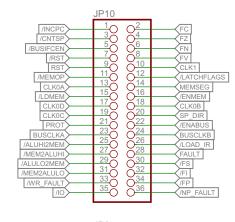


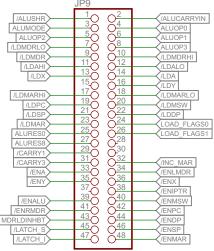




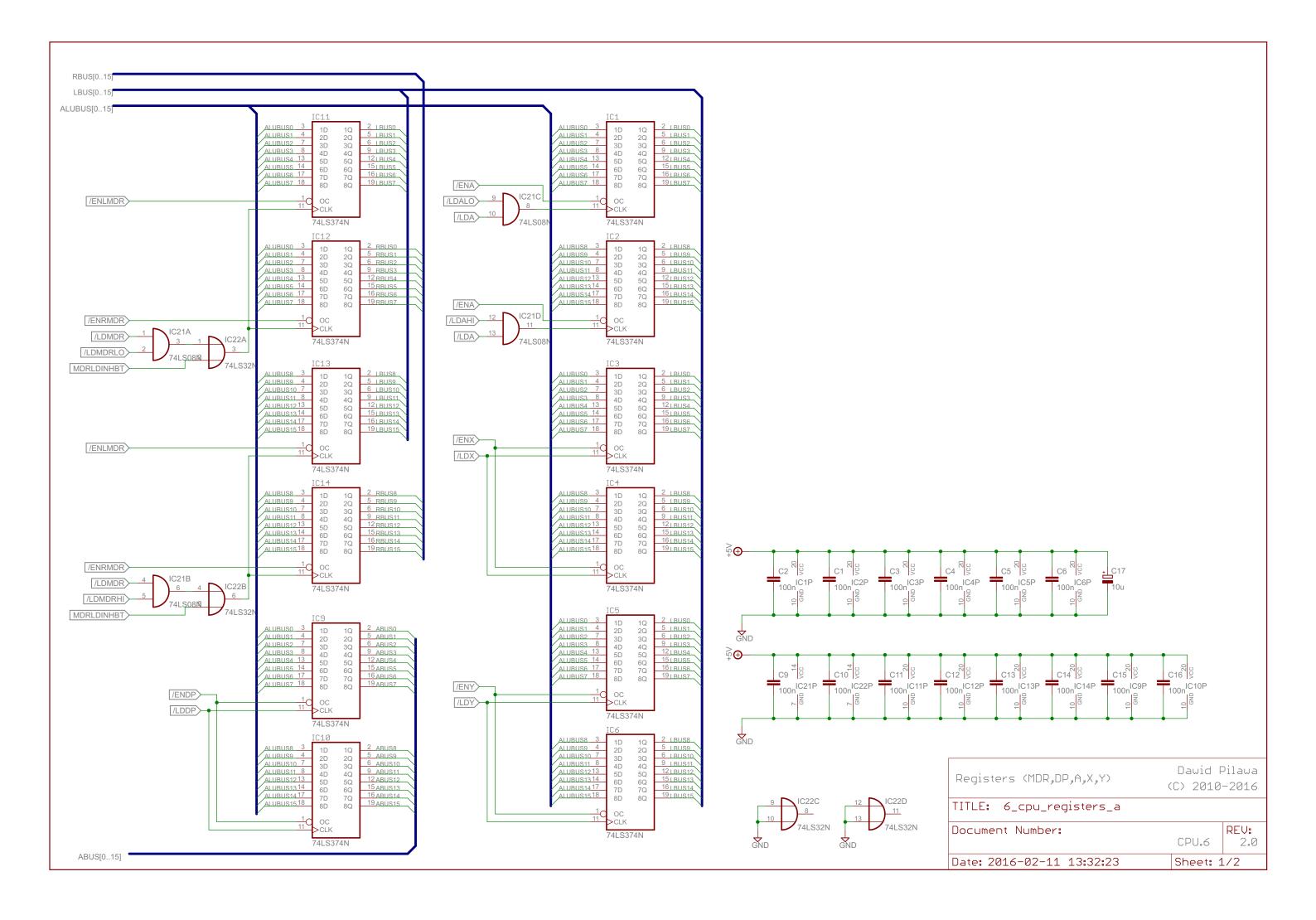
7		JP4		
RBUS	30	1	$\Omega^2$	RBUS1 /
RBUS	32	3	$\sim$ 4	RBUS3 /
RBUS	64	5	$\sim$ 6	RBUS5 /
RBUS	36	7	$\gtrsim$ 8	RBUS7 /
RBUS	88	9	$\simeq$ 10	RBUS9 /
RBUS	310	11	<u></u>	RBUS11 /
RBUS	312	13	<u></u>	RBUS13/
RBUS	314	15	<u></u> 16	RBUS15/

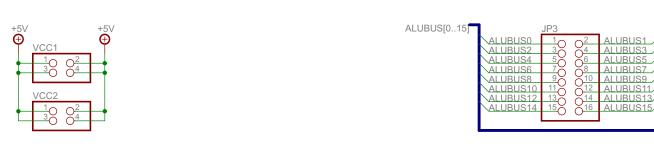
1	JP5	
LBUS14	$^{1}$ 0 0 <sup>2</sup>	LBUS15 /
LBUS12	30 04	LBUS13
LBUS10	50 06	LBUS11
LBUS8	70 08	LBUS9
LBUS6	9 210	LBUS7
LBUS4	11 0 012	LBUS5
LBUS2	13 2 14	LBUS3
LBUS0	15 216	LBUS1
		-



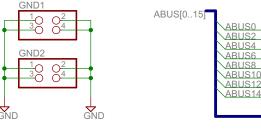


Arithmetic Logic Unit (ALU)	Dawid F (C) 2010	
TITLE: 5_cpu_alu		
Document Number:	CPU.5	REV: 2.0
Date: 2016-02-11 13:32:23	Sheet: 2	2/2



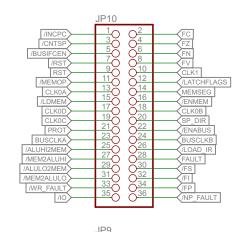


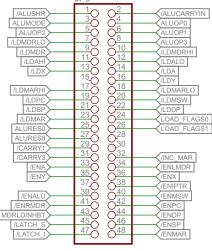
ABUS1/ ABUS3/ ABUS5/ ABUS7/ ABUS9/ ABUS1/ ABUS1/3/ ABUS1/3/



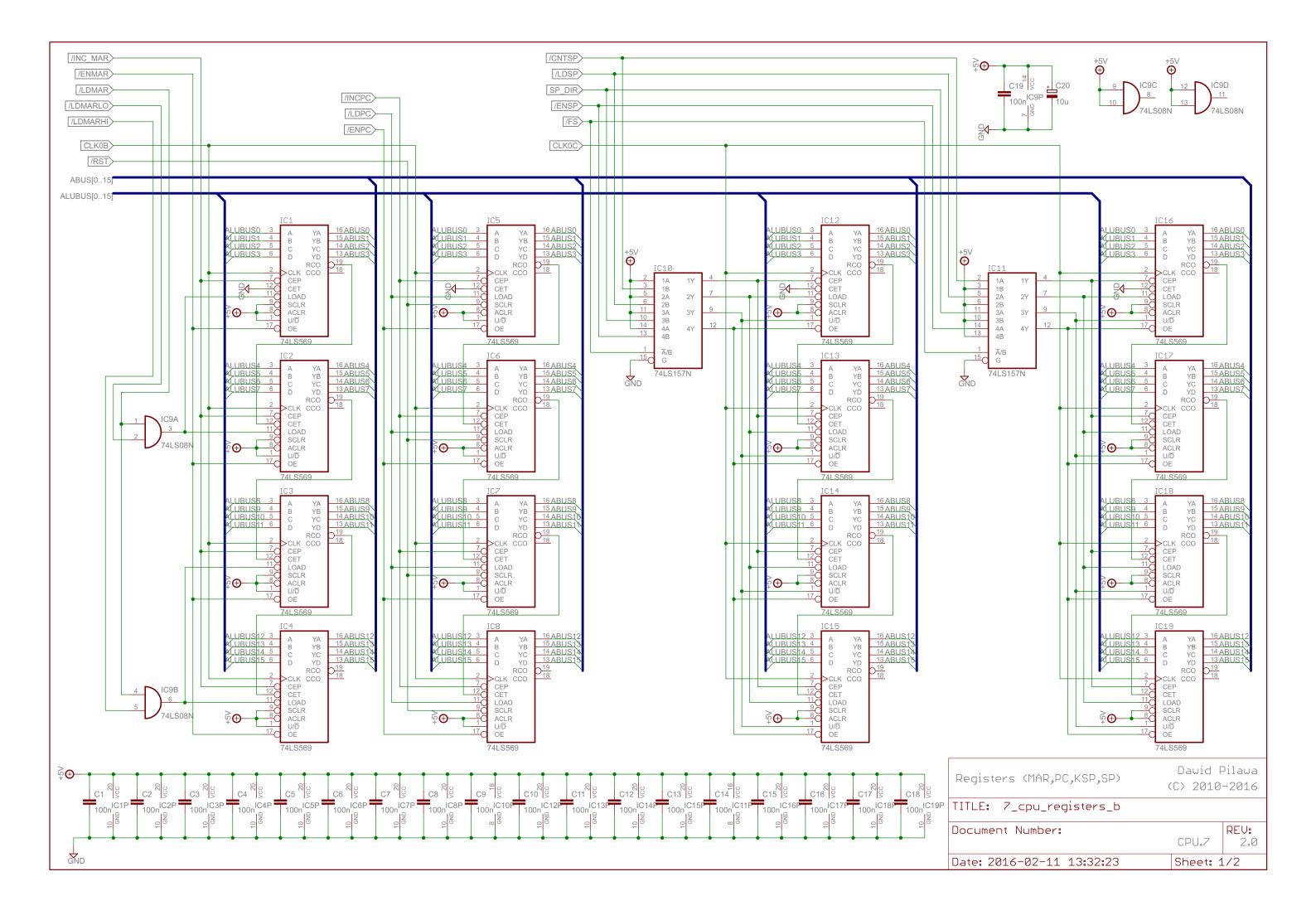
RBUS0	1	$     \begin{array}{c}             2 \\             4 \\           $	RBUS1
RBUS2	3		RBUS3
RBUS4	5		RBUS5
RBUS6	7		RBUS7
RBUS8	9		RBUS9
RBUS12 RBUS14	13 15 0	014	RBUS13 RBUS15

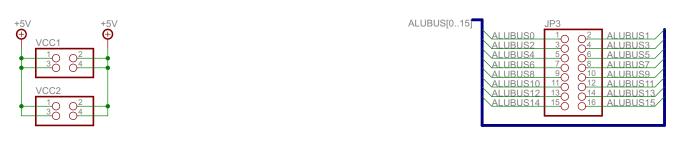
7	JP5		
LBUS14	10	$\Omega^2$	LBUS15 /
LBUS12	3	$\sim$ 4	LBUS13
LBUS10	5	$\gtrsim_6$	LBUS11 /
LBUS8	7	$\gtrsim_8$	LBUS9
LBUS6	9	$\simeq 10$	LBUS7 /
LBUS4	11	<u></u>	LBUS5
LBUS2	13	<u> 14</u>	LBUS3 /
LBUS0	15	<u> 16</u>	LBUS1 /

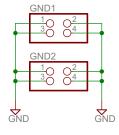


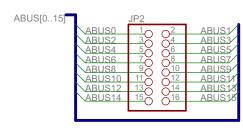


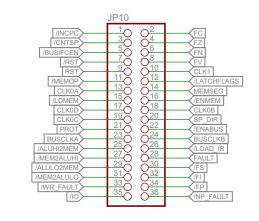
Registers (MDR,DP,A,X,Y)	Dawid ( (C) 2010	
TITLE: 6_cpu_registers_a		
Document Number:	CPU.6	REV: 2.0
Date: 2016-02-11 13:32:23	Sheet: 2	2/2

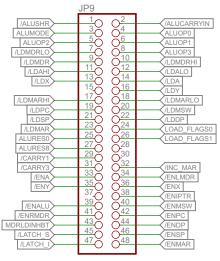












Date: 2016-02-11 13:32:23	Sheet: 2/2	
Document Number:	CPU.7	REV: 2.0
TITLE: 7_cpu_registers_b		
Registers (MAR,PC,KSP,SP)	Dawid F (C) 2010	

