Introduction

The Phase Locked Loop primitive in Virtex-5 and Spartan 6 parts is used to generate multiple clocks with defined phase and frequency relationships to a given input clock. The Phase Locked Loop (PLL) module is a wrapper around the PLL_ADV primitive that allows the PLL to be used in the EDK tool suite.

Features

- Wrapper around the PLL_ADV primitive
- Full support for use with EDK 11.1 and later versions
- Configurable BUFG insertion
- Configurable output delay adjustment for PPC block clock insertion delay compensation in Virtex-5FXT parts
- Six output clocks with independently selectable frequencies

LogiCORE™ Facts				
Core Specifics				
Supported Device Family	Virtex®-5, Spartan 6			
Resources Used	I/O	LUTs	FFs	Block RAMs
	N/A	N/A	N/A	N/A
Special Features	1 PLL Block			
Provided with Core				
Documentation	Product Specification			
Design File Formats	VHDL			
Constraints File	N/A			
Verification	N/A			
Instantiation Template	N/A			
Additional Items	None			
Design Tool Requirements				
Xilinx Implementation Tools	ISE® 11.1 or later			
Verification	N/A			
Simulation	N/A			
Synthesis	N/A			
Support				
Provided by Xilinx, Inc.				

Functional Description

The PLL Module takes an input clock named CLKIN1, then generates several output clocks, each of which can be configured to have a different frequency that is dependent on the input clock frequency. The PLL Module encapsulates the PLL_ADV primitive as shown in Figure 1. The PLL_ADV primitive is described in the Libraries Guide for the applicable family that is provided as part of the ISE tools documentation.

The PLL Module provides optional buffers for the CLKIN1 input, and the CLKOUT*, and CLKFBOUT outputs. CLKOUT* represents the six clock outputs CLKOUT0, CLKOUT1, CLKOUT2, CLKOUT3, CLKOUT4, and CLKOUT5. The second clock input of the PLL_ADV primitive is not used, and the clock input select input of the PLL_ADV primitive is connected to a constant to always select the CLKIN1 signal. The dynamic reconfiguration inputs and outputs of the PLL_ADV primitive are hidden or terminated within the PLL module, as is the control input for the PMCD mode. All other inputs and outputs of the PLL_ADV primitive are inputs and outputs of the PLL module.
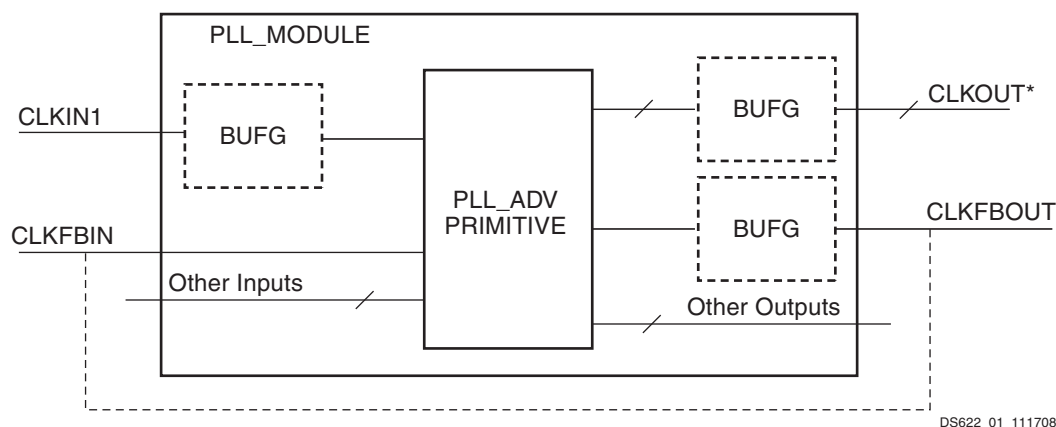

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Figure 1: PLL Module Implementation and Usage

In the context of an embedded processor system, the recommended usage of the PLL module is to take a single reference clock input, then configure the CLKOUT* signals to produce the different clock frequencies and phases required, with the CLKOUT* and CLKFBOUT signals buffered and connected as shown by the dashed lines in Figure 1.

The output clock frequencies are derived from the input clock frequency, and the values of the following parameters: C_DIVCLK_DIVIDE, C_CLKFBOUT_MULT, C_CLKOUTn_DIVIDE.

*Frequency of CLKOUTn = Frequency of CLKIN1 * (C_CLKFBOUT_MULT/C_DIVCLK_DIVIDE) / C_CLKOUTn_DIVIDE*

PLL Module Parameters

The PLL module is configured by selecting appropriate values for the MPD (Microprocessor Peripheral Definition) parameters described in Table 1.

Table 1: MPD Parameters for PLL Module

Parameter Name	Description	Allowed Values	Default Value	Type
C_BANDWIDTH	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	OPTIMIZED	string
C_CLKFBOUT_BUF	If C_CLKFBOUT_BUF = true, a BUFG is inserted between the CLKFBOUT pin of the PLL_ADV primitive and CLKFBOUT output	true, false	false	Boolean
C_CLKFBOUT_DESKEW_ADJUST	Clock delay attribute for CLKOUT5 output	NONE, PPC[1]	NONE	string
C_CLKFBOUT_MULT	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	1	integer
C_CLKFBOUT_PHASE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.0	real
C_CLKIN1_BUF	If C_CLKIN1_BUF = true, a BUFG is inserted between the CLKIN1 input and the CLKIN1 pin of the PLL_ADV primitive	true, false	false	Boolean
C_CLKIN1_PERIOD	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.0	real
C_CLKOUT0_BUF	If C_CLKOUT0_BUF = true, a BUFG is inserted between the CLKOUT0 pin of the PLL_ADV primitive and CLKOUT0 output	true, false	false	Boolean
C_CLKOUT0_DESKEW_ADJUST	Clock delay attribute for CLKOUT0 output	NONE, PPC[1]	NONE	string
C_CLKOUT0_DIVIDE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	1	integer
C_CLKOUT0_DUTY_CYCLE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.5	real
C_CLKOUT0_PHASE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.0	real
C_CLKOUT1_BUF	If C_CLKOUT1_BUF = true, a BUFG is inserted between the CLKOUT1 pin of the PLL_ADV primitive and CLKOUT1 output	true, false	false	Boolean
C_CLKOUT1_DESKEW_ADJUST	Clock delay attribute for CLKOUT1 output	NONE, PPC[1]	NONE	string

Table 1: MPD Parameters for PLL Module *(Cont'd)*

Parameter Name	Description	Allowed Values	Default Value	Type
C_CLKOUT1_DIVIDE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	1	integer
C_CLKOUT1_ DUTY_CYCLE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.5	real
C_CLKOUT1_PHASE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.0	real
C_CLKOUT2_BUF	If C_CLKOUT2_BUF = true, a BUFG is inserted between the CLKOUT2 pin of the PLL_ADV primitive and CLKOUT2 output	true, false	false	Boolean
C_CLKOUT2_DESKEW _ADJUST	Clock delay attribute for CLKOUT2 output	NONE, PPC[1]	NONE	string
C_CLKOUT2_DIVIDE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	1	integer
C_CLKOUT2_ DUTY_CYCLE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.5	real
C_CLKOUT2_PHASE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.0	real
C_CLKOUT3_BUF	If C_CLKOUT3_BUF = true, a BUFG is inserted between the CLKOUT3 pin of the PLL_ADV primitive and CLKOUT3 output	true, false	false	Boolean
C_CLKOUT3_DESKEW _ADJUST	Clock delay attribute for CLKOUT3 output	NONE, PPC[1]	NONE	string
C_CLKOUT3_DIVIDE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	1	integer
C_CLKOUT3_ DUTY_CYCLE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.5	real
C_CLKOUT3_PHASE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.0	real
C_CLKOUT4_BUF	If C_CLKOUT4_BUF = true, a BUFG is inserted between the CLKOUT4 pin of the PLL_ADV primitive and CLKOUT4 output	true, false	false	Boolean
C_CLKOUT4_DESKEW _ADJUST	Clock delay attribute for CLKOUT4 output	NONE, PPC[1]	NONE	string
C_CLKOUT4_DIVIDE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	1	integer

Table 1: MPD Parameters for PLL Module *(Cont'd)*

Parameter Name	Description	Allowed Values	Default Value	Type
C_CLKOUT4_DUTY_CYCLE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.5	real
C_CLKOUT4_PHASE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.0	real
C_CLKOUT5_BUF	If C_CLKOUT5_BUF = true, a BUFG is inserted between the CLKOUT5 pin of the PLL_ADV primitive and CLKOUT5 output	true, false	false	Boolean
C_CLKOUT5_DESKEW_ADJUST	Clock delay attribute for CLKOUT5 output	NONE, PPC[1]	NONE	string
C_CLKOUT5_DIVIDE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	1	integer
C_CLKOUT5_DUTY_CYCLE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.5	real
C_CLKOUT5_PHASE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.0	real
C_COMPENSATION	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	SYSTEM_SYNCHRONOUS	string
C_DIVCLK_DIVIDE	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	1	integer
C_EXT_RESET_HIGH	IF C_EXT_RESET_HIGH = 0, the RST signal is inverted before connecting to the PLL_ADV	0,1	1	integer
C_FAMILY	Target FPGA family	virtex5, virtex5fx	virtex5	string
C_REF_JITTER	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	0.1	real
C_RESET_ON_LOSS_OF_LOCK	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	false	Boolean
C_RST_DEASSERT_CLK	This parameter passes the value to the equivalent attribute of the PLL_ADV	Same as PLL_ADV	CLKIN1	string

Notes:

1. The C_CLKOUTn_DESKEW_ADJUST value "PPC" applies only to Virtex-5FXT designs.

Allowable Parameter Combinations

The C_CLKOUTn_DESKEW_ADJUST parameter must be set to NONE for clock outputs connected to the CPMC440CLK and CPMINTERCONNECTCLK pins on the ppc440 primitive in Virtex-5 FXT. Clock output

signals connected to any other pins on the ppc440 primitive must have the C_CLKOUTn_DESKEW_ADJUST parameter set to PPC. Clock output signals connected to soft logic modules that connect to the ppc440 primitive must have the C_CLKOUTn_DESKEW_ADJUST parameter set to PPC. For Virtex-5 FXT designs, the C_CLKFBOUT_BUF parameter must be set to true when used in the recommended configuration shown in Figure 1. For Virtex-5 FXT designs, the C_CLKOUTn_BUF parameters must be set to true for any clock output that is used. The PLL_ADV primitive has additional restrictions on parameter combinations that are allowed for Virtex-5 FXT designs, and these restrictions are documented in the *Virtex-5 User Guide and* Virtex-5 Libraries Guide.

Note: The PLL Module wrapper does not perform any error checking to enforce the design rules and restrictions described in the *Virtex-5 User Guide.*

PLL Module I/O Signals

The input and output signals of the PLL module are described in <RD Red>Table 2.

The table below contains an example of how to create cross-references from the table body to the table notes.

Table 2: PLL Module Input and Output Signals

Signal	Signal Direction	Default Value	Description
CLKFBDCM	Output	Same as PLL_ADV primitive	Feedback clock signal to use when the PLL drives a DCM or is driven by a DCM
CLKFBOUT	Output		Feedback clock output to be connected to CLKFBIN
CLKOUT0	Output		Clock output 0
CLKOUT1	Output		Clock output 1
CLKOUT2	Output		Clock output 2
CLKOUT3	Output		Clock output 3
CLKOUT4	Output		Clock output 4
CLKOUT5	Output		Clock output 5
CLKOUTDCM0	Output		Local copy of CLKOUT0 that connects to the DCM within the same tile
CLKOUTDCM1	Output		Local copy of CLKOUT1 that connects to the DCM within the same tile
CLKOUTDCM2	Output		Local copy of CLKOUT2 that connects to the DCM within the same tile
CLKOUTDCM3	Output		Local copy of CLKOUT3 that connects to the DCM within the same tile
CLKOUTDCM4	Output		Local copy of CLKOUT4 that connects to the DCM within the same tile
CLKOUTDCM5	Output		Local copy of CLKOUT5 that connects to the DCM within the same tile
LOCKED	Output		Synchronous output that goes high when the PLL has achieved phase alignment and frequency matching

Table 2: PLL Module Input and Output Signals

Signal	Signal Direction	Default Value	Description
CLKFBIN	Input		Clock feedback input
CLKIN1	Input		Primary clock input
RST	Input		Asynchronous reset signal

Register Descriptions

Not Applicable.

Timing Diagrams

See the Virtex-5 User Guide for more information.

Design Implementation

Target Technology

This module is intended for use solely on Virtex-5 FXT devices, as well as Spartan 6 devices, although the PLL_ADV primitive is available on all Virtex-5 devices.

Device Utilization and Performance Benchmarks

This module uses one PLL primitive and one BUFG primitive for each clock output that is used.

Reference Documents

1. UG190 *Virtex-5 User Guide*
2. *Virtex-5 Libraries Guide for HDL Designs*

Revision History

Date	Version	Revision
3/2/2009	1.0	Initial Xilinx release.

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