EE517
Analog VLSI Lab
Experiment 6

Design and analysis of a 2-stage op-amp

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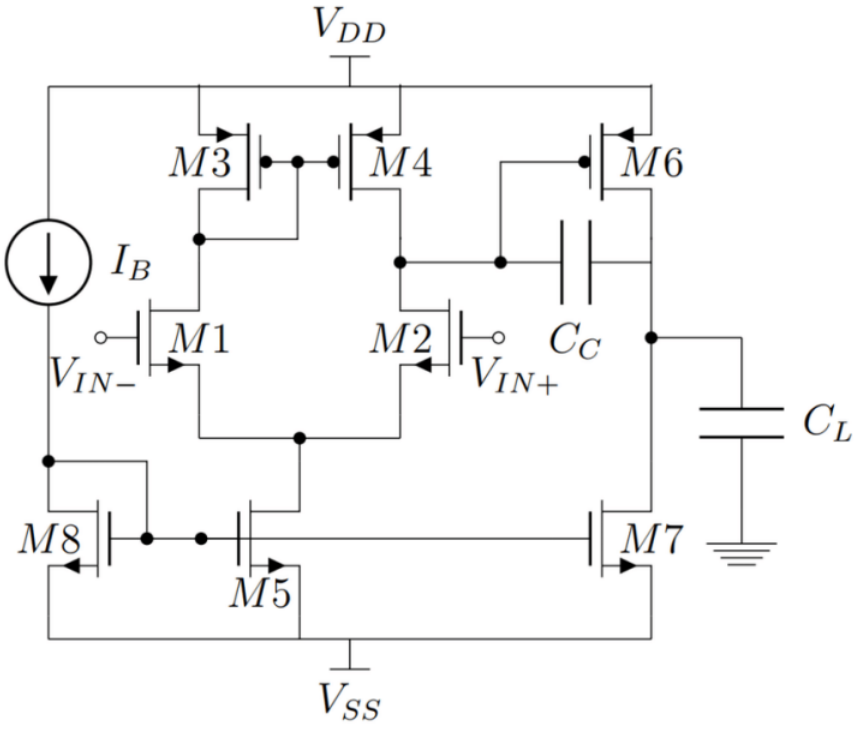
1 Objective

Design and analyze a 2-stage op-amp with the Design specification mentioned below.
Design Specification:

1. Av=2000; GBW = 15MHz; CL = 10pF; ICMR = 0.8-1.6V; Slew Rate = 10V/µs
2. MOSFET length of 180nm is assumed.
3. A bias current of 40µA is assumed.
4. A voltage supply of 1.8V is used.

2 Theory



From the figure, M1 and M2 are taking the inputs. M3 and M4 are PMOS current source and M5 is providing constant current (acting as current source)

Here, M1,M2,M3,M4 and M5 can be considered to be in stage 1 where it provides maximum gain. M6 and M7 are considered to be in stage 2 which provides maximum output swing.

An operational transconductance amplifier is a differential to single ended amplifier. The structure is a bit different compared to a differential structure since it uses a current mirror in above. This is done to increase the transconductance which in turn increases the Gain of the single ended output. Here we have shown a single stage OTA however multistage OTAs are also used.

Two stage OTAs give advantages in two aspects. This can be used to get higher gain compared to single stage and the output swing is also higher than single stage.

3 Calculations

1. From the desired phase margin, choose the minimum value for Cc, i.e. for a 60° phase margin we use the following relationship. This assumes that z>= 10GB. Hence we get

$$C_c = 0.22 * C_L \tag{1}$$

   The Cc is chosen as 4pF.

2. Determine the minimum value for the "tail current" (I5) from

$$I_5 = SR * C_c \tag{2}$$

   Given SR = 10 V/us. So I_5 = 40 uA.

3. Design for $(W/L)_3$ from the maximum input voltage specification.

$$(W/L)_3 = \frac{I_5}{K'_p(V_{DD} - V_{in(max)} - V_{Tp} + V_{Tn})} \tag{3}$$

4. Verify that the pole of M3 due to Cgs3 and Cgs4 will not be dominant by assuming it to be greater than 10 GB

$$g_{m3} = \sqrt{2I_D K'_p (W/L)_3} \tag{4}$$

$$\rho 3 = -\frac{gm3}{2Cgs3} \tag{5}$$

5. Design for (W/L)1 ((W/L)2) to achieve the desired GB.

$$gm1 = GBW * C_c * 2\pi \tag{6}$$

Here, gm1 = 376.99μA/V

$$(W/L)1, 2 = \frac{g_{m1}^2}{2K'_n I_1} \tag{7}$$

6. Design for (W/L)5 from the minimum input voltage. First calculate VDS5(sat) then find (W/L)5.

$$(Vds)5, sat = Vin(min) - VSS - \sqrt{I5/B1} - V_{Tn}) \tag{8}$$

$$(W/L)5 = \frac{2I_5}{K'nV_{ds5,sat}} \tag{9}$$

7. Find S6 by letting the second pole (p2) be equal to 2.2 times GB and assuming that VSG4 = VSG6.

$$gm6 >= 10gm1 \tag{10}$$

$$(W/L)6 = (gm6/gm4)(W/L)4 \tag{11}$$

8. Calculate I6 from

$$I6 = \frac{g^2 m6}{2K'n(W/L)6} \tag{12}$$

Check to make sure that (W/L)6 satisfies the Vout(max) requirement and adjust as necessary.

9. Design S7 to achieve the desired current ratios between I5 and I6. (Check the minimum output voltage requirements)

$$(W/L)7 = (I6/I5)(W/L)5 \tag{13}$$

10. From above equations we get:

$$(W/L)_{1,2} = 11.1 \approx 12 \tag{14}$$

$$(W/L)_{3,4} = 8.33 \approx 9 \tag{15}$$

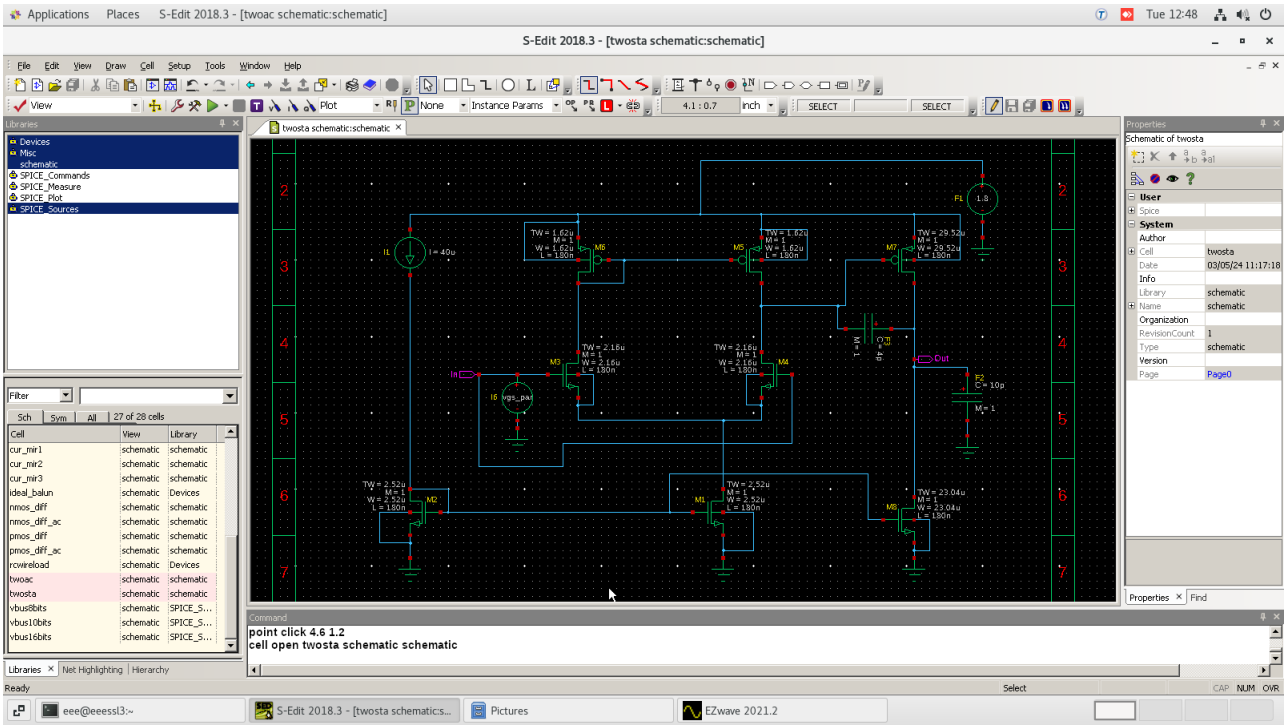
$$(W/L)_{5,8} = 13.516 \approx 14 \tag{16}$$

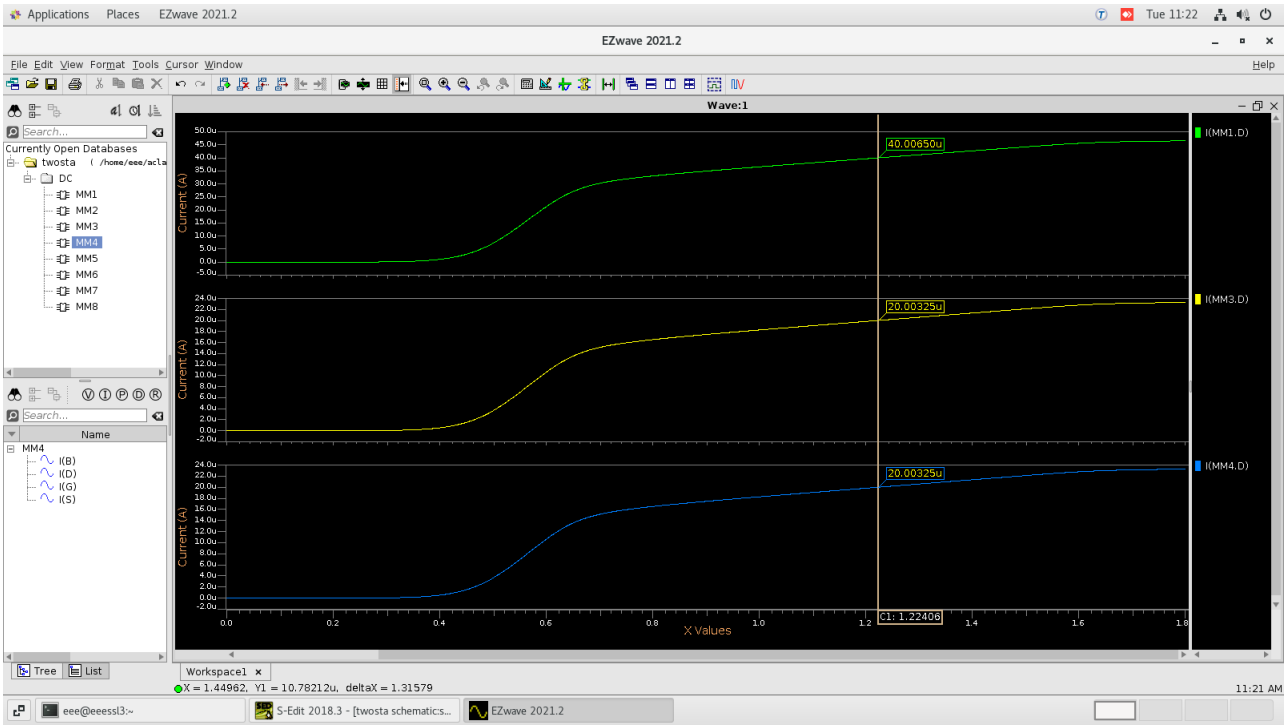
$$(W/L)_{6} = 163.245 \approx 164 \tag{17}$$

$$(W/L)_{7} = 127.55 \approx 128 \tag{18}$$

Here, I am considering L= 320nm to get Av to be 2000 approximately.

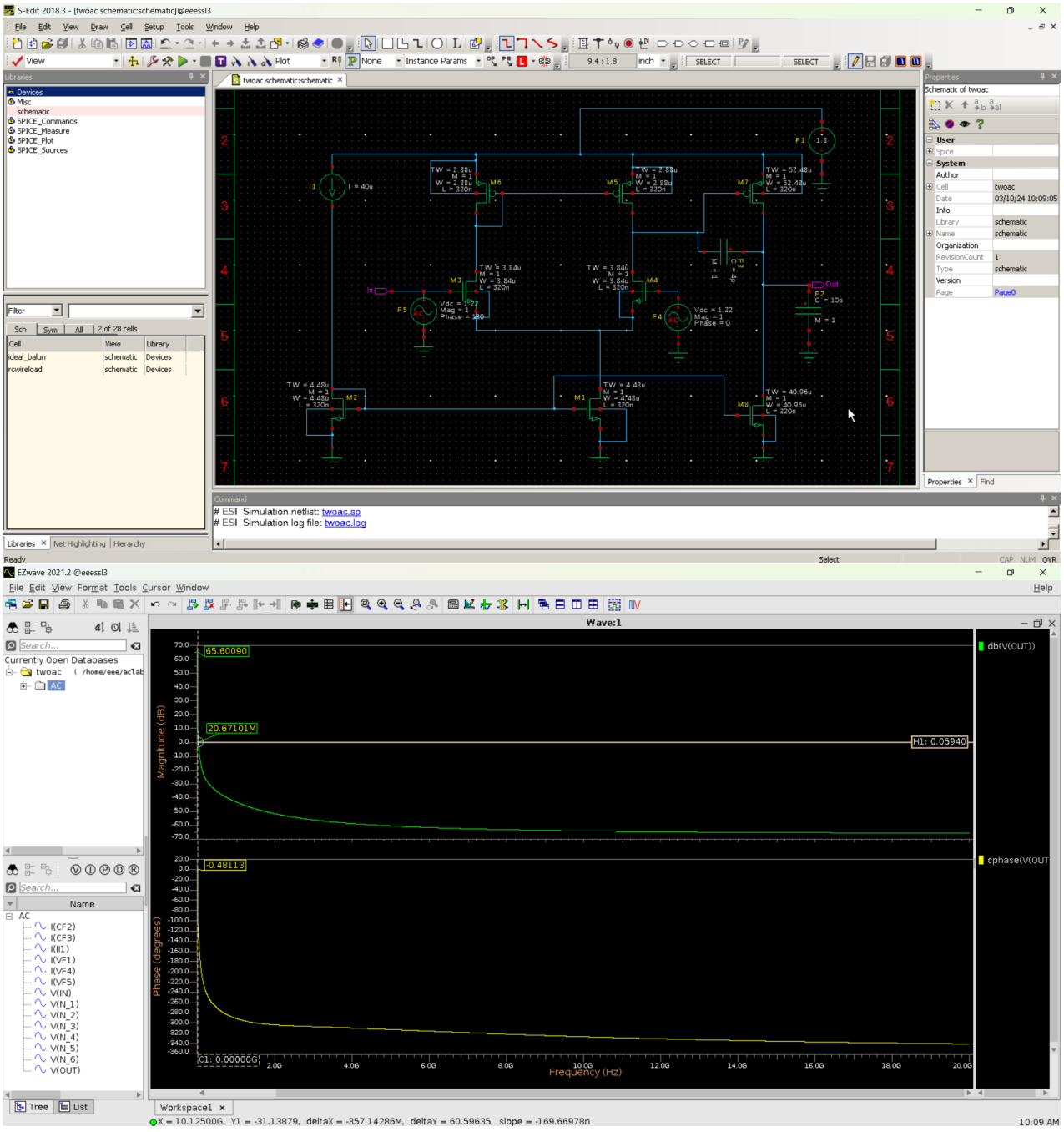
4 DC Analysis





From the DC analysis, we found the Vgs value to be 1.22V

5 AC Analysis



6 Observations:

Parameter	Experimental Values	Expected Values
Voltage Gain	65.6dB	66.6dB
GBW	20.671MHz	15MHz

- As the (W/L)6 was changed the gain was varying. So it is adjusted to have higher gain.
- As feedback is introduced in the open loop system the Gain is reduced and Bandwidth is increased. Also the Phase-Margin is increased significantly which makes the system more stable.

7 Conclusion

All the results have been obtained practically and matching with the theoretical justification. The theoretical calculations have been done.