EE517
Analog VLSI Lab
Experiment 3

Design and analysis of various current mirror circuits

Submitted by,
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1 Objective

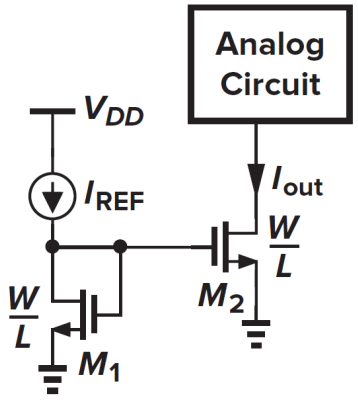
Design and analysis of various current mirror circuits. Also, find the region of operation of the MOSFETS and observe the effect of channel length modulation in all four cases.

1. Basic current mirror circuit with (W/L) = (0.36/0.18) to generate (3Iref) and one third of the reference current (1/3 Iref).
2. Multiple finger based current mirror circuit.
3. Normal cascode current mirror circuit.
4. High swing cascode current mirror circuit.

Provided: Supply of 1.2V, Lmin=180nm, Golden Reference current source of 20uA.

2 Theory

A current mirror is a circuit block which functions to produce a copy of the current flowing into or out of an input terminal by replicating the current in an output terminal. An important feature of the current mirror is a relatively high output resistance which helps to keep the output current constant regardless of load conditions. Another feature of the current mirror is a relatively low input resistance which helps to keep the input current constant regardless of drive conditions.



$$I_{REF} = k'_n(W/L)_1(V_{GS} - VTH)^2 \tag{1}$$

$$I_{out} = k'_n(W/L)_2(V_{GS} - VTH)^2 \tag{2}$$

From (1) and (2) we get,

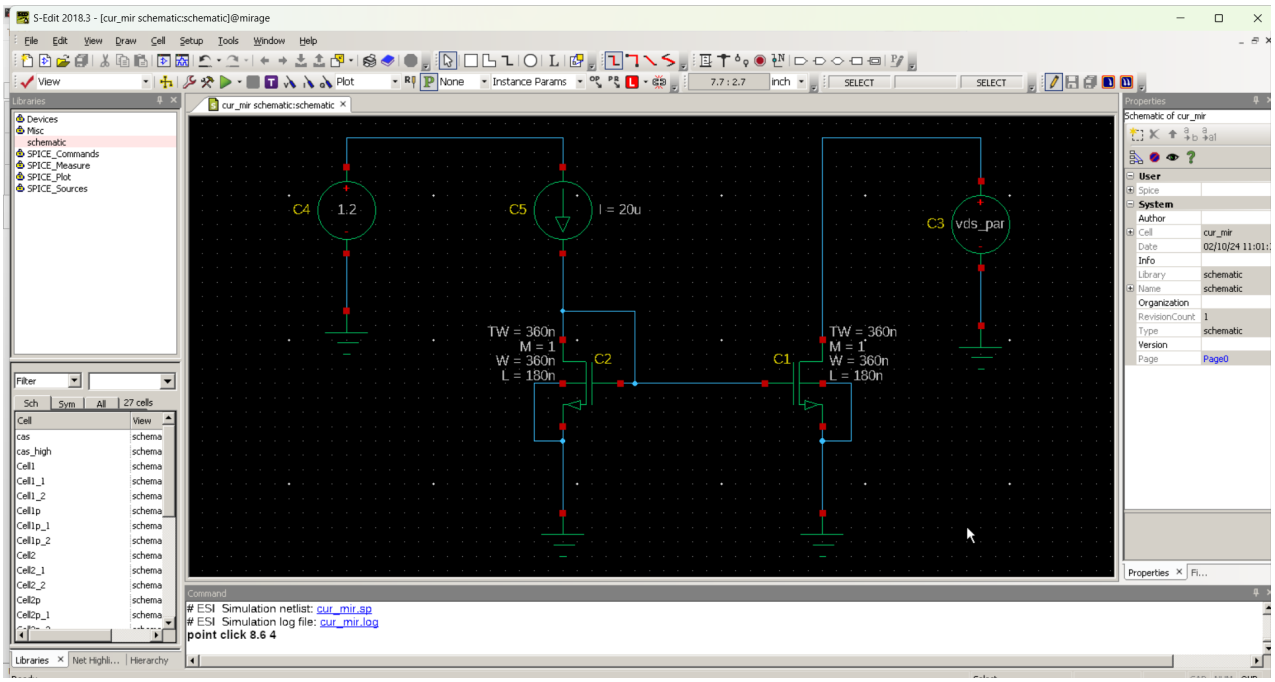
$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF} \tag{3}$$

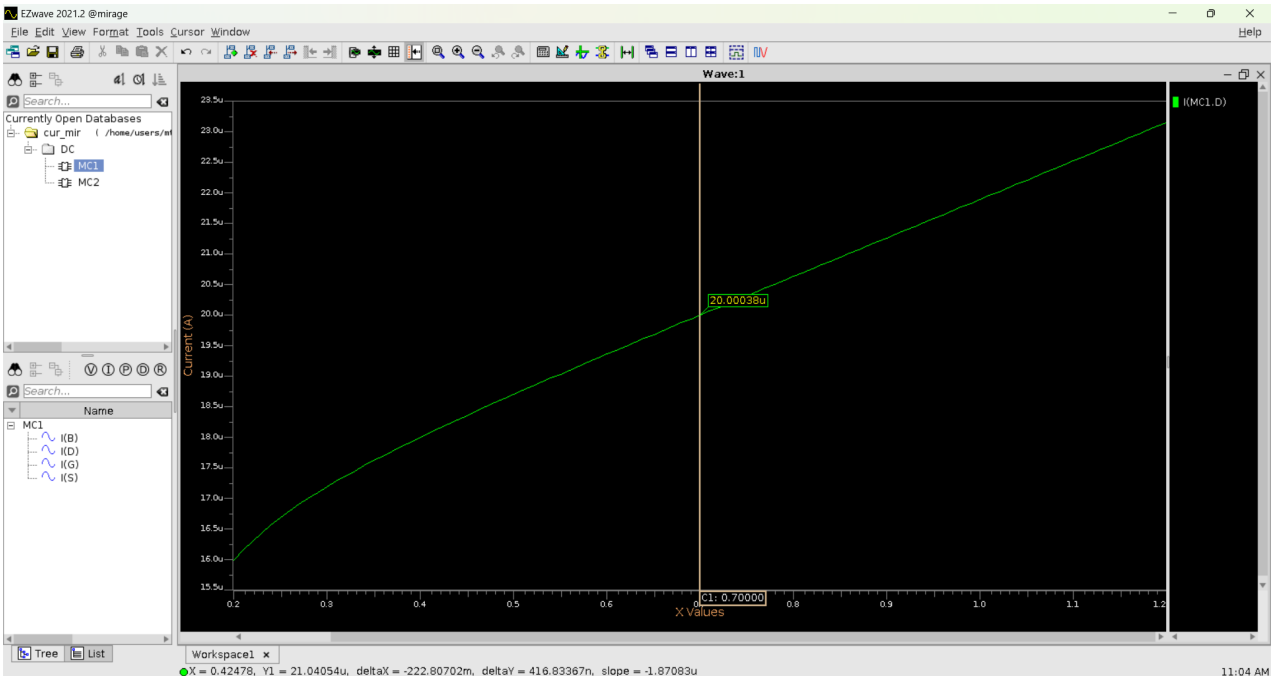
The above equation, in general can be written as,

$$\boxed{I_{COPY} = \frac{(W/L)_{COPY}}{(W/L)_{REF}} I_{REF}} \tag{4}$$

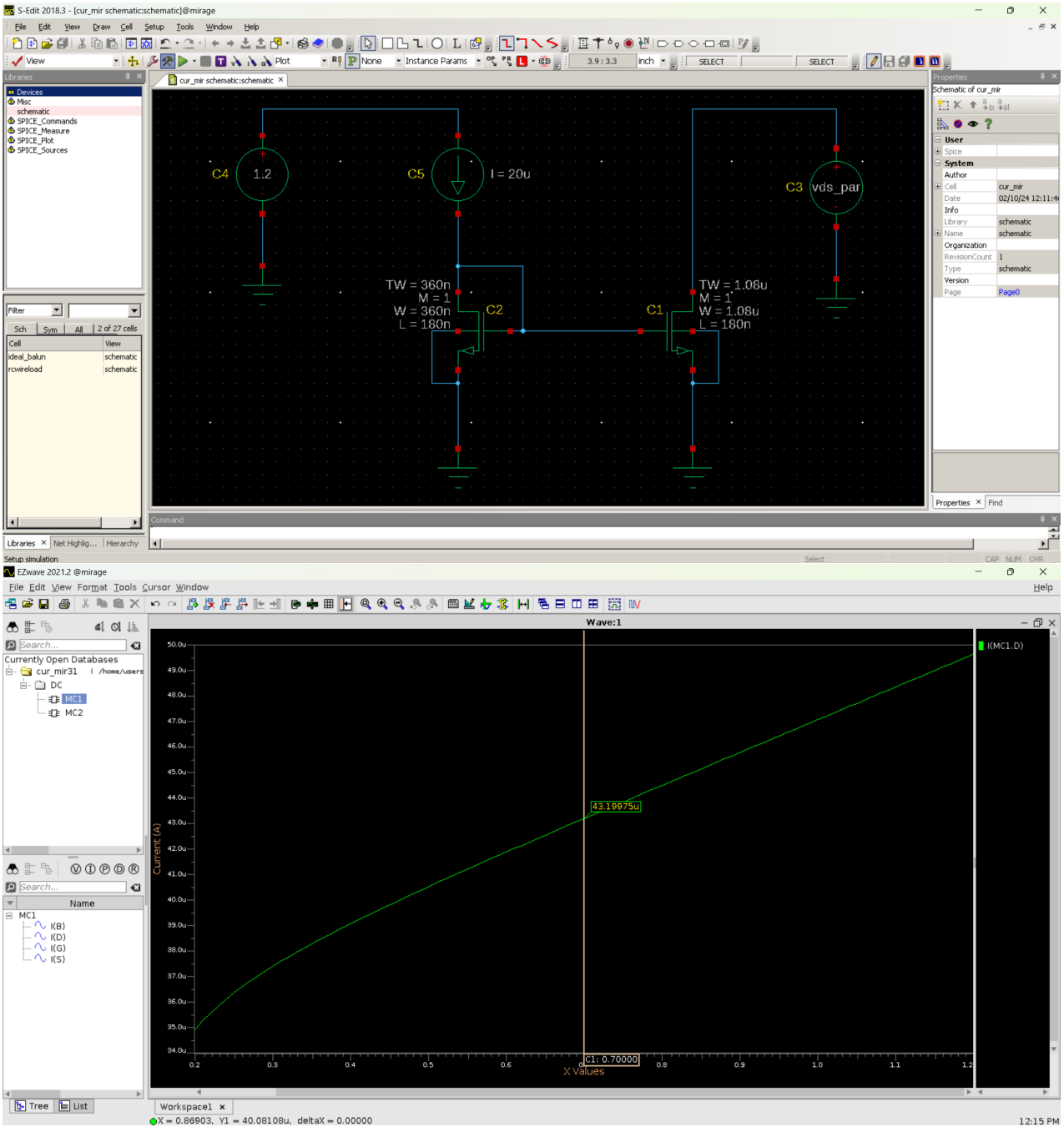
2.1 Basic Current Mirror

2.1.1 Schematic and I_D vs. V_{DS} Graph for $I_{copy} = I_{ref}$

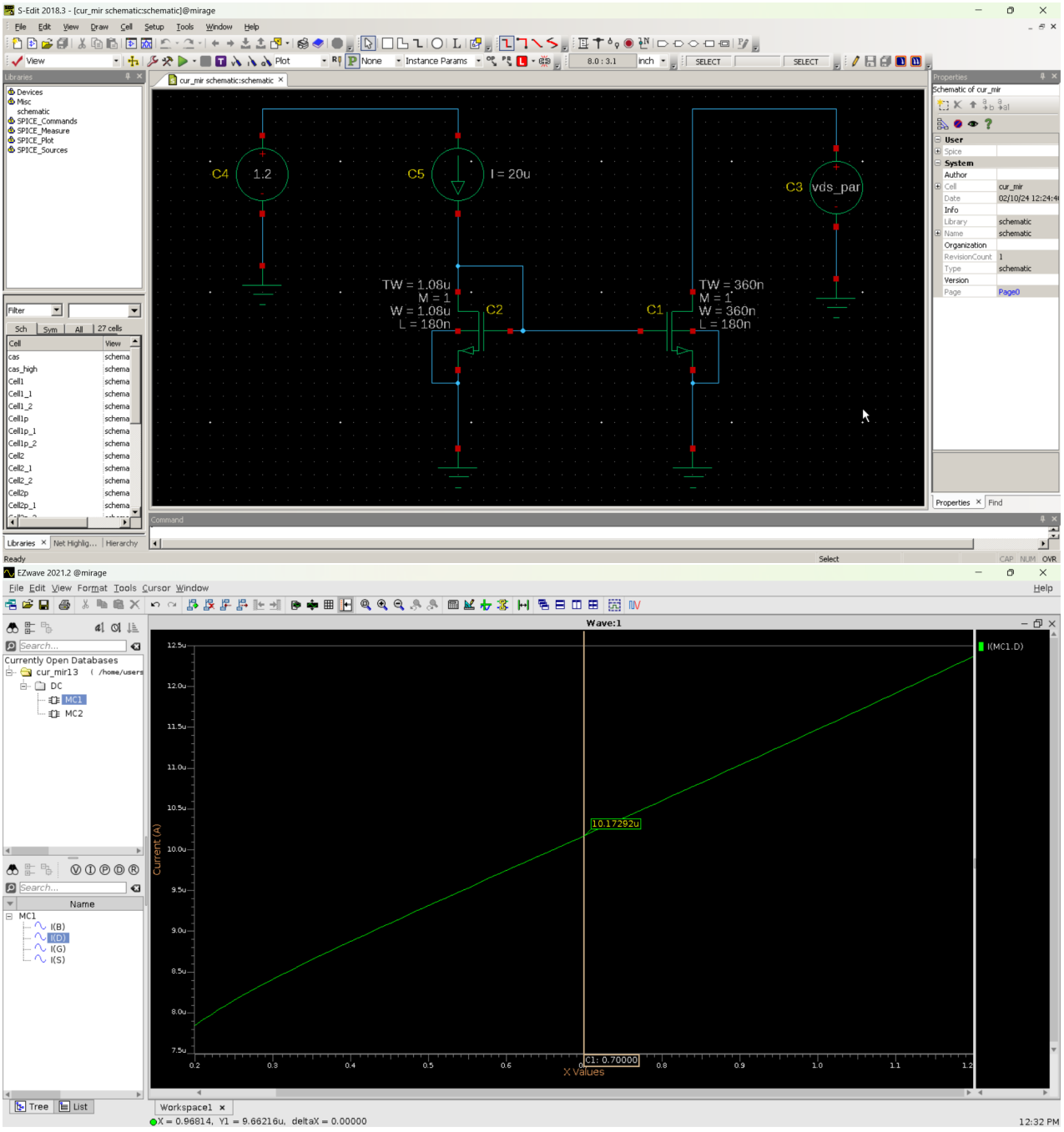



EZwave 2021.2 @mirage
File Edit View Format Tools Cursor Window
Help
Currently Open Databases
cur_mir
DC
MC1
MC2
Name
MC1
I(B)
I(D)
I(G)
I(S)
Tree
List
Wave:1
I(MC1.D)
Current (A)
23.5u
23.0u
22.5u
22.0u
21.5u
21.0u
20.5u
20.0u
19.5u
19.0u
18.5u
18.0u
17.5u
17.0u
16.5u
16.0u
15.5u
20.00038u
C1: 0.70000
0.2
0.3
0.4
0.5
0.6
0.8
0.9
1.0
1.1
1.2
X Values
Workspace1
X = 0.42478, Y1 = 21.04054u, deltaX = -222.80702m, deltaY = 416.83367n, slope = -1.87083u
11:04 AM

2.1.2 Schematic and I_D vs. V_{DS} Graph for $I_{copy} = 3I_{ref}$



2.1.3 Schematic and I_D vs. V_{DS} Graph for $I_{copy} = (1/3)I_{ref}$



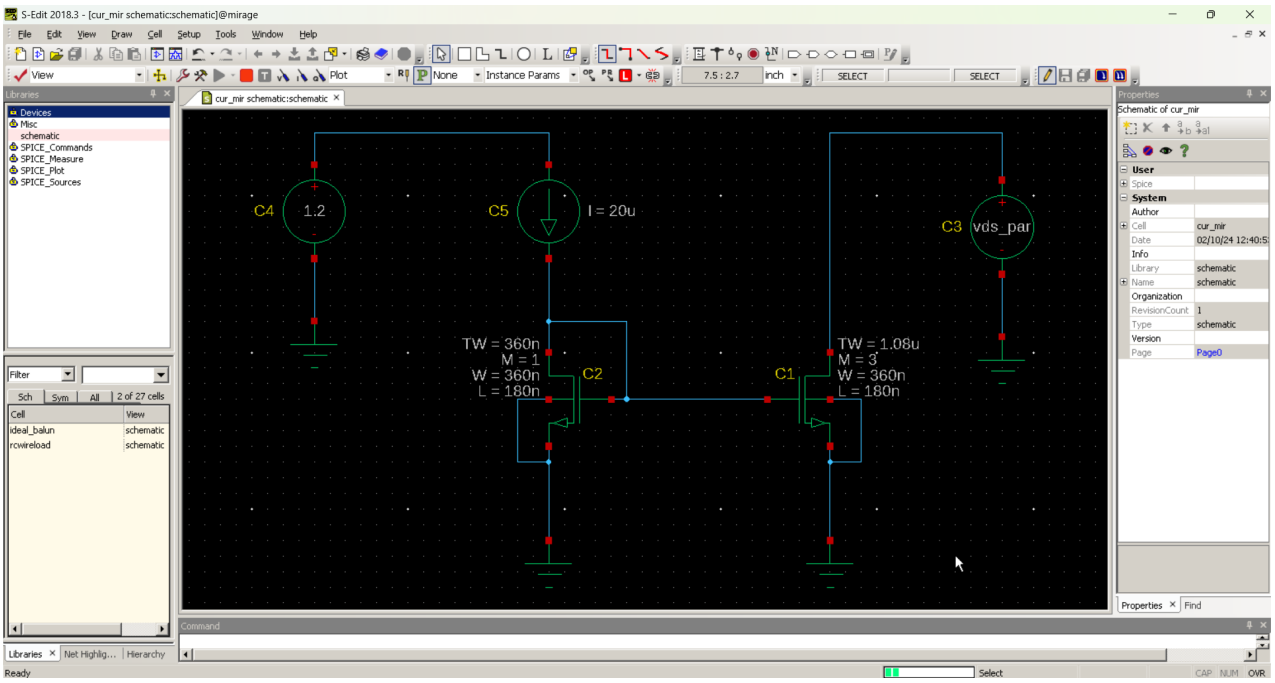
$\frac{I_{COPY}}{I_{REF}}$	$I_D(\mu A)$
1	20
3	43.199
1/3	10.172

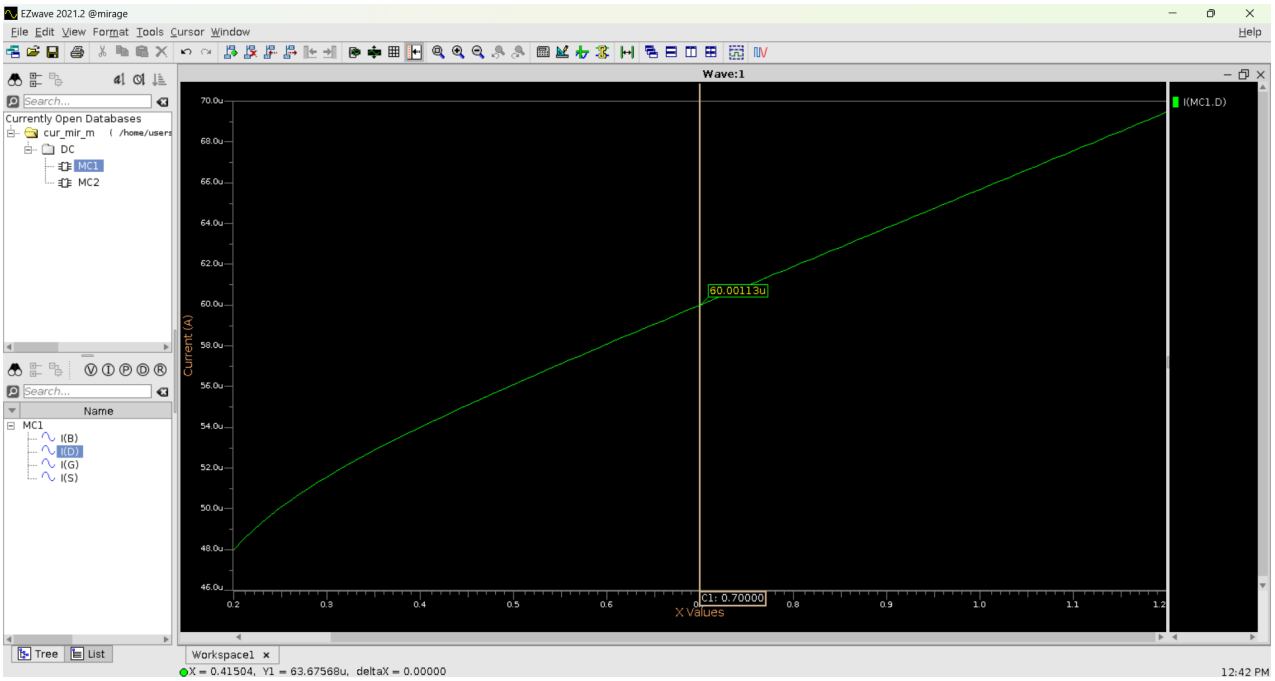
Here, in the circuit, the current is not reaching 3 times that of the reference current because when we increase width to 3 times of that of the reference MOSFET width, the output resistance decreases hence current flows through r_o, thereby loading effect becomes prominent.

2.2 Multiple finger based Current Mirror

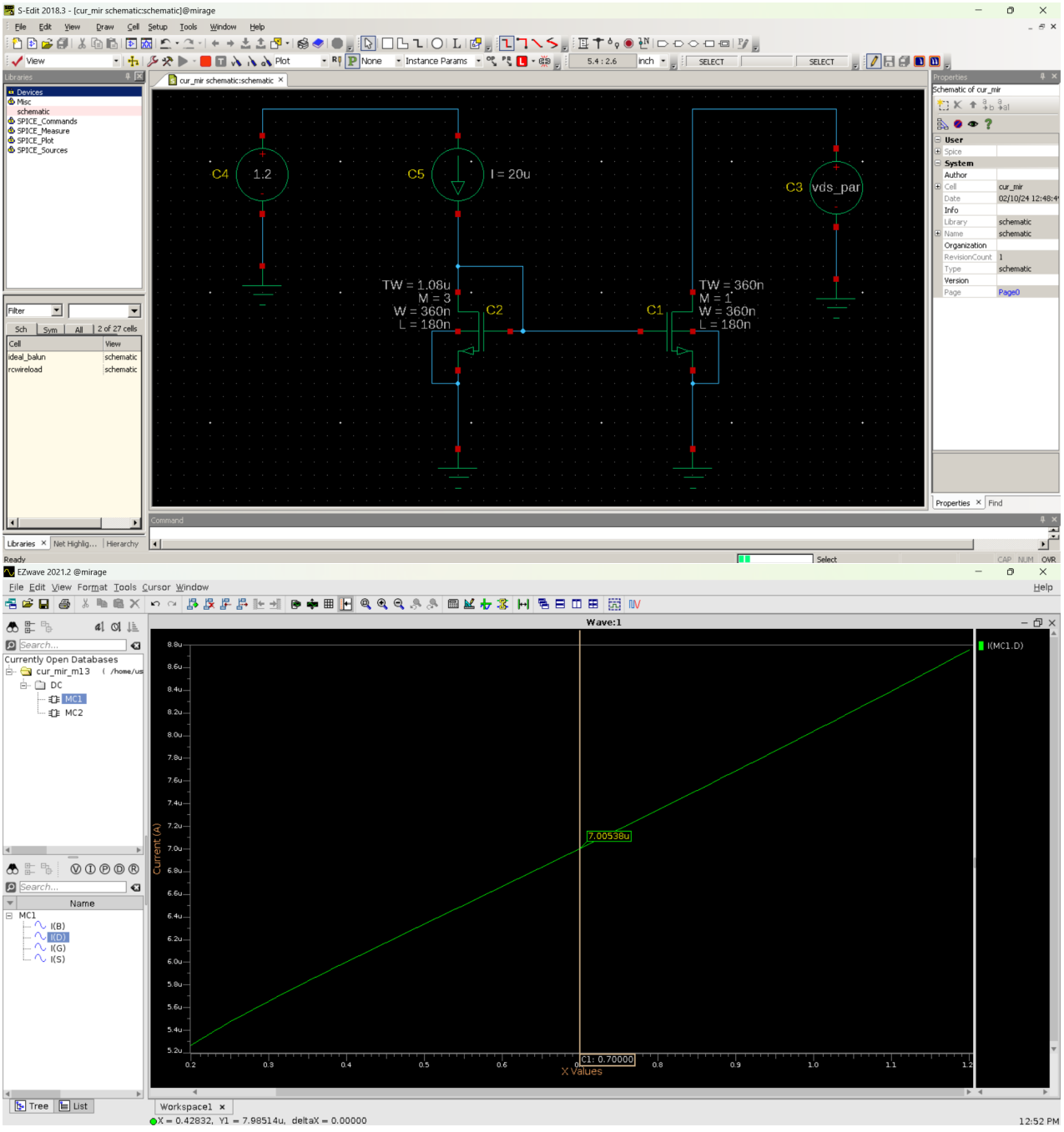
By, increasing the finger, we are keeping the MOSFETs in parallel, thereby not changing W and output impedance remains the same. Here, each mosfet will contribute to current, therefore we get accurate value of 3times that of I_{ref}.

2.2.1 Schematic and I_D vs. V_{DS} Graph for $I_{copy} = 3I_{ref}$




EZwave 2021.2 @mirage
File Edit View Format Tools Cursor Window
Help
Wave:1
Currently Open Databases
cur_mir_m
DC
MC1
MC2
Name
MC1
I(B)
I(D)
I(G)
I(S)
I(MC1.D)
60.00113u
Current (A)
X Values
C1: 0.70000
Tree
List
Workspace1
X = 0.41504, Y1 = 63.67568u, deltaX = 0.00000
12:42 PM

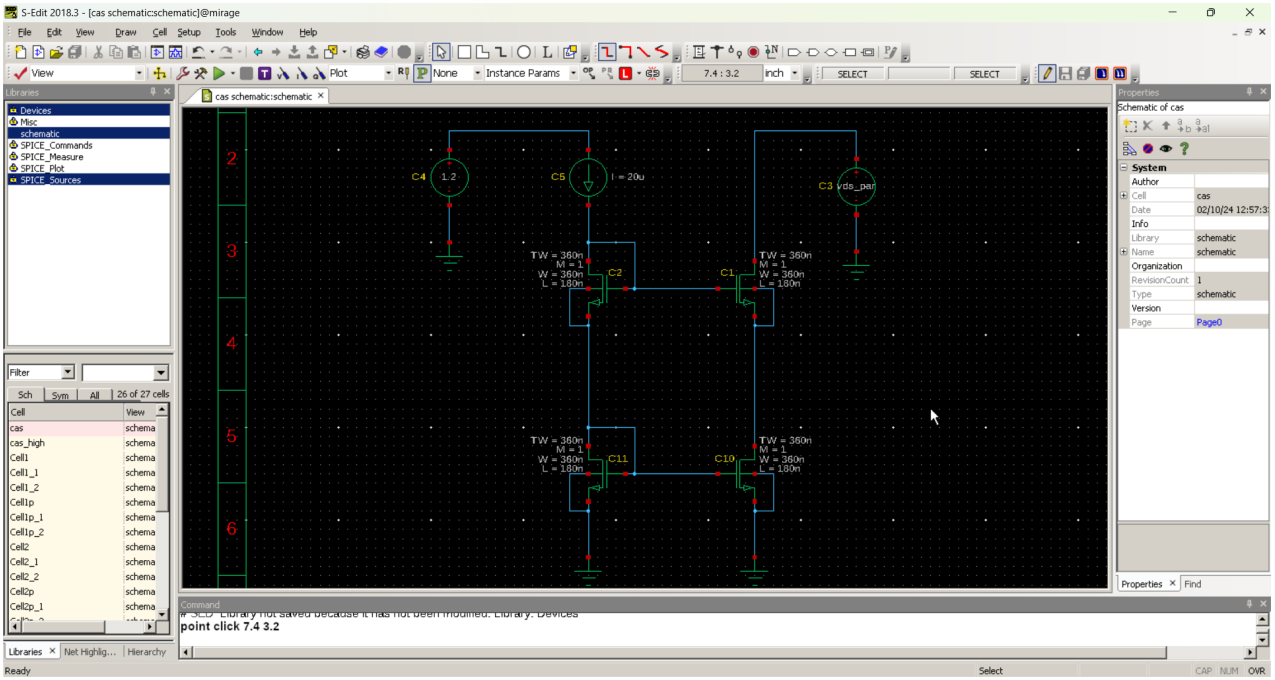
2.2.2 Schematic and I_D vs. V_{DS} Graph for $I_{copy} = (1/3)I_{ref}$

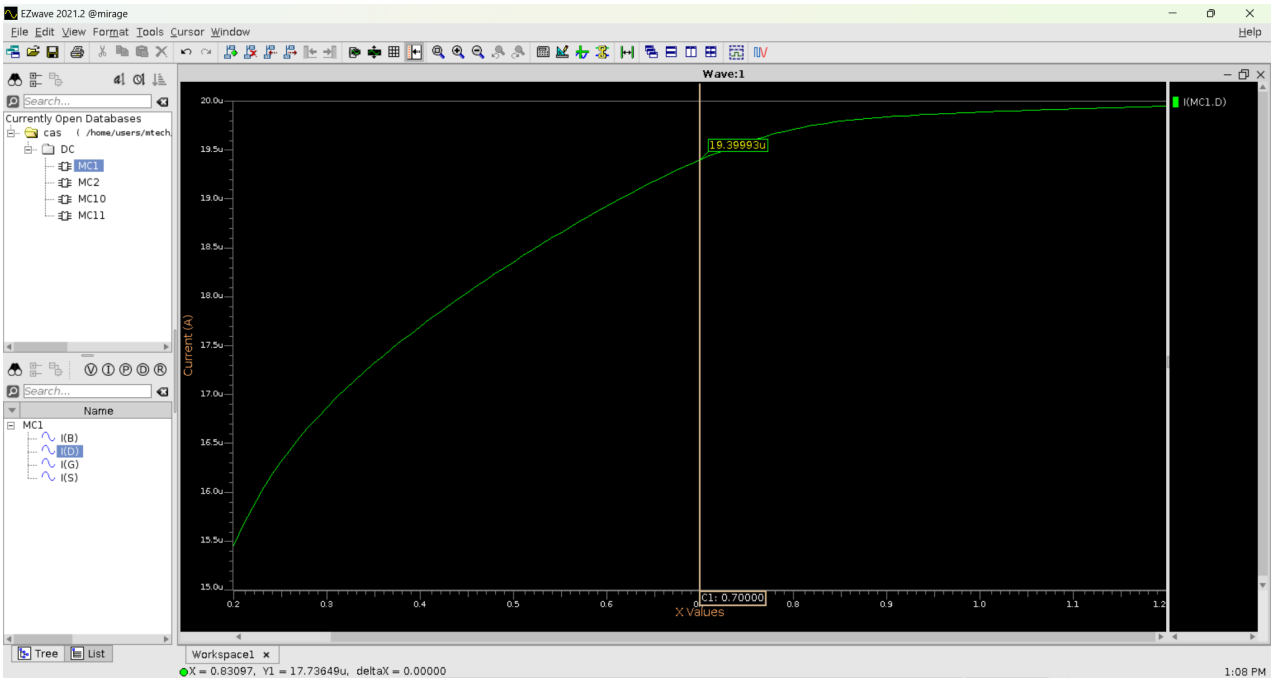


$\frac{I_{COPY}}{I_{REF}}$	$I_D(\mu A)$
3	60
1/3	7.005

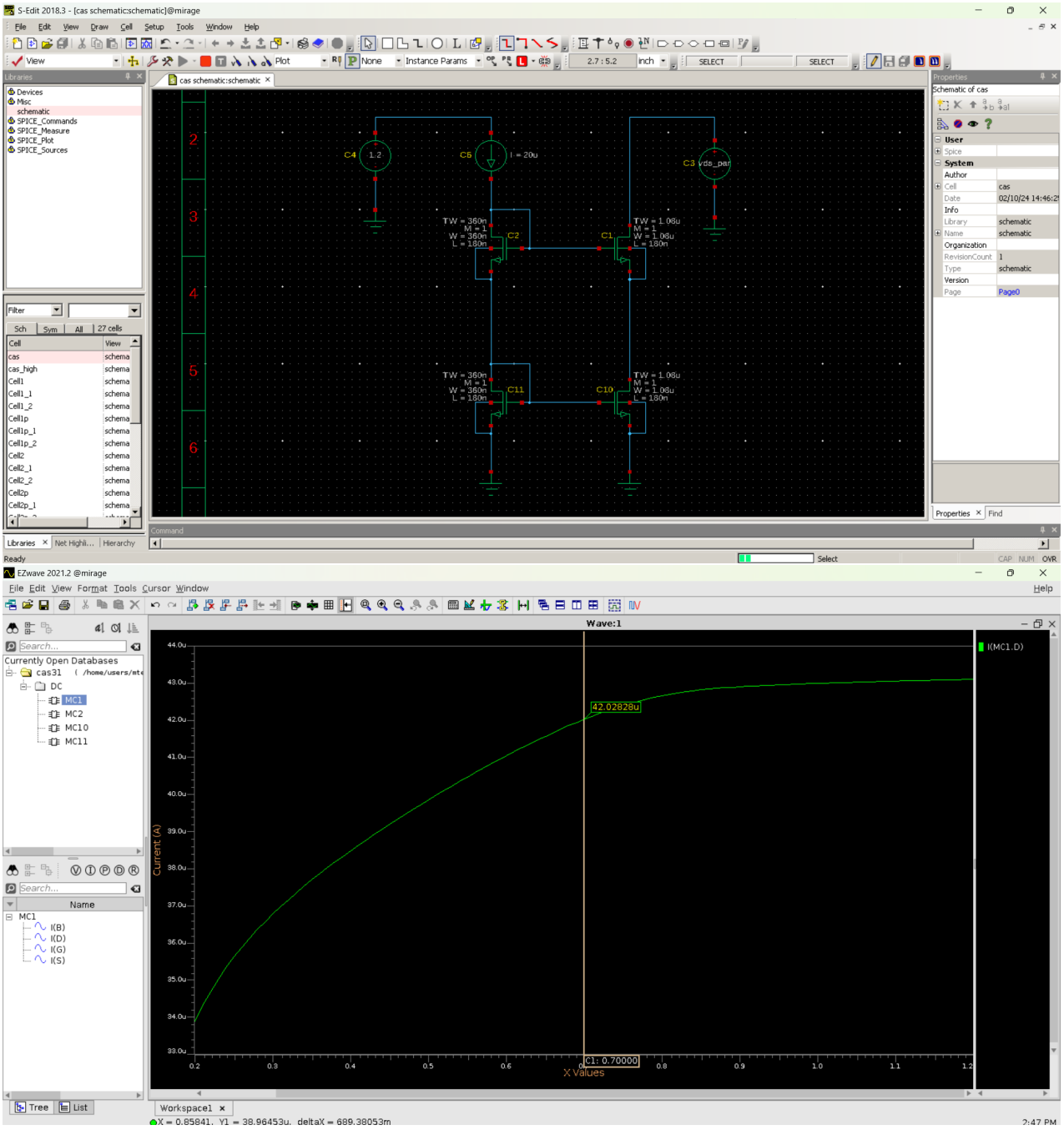
2.3 Cascode Current Mirror

2.3.1 Schematic and I_D vs. V_{DS} Graph for $I_{copy} = I_{ref}$

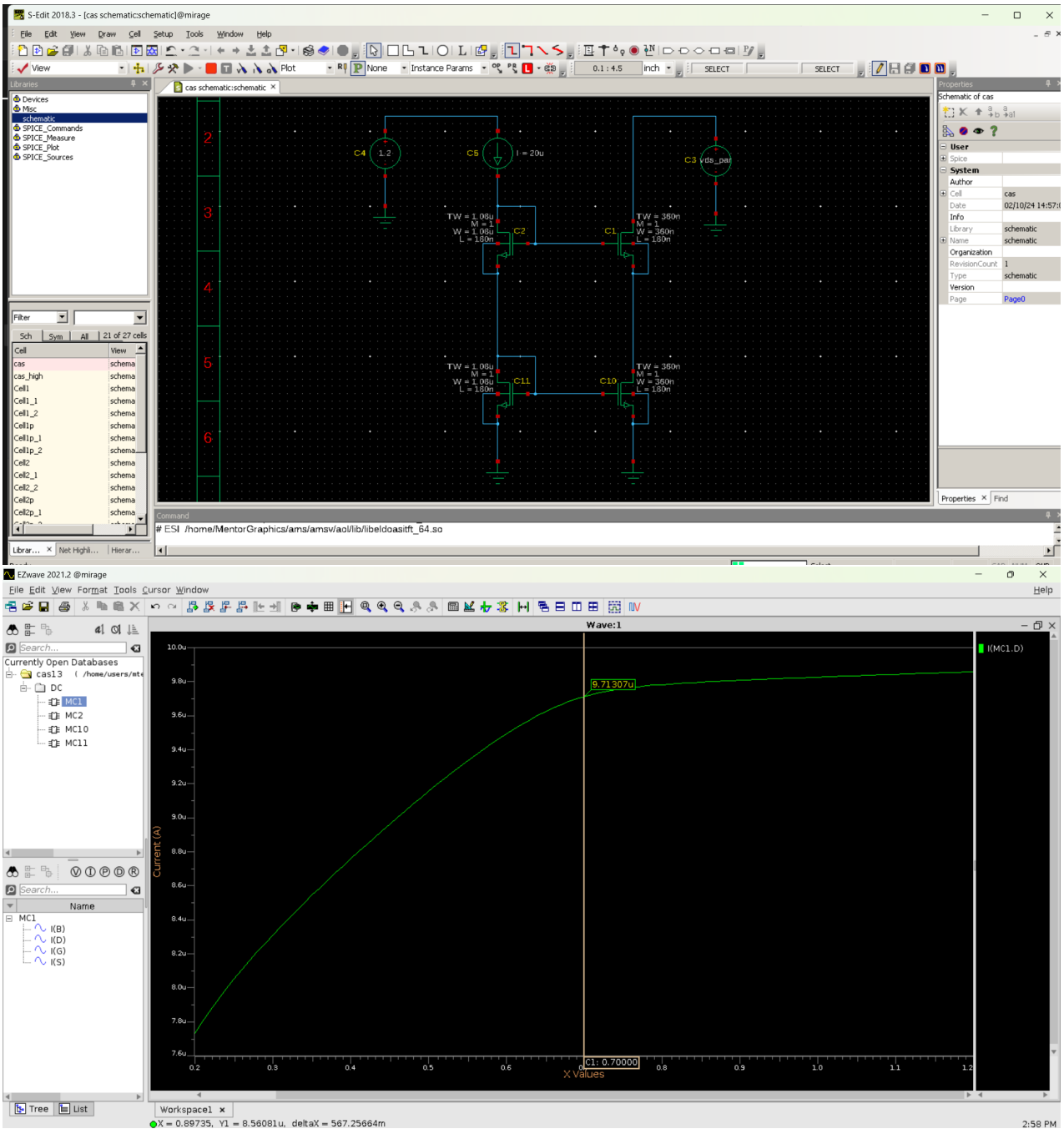



EZwave 2021.2 @mirage
File Edit View Format Tools Cursor Window
Help
Wave:1
Currently Open Databases
cas (/home/users/mtech
DC
MC1
MC2
MC10
MC11
Name
MC1
I(B)
I(D)
I(G)
I(S)
I(MC1.D)
19.39993u
Current (A)
X Values
C1: 0.70000
Tree
List
Workspace1
X = 0.83097, Y1 = 17.73649u, deltaX = 0.00000
1:08 PM

2.3.2 Schematic and I_D vs. V_{DS} Graph for $I_{copy} = 3I_{ref}$



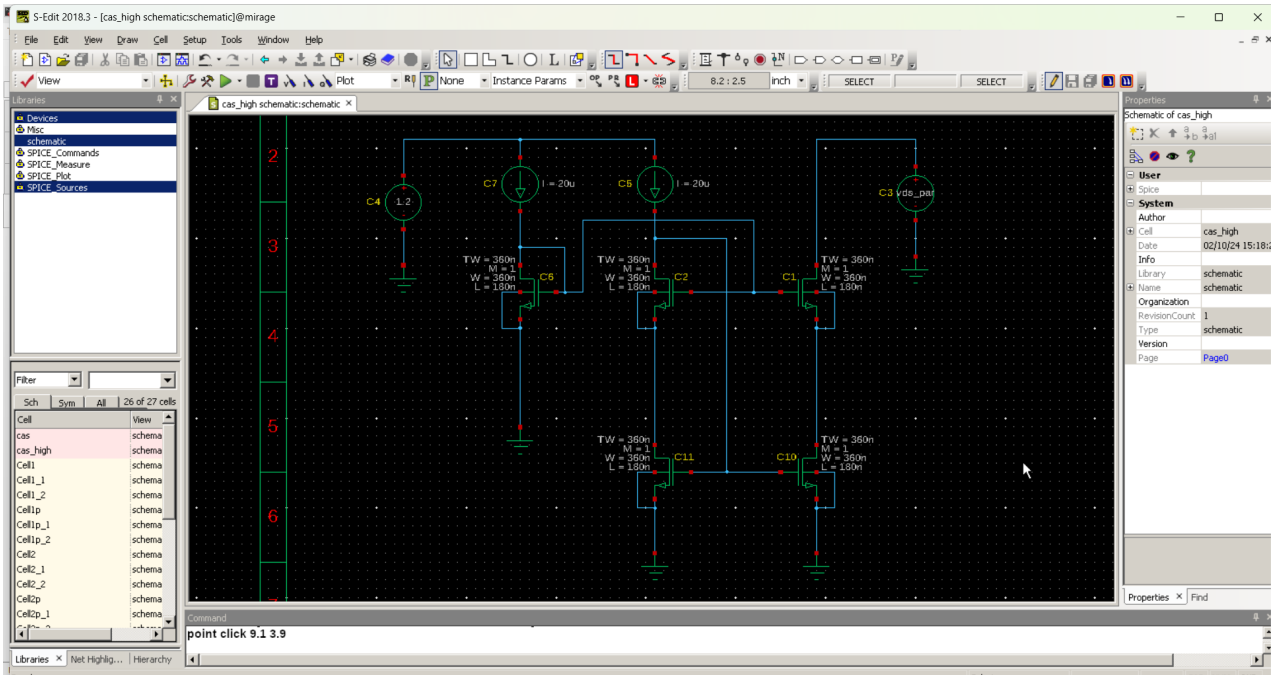
2.3.3 Schematic and I_D vs. V_{DS} Graph for $I_{copy} = (1/3)I_{ref}$

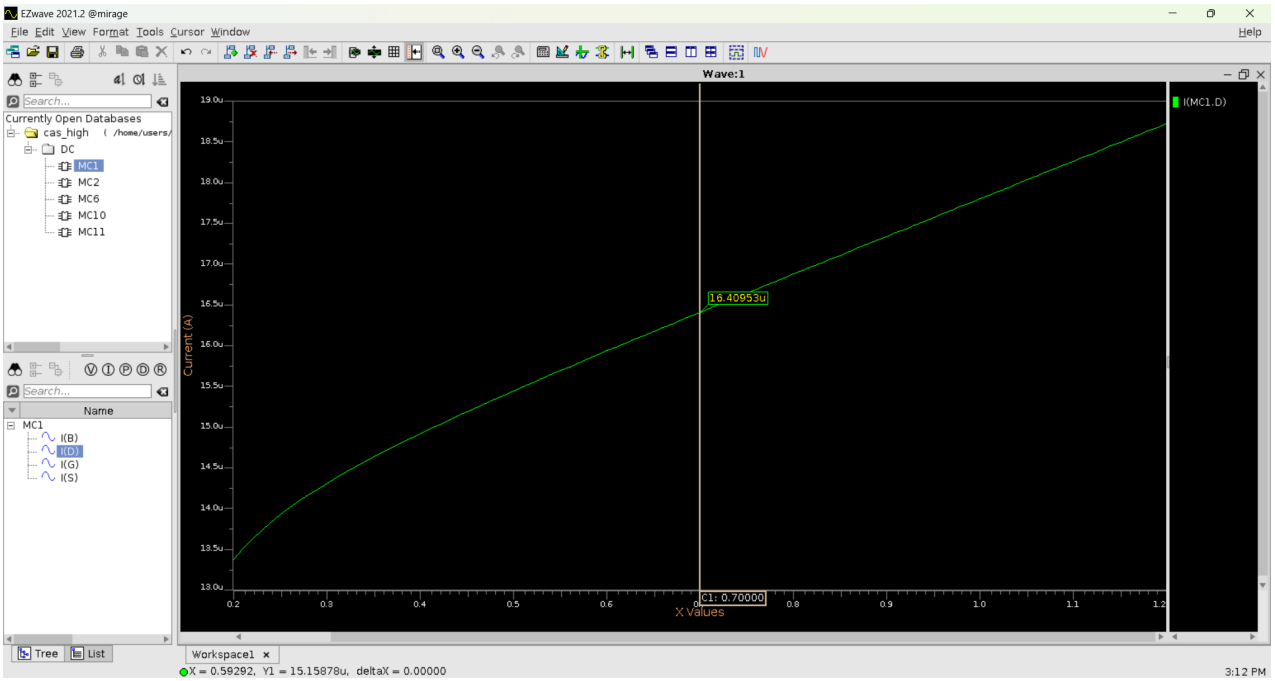


$\frac{I_{COPY}}{I_{REF}}$	$I_D(\mu A)$
1	19.399
3	42.028
1/3	9.713

2.4 High Swing Cascode Current Mirror

2.4.1 No changes in W



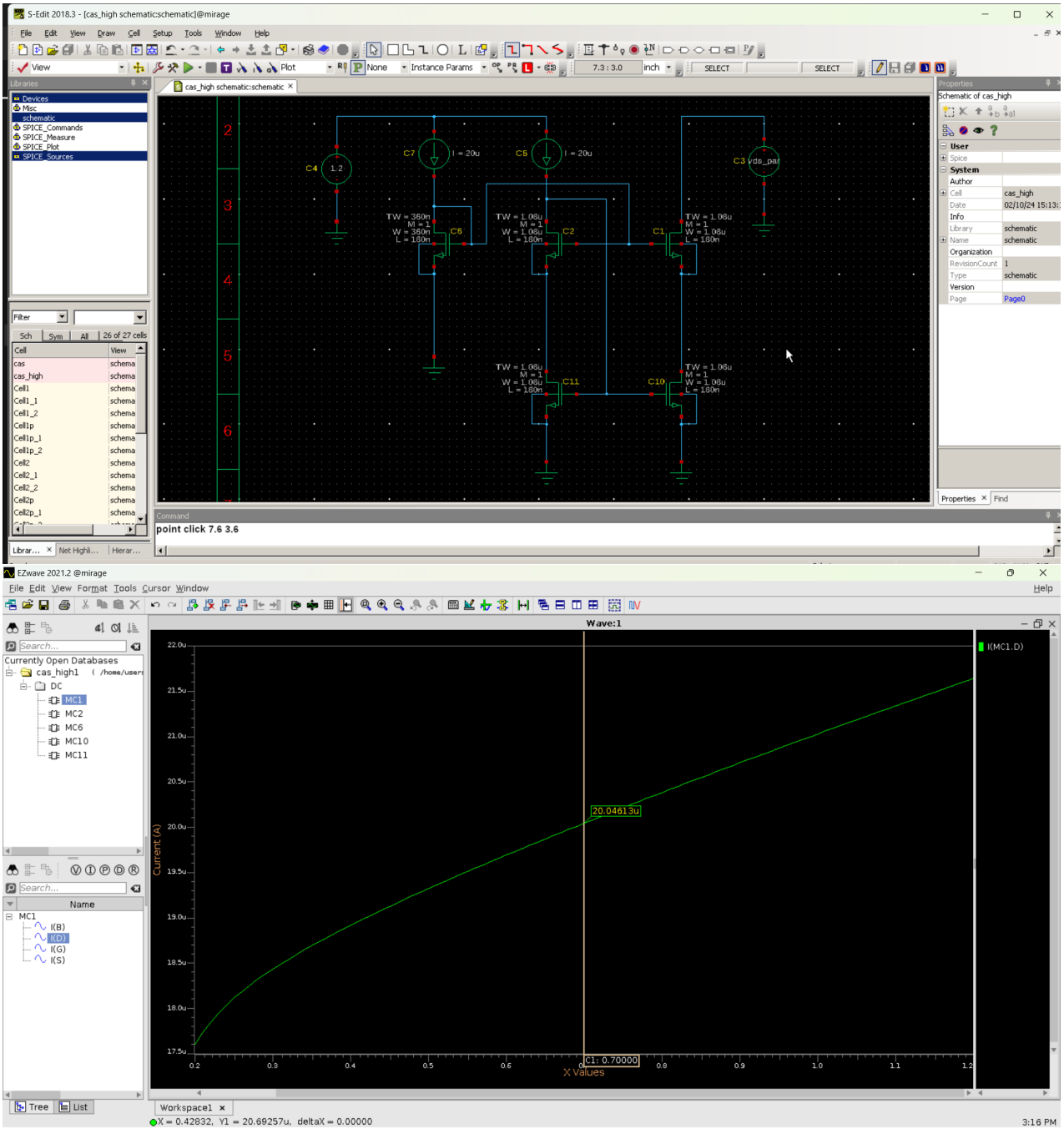


2.4.2 Making C6 MOSFET W=1/4

Since the current is less than I_{REF} in the previous section, we know that,

$$V_{GS} = \sqrt{\frac{2I_D}{k'_n(W/L)}} + V_{TH} \tag{5}$$

Decrease W to (1/4)W of the C6 mosfet or increase 4 times of W for all other mosfets except C6, then we get the V_{DS} twice to its previous value.


S-Edit 2018.3 - [cas_high schematic:schematic]@mirage
cas_high schematic:schematic
C7
I = 20u
C5
I = 20u
C4
1.2
C3
Vds_par
TW = 360n
M = 1
W = 360n
L = 180n
C6
TW = 1.08u
M = 1
W = 1.08u
L = 180n
C2
C1
TW = 1.08u
M = 1
W = 1.08u
L = 180n
C11
C10
point click 7.6 3.6
EZwave 2021.2 @mirage
Wave:1
I(MC1.D)
20.0463u
Current (A)
X Values
C1: 0.70000
MC1
MC2
MC6
MC10
MC11
I(B)
I(D)
I(G)
I(S)
Workspace1
X = 0.42832, Y1 = 20.69257u, deltaX = 0.00000
3:16 PM

Parameter	$I_D(\mu A)$
No change in W	16.40
C6 made to W=1/4	20.04

2.5 Observation

2.5.1 Basic current mirror circuit

- Merit: There is good swing compared to other current mirror circuits as the voltage at output is measured to be $V_{DSAT} = V_{GS}$ - V_{TH}
- Demerit: There is high dependency with respect to V_{DS} because, as we increase W, r_o decreases thereby we can see loading effect here.

2.5.2 Multiple fingers current mirror circuit

- Merit: The MOS devices are in parallel thereby, less dependency with respect to V_{DS}, hence loading effect is not more.

2.5.3 Cascode Current mirror circuit

- Merit: Less dependency with respect to V_{DS}
- Demerit: Low swing as the voltage at the output is $2V_{DS}$+$2V_{TH}$

2.5.4 High Swing Cascode current mirror circuit

- Merit: High swing ie., the voltage at the output is $2V_{DS}$ but compared to basic current mirror the swing is less. Less dependency of V_{DS}.

2.6 Conclusion

All the results have been obtained practically are matching with the theoretical justification. The analysis has been done in each section and merits and demerits are noted in the previous section.