EE518
Digital IC design
Experiment 3

Design of an inverter chain using progressive sizing to improve delay performance and compare its delay with single-stage inverter.

(a) To calculate delay and input capacitance for single-stage inverter.

(b) To compare the propagation delay of 'single-stage inverter' vs 'inverter chain' using progressive sizing.

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1 OBJECTIVE

(a) To design a single-stage CMOS inverter. Obtain input capacitance using ac analysis. Also, calculate the delays using transient analysis.

(b) To design a CMOS inverter chain using progressive sizing. Depending upon the input capacitance, load capacitance, and number of stages, obtain W/L ratio of each inverter stage. Calculate the delays using transient analysis.

2 THEORY

When the inverter is sized up an, delay is reduced, but increases input capacitance of the inverter. To determine the input loading effect, the relationship between the input gate capacitance and the intrinsic output capacitance of the inverter has to be established. Both are proportional to the gate sizing. Hence, the following relationship holds, independent of gate sizing.
F represents the overall effective fanout of the circuit, and equals $\frac{C_{load}}{Cin}$. Observe how the relationship between t_p and F is a very strong function of the number of stages.As expected, the relationship is linear when only 1 stage is present. Introducing a second stage turns it into square root, and so on.
The optimum N is found by differentiating the minimum delay expression divided by the number of stages and setting the result to 0, giving
$N = ln(F)$.

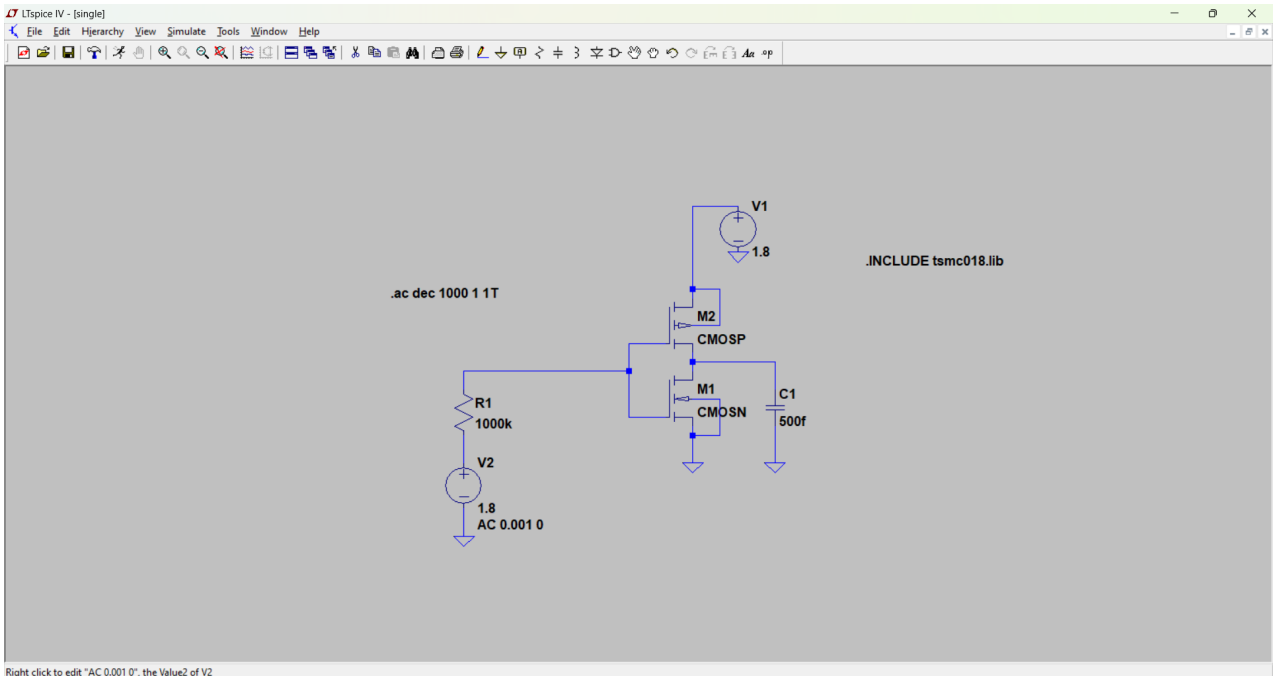
3 FORMULAE

1. We find input capacitance using this formula. Knowing the frequency, we can easily find the capacitance as R=1$M\Omega$, $f_c = \frac{1}{2*\pi*R*C_{in}}$
2. Optimum $N = ln(F)$
3. We find the overall effective fanout using the formula, F = $(\frac{C_{load}}{Cin})$
4. The effective fanout is found using the formula, f = $(F)^{\frac{1}{N}}$

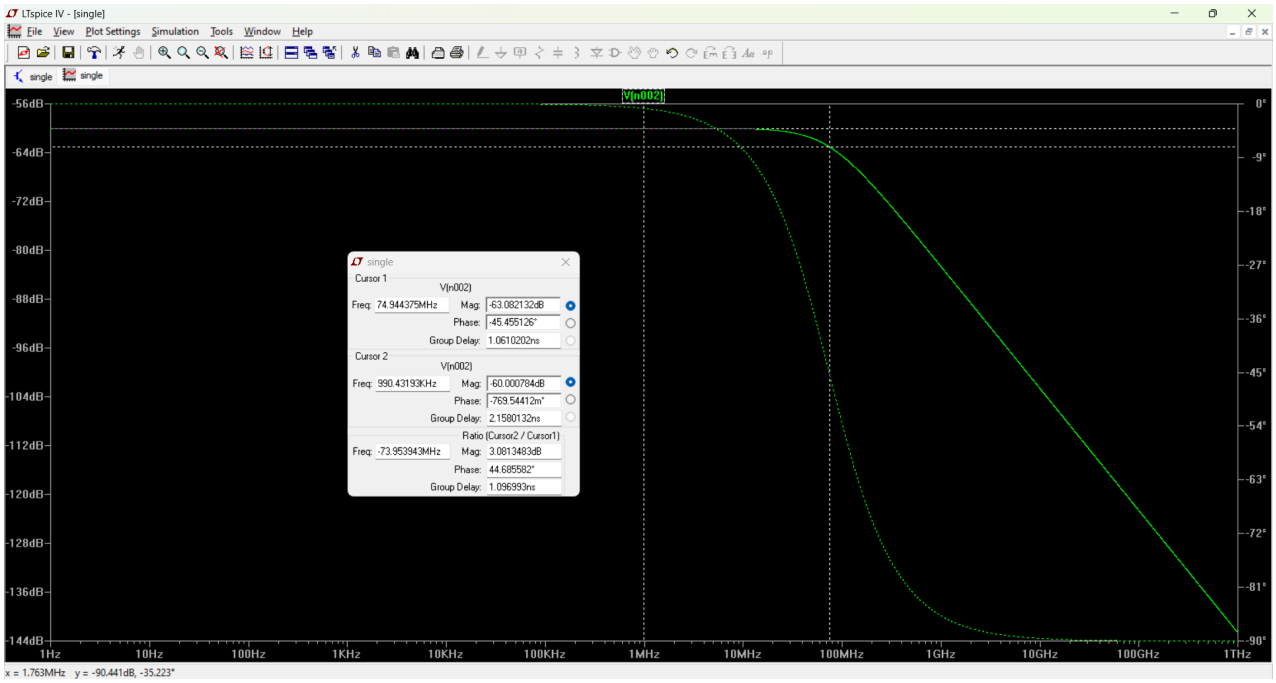
4 PROCEDURE AND RESULTS

4.1 Single CMOS Inverter

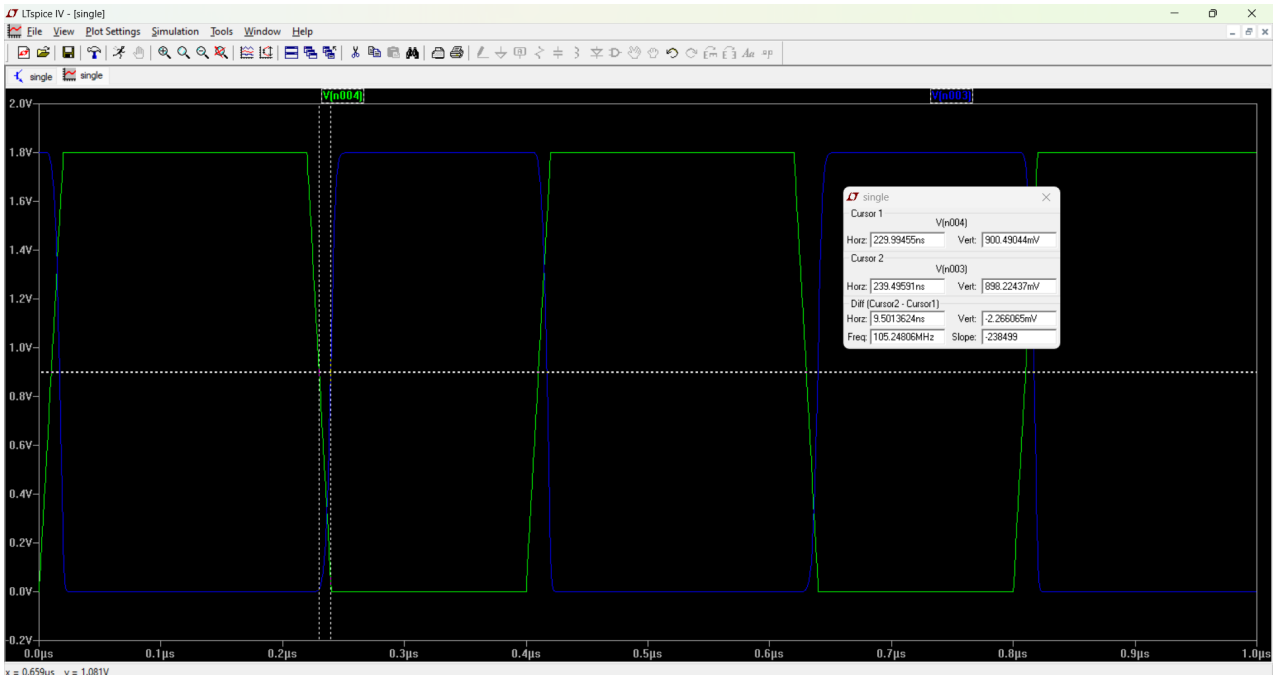
Connect the inverter as shown in the schematic.



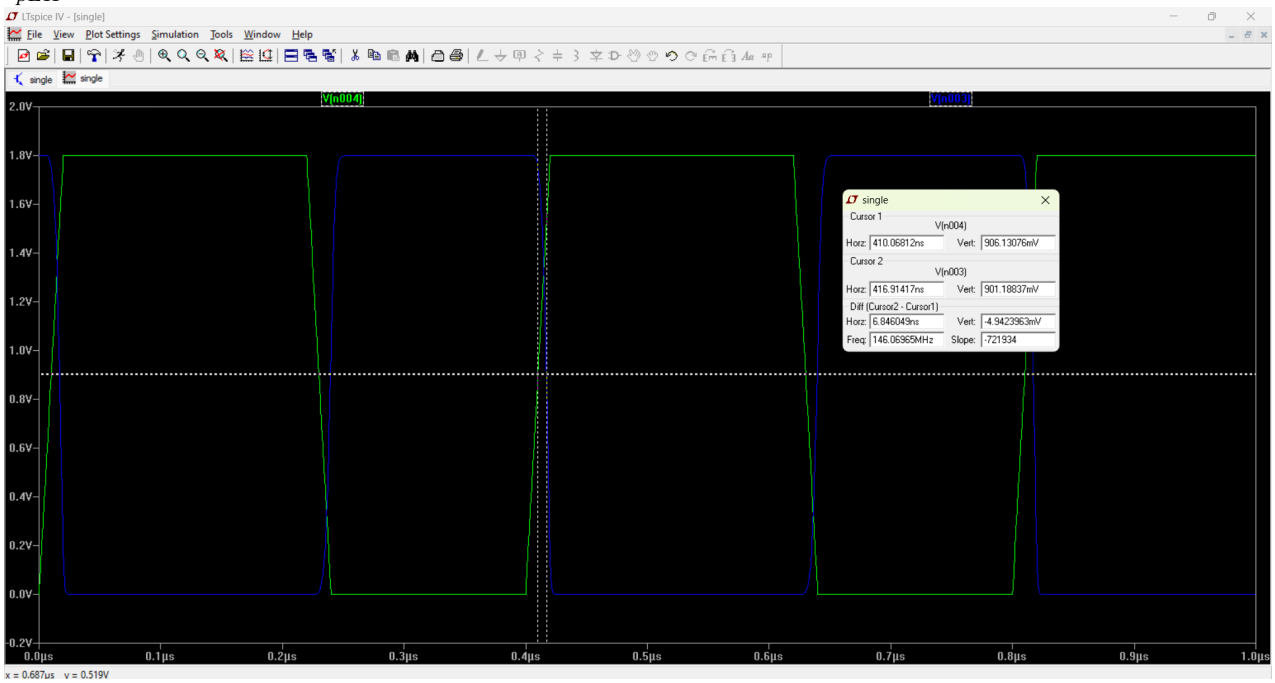
To find input capacitance, connect the Resistor of $1M\Omega$ at gate terminal. Apply ac input and vary its frequency from 1Hz-1THz. Plot the graph for the voltage across Gate terminal (input terminal) and the frequency. Note the -3dB frequency from the plot as shown below. Calculate the gate/input capacitance using the formula $f_c = \frac{1}{2*\pi*R*C_{in}}$



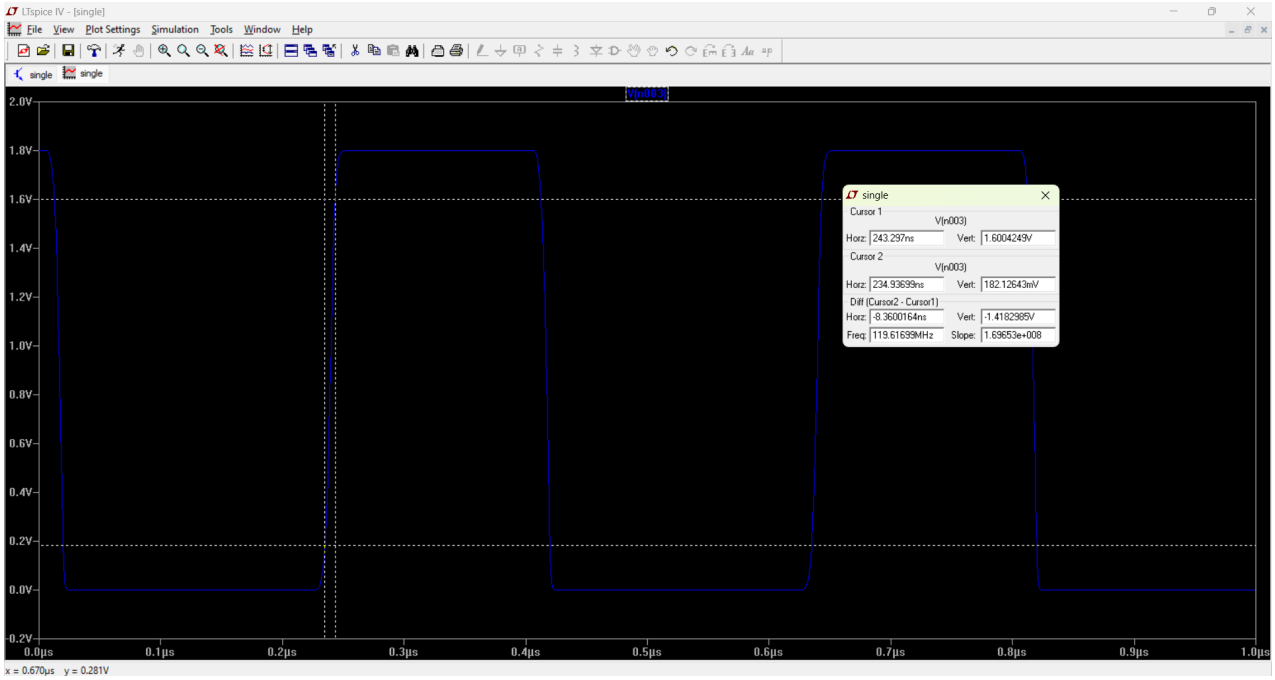
Now find transient parameters V_{in}, V_{out} wrt time axis. Measure t_{rise}, t_{fall}, t_{pHL} and t_{pLH} from the plot.



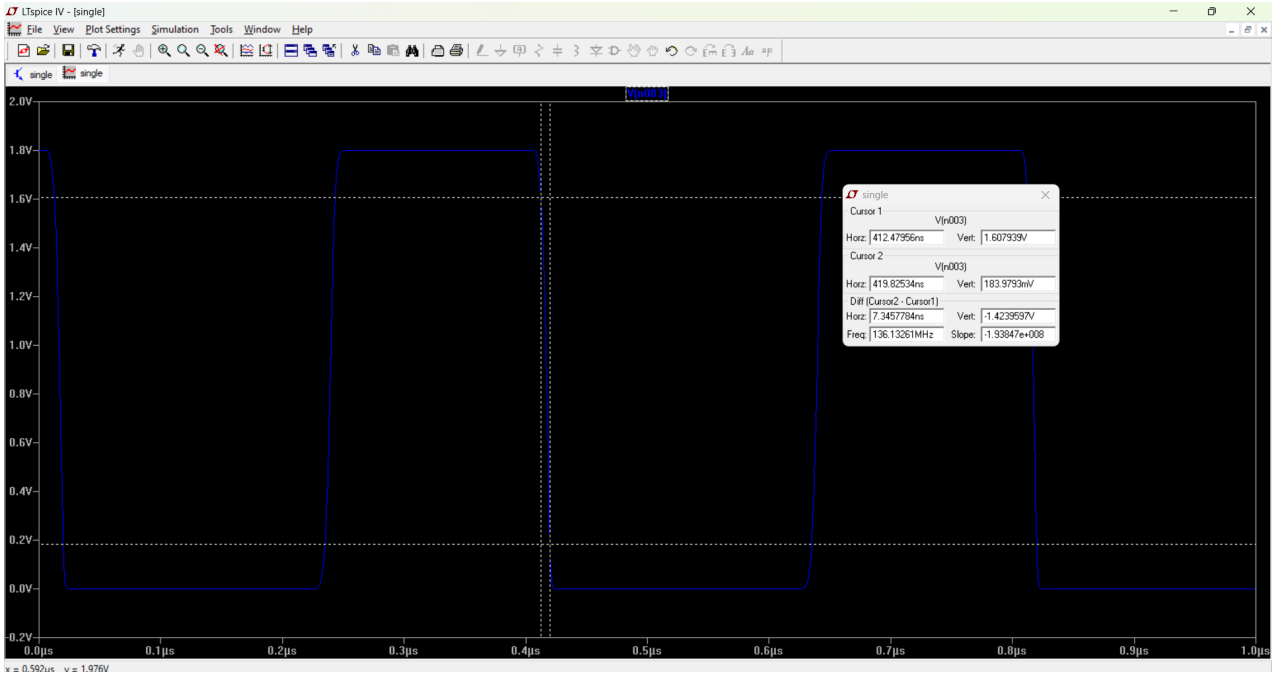
$t_{pLH} = 9.5014ns$



$t_{pHL} = 6.846ns$



$t_{rise} = 8.360ns$



$t_{fall} = 7.345ns$

4.2 CMOS Inverter Chain

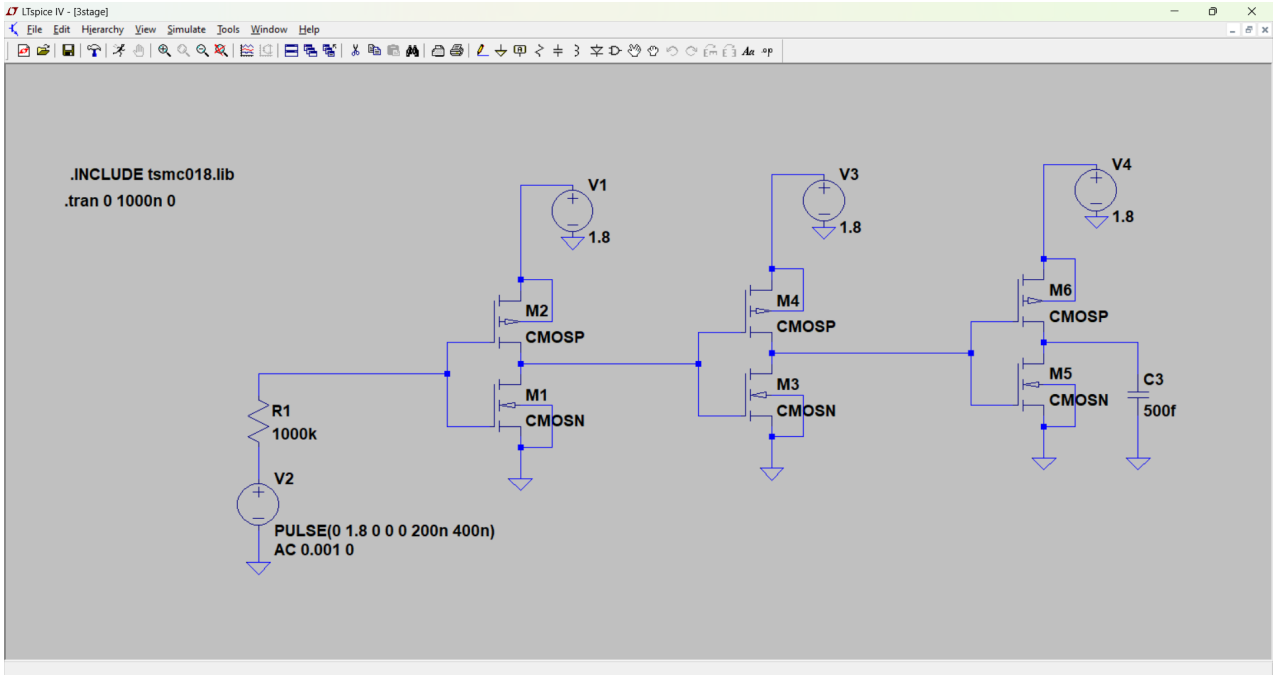
To find optimum number of stages for inverter chain, keep adding a inverter stage to a chain. Calculate the value of f using C_{out} and C_{in}. For the size the inverter stages we calculate the effective fanout is found using this formula f = $(F)^{\frac{1}{N}}$. For N = 3, f came to be 6.1749, N = 5, f is 2.9811 and for N = 7, f is 2.1819. With given f for the particular stage, use geometric progression, ie., example for a stage 3 inverter chain, the first inverter

would have the $(\frac{W}{L})_p$: $(\frac{W}{L})_n$ ratio as 2:1 but the subsequent ratio would be 2f:1 and $2f^2$: 1

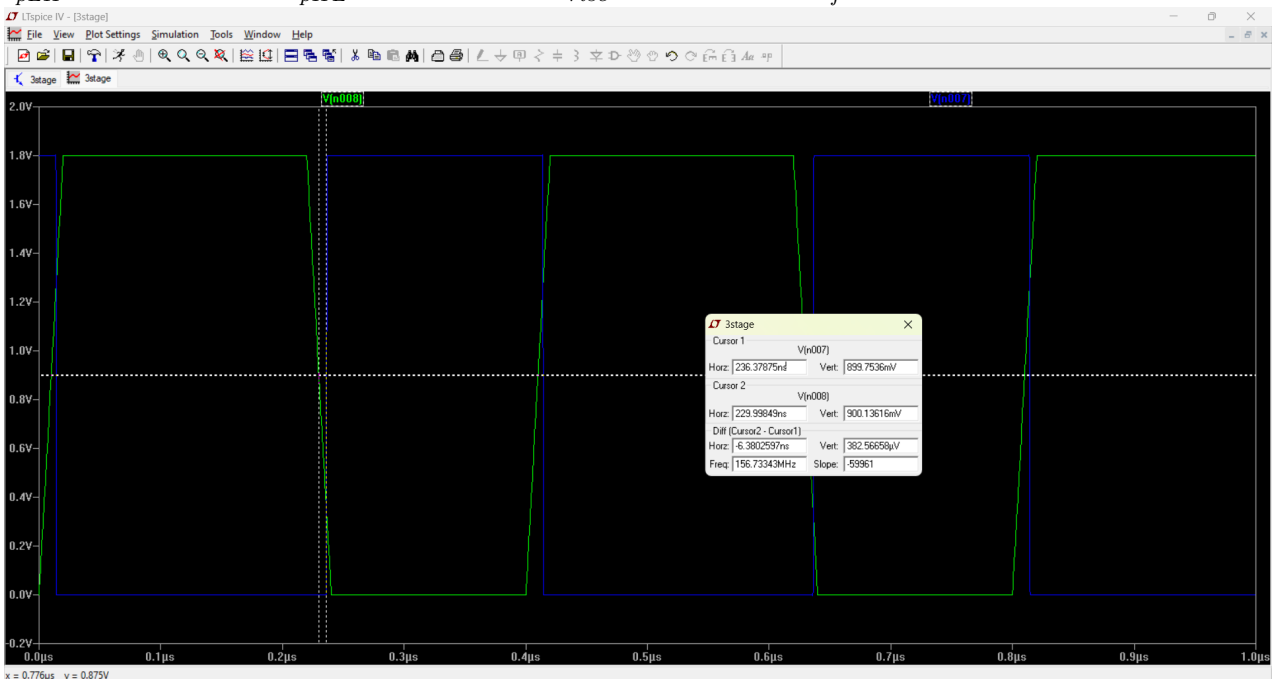
Similarly, using geometric progression, we would calculate the sizing of the inverters for stage 5 as well as stage 5.

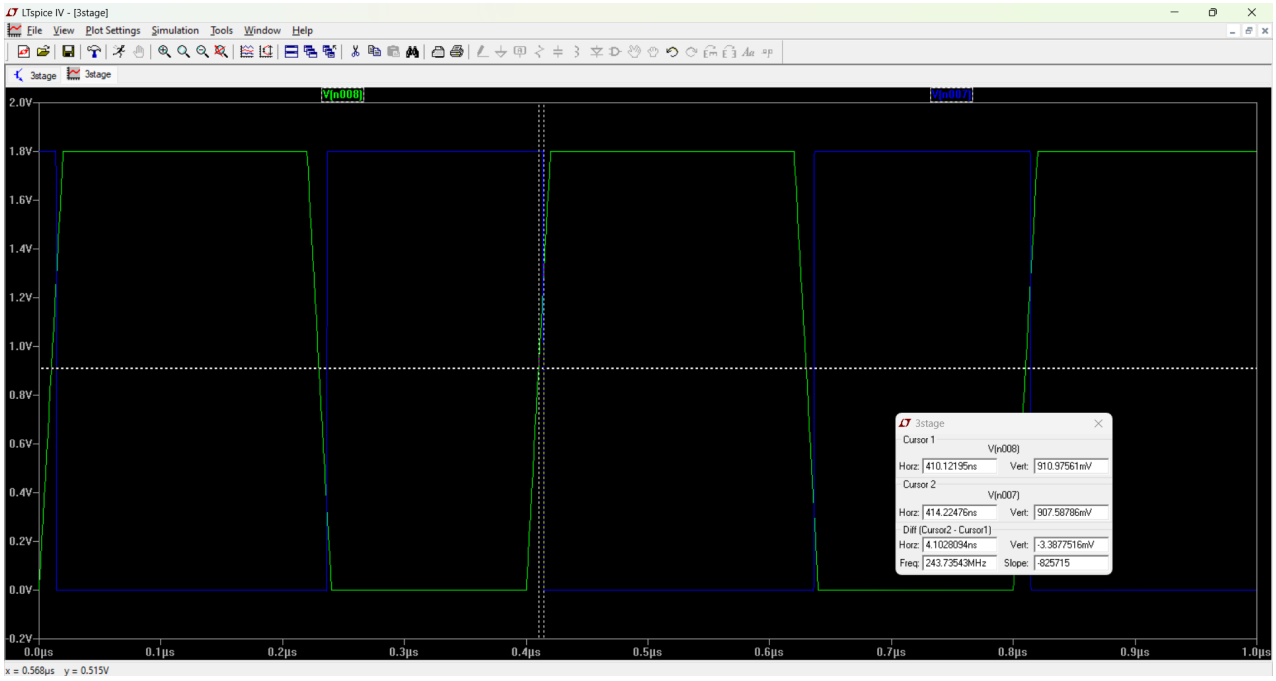
Now analyse transient characteristics and calculate t_{rise}, t_{fall}, t_{pHL} and t_{pLH} from the plot and the corresponding schematic and plots for N =3,5 and 7 are shown below.

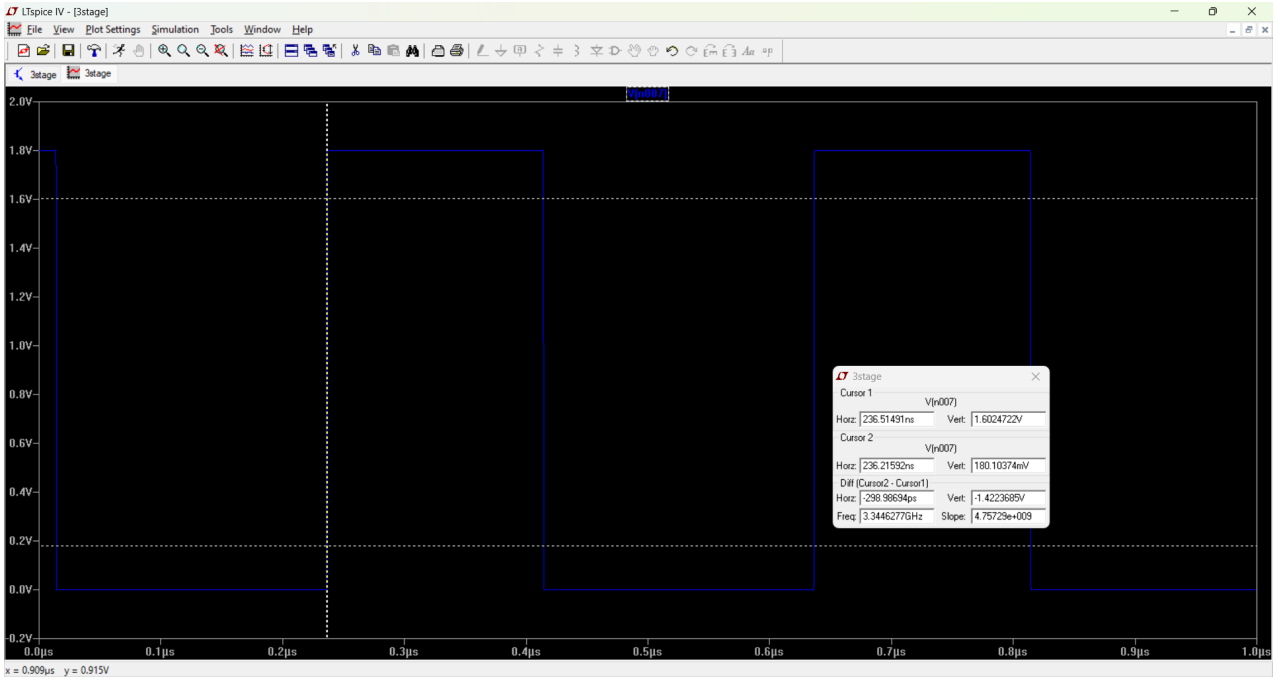
N=3

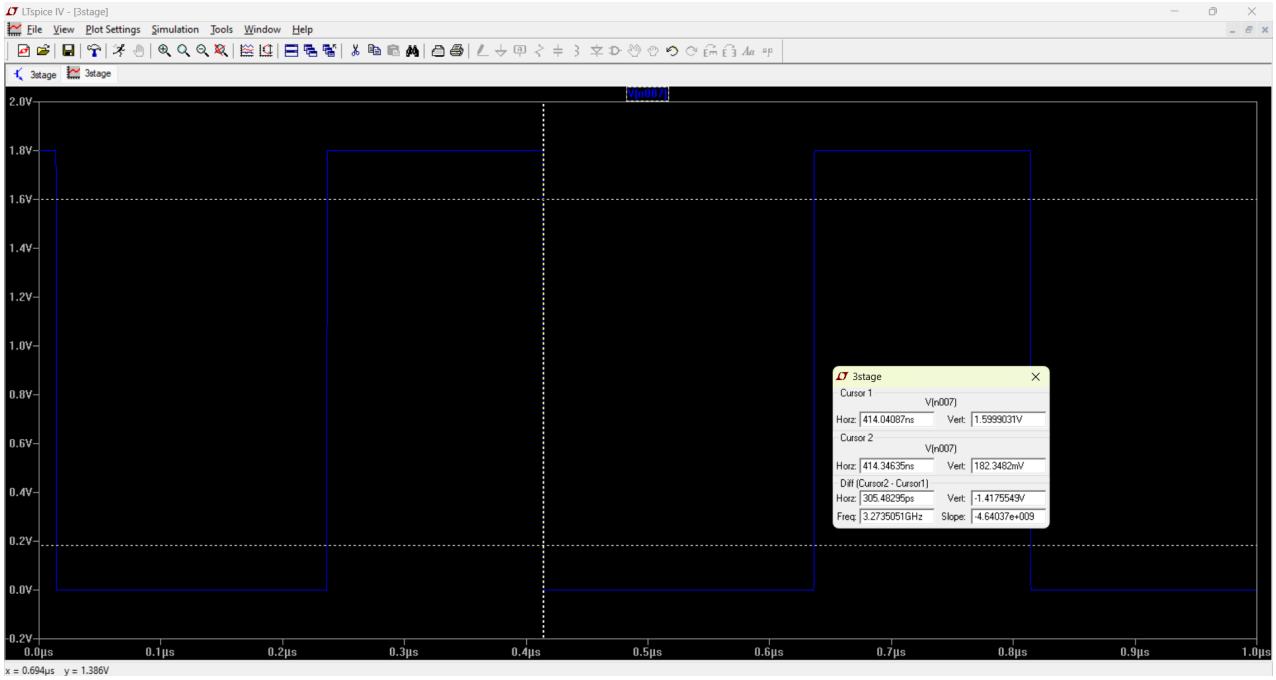


$t_{pLH} = 6.3802ns$ $t_{pHL} = 4.102ns$ $t_{rise} = 0.298ns$ $t_fall = 0.305ns$

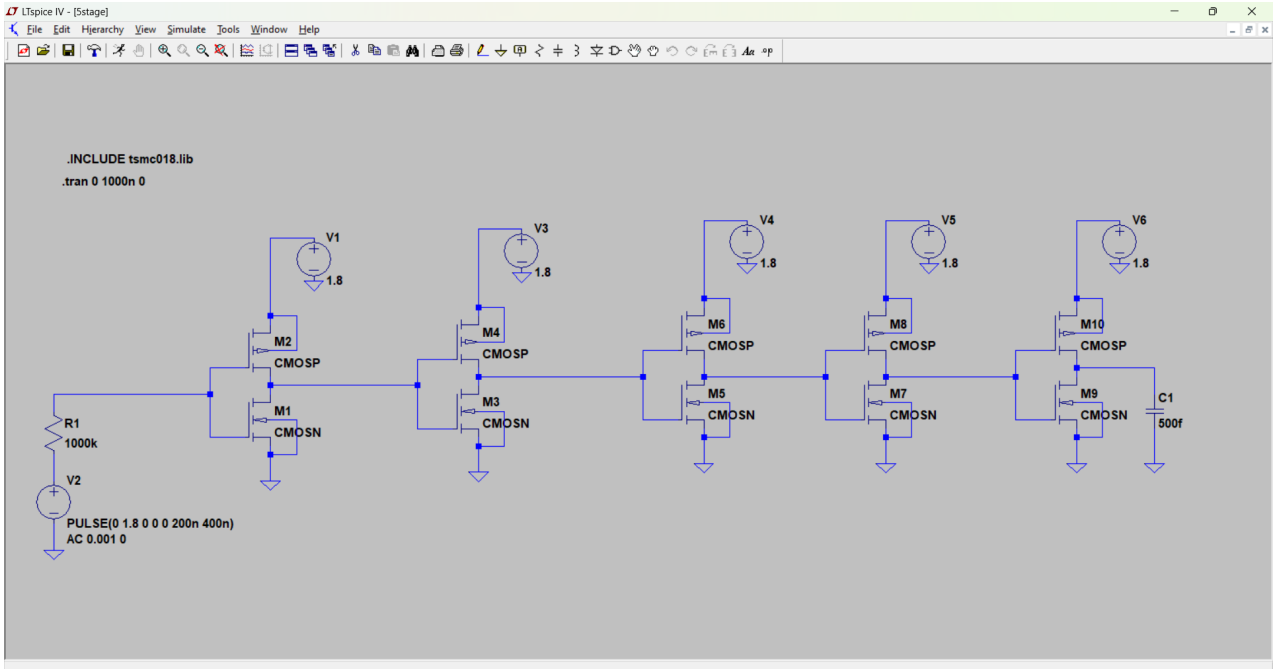



LTspice IV - [3stage]
File View Plot Settings Simulation Tools Window Help
3stage
V(n008)
V(n007)
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
0.0µs 0.1µs 0.2µs 0.3µs 0.4µs 0.5µs 0.6µs 0.7µs 0.8µs 0.9µs 1.0µs
Cursor 1
V(n008)
Horz: 410.12195ns Vert: 910.97561mV
Cursor 2
V(n007)
Horz: 414.22476ns Vert: 907.58786mV
Diff (Cursor2 - Cursor1)
Horz: 4.1028094ns Vert: -3.3877516mV
Freq: 243.73543MHz Slope: -825715
x = 0.568µs y = 0.515V

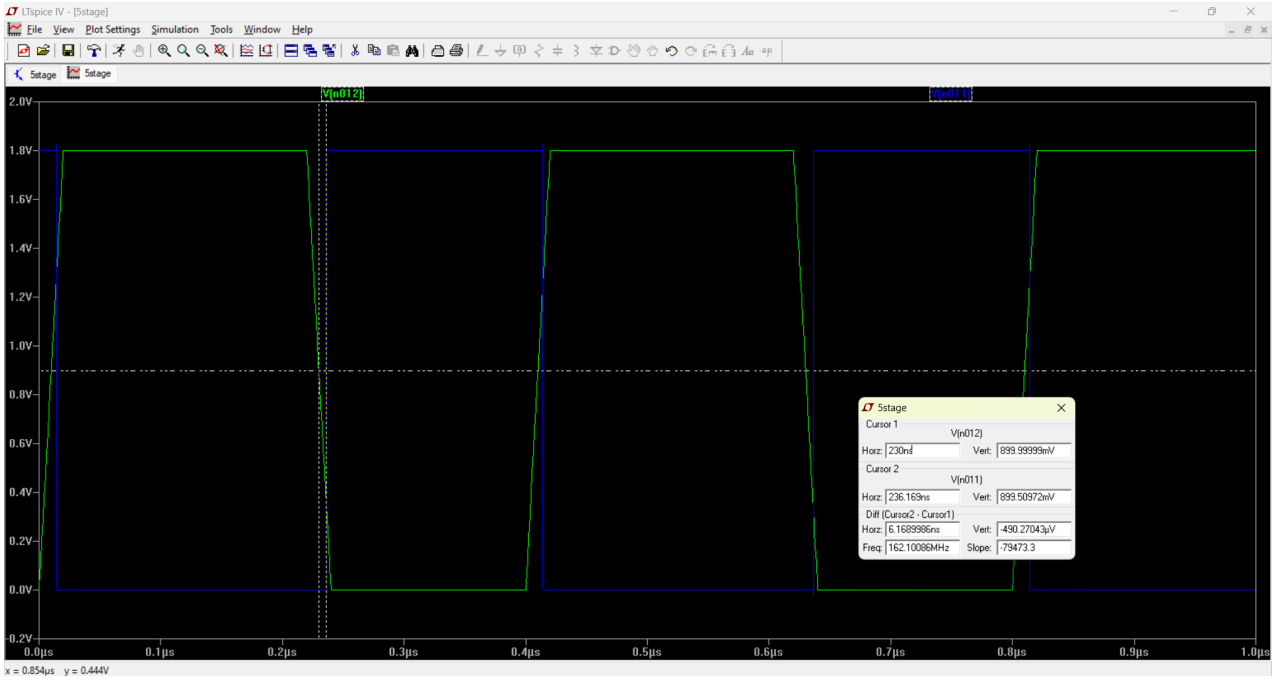

LTspice IV - [3stage]
File View Plot Settings Simulation Tools Window Help
3stage
V(n007)
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
0.0µs 0.1µs 0.2µs 0.3µs 0.4µs 0.5µs 0.6µs 0.7µs 0.8µs 0.9µs 1.0µs
Cursor 1
V(n007)
Horz: 236.51491ns Vert: 1.6024722V
Cursor 2
V(n007)
Horz: 236.21592ns Vert: 180.10374mV
Diff (Cursor2 - Cursor1)
Horz: -298.98694ps Vert: -1.4223685V
Freq: 3.3446277GHz Slope: 4.75729e+009
x = 0.909µs y = 0.915V

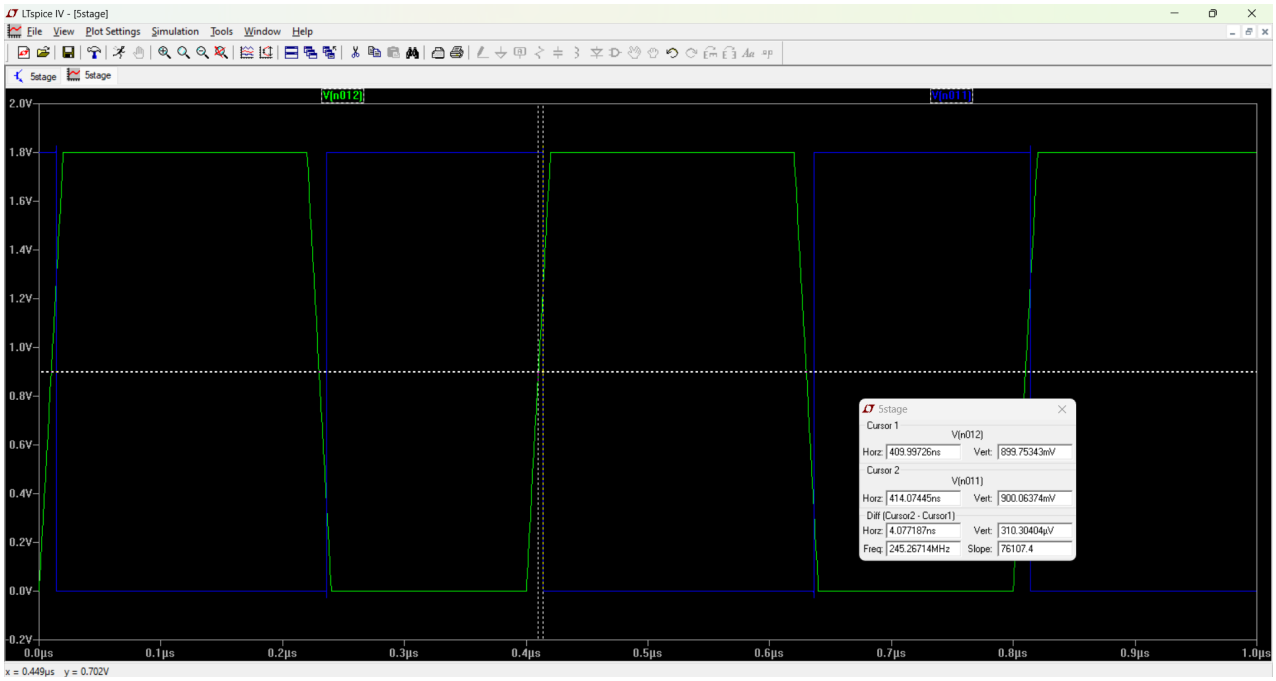


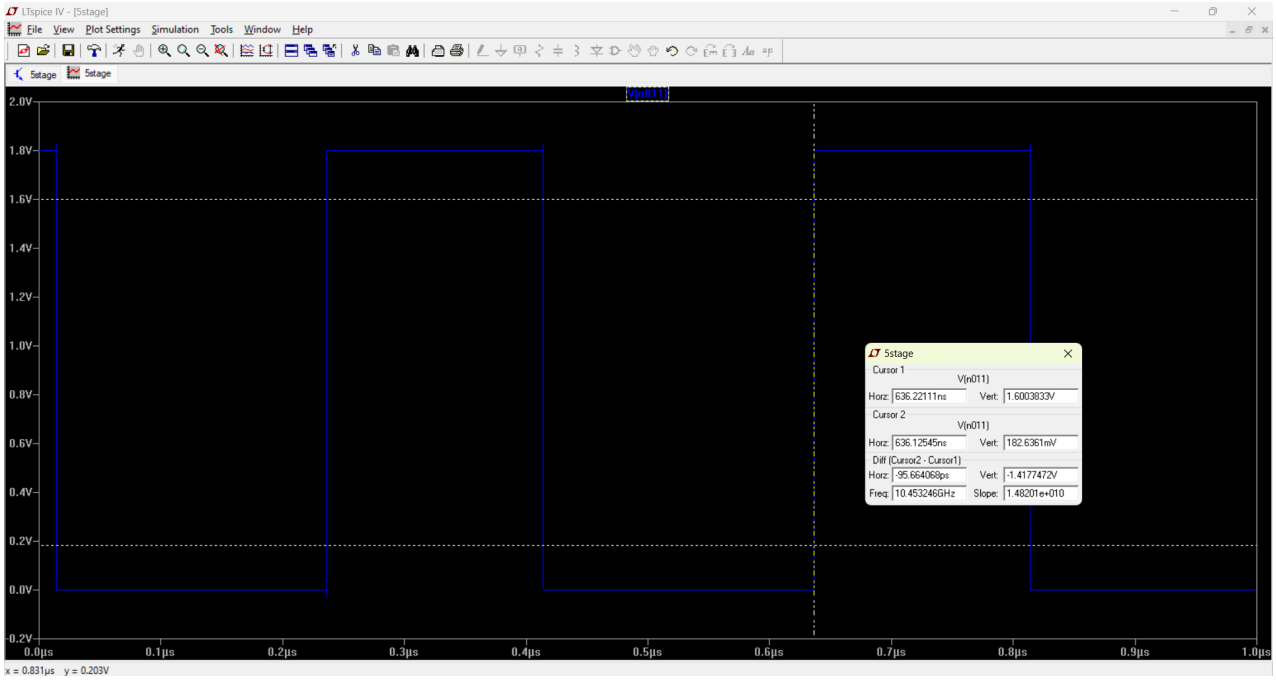
N=5

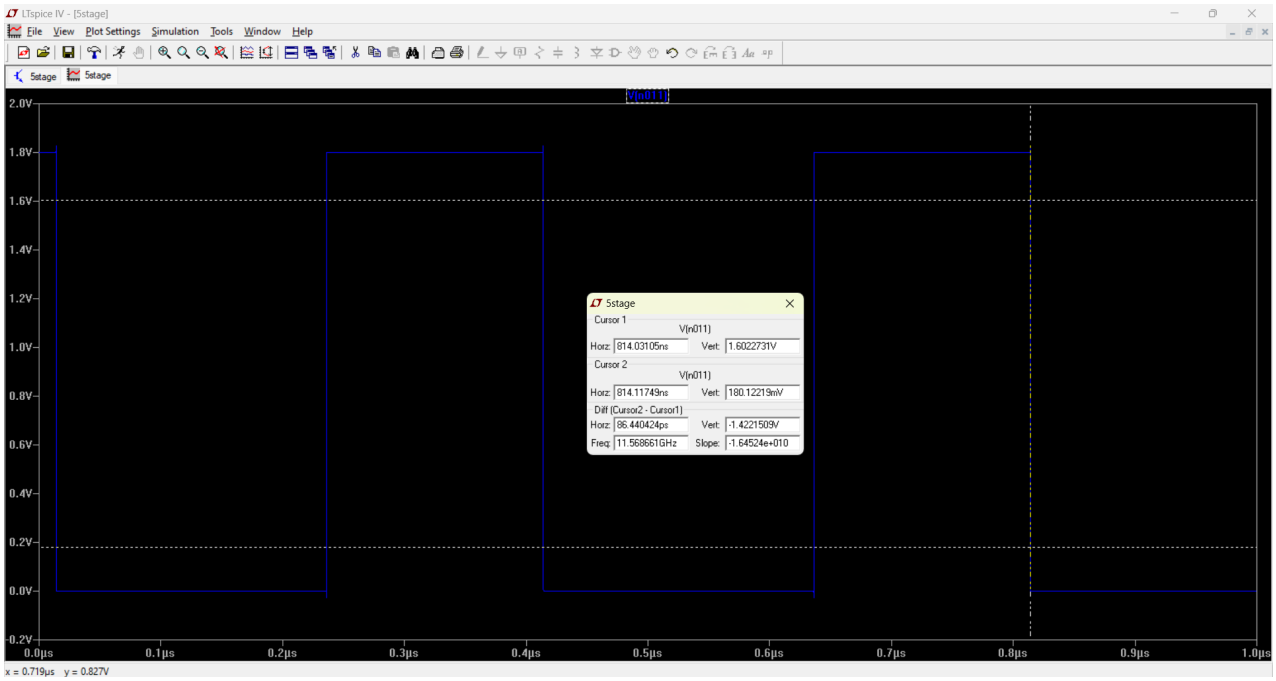


$t_{pLH} = 6.168ns$ $t_{pHL} = 4.077ns$ $t_{rise} = 0.0956ns$ $t_fall = 0.0864ns$

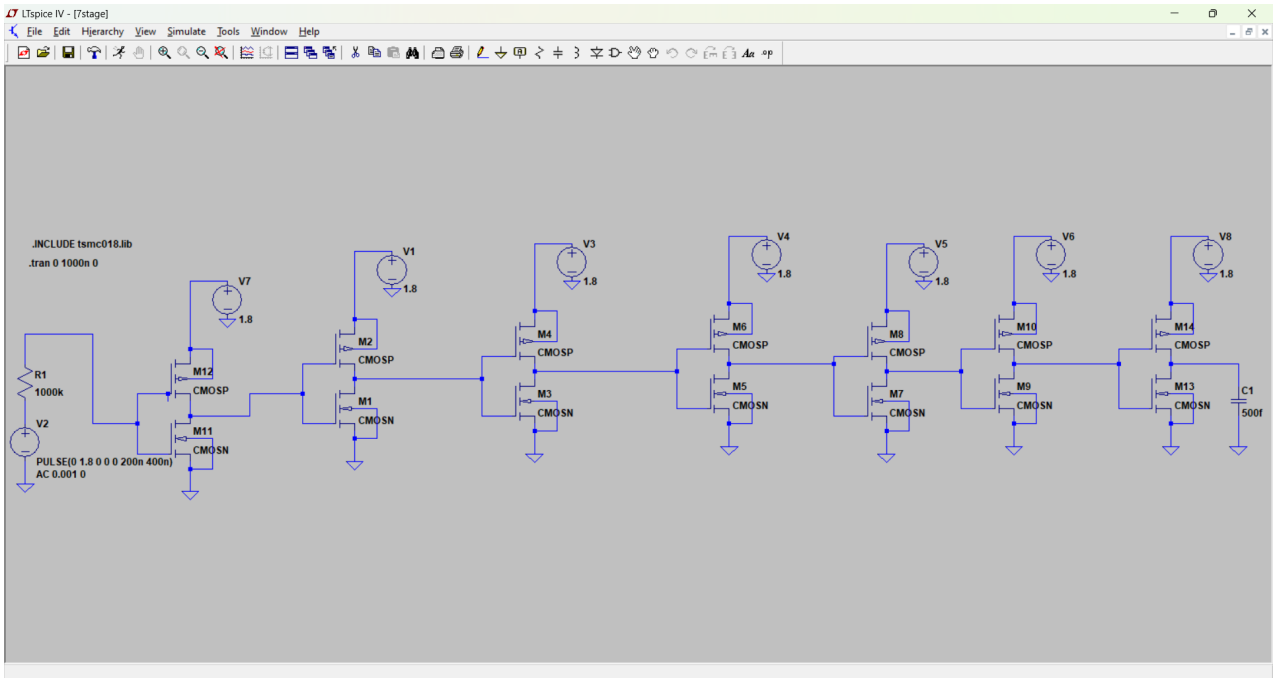

LTspice IV - [5stage]
File View Plot Settings Simulation Tools Window Help
5stage 5stage
V(n012)
V(n011)
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
0.0µs 0.1µs 0.2µs 0.3µs 0.4µs 0.5µs 0.6µs 0.7µs 0.8µs 0.9µs 1.0µs
5stage
Cursor 1
V(n012)
Horz: 230ns
Vert: 899.99999mV
Cursor 2
V(n011)
Horz: 236.169ns
Vert: 899.50972mV
Diff (Cursor2 - Cursor1)
Horz: 6.1689986ns
Vert: -490.27043µV
Freq: 162.10086MHz
Slope: -79473.3
x = 0.854µs y = 0.444V


LTspice IV - [5stage]
File View Plot Settings Simulation Tools Window Help
5stage 5stage
V(n012)
V(n011)
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
0.0µs 0.1µs 0.2µs 0.3µs 0.4µs 0.5µs 0.6µs 0.7µs 0.8µs 0.9µs 1.0µs
5stage
Cursor 1
V(n012)
Horz: 409.99726ns
Vert: 899.75343mV
Cursor 2
V(n011)
Horz: 414.07445ns
Vert: 900.06374mV
Diff (Cursor2 - Cursor1)
Horz: 4.077187ns
Vert: 310.30404µV
Freq: 245.26714MHz
Slope: 76107.4
x = 0.449µs y = 0.702V

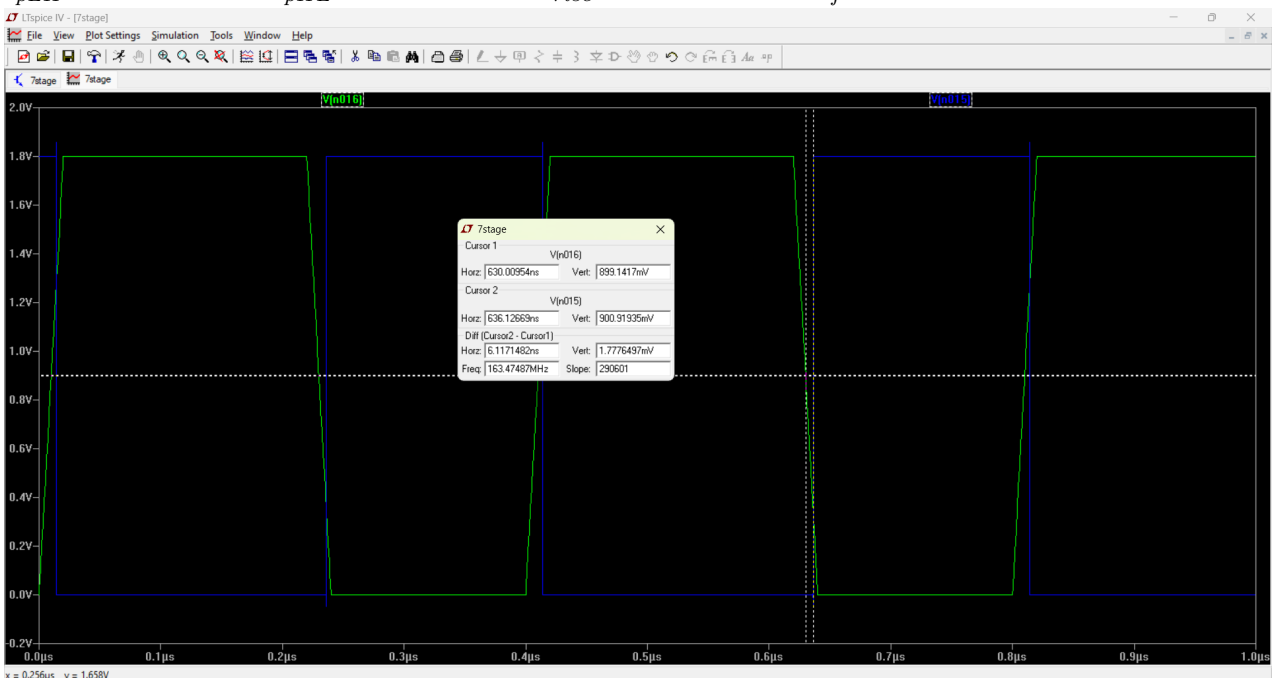

LTspice IV - [5stage]
File View Plot Settings Simulation Tools Window Help
5stage 5stage
V(n011)
2.0V 1.8V 1.6V 1.4V 1.2V 1.0V 0.8V 0.6V 0.4V 0.2V 0.0V -0.2V
0.0µs 0.1µs 0.2µs 0.3µs 0.4µs 0.5µs 0.6µs 0.7µs 0.8µs 0.9µs 1.0µs
5stage
Cursor 1
V(n011)
Horz: 636.22111ns Vert: 1.6003833V
Cursor 2
V(n011)
Horz: 636.12545ns Vert: 182.6361mV
Diff (Cursor2 - Cursor1)
Horz: -95.664068ps Vert: -1.4177472V
Freq: 10.453246GHz Slope: 1.48201e+010
x = 0.831µs y = 0.203V

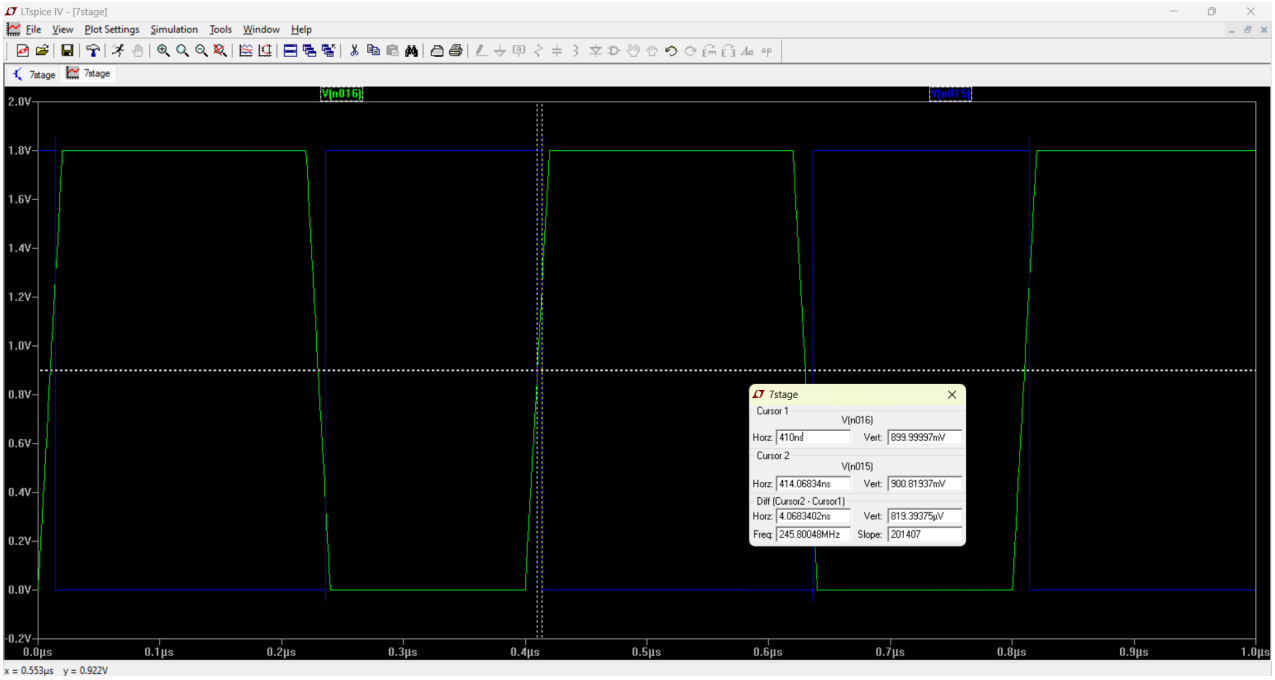

LTspice IV - [5stage]
File View Plot Settings Simulation Tools Window Help
5stage 5stage
V(n011)
2.0V 1.8V 1.6V 1.4V 1.2V 1.0V 0.8V 0.6V 0.4V 0.2V 0.0V -0.2V
0.0µs 0.1µs 0.2µs 0.3µs 0.4µs 0.5µs 0.6µs 0.7µs 0.8µs 0.9µs 1.0µs
5stage
Cursor 1
V(n011)
Horz: 814.03105ns Vert: 1.6022731V
Cursor 2
V(n011)
Horz: 814.11749ns Vert: 180.1221mV
Diff (Cursor2 - Cursor1)
Horz: 86.440424ps Vert: -1.4221509V
Freq: 11.568661GHz Slope: -1.64524e+010
x = 0.719µs y = 0.827V

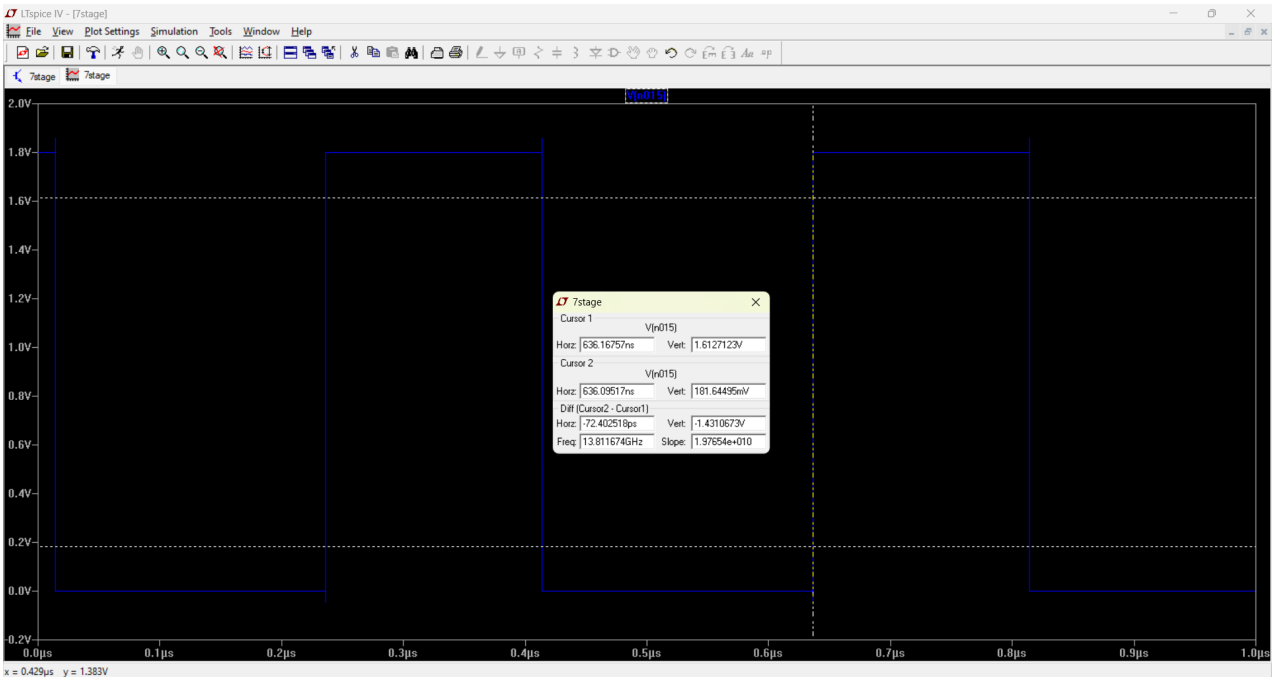
N=7

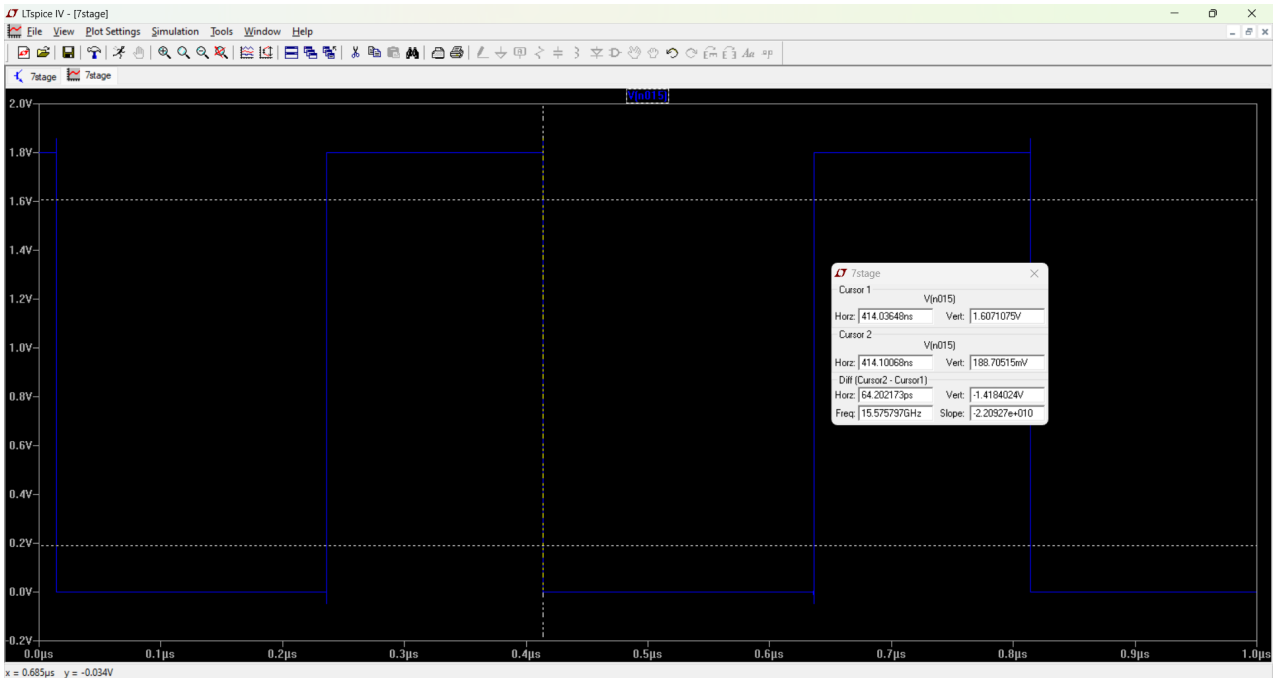


$t_{pLH} = 6.117ns$ $t_{pHL} = 4.068ns$ $t_{rise} = 0.0724ns$ $t_fall = 0.0642ns$




LTspice IV - [7stage]
File View Plot Settings Simulation Tools Window Help
7stage 7stage
V(n016)
V(n015)
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
0.0µs 0.1µs 0.2µs 0.3µs 0.4µs 0.5µs 0.6µs 0.7µs 0.8µs 0.9µs 1.0µs
7stage
Cursor 1
V(n016)
Horz: 410n
Vert: 899.99997mV
Cursor 2
V(n015)
Horz: 414.06834ns
Vert: 900.81937mV
Diff (Cursor2 - Cursor1)
Horz: 4.0683402ns
Vert: 819.39375µV
Freq: 245.80048MHz
Slope: 201407
x = 0.553µs y = 0.922V


LTspice IV - [7stage]
File View Plot Settings Simulation Tools Window Help
7stage 7stage
V(n015)
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
0.0µs 0.1µs 0.2µs 0.3µs 0.4µs 0.5µs 0.6µs 0.7µs 0.8µs 0.9µs 1.0µs
7stage
Cursor 1
V(n015)
Horz: 636.16757ns
Vert: 1.6127123V
Cursor 2
V(n015)
Horz: 636.09517ns
Vert: 181.64495mV
Diff (Cursor2 - Cursor1)
Horz: -72.402518ps
Vert: -1.4310673V
Freq: 13.811674GHz
Slope: 1.97654e+010
x = 0.429µs y = 1.383V



5 TABULATION

Calculation of input capacitance of single CMOS inverter by AC analysis.

Frequency(MHz)	Input Capacitance(fF)
74.944	2.123

Comparison of the propagation delay of single-stage inverter and inverter chain using progressive sizing.

Inverter Transient Characteristics									
Inverter Chain using progressive scaling					Single stage Inverter				
$(\frac{W}{L})_p : (\frac{W}{L})_n$	t_{pLH}	t_{pHL}	t_{rise}	t_{fall}	$(\frac{W}{L})_p : (\frac{W}{L})_n$	t_{pLH}	t_{pHL}	t_{rise}	t_{fall}
(stage 3)	6.380ns	4.103ns	298.9ps	305.4ps					
(stage 5)	6.168ns	4.077ns	95.66ps	86.44ps					
(stage 7)	6.11ns	4.068ns	72.402ps	64.202ps	2 : 1	9.501ns	6.846ns	8.360ns	7.345ns

6 OBSERVATIONS

- The input capacitance of single CMOS inverter is obtained to be 2.123fF.
- Theoretical value of N given to be

$$N = 5.46 \approx 5$$

- We observe that as we increase N, delay decreases due to reduction of effective fanout at each stage upto optimum N stages, thereafter again delay increases due to intrinsic capacitance. Here from the experiment, we can see that the delay doesn't increase but doesn't decrease extremely. As there is no much difference in the delay 5th stage to 7th stage, we take 5th stage to be the optimum number.
- From experiment the optimum N=5 has $t_p = 5.123ns$, $t_{rise} = 95.66ps$, $t_{fall} = 86.44ps$.
- Theoretical and experimental values of N are matched.