FPGA-Based Electronics Voting Machine

Proposal By - Deepak Sharda

Overview:

The conventional Electronic Voting Machine (EVM), comprising a control unit and balloting unit has been in use for nearly a decade and is deemed complex. This proposal proposes an innovative approach by implementing the Electronic Voting Machine using Field-Programmable Gate Array (FPGA) technology. The FPGA-based method, an application of Very Large Scale Integration (VLSI), aims to overcome the complexities of traditional EVMs, offering increased safety and ease of use. This technological advancement, aligned with the future scope of VLSI in real-time applications, has the potential to revolutionize the electoral process. The FPGA-based Voting Machine prioritizes security and user-friendliness, particularly addressing challenges in rural areas like booth capturing. The research signifies a commitment to advancing electoral technology for a more efficient and secure voting experience.

---

1. Objective:

Designing an FPGA-Based Electronic Voting Machine.

2. Introduction:

The Electronic Voting Machine (EVM) has been a fixture in global elections for an extended period, offering efficiency in the voting process. Despite its widespread use, concerns persist about the lack of security, with instances of booth-capturing compromising the fairness of results. This becomes particularly significant when ruling parties employ questionable tactics to influence outcomes, potentially undermining the democratic process and the global perception of a country.

In response to these challenges, I propose an alternative approach to ensure a fair and secure global voting system. While the existing EVM method has proven efficient, it needs to provide the necessary safeguards. From a global perspective, where billions of people are eligible to vote, a secure, portable, and compact voting machine becomes essential for maintaining the integrity of elections worldwide.

This proposal proposes the design of an Electronic Voting Machine using a digital technique that prioritizes security, safety, and error-free operation. The design's core centers around utilizing a Field Programmable Gate Array (FPGA), rooted in the principles of Very Large Scale Integration (VLSI).

The proposed Electronic Voting Machine, developed in Verilog using open-source Icarus Verilog, aims to address the challenges associated with traditional voting

methods on a global scale. Recognizing the difficulty in managing the entire voting process with traditional ballot papers, the paper underscores the need for an advanced and secure solution to uphold the integrity of the global electoral system.

Hence I am proposing an Electronic Voting Machine using Verilog HDL with Lattice Semiconder FPGA.

3. Features:

Security and Tamper-Resistance:

- Develop an intricate security infrastructure utilizing FPGA capabilities to safeguard against unauthorized access and tampering.
- Implement advanced encryption algorithms, such as AES, to secure voter data both in transit and at rest.
- Integrate tamper detection mechanisms, including physical sensors, to promptly identify and report any attempts to compromise the system.

User-Friendly Interface:

- Design a highly intuitive and accessible user interface catering to voters with diverse technological literacy levels.
- Ensure seamless interaction through the incorporation of user-friendly input devices like touchscreens or other intuitive methods.

Confidentiality, Integrity, and Accuracy:

- Establish robust measures to maintain the confidentiality of votes, ensuring that each voter's choice remains private.
- Implement integrity checks in the system to detect and rectify any data corruption or manipulation during the voting process.

Scalable and Real-Time Processing:

- Leverage FPGA's parallel processing capabilities to create a scalable system capable of accommodating a large number of voters simultaneously.
- Optimize FPGA code for real-time processing, ensuring minimal latency and quick response times during the voting process.
- Conduct stress testing to evaluate the system's performance under high loads and identify potential bottlenecks.

4. Design & Implementation:

The Electronic Voting Machine (EVM) is implemented on the FPGA board, featuring a design that accommodates votes for four different candidates. The initial setup includes four switches on the FPGA board, each representing votes for individual candidates. A reset button is incorporated to reset the entire system, ensuring a clean slate for each voting session. Additionally, a mode button enhances the safety of the Voting Machine.

The mode button plays a crucial role in the functioning of the system. When set to 0, voters can cast their votes for specific candidates. However, switching the mode button from 0 to 1 transforms the Voting Machine into a vote-counting mode, disabling the casting of votes. This innovative concept introduces the idea of a "Valid Vote." A Valid Vote is registered when a switch is pressed for a duration of 1 second. Upon casting a valid vote, the LEDs on the FPGA illuminate, providing a visual confirmation of a successfully cast fair vote.

If a switch is pressed for less than 1 second, it is not counted as a valid vote.

The implementation will be Carried out on a Pico-ice FPGA board, connected with external: 4 user switches and 4user LEDs for customizable inputs.

This comprehensive setup ensures a secure, feature-rich, and flexible Electronic Voting Machine, utilizing the advanced capabilities of the pico-ice FPGA board.

5. Schematic:

Fig 1. depicts the schematic of the proposed electronic voting machine with input and output signals.

The schematic diagram consists of clk, party1, party2, party3, reset and select_party as input and count1_op, count2_op, and count3_op of 6 bits each as output signals.count1, count 2 and count 3 are the intermediate signals and the six states that are used are initial, check, party1_state, party2_state, party3_state and done.

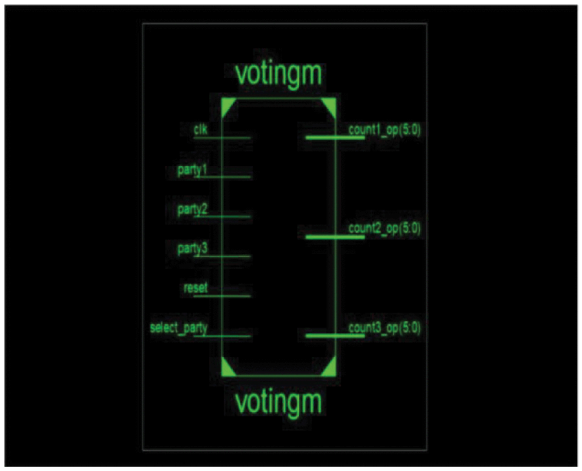

Fig 1. Schematic Diagram Of EVM

6. State Diagram -

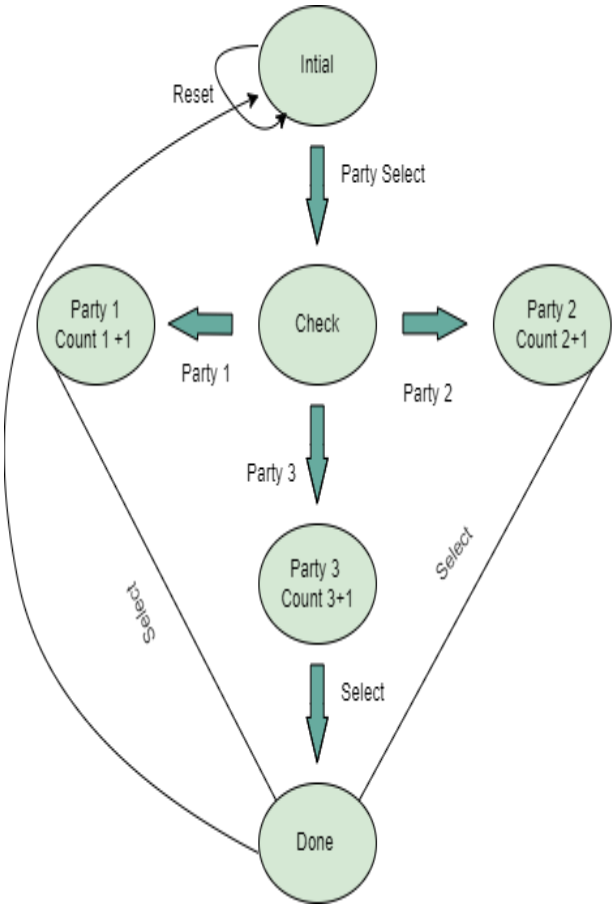

Fig2. State Diagram of EVM

7. Tech Stack:

1. Verilog -2005
2. Lattice Diamond Development Tools
3. APIO Project
4. Project-IceStrom
5. Icarus Verilog

8. Timeline:

Phase	Timeline	Time Frame
System Design	Week 1	Jan 2024
Verilog Programming	Week 2 & 3	Feb 2024
Implementation	Week 4	Feb 2024
Testing	Week 4 & 5	Feb 2024
Final Report	Week 6	Mark 2024

9. Proposed- Budget:

Particulars	Qua.	Price	Vendor
Pico -ice	1	$ 35	Tindi
Custom PCB	1	$ 22	JLC PCB
Programming - Cable	1	$3	Amazon
Encloser	1	$6	Amazon
Power Adapter	1	$4	Amazon
Total		$70	

10. Deliverable:

A fully functional Electronic Voting Machine prototype implemented on the Pico-ICe FPGA board.
Four switches correspond to individual candidates, enabling voters to cast valid votes. Reset button for system initialization and a mode button to toggle between voting and vote-counting modes.
LED indicators to visually confirm the casting of a valid vote.

11. Conclusion:

The Electronic Voting Machine should be successfully implemented on the Pico-Ice FPGA, incorporating various concepts from Very Large Scale Integration (VLSI). Through meticulous implementation and testing, the prototype has demonstrated its capability to meet the specified requirements. Utilizing the Pico-Ice FPGA board in conjunction with Verilog will prove effective in achieving the desired functionality.

With the successful implementation and testing, the FPGA-based Voting Machine will be poised for deployment in actual Elections.
The Pico-Ice FPGA, with its advanced features, will prove instrumental in realizing a Voting Machine that meets the stringent requirements of real-world elections. This FPGA-based solution is poised to contribute to the efficiency, security, and transparency of the electoral process in Elections.

12. References:

[1] Hossain, Tabia, et al. "Proficient FPGA Execution of Secured and Apparent Electronic Voting Machine Using Verilog HDL." International Journal of Envirnment41 (2014): 18-24.

[2] Yang, Chung-Huang, Shih-Yi Tu, and Pei-Hua Yen. "Implementation of an electronic voting system with contactless IC cards for smallscale voting." 2009 Fifth International Conference on Information Assurance and Security. Vol. 2. IEEE, 2009.

[3] Soomro, Z. A., Memon, T. D., Naz, F., & Ali, A. (2020, January). FPGA-Based Real-Time Face Authorization System for Electronic Voting System. In 2020 3rd International Conference on Computing, Mathematics and Engineering Technologies (iCoMET) (pp. 1-6). IEEE

[4] P. Kudesia, Manika, A. Kulshrestha and A. Kumar, "Nano Ballot Box: A Low Power, Thermal Resistant FPGA Based Electronic Voting Machine," 2021 International Conference on Simulation, Automation & Smart Manufacturing (SASM), Mathura, India, 2021, pp. 1-6, doi: 10.1109/SASM51857.2021.9841124.