

A
BACHELOR'S DEGREE IN TELECOMMUNICATION ENGINEERING
ACADEMIC COURSE 2021/2022

Tree Inspection Kit handheld device

B
Part of the Bachelor's Thesis:

**"Development of an acoustic measurement system of
the Modulus of Elasticity in trees, logs and boards"**

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UNIVERSIDAD
DE GRANADA



LIFE WOOD
FOR FUTURE

Project title: TIK_HandheldDevice.PjPcb

Date: 2022-07-29	Revision: 0.6
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Sheet 1 of 20

Introduction

Objective

The present project has the goal of developing a handheld electronic device capable of measuring the MOE (Modulus Of Elasticity) of standing trees and logs from silviculture, so their wood can be classified for structural purpose.

The MOE (Modulus Of Elasticity) is the resistance of an object or substance to being elastically deformed when a stress is applied to it.

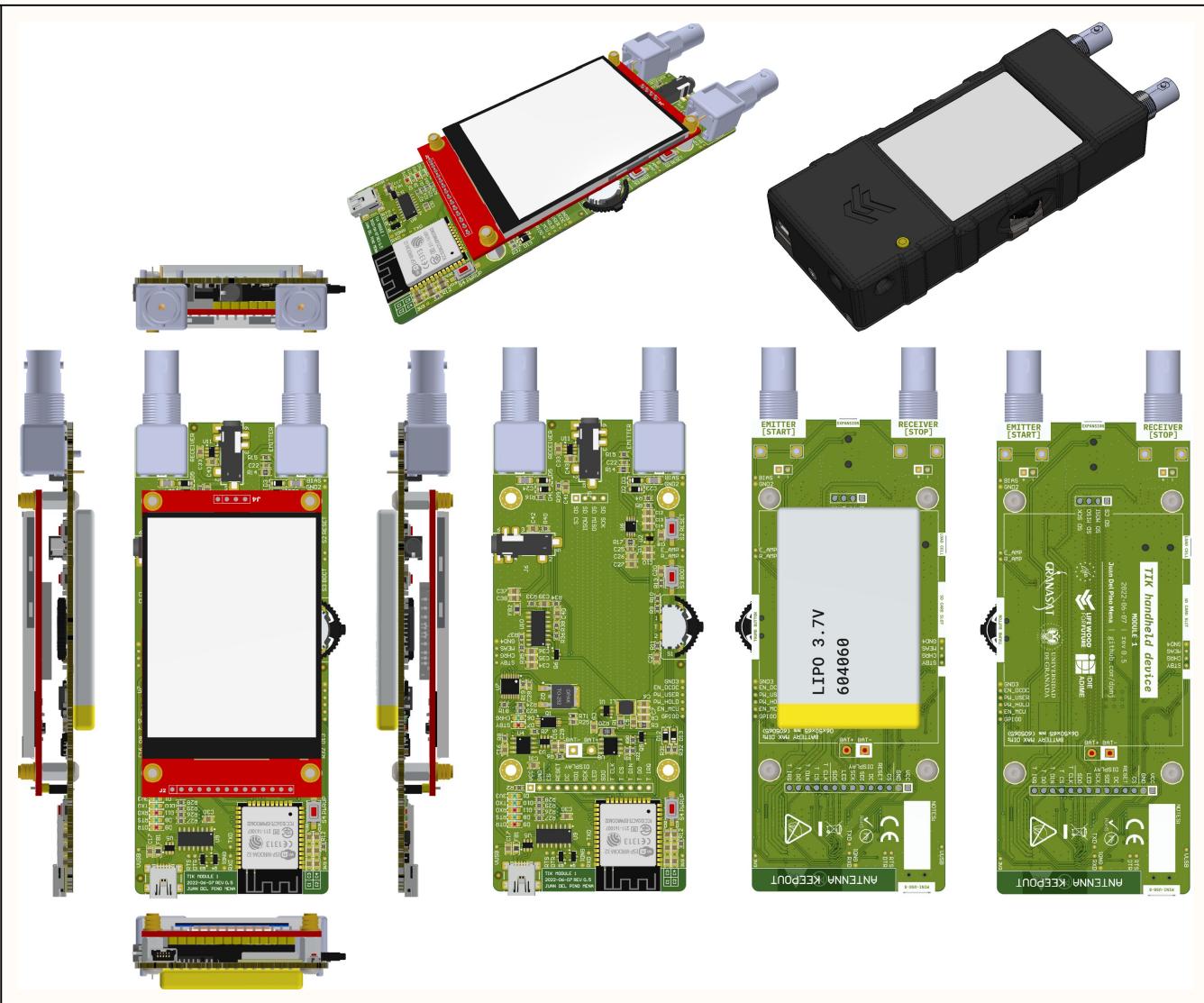
The device is equipped with the electronics needed to measure the delay between two signals which come from two piezoelectric sensors nailed into a piece of wood. It can be a standing tree, a tree trunk or a wooden board. The transit time of a wave travelling through the longitudinal axis of the wood is inversely related to the MOE and thus to the material rigidity. This device can also weight trunks to estimate its density by using a load cell.

At the right side you can see some renders of the PCB (version 0.5) which has been manufactured.

Motivation

Collaborators

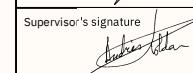
This work has been possible thanks to the GranaSat team. Huge thanks to all the IDIE-ADIME research team and to the LIFE Wood For Future programme for offering the project, for its organization, support and financing.



Tree Inspection Kit handheld device

A device capable of determining the microsecond delay between 2 signals coming from piezoelectric probes nailed into a tree, trunk or wood board. This allows the indirect calculus of the Modulus of Elasticity in a non-destructive way.

Designer's signature

Supervisor's signature


Sheet title: **Introduction and PCB renders**

Project title: **TIK_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

Date: **2022-07-29** Revision: **0.6**

Sheet 2 of 20

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Changelog

Revision 0.6 | 2022-07-29

NEW

- Completed documentation (final version)
- Added a DCDC converter substitute IC.
- Updated block diagram.

FIXED

- Changed 3D models to fit the real board.
- Added circuits' correction notes for future development.

Revision 0.5 | 2022-06-07 [MANUFACTURED VER.]

NEW

- Added multilayer connector to the battery
- Added a power budget & battery selection
- Adjusted the charging current resistor value of the TP4056.
- Added a expansion port and load cell connectors footprints. (4-pole jacks).
- Added support for jack plug switches.
- Applied JLCPCB design rules via .rul file.
- All vias are tented to avoid corrosion.
- Added detailed explanation of trace design with Saturn PCB toolkit.
- Applied a nice format to the BOM.
- Added an introduction, updated renders.
- Added mechanical drawings with 3D isometric views, part drawing views, measurements, layer stackup, drills, etc.
- Added Gerber and NC Drills fabrication jobs for ordering PCB and its stencil.

FIXED

- Corrected LEDs' series resistors values
- Relocated the battery below the PCB. This makes the product wider, but solves a lot of space constraints.
- Removed VBIAS plane to avoid splitting planes, for EMI considerations.
- A lot of cosmetic improvements and corrections on PCB top & bottom overlays.
- Replaced logos and added new ones.
- Improved routing.
- A few cosmetic changes on the schematic sheets and cover.
- Removed rooms.
- NTC connector changed, now it's meant for soldering the NTC cable from a battery.

Revision 0.4 | 2022-05-22

NEW

- Added parameters for fabrication groups and fabrication order
- Added a Bill of Materials. The one in this document is simple. Refer to the manually configured BOM of this project.
- Added a PCB track legend and description for visible layers.
- Given more info about ESP32 pins.
- Added a precise block diagram.
- Added support for an extension port.
- Added a HX711-based load cell acquisition system.

FIXED

- Corrected I2C pins on the ESP32.
- Removed "same length" directive on UART and I2C nets.
- Improved routing.
- Removed via shielding on I2C traces.
- Solved all DRC warnings and errors.
- Avoided disrupting the ESP32's strapping pins default configuration during boot.
- Corrected a pin assignment error between the schematic symbol and the footprint of the MDJ210 PNP BJT transistor.
- Removed PCB cutouts.

Revision 0.3 | 2022-04-28

NEW

- Changed rotary encoder vertical for horizontal, side-placed, SMD type multipurpose 'thumb button'.
- Added a explanation of PCB trace widths.
- Adopted JLCPCB design rules.
- Full PCB component placement and routing, with no important DRC messages.
- Added silkscreen logos to the back of the PCB, as well as port markings, information and regulatory graphics: CE, WEEE, ESD sensitive warning and RoHS.

FIXED

- Changed numerical test point designators to net/rail names, to be quickly identified.
- Changed LEDs footprints.
- Corrected a faulty connection on the DW01A Lithium battery protection IC.
- The MCU has no longer the possibility to stop battery charging. This is because the ENABLE signals required by the chargers work on 5V and this could cause damage to the ESP32.

Revision 0.2 | 2022-04-23 [FIRST PCB]

NEW

- Schematic hierarchy and block diagram.
- Initial PCB layout
- Added a vertical rotary encoder. PCBLib contains a 90-degree alternative.
- Added an alternative Ni-MH charger.
- Added footprints for all neccessary components to the PCB Library.
- Added explanatory footprints and photos to schematic ICs.
- Added board mounting holes (making use of the TFT LCD module mounting hole positions)
- Added test points
- Added fiducials
- Added a power-up button
- Added net classes and parameter sets to most important nets: power, digital communications, analog signals, etc.

FIXED

- Removed errors in the lithium charger
- Removed errors in the adequation circuit
- Changed ESD USB Protection IC.
- Changed some adequation circuit values and made topology more clear.
- Revised all passive components values and sizes to match existing component disponibility.
- Corrected various pin definitions from the ESP32-WROOM-32D symbol

REVISION 0.1 | 2022-04-01 [FIRST VERSION]

NEW

- TFT LCD / SD card connections.
- First adequation circuit iteration
- LiPo battery charger with TP4056
- Auto programming circuit.

FIXED

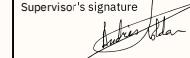
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Revision history and document index

Detailed changelog and complete document sheets index.

All along the schematic pages, a sheet title and description will be written on this corner.

Designer's signature

Supervisor's signature


Sheet title: **Changelog and document index**

Project title: **TIK_HandheldDevice.PxjPcb**

Designer: **Juan Del Pino Mena**

Date: **2022-07-29** Revision: **0.6**

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SPI traces (@ 80 MHz, digital)

Er Effective
Conductor Width (W)
0,254 mm
Conductor Height (H)
1,50 mm
Frequency (MHz)
80

10-mil "default" trace width

Note:
This calculator uses a complex formula presented by E. Hammarstad and O. Jensen, not the simplified formula presented by the IEC-2141A.

Wavelength Calculator
Input Method
 Frequency
Frequency
80 MHz
Er Eff
2,8905

Wavelength Information
 Er Effective Information
Speed of Light

CrossTalk Calculator
Signal Rise Time
5 ns
Signal Voltage
3,3 V
Coupled Length
80 mm
Conductor Spacing (S)
0,254 mm
Conductor Height (H)
1,5 mm

5 ns as a possible rise time of the SPI signal

$\lambda = \frac{C}{f * \sqrt{(ErEff)}}$

Wavelength Divide
1/20 Wave Length
11.02083 cm

Er Effective Information

Er Eff Calculator

Send to Wavelength Calculator

Note: Enter an Er Eff of 1 for wavelength in air.

△ SPI traces should not be longer than this result to avoid a transmission line. Note that this is rather a pessimistic value, as we are dividing the real wavelength by 20. Er Eff has been estimated with the expected fabrication characteristics.

△ As you can clearly see, a 2-layer, 1-6 mm height PCB is not great for signal integrity. We have great crosstalk between SPI lines. A common solution is to include GND copper between SPI lines with good connection to ground. This can be achieved by via shielding.

0.254 mm (10 mil) traces

Via Characteristics
Via Hole Diameter
0,3 mm
Internal Pad Diameter
0,6 mm
Ref Plane Opening Diam
1,016 mm
Via Height
1,6 mm
Via Plating Thickness
0,035 mm

Ref Plane Opening
Via Pad
Via Plating
Ref Plane

IPC-2152 with modifiers mode

Via Capacitance
0,5893 pF
Via DC Resistance
0,00086 Ohms
Power Dissipation
0,00326 Watts
Via Inductance
1,2993 nH
Resonant Frequency
5751.849 MHz
Conductor Cross Section
0,0368 Sq.mm
Via Impedance
46.956 Ohms
Step Response
30.4373 ps
Via Current
1.9514 Amps

Conductor Characteristics
Solve For
 Amperage
 Help
 No
 Conductor Width
Conductor Width
0,254 mm
Conductor Length
10 mm
Parallel Conductors?
 Yes
 No

Options
Solve For Copper Weight
 Imperial
 Metric
Substrate Options
Material Selection
FR-4 STD
Parallel Conductors?
 Yes
 No

Frequency
 DC
80 MHz
Distance to Plane
1,5 mm

Plating Thickness
4,6 µm
Temp Rise (°C)
10
Temp in (°F) = 18.0
Ambient Temp (°C)
130
Temp in (°F) = 77.0
Plane Thickness
0,5oz / 1oz
2oz
Skin Depth
7,39772 um
Power Dissipation
0,03469 Watts
Conductor DC Resistance
0,01529 Ohms

Skin Depth Percentage
21.08 %
Power Dissipation in dBm
15.4023 dBm
Conductor Cross Section
0,0129 Sq.mm

Voltage Drop
0,0230 Volts
Conductor Current
1.5064 Amps

Information
Total Copper Thickness
70 um
Via Thermal Resistance
N/A

Print
Solve!

IPC-2152 with modifiers mode
Etch Factor: 1:1

△ Trace AC/DC characteristics in one centimetre of trace for a given frequency/DC and for a trace temperature increase of 10 °C over a standard ambient temperature of 25°C in a FR-4 dielectric.

0.254 mm (10 mil) is the default trace width. It's thin so we can save space, but has the worst DC characteristics and should not be used for power. These are the kind of traces used by the SPI bus. The skin depth is not optimal but this will depend on frequency and again, AC current is not a critical aspect here. It's a "good enough" approach.

Sensor analog signals (1 MHz max BW)

Wavelength Calculator
Input Method
 Frequency
Frequency
1 MHz
Er Eff
3,0260

Wavelength Information
 Er Effective Information
Speed of Light

Conductor Impedance
Conductor Width (W)
0,8 mm
Conductor Height (H)
1,5 mm
Conductor Gap (G)
0,254 mm
Conductor Height (H)
1,5 mm

Formula Restrictions:
 $0.1 < W/H < 2.0$
 $T = 13um$

Wavelength Divide
1/20 Wave Length
60.6257 Ohms

CrossTalk Calculator
Signal Rise Time
2000 ns
Signal Voltage
3,3 V
Coupled Length
150 mm
Conductor Spacing (S)
0,254 mm
Conductor Height (H)
1,5 mm

Estimated signal rise time. See simulations

$\lambda = \frac{C}{f * \sqrt{(ErEff)}}$

Wavelength Divide
1/20 Wave Length
861.70030 cm

Z₀
60.6257 Ohms

CrossTalk Coefficient
-0,19079 dB
Coupled Voltage
0,03228 Volts

△ Er_Eff calculated with a 0.8 mm wide trace. Trace length will not be a problem.

△ We cannot totally match the 50-Ohm impedance of the cable but are fairly close. Besides, this is not by any means critical in a low-speed design such as these, and there's no impedance control on the end of the lines

△ Crosstalk and EMI can be a problem given the needed precision. Place these far from high-speed, with via shielding, as well as a good GND/power planes below.

Via characteristics

Via Characteristics
Via Hole Diameter
0,3 mm
Internal Pad Diameter
0,6 mm
Ref Plane Opening Diam
1,016 mm
Via Height
1,6 mm
Via Plating Thickness
0,035 mm

IPC-2152 with modifiers mode

Via Capacitance
0,5893 pF
Via DC Resistance
0,00086 Ohms
Power Dissipation
0,00326 Watts
Via Inductance
1,2993 nH
Resonant Frequency
5751.849 MHz
Conductor Cross Section
0,0368 Sq.mm
Via Impedance
46.956 Ohms
Step Response
30.4373 ps
Via Current
1.9514 Amps

Ref Plane Opening
Via Pad
Via Plating
Ref Plane

△ We are using only one type of via. We are far from the resonant frequency and the step response is very fast. Parasites are very low. In DC it can stand the required amount of current. Nevertheless, it should be always used various in parallel to ensure a low resistance path for power and returning currents.

0.35 mm traces

Conductor Characteristics
Solve For
 Amperage
 Help
 No
 Conductor Width
Conductor Width
0,35 mm
Conductor Length
10 mm
Parallel Conductors?
 Yes
 No

Options
Solve For Copper Weight
 Imperial
 Metric
Substrate Options
Material Selection
FR-4 STD
Parallel Conductors?
 Yes
 No

Frequency
 DC
1 MHz
Distance to Plane
1,5 mm

Plating Thickness
4,6 µm
Temp Rise (°C)
10
Temp in (°F) = 18.0
Ambient Temp (°C)
130
Temp in (°F) = 77.0
Plane Thickness
0,5oz / 1oz
2oz
Skin Depth
66.00620 um
Power Dissipation
0,03710 Watts
Conductor DC Resistance
0,01005 Ohms

Skin Depth Percentage
100%
Power Dissipation in dBm
15.6940 dBm
Conductor Cross Section
0,0196 Sq.mm

Voltage Drop
0,0193 Volts
Conductor Current
1.9218 Amps

Information
Total Copper Thickness
70 um
Via Thermal Resistance
N/A

Print
Solve!

IPC-2152 with modifiers mode
Etch Factor: 1:1

△ 0.35 mm traces are used by connecting power pins to the power net in low-power components whose pins are very close together and cannot fit a trace of more width without breaking design rules.

△ This trace width has good properties and can be used even for low-speed analog signals if needed.

0.5 mm traces

Conductor Characteristics
Solve For
 Amperage
 Help
 No
 Conductor Width
Conductor Width
0,5 mm
Conductor Length
10 mm
Parallel Conductors?
 Yes
 No

Options
Solve For Copper Weight
 Imperial
 Metric
Substrate Options
Material Selection
FR-4 STD
Parallel Conductors?
 Yes
 No

Frequency
 DC
1 MHz
Distance to Plane
1,5 mm

Plating Thickness
4,6 µm
Temp Rise (°C)
10
Temp in (°F) = 18.0
Ambient Temp (°C)
130
Temp in (°F) = 77.0
Plane Thickness
0,5oz / 1oz
2oz
Skin Depth
66.00620 um
Power Dissipation
0,03974 Watts
Conductor DC Resistance
0,00654 Ohms

Skin Depth Percentage
100%
Power Dissipation in dBm
15.9921 dBm
Conductor Cross Section
0,0301 Sq.mm

Voltage Drop
0,0161 Volts
Conductor Current
2.4647 Amps

Information
Total Copper Thickness
70 um
Via Thermal Resistance
N/A

Print
Solve!

IPC-2152 with modifiers mode
Etch Factor: 1:1

△ This is an optimal width in terms of area/specs for power delivery as it can withstand a lot of current (more than the system will continuously need) with low losses.

0.8 mm traces

Conductor Characteristics
Solve For
 Amperage
 Help
 No
 Conductor Width
Conductor Width
0,8 mm
Conductor Length
10 mm
Parallel Conductors?
 Yes
 No

Options
Solve For Copper Weight
 Imperial
 Metric
Substrate Options
Material Selection
FR-4 STD
Parallel Conductors?
 Yes
 No

Frequency
 DC
1 MHz
Distance to Plane
1,5 mm

Plating Thickness
4,6 µm
Temp Rise (°C)
10
Temp in (°F) = 18.0
Ambient Temp (°C)
130
Temp in (°F) = 77.0
Plane Thickness
0,5oz / 1oz
2oz
Skin Depth
66.00620 um
Power Dissipation
0,04325 Watts
Conductor DC Resistance
0,00385 Ohms

Skin Depth Percentage
100%
Power Dissipation in dBm
16.3599 dBm
Conductor Cross Section
0,0511 Sq.mm

Voltage Drop
0,0129 Volts
Conductor Current
3.3503 Amps

Information
Total Copper Thickness
70 um
Via Thermal Resistance
N/A

Print
Solve!

IPC-2152 with modifiers mode
Etch Factor: 1:1

△ This trace width is employed by the analog signals to maintain good signal integrity at low line impedance.

It can also be used as a power main bus for ensuring low power losses across a distance and for devices with a pulsed, aggressive power consumption such as the ESP32 and the LCD.

Trace & via characteristics

Trace width based on results from PCB Toolkit by Saturn PCB Design INC.

Used JLPCB 2-layer, FR-4, 1.6 mm height, 35 um conductor height (1 oz/ft²) board characteristics as reference.

Designer's signature

Sheet title: **Trace width design**

Project title: **TIK_HandheldDevice.PjtPcb**

Supervisor's signature

Designer: **Juan Del Pino Mena**

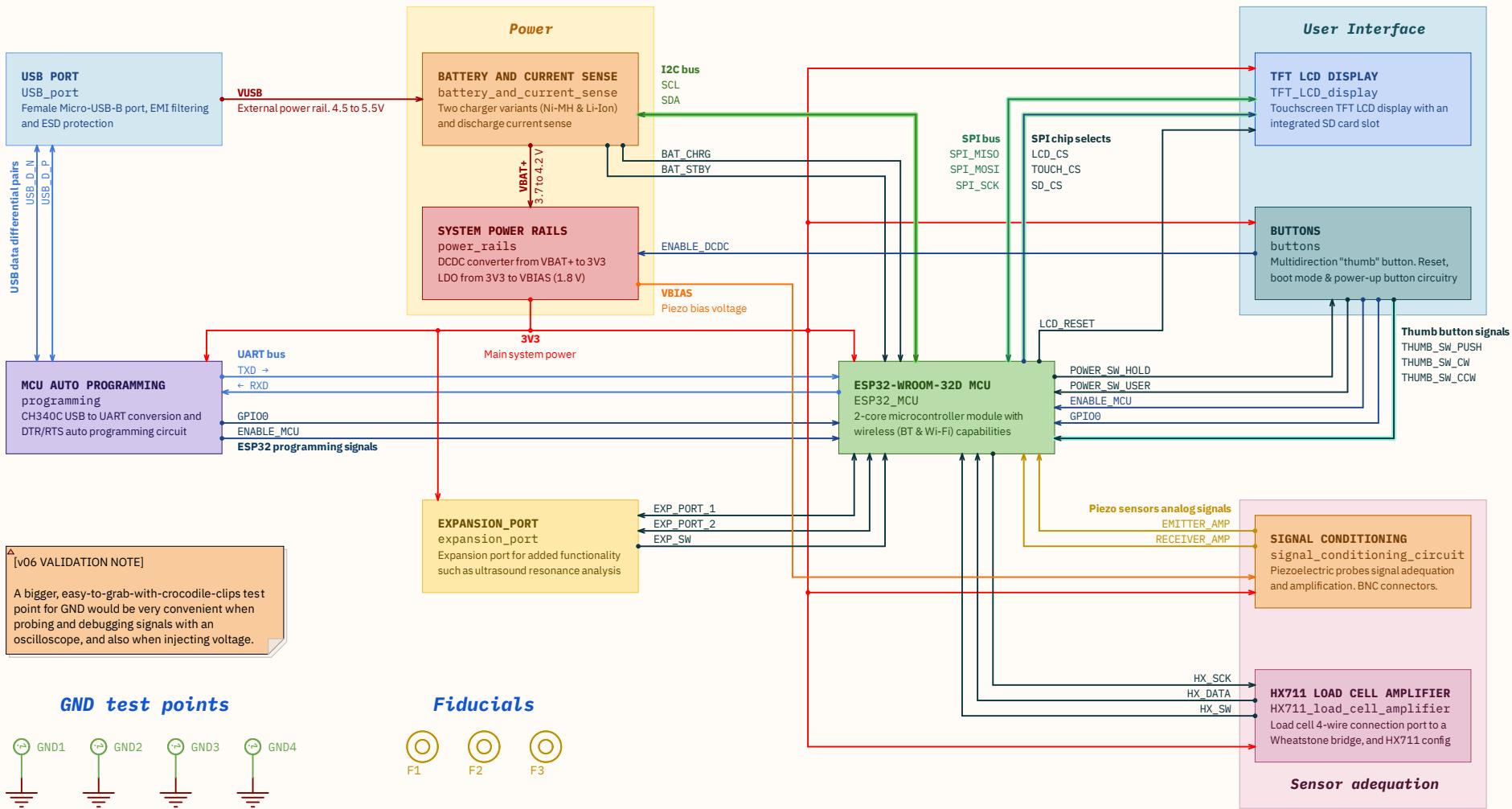
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System blocks organization and connections

The project's global block diagram. Arrows show how modules are interconnected and include net names. PCB includes 3 fiducials for fabrication purposes. GND test points are distributed along the PCB for easy access.

Designer's signature
Supervisor's signature

Sheet title: System blocks organization and connections

Project title: TIK_HandheldDevice.PjPcb

Designer: Juan Del Pino Mena

Date: 2022-07-29

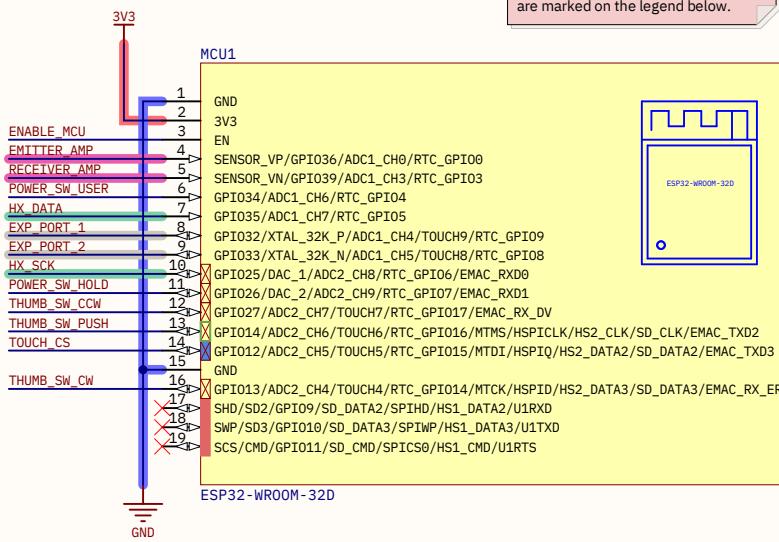
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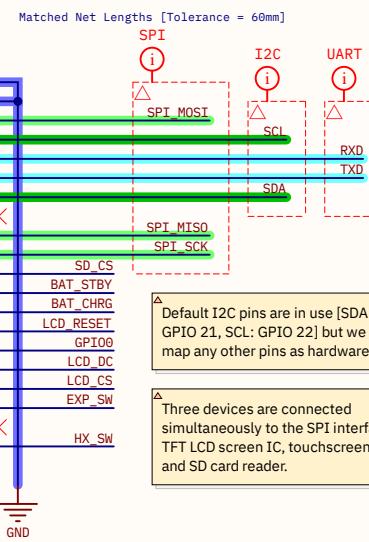


Some ESP32's pins behave in a way that prevent using them freely. They are marked on the legend below.

The ADC2 peripheral is not usable while using Wi-Fi or Bluetooth and should be left unused if not necessary. Digital I/O on those pins while on Wi-Fi or BT is fine.

- Strapping pins (boot parameters selection)
- Connected to internal SPI flash
- [USAGE NOT RECOMMENDED]
- ADC2 peripheral unusable if Wi-Fi is ON
- Outputs PWM/debug info at boot

GPIO23/VSPID/HS1_STROBE
GPIO22/VSPINP/U0RTS/EMAC_TXD1
TXD0/GPIO1/U0TXD/CLK_OUT3/EMAC_RXD2
RXD0/GPIO3/U0RXD/CLK_OUT2
GPIO21/VSPID/EMAC_TC_EN
NC
GPIO19/VSPIQ/U0CTS/EMAC_TXD0
GPIO18/VSPICLK/HS1_DATA1
GPIO05/VSPICSO/HS1_DATA6/EMAC_RX_CLK
GPIO17/HS1_DATA5/U2TXD/EMAC_CLK_OUT180
GPIO16/HS1_DATA4/U2RXD/EMAC_CLK_OUT
GPIO04/ADC2_CH0/TOUCH0/RT_GPIO10/HSPID/HS2_DATA1/SD_DATA1/EMAC_TX_ER
GPIO100/ADC2_CH1/TOUCH1/RTC_GPIO11/CLK_OUT1/EMAC_TX_CLK
GPIO02/ADC2_CH2/TOUCH2/RTC_GPIO12/HSPIMP/HS2_DATA0/SD_DATA0/EMAC_RXD0
GPIO15/ADC2_CH3/TOUCH3/MTDO/HSPICSO/RTC_GPIO13/HS2_CMD/SD_CMD/EMAC_RXD3
SDI/SD1/GPIO8/SD_DATA1/SPIID/HS1_DATA1/U2CTS
SDO/SD0/GPIO7/SD_DATA0/SPIQ/HS1_DATA0/U2RTS
SCK/CLK/GPIO6/SD_CLK/SPICLK/HS1_CLK/U1CTS



Default I2C pins are in use [SDA: GPIO 21, SCL: GPIO 22] but we can map any other pins as hardware I2C.

Three devices are connected simultaneously to the SPI interface: TFT LCD screen IC, touchscreen IC and SD card reader.

Strapping pins digital state are registered during reset and modify the boot sequence parameters according to the [ESP32 datasheet, table 5, page 21]. We must make sure that if pull-up/down resistors are connected to these pins (i.e for buttons) they do not alter the default configuration unintentionally.

Voltage of Internal LDO (VDD_SDIO)					
Pin	Default	3.3 V	1.8 V		
MTDI	Pull-down	0	1		
Booting Mode					
GPIO0	Pull-up	1	0		
GPIO2	Pull-down	Don't-care	0		
Enabling/Disabling Debugging Log Print over U0TXD During Booting					
Pin	Default	U0TXD Active	U0TXD Silent		
MTDO	Pull-up	1	0		
Timing of SDIO Slave					
Pin	Default	FE Sampling FE Output	FE Sampling FE Output	RE Sampling RE Output	RE Sampling RE Output
MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1



[v06 VALIDATION NOTE]

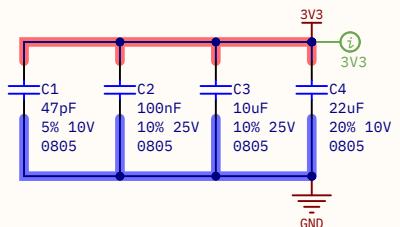
Footprint is adequate, no soldering errors found. SPI, I2C, UART and USB-to-serial work as expected. Programming circuit works and we can upload programs after cutting some tracks (see validation note on the right). Buttons are read correctly. ADC1 can register analog signals correctly.

Following the [ESP32-WROOM-32D datasheet, page 9] GPIO106 to GPIO11 (pins 17 to 22) will remain floating as they are connected to the integrated SPI flash memory and its usage is not recommended for other uses.

Although not recommended, GPIO6 and GPIO8 are used for a very basic task: reading plug switches.

[v06 VALIDATION NOTE]

The jack connector switches interfere with the SPI flash during programming resulting in a programming error. A different circuit (which doesn't pull up these pins) would be needed. As a temporary solution, both EXP_SW and HX_SW tracks were cut in the PCB.



Recommended bucket/bypass capacitors are 0.1 μ F and 10 μ F, ceramic, low ESR. Should be placed close to the chip and with short return paths. [ESP32-WROOM-32D datasheet, page 21]

Added one extra MLC 22 μ F electrolytic cap to filter current spikes during ESP32 RF usage and a small 47pF capacitor to be more effective filtering high frequencies

ESP32-WROOM-32D MCU, Wi-Fi + Bluetooth module

This module integrates an ESP32-D0WD chip, a 240 MHz, dual-core processor with Wi-Fi and Bluetooth capabilities. This sheet describes its hardware configuration and I/O pins

Designer's signature
Supervisor's signature

Sheet title: **ESP32-WROOM-32D MCU**
Project title: **TIK_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

Date: **2022-07-29** Revision: **0.6** Sheet 6 of 20

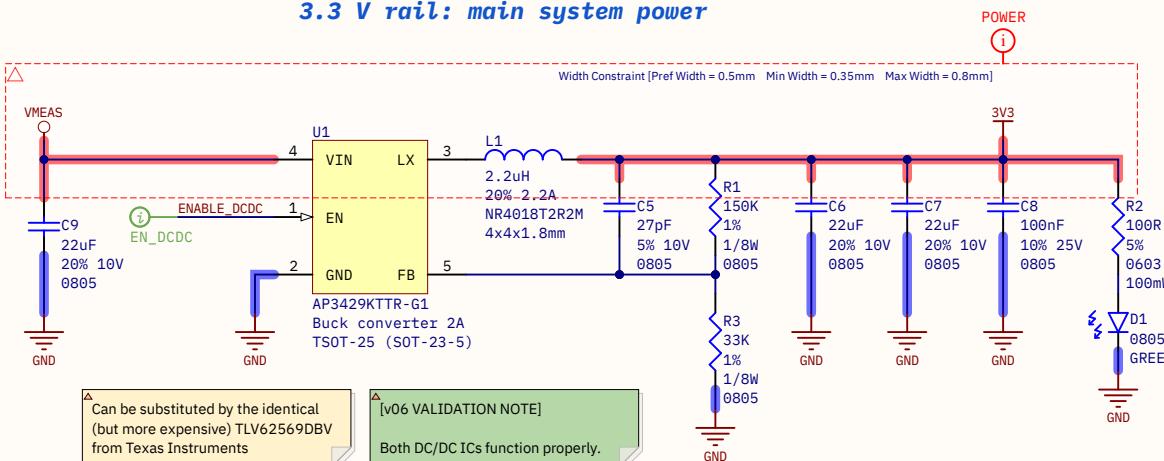
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3.3 V rail: main system power

Typical Application Circuit. [AP3429/A datasheet, page 2]
with some values modified as needed and/or part availability.
Capacitors should be placed close to the chip and circuit should be traced in short loops.
Feedback voltage V_{FB} is regulated at 0.6 V.

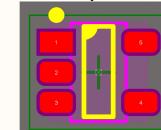
Resistors are adjusted as a voltage divider. So, if 3.3V are needed at the converter output:
 $V_{FB} = 0.6V = V_{out} \cdot (R2)/(R1+R2)$
Thus, $R2 = 2/9 \cdot R1$
Resistor values must be high (kOhms) in order to maintain a low power consumption on the feedback circuit.



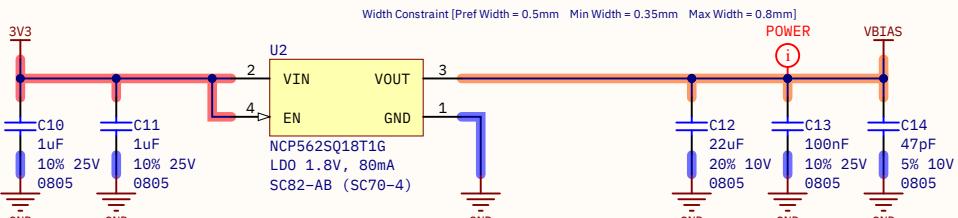
Real model:



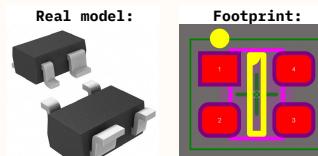
Footprint:



1.8 V rail: Vbias for signal conditioning circuit



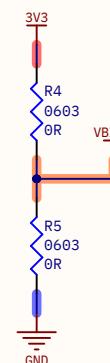
Usage of multiple input capacitors to reduce ESR and ESL. Recommended Cin is 1 uF. There are no recommended values for Cout but these 3 caps should probe more than enough for low ESR and ripple reduction at a wide frequency range. Datasheet specifies a typical 100 uVRMS noise on Vout, somewhat high.



[v06 VALIDATION NOTE] The LDO works as expected.

Optional 1V8 rail bypass jumpers

IMPORTANT:
1V8 rail is bypassable by soldering these optional 0-ohm resistors. This is for experimenting with different voltages and if it affects the overall performance of the acquisition circuit.
Do NOT connect both OR resistors at the same time or it will jump VCC and GND. And keep the LDO disabled at all times.



This can also be used to insert a voltage divider, i.e.: if you want to reduce the rail voltage to VCC/2 you only have to add two >= 10 KOhm 0603 resistors. Just keep in mind that voltage won't be as stable as in a LDO as it will be greatly dependent on the load impedance.

If you do this, populate the LDO's output caps, so VBIAS it behaves as a small-signal GND.

Power rails

Battery DC/DC step-down converter and Vbias for signal conditioning circuit. 3V3 is the main system power and can deliver up to 2 amps. VBIAS is only for polarization of the probes and won't drag much current.

Designer's signature
Supervisor's signature

Sheet title: Power rails
Project title: TIK_HandheldDevice.PjPcb

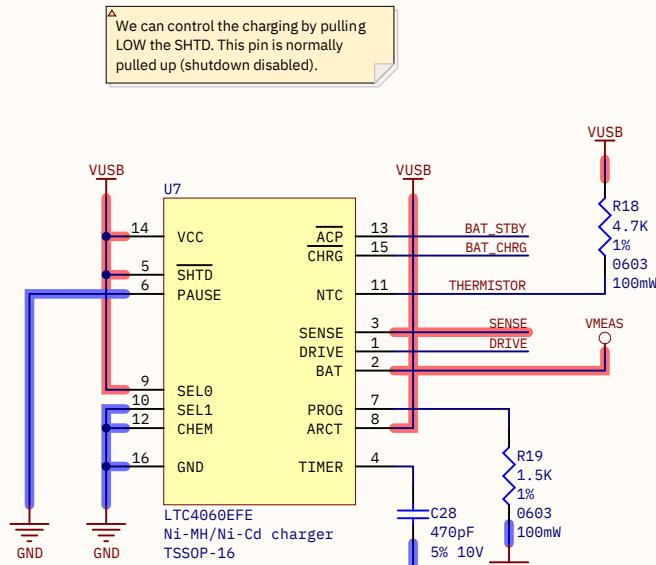
Designer: Juan Del Pino Mena

Date: 2022-07-29 Revision: 0.6 Sheet 7 of 20

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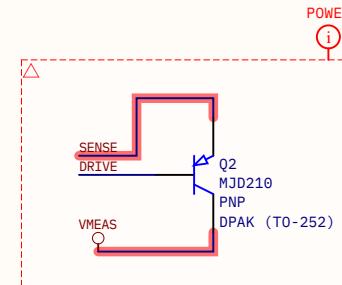
NiMH/NiCd battery charger IC



[v06 VALIDATION NOTE]
NOT POPULATED AND UNTESTED.

Width Constraint [Pref Width = 0.5mm Min Width = 0.35mm Max Width = 0.8mm]

POWER

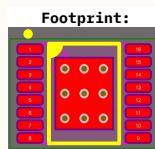


Following the [LTC4060 datasheet, page 13], if using a 10 K NTC thermistor, Its R_{HOT} should be 4.42 kΩ, 1% to trigger the temperature warning at 45 °C. However, this value being too much specific is problematic.

This can be disabled by connecting a 0-ohm resistor in place of the thermistor.

[CURRENTLY NOT IMPLEMENTED] This IC can do power path control. This is, to power the load from external source while charging the battery.

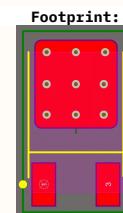
DRIVE pin on the LTC4060 provides a controlled sink current that drives the PNP base. So, it's not necessary to have a base resistor.



TIMER capacitor and PROG resistor program the charge T_{max} (maximum charging time, a security measure). [LTC4060 datasheet, page 13]. These values should complete a full charge in at most 1 h 6'.

PROG resistor programs the maximum current that the battery will receive while charging. For 1.5 kΩ this is 0.93 A.

i.e.: a 1000 mAh battery will charge at approx 1C with this configuration, but can be insufficient time for a 3000 mAh one.



Battery charging circuitry for Ni-MH

Battery charger circuit variant #1. By default the device uses a Nickel-metal hydride battery which are chemically and thermally more stable (and safer) than Lithium-based ones; at the cost of a lower charge/volume ratio.

Designer's signature
Supervisor's signature

Sheet title: **Battery charger**
Project title: **TIK_HandheldDevice.PjPcb**

Desinger: **Juan Del Pino Mena**

Date: **2022-07-29** Revision: **0.6**

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Lithium battery charger IC

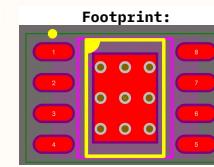
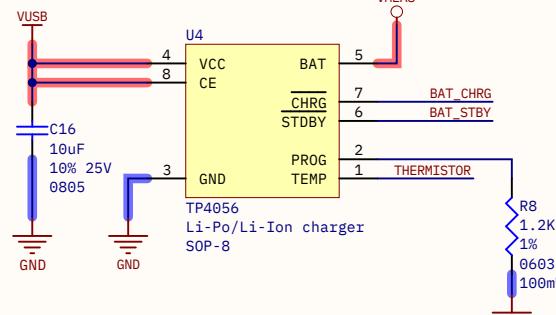
The TP4056 datasheet recommends to connect a resistor of 0.2 to 0.5 Ohm between VUSB and its VCC pin. It does not explain why, but probably for chip temperature concerns.

However, it is omitted as we don't have any resistor of these values available. As a note: not a single commercial TP4056 charger module uses any resistor at all (and they work fine at higher charge rates).

The TP4056 is only specified for charging single-cell Li-Ion batteries on its datasheet. However, many sites, forums and online stores list TP4056-based modules as compatible with both Li-Ion and Li-Po given the chemistry similarity. Take this with caution.

Resistor in PROG regulates the maximum battery charging current. At 2 kOhm, this is 580 mA. At 1 kOhm, it is > 1 A. Change according to battery capacity. [TP4056 english datasheet, page 3]

TEMP expects a NTC thermistor (of unspecified value). On some Lithium-Ion batteries this NTC can be integrated on the package.



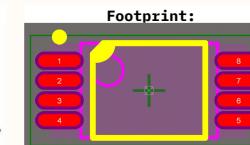
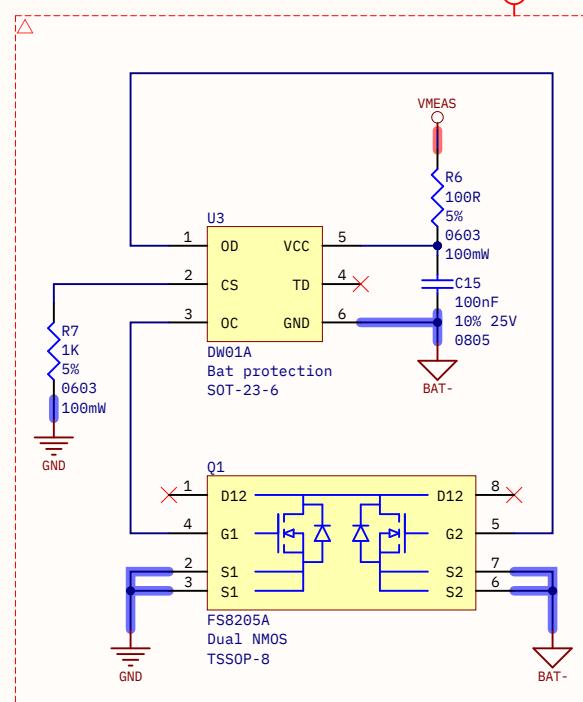
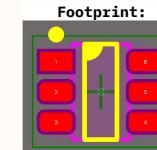
This device will get hot, and has a thermal pad to dissipate to PCB GND plane

Lithium battery protection

Width Constraint [Pref Width = 0.5mm Min Width = 0.35mm Max Width = 0.8mm]

POWER

i

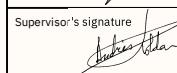


[v06 VALIDATION NOTE]
This charger works correctly and protection circuit trips under 2.8-3 V. Tested using a single-cell lithium-polymer battery.

Battery charging circuitry for Li-Po & Li-Ion

Battery charger circuit variant #2. Li-Ion and Li-Po batteries offer much more power density at the cost of instability. This circuit must NOT be placed if the Ni-MH charger is present on the board (and vice-versa).

Designer's signature

Supervisor's signature


Sheet title: **Battery charger**

Project title: **TIK_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

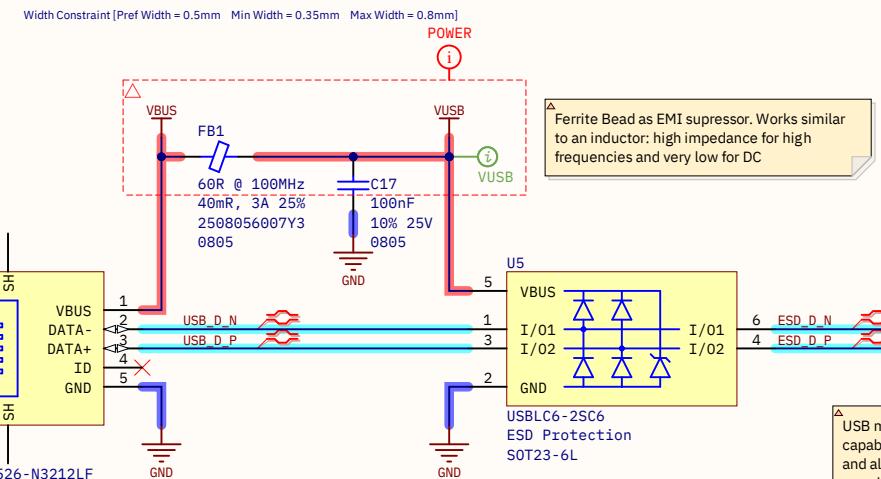
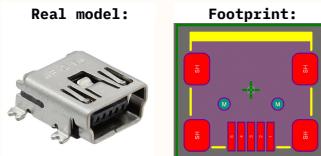
Date: **2022-07-29** Revision: **0.6** Sheet 10 of 20

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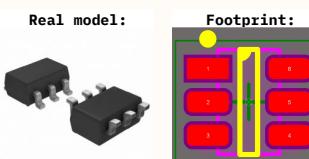


△ 'SH' pads are the USB connector metal shield, which is structural. This particular connector has 4 which are not connected to any circuit traces, not even GND. In any case, it should be connected to the device's metal chassis (as a faraday cage).

△ An USB-Mini-B has been chosen for various reasons:
 - Over an USB-micro: because of the structural robustness of the mini-B.
 - Over an USB-Type-C: because of the ease of implementation, less pins, and to make clear this device is not a host.



△ [v06 VALIDATION NOTE]
 The selected USB-mimi-B port is very stiff and has a good quality of construction, however one must be cautious while soldering as its plastic can melt resulting in an unusable connector.



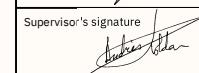
USB connector and ESD protection circuit

USB is used as a programming interface, as well as a power source for the charging circuit. Since it's an external connector, it needs to have a protection circuit against electro-static discharge (ESD) and noise.

Designer's signature



Supervisor's signature



Sheet title: **USB connector and ESD protection circuit**

Project title: **TIK_HandheldDevice.PxjPcb**

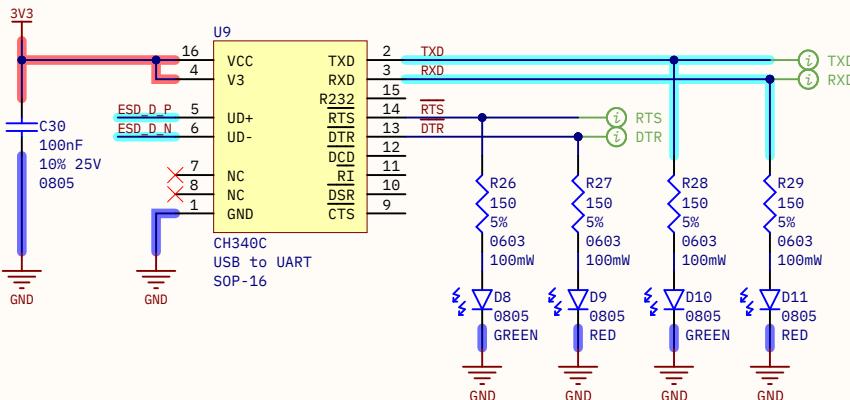
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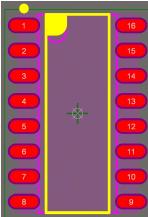
USB to UART conversion



Real model:



Footprint:



These LEDs serve as a visual testimony of UART communication and help during debugging.

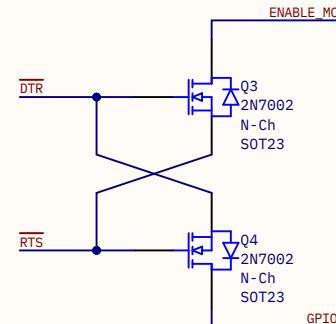
If they drag too much current they can be used with 1 kΩ resistors or be completely disconnected.

Should not be present on a commercial product.

[v06 VALIDATION NOTE]

This IC works correctly. However, debug LEDs are both not very visible (they blink fast for short times) and not very useful (sometimes redundant), so they can be removed.

Auto programming circuit



ESP32 GPIO0 is a Strapping pin. Strapping pins modify the device's boot mode during chip reset. GPIO0 is pulled up during reset by default. ENABLE_MCU is pulled up by an external pullup resistor

When GPIO0 is HIGH, it boots from internal SPI memory, but when it's LOW the boot sequence changes to 'Download' and we can upload a program to the MCU.

[ESP32 Datasheet, section 2.4, pages 19-20]

Circuit truth table

DTR	RTS	ENABLE_MCU	GPIO00
0	0	1	1
0	1	1	0
1	0	0	1
1	1	1	1

*(DTR, RTS active low)

[v06 VALIDATION NOTE]

This circuit works correctly, the programming signaling sequence (RESET to Low, then GPIO0 to low) is correct and we can program the MCU.

USB to UART and MCU programming

This circuit allows a computer to the ESP32 via USB so it can be reprogrammed. This is possible by sending RTS and DTR signals with a determined timing so the device enters an alternative boot mode.

Designer's signature
Supervisor's signature

Sheet title: **USB to UART and MCU programming**

Project title: **TIK_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

Date: **2022-07-29**

Revision: **0.6**

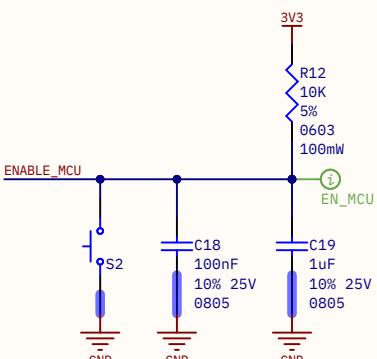
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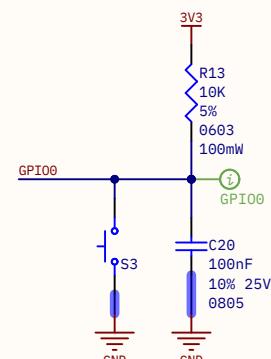


Reset

To ensure power stability to the microcontroller during powerup, this RC filter introduces a delay on the ENABLE pin. Usual values are $10\text{ k}\Omega$, $1\text{ }\mu\text{F}$ ($\tau = 10\text{ ms}$, $t_{10-90} = 22\text{ ms}$).
[ESP32-WROOM-32D datasheet, page 22]

**Boot mode selection (debug)**

Allows to force 'Download' boot sequence
Same design as in ESP32 DevKit boards.
100 nF cap are for debouncing and should be placed close to the buttons



[V06 VALIDATION NOTE]
These buttons function properly.

POWERUP BUTTON
powerup_button
Power-up button circuitry for enabling the DCDC buck converter

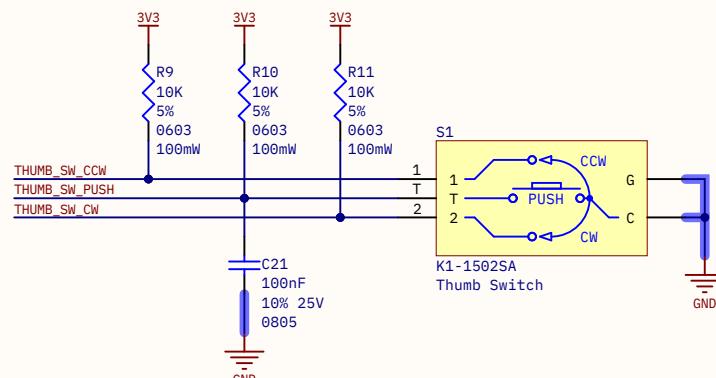
Buttons

TIK buttons. Some of them are meant for debugging like boot mode selection and reset, and will not be accessible to the end user. The power-up button and the "thumb" button are meant to be part of the UI.

Multidirection 'thumb' button (UI navigation)

Horizontal SMD device, multi-directional / muti-function rotary slider button. Accessed from the right side.

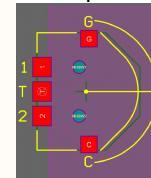
[V06 VALIDATION NOTE]
The 'thumb' button functions properly.



Real model:

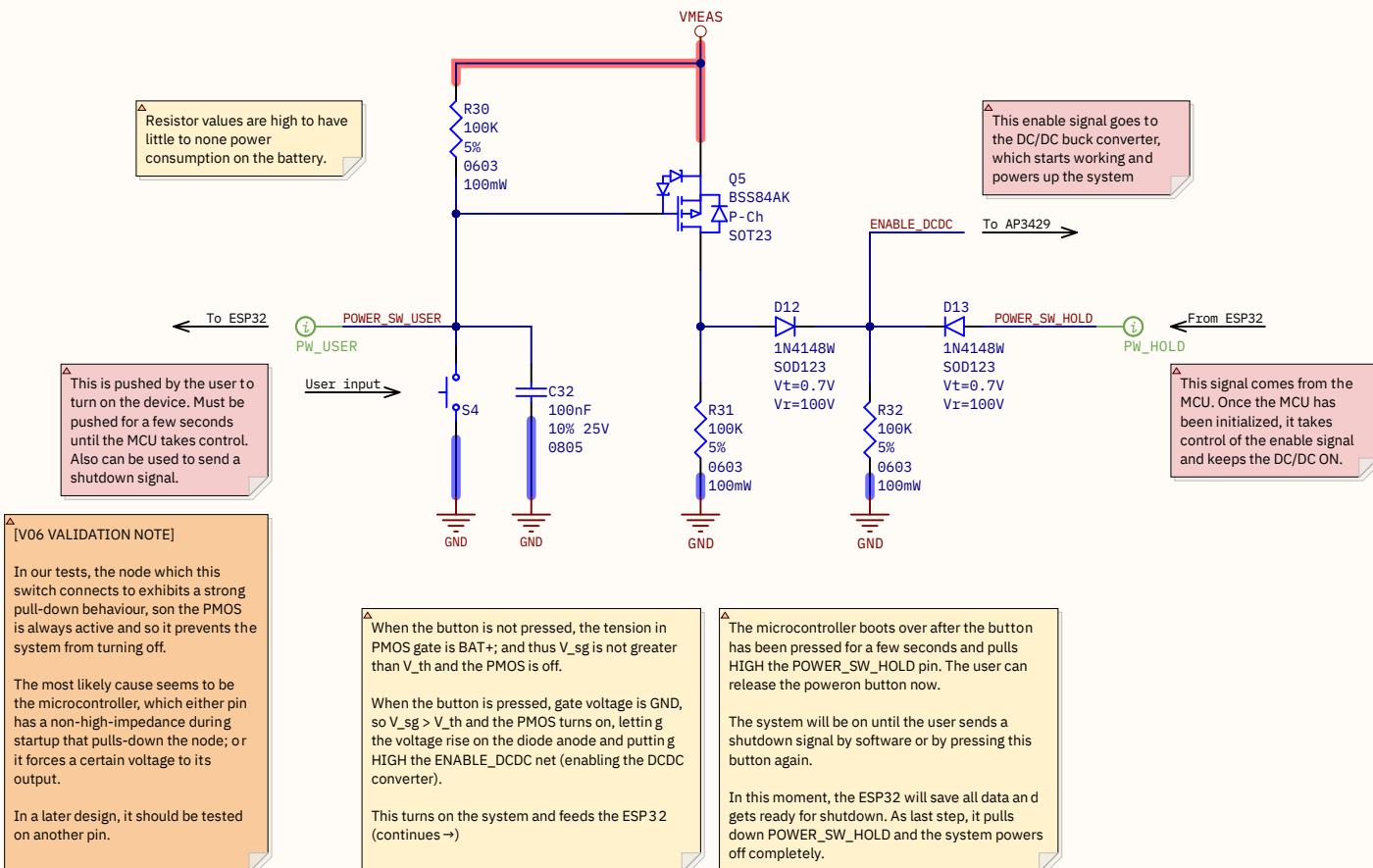


Footprint:



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Powerup button

This circuit avoids using a power-up switch, which can shutdown the device without prior warning. The user pushes a button during a couple of seconds, in which the ESP32 will boot and keep the system on until a shutdown signal is sent.

Designer's signature
Supervisor's signature

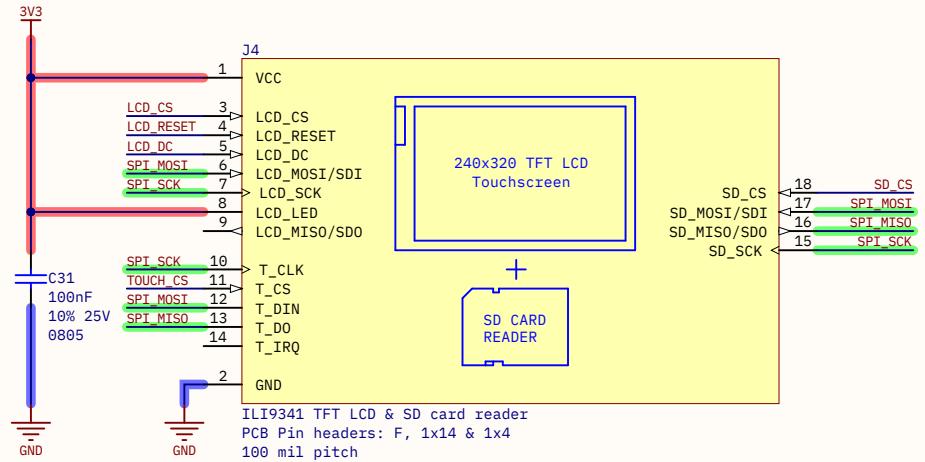
Sheet title: **Powerup button**
Project title: **TIK_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

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[v06 VALIDATION NOTE]

Screen and touch works with no problems.

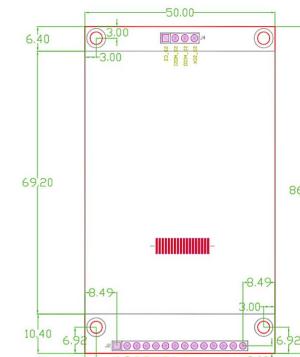
Real model:



Footprint:



As ILI9341 2.8" TFT LCD module has the bigger footprint t and needs mechanical support. Our PCB inherits its mounting holes position.



LCD TFT touchscreen & SD card reader

TIK uses an ILI9341 2.8" TFT LCD display module as a graphic user interface. This module has touchscreen capabilities and also integrates a SD card reader on one of its sides. All three elements are managed via SPI.

Designer's signature
Supervisor's signature

Sheet title: LCD TFT touchscreen & SD card reader

Project title: TIK_HandheldDevice.PxjPcb

Designer: Juan Del Pino Mena

Date: 2022-07-29 Revision: 0.6

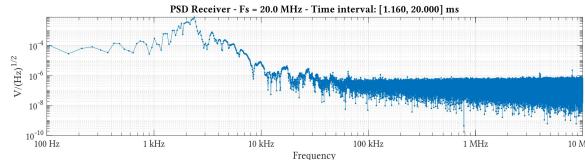
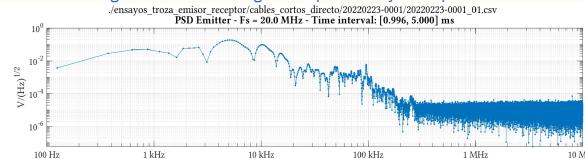
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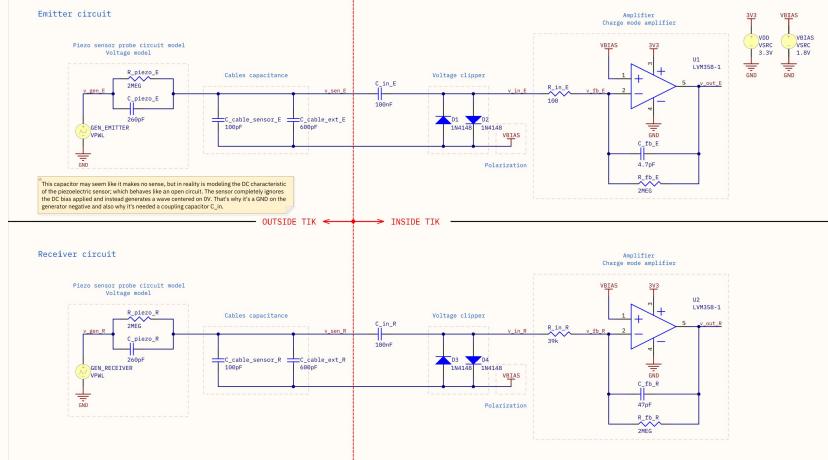
Trunk signal's Voltage Spectral Density

Example VSD of a generic trunk signal captured by the piezoelectric sensors



Simulated circuit

Circuit from a subproject inside ./SIMULATIONS

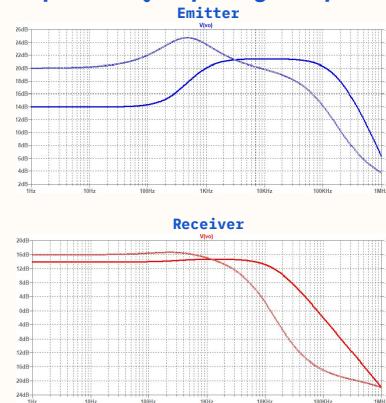


[TOPOLOGY DOES NOT CHANGE, BUT COMPONENT VALUES MAY NOT BE UP TO DATE]

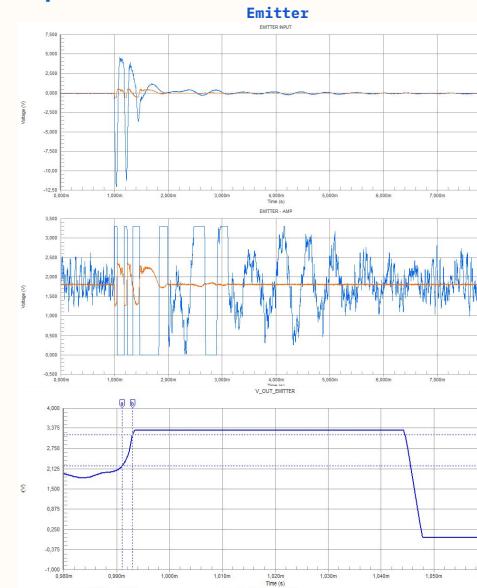
A piezoelectric is commonly modeled as a charge source in parallel with a resistor and a capacitor (charge model). This, however, is not practical for simulated analysis. Instead, we resorted to the voltage model, which is a voltage source in series with a resistor and a capacitor in parallel.

Nevertheless, in empirical analysis we found that our probes are far more complex than this simple model: They behave like an open circuit for DC (thus ignoring VBIAS). They have a great resistance and capacitance dependency on frequency, and a resonance around 100 kHz.

Expected frequency response



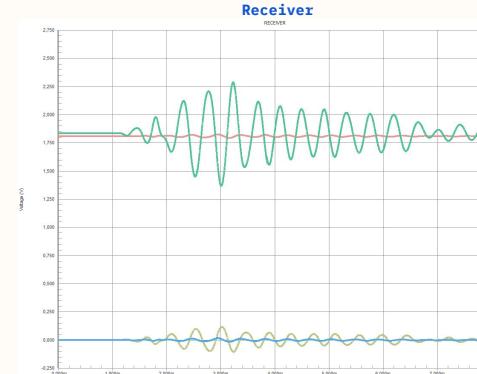
Expected transient behavior



The emitter input signal can be of 10 to 20 V if the piezoelectric probe is hit very hard. This voltage can damage electronics. As a countermeasure we use two 4148 diodes on the input that clip the signal to ± 0.7 volts around VBIAS, allowing us to manipulate it without risk.

The adequate circuit for the emitter has more gain than it needs, so the output of the OpAmp is saturated. This gives us a very step flank where the signal clearly begins and it's very easy to identify. In this simulation it's clear that maybe it's not needed so much gain as the output is very noisy and could be easily false-triggered.

Zoom over the first pulse. The expected rise time will be around 2 us, so the delay is of 1 sample ($F_s = 500 \text{ kHz}$)



The receiver on the other hand has a very weak signal that needs to be amplified and centered over 1.8V. We have to be more cautious in this case so we don't distort it as we have to sample and process it with precision.

The adequate circuit for the receiver has more gain than it needs, so the output is saturated. This gives us a very step flank where the signal clearly begins and it's very easy to identify.

Signal conditioning circuit simulations

SPICE simulations of the adequation circuit. These are only the results. You can find the simulation circuit and models on the ./SIMULATIONS/ folder inside this project.

Designer's signature
Supervisor's signature

Sheet title: **Signal Conditioning Theoreticals**
Project title: **TIK_HandheldDevice.PjPcb**

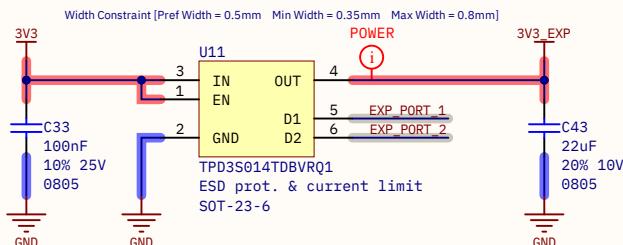
Designer: **Juan Del Pino Mena**

Date: **2022-07-29** Revision: **0.6** Sheet 17 of 20

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Current limiter and ESD protection



Since this is an external connector directly connected to the 3V3 rail, this will have a current limit switch and ESD protection IC to avoid damaging the device.

3.5mm jack connector considerations

We are using the 3.5mm jack connector in a non-standard application, as we are not transferring audio but power and/or analog and digital signals of different nature.

Nevertheless, we have adjusted the connector to somewhat fit the OMPT convention (GND in sleeve, signals in rings).

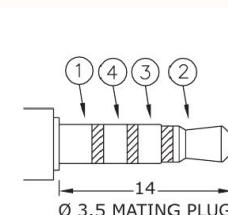
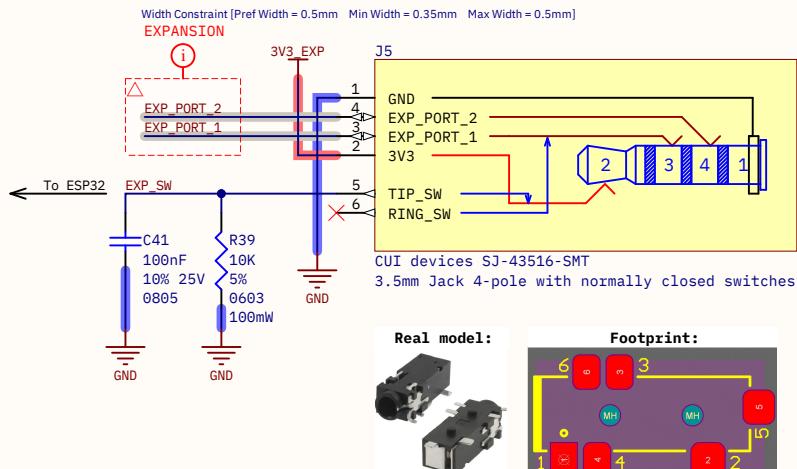
The mating socket and plug are connected as follows. In this connector series there is the possibility of up to 6 pads, the additional 2 pads being connected to switches for detecting the plug insertion. We only use the tip switch (pin 5) to allow using both the SJ-43516 as well as the SJ-43515 models. We prefer the 6-pad version as it offers more mechanical integrity.
[CUI Devices SJ-4351X-SMT Datasheet, page 2]

Expansion port connector

Expansion port pins are both Input/Output and are connected to the ADC1 so we give the maximum amount of functionality available to the expansion module.

Plug detection switch circuitry operation: The switch is normally closed. So, normally EXP_SW is HIGH. When plugged in, the switch opens and EXP_SW will be LOW

[v06 VALIDATION NOTE]
UNTESTED



Model No.	SJ-43516-SMT
Schematic	
PIN	
1	sleeve
2	tip
3	ring 1
4	ring 2
5	tip switch
6	ring switch

To avoid shorting GND and VCC, the 3V3 rail is located at the tip, so it will make contact last. This also allows us to easily add the tip switch circuitry.

Expansion port & jack connector

Expansion port for added functionality, such as an ultrasound resonance analysis for wood boards. Also, this sheet includes a description of the jack connector properties.

Designer's signature

Sheet title: Expansion port

Project title: TIK_HandheldDevice.PjPcb

Supervisor's signature

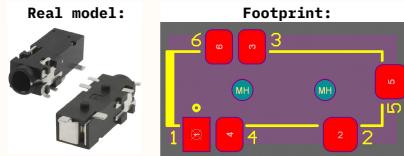
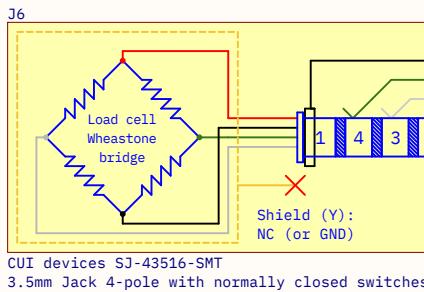
Desinger: Juan Del Pino Mena

Date: 2022-07-29 Revision: 0.6

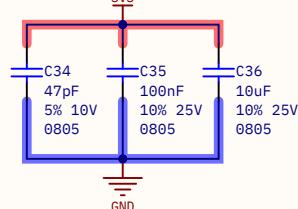
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There's no "standard load cell connector". We have selected a 3.5mm jack 4-pole connector and organized the pins in the usual order and with usual colors. Note that the shield is unconnected. A more appropriate alternative could be a RJ-11 6-pin connector, but was discarded because of the large socket size.

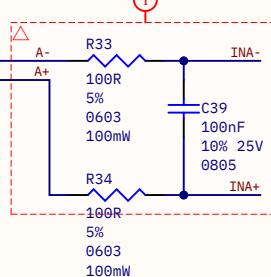


VCC/VDD bypass caps for noise filtering and voltage stabilization for the HX711.

[v06 VALIDATION NOTE]
UNTESTED

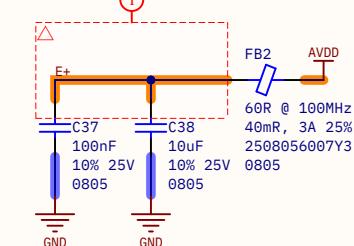
Width Constraint [Pref Width = 0.5mm Min Width = 0.35mm Max Width = 0.5mm]

LOAD_CELL_SIGNAL



Width Constraint [Pref Width = 0.5mm Min Width = 0.35mm Max Width = 0.5mm]

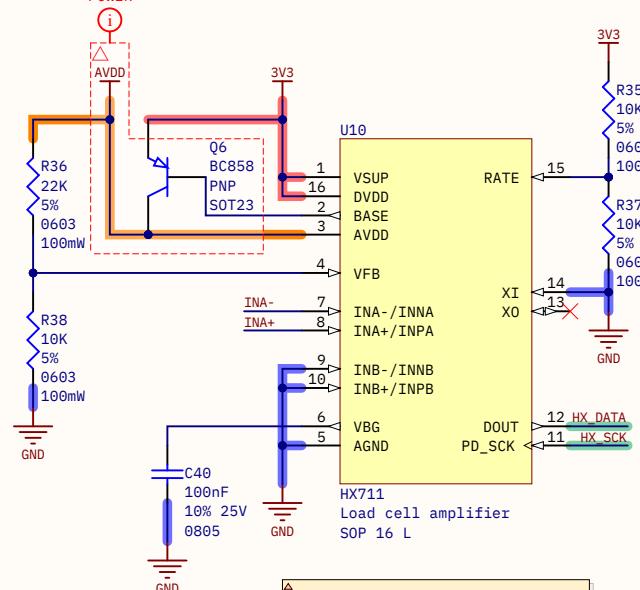
POWER



Noise/EMI filtering on AVDD. Sparkfun's design uses a 2.2 uH chip inductor. Instead we use a ferrite bead.

Width Constraint [Pref Width = 0.5mm Min Width = 0.35mm Max Width = 0.5mm]

POWER



RATE pin config:
- Pulled down: normal mode, 10 SpS
- Pulled up: fast mode, 80 SpS, noisier



HX711 load cell amplifier

This circuit is used to get weight measurements out from load cells in order to estimate the density of a trunk or board.
This design is based on the Sparkfun HX711 module by N. Seidle and A. Wende.

Designer's signature
Supervisor's signature

Sheet title: **HX711 load cell amplifier**

Project title: **TIK_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

Date: **2022-07-29**

Revision: **0.6**

Sheet 19 of 20

Supervisor:
Sr. Andrés Roldán Aranda
Dpto. Electrónica y Tecnología de Computadores
University of Granada
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Granada, Granada, Spain

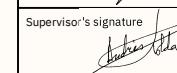


A	Block	Component	Description/Conditions	Units	Supply voltage (V)	Current consumption per unit (μ A)		Total dissipated power (μ W)		Notes
						Typical	Maximum	Typical	Maximum	
	MCU	ESP32-WROOM-32D	MCU + wireless comm. Module	1	3.3	500 mA		1.7 W		Current spikes during wireless TX
Power rails		AP3429	DC/DC Buck converter IC	1	4.2	90 μ A		378 μ W		
		NCP562SQ18T1G	Low-Dropout regulator IC	1	3.3	3 μ A		9.9 μ W		
		150 k Ω + 33 k Ω voltage divider	FB pin feedback. Fixed consumption	1	3.3	18 μ A		59.4 μ W		
		[Optional] bypass voltage divider	Assuming 3V3/2 with 10 k Ω resistors	1	3.3	165 μ A		544.5 μ W		Consider only if populated
		Generic 0805 green LED	Assuming Vf = 3V & 39 Ω series resistor	1	3.3	7.7 mA		25.4 mW		Consider only if populated
Battery & current sense		INA219	Voltage & current sense IC	1	4.2	0.7 mA	1 mA	3 mW	4.2 mW	
		Generic 0805 green LED	Assuming Vf = 3V & 220 Ω series resistor	1	5.5	11.4 mA		62.5 mW		Consider only if populated
		Generic 0805 red LED	Assuming Vf = 2V & 470 Ω series resistor	1	5.5	7.5 mA		41 mW		Consider only if populated
		I2C pull-up resistor	Assuming line level is LOW, with 4.7k Ω resistors	2	3.3	0.7 mA		4.6 mW		
B		LTC4060EFE	NiMH/NiCd charger IC	1	5.5	2.9 mA	4.3 mA	16 mW	23.7 mW	
	[Optional] NiMH charger	MDJ201	Power PNP BJT. Ice=0.95 A, Ibe=120mA, Vce=1.8V, Vbe=0.7 V	1	--	--		1.71 W + 84 mW \approx 1.8 W		Consider only if populated. For charging ICs and BJT: consider only when charging the battery (else they are off). In this case power consumption comes from external supply not from the internal battery.
		4.42 k Ω + NTC voltage divider	NTC pin. Assuming NTC at 50°C (3.54 k Ω)	1	5.5	691 μ A		3.8 mW		
[Optional] Li-Ion/Li-Po charger		TP4056	Li-Ion/LiPo charger IC, Vbus-Vbat=1.8 V, Ibat=1 A	1	5.5	150 μ A	500 μ A	1.8 W + 2.8 mW \approx 1.8 W		
	DW01A	Battery protection IC		1	4.2	3 μ A	6 μ A	12.6 μ W	25.6 μ W	
	FS825A	Dual power NMOS, Rds(on)=25 m Ω , Ibat=1 A		1	--	--		50 mW (both NMOS)		
USB connector	USBLC6-2SC6	USB ESD protection IC		1	5.5	10 nA	150 nA	55 nW	825 nW	Consider only when USB is plugged
	CH340C	USB to UART converter IC		1	3.3	12 mA	30 mA	39.6 mW	99 mW	Worst case when programming
Programming	2N7002	G.P. NMOS. Ib=0 A, Vds=3.3 V, Ids=330 μ A (during conmutation)		2	--	--		1 mW		Consider only when programming
	Generic 0805 green LED	Assuming Vf = 3V & 39 Ω series resistor		2	3.3	7.7 mA		50.8 mW		Consider when programming, using UART and if populated.
	Generic 0805 red LED	Assuming Vf = 2V & 150 Ω series resistor		2	3.3	8.7 mA		57.4 mW		
Buttons	Pull-up resistors	Assuming line level is LOW, 10k Ω resistors		5	3.3	0 (not pushed)	330 μ A	0 (not pushed)	5.4 mW	Worst case: all pressed at once
	BSS84AK	G.P. PMOS. Rsd(on) = 7.5 Ω , Ib=0, Isd = 77 μ A		1	--	--		45 nW		
Power-up button	1N4148W	Small signal diode. Vf=0.7 V, If=26 μ A		2	--	--		36.4 μ W		Worst case: both ON
	100 k Ω pull-up resistor	100 k Ω pull-up resistor		1	4.2	42 μ A		176.4 μ W		
TFT LCD display	LCD TFT ILI9341 module	320x240p LCD (Measured)		1	3.3					Worst case: all pixels white, 60 FPS
Signal conditioning	LMV358DGKR	General purpose dual OpAmp, with no load		1	3.3	140 μ A	340 μ A	462 μ W	1.1 mW	Both OpAmps, high Z load
	1N4148W	Small signal diode. Vf=0.7 V, If= μ A (Measured)		4	--					Consider only when measuring
Load cell amplifier	HX711	Load cell amplifier & ADC IC		1	3.3	1.4 mA		4.6 mW		Enters sleep if the data clock stops
	BC858	General purpose PNP BJT. Vce=1.8V, Ice=? μ A (Measured)		1	--					Consider only when HX711 is awake
	22 k Ω + 10 k Ω voltage divider	VFB pin feedback for AVDD=1.82 V regulation.		1	1.82	57 μ A		103.7 μ W		Consider only when HX711 is awake

Power budget

Detailed estimation of typical and worst-case power consumption per component in order to define battery requirements. Choosing a battery.

Designer's signature

Supervisor's signature


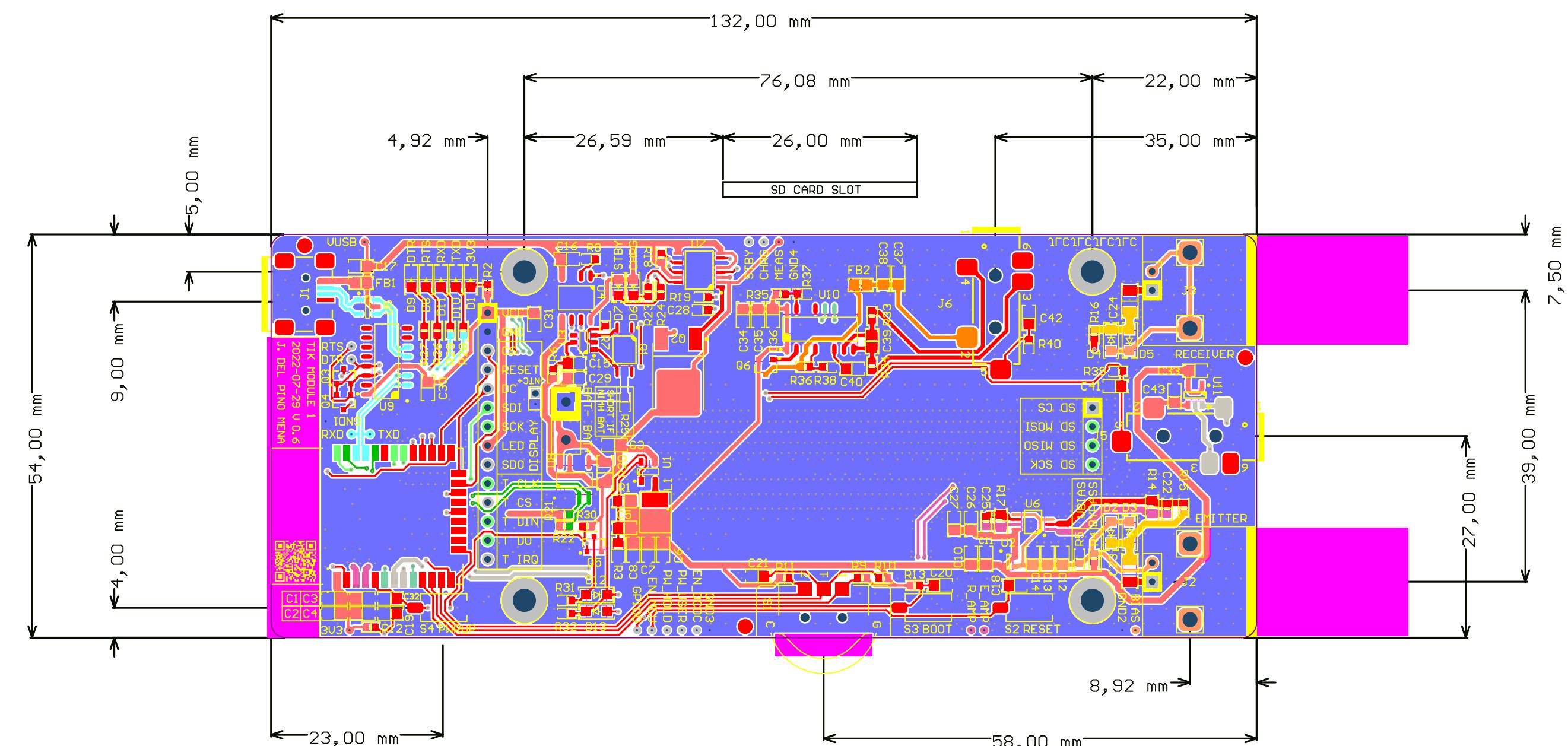
Sheet title: **Power budget**
Project title: **TIK_HandheldDevice.PjPcb**
Desinger: **Juan Del Pino Mena**
Date: **2022-07-29** Revision: **0.6** Sheet 20 of 20

Supervisor:
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A

A



VISIBLE LAYERS

Board outline + Multilayer + Top
overlay + Top layer + Keep-out
dimensions

TRACKS & POLYGONS COLOR LEGEND:

 Emitter/Receiver Analog Signals	 Power Reference GND/BAT-	 SPI
 Generic Net on Top Layer	 Power Rail 3V3/BAT+/VUSB/ VMEAS/VSENSE	 I2C
 Generic Net on Bottom Layer	 Power Rail VBIAS	 SERIAL UART/USB

TIK handheld device PCB

PCB orientation: vertical. Screen facing front, BNCs on top, USB at the bottom, SD Card reader at the left, powerup button at the bottom front right, and multipurpose button on the right side.

Designer's signature

Sheet title: TIK Handheld Device PCB

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Sr. Andres Boldan Aranda

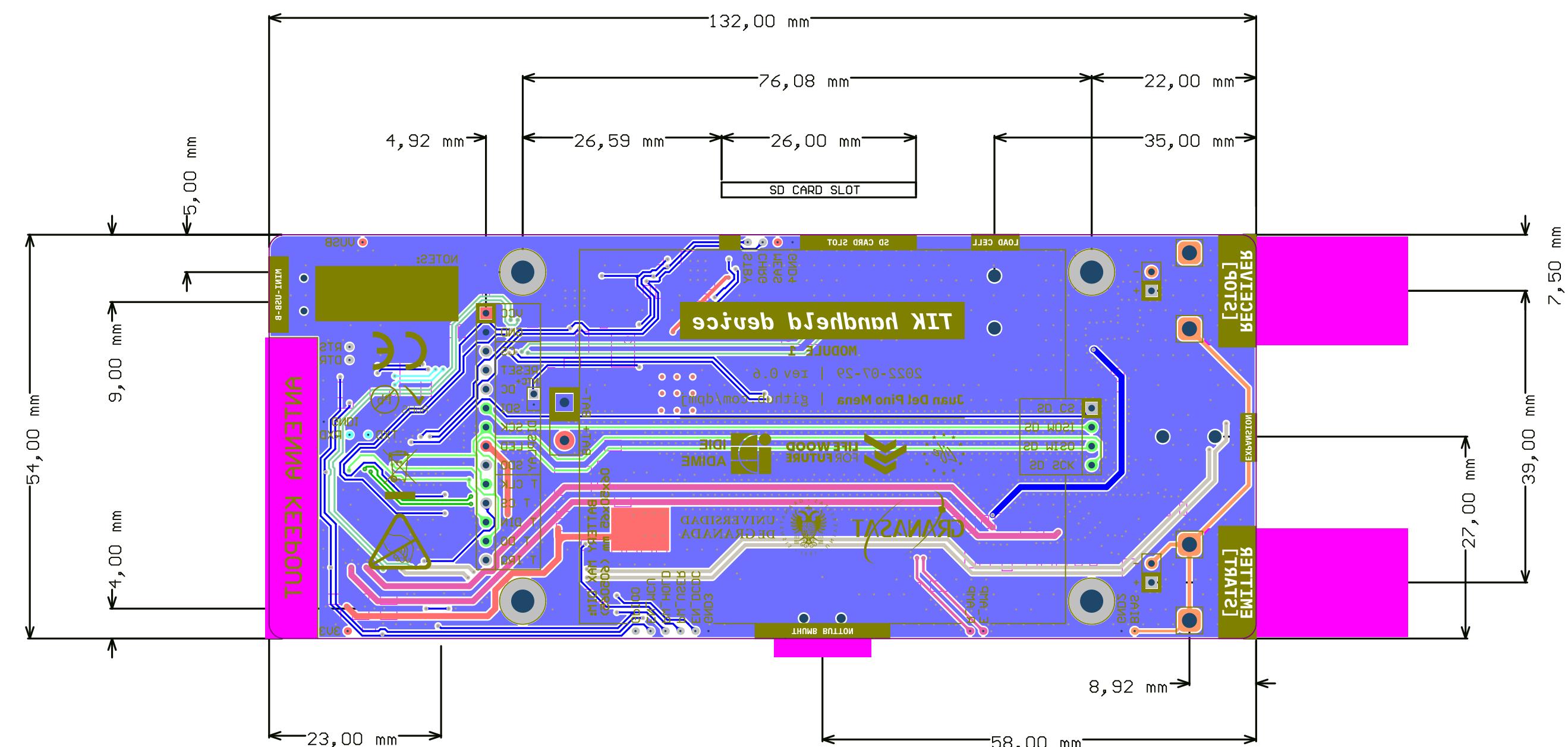
Supervisor's signature

Design by Juan Del Rio Mena

Date: 2022-07-29
Revision: 0.6 Sheet 1 of 1



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VISIBLE LAYERS:

Board outline + Multilayer + Bottom overlay + Bottom layer + Keep-out + dimensions

TRACKS & POLYGONS COLOR LEGEND:

EMITTER/RECEIVER ANALOG SIGNALS	POWER REFERENCE GND/BAT-	SPI
GENERIC NET ON TOP LAYER	POWER RAIL 3V3/BAT+/VUSB/VMEAS/VSENSE	I2C
GENERIC NET ON BOTTOM LAYER	POWER RAIL VBIAS	SERIAL UART/USB

TIK handheld device PCB

PCB orientation: vertical. Screen facing front, BNCs on top, USB at the bottom, SD Card reader at the left, powerup button at the bottom front right, and multipurpose button on the right side.

Designer's signature:

Supervisor's signature:

Sheet title: TIK Handheld Device PCB

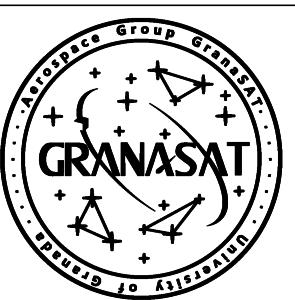
Project title: TIK_HandheldDevice

Designer: Juan Del Pino Mena

Supervisor: Andres Roldan Aranda

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de Computadores
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Granada, Granada, Spain
Sr. Andres Roldan Aranda

Date: 2022-07-29
Revision: 0.6 Sheet 1 of 1



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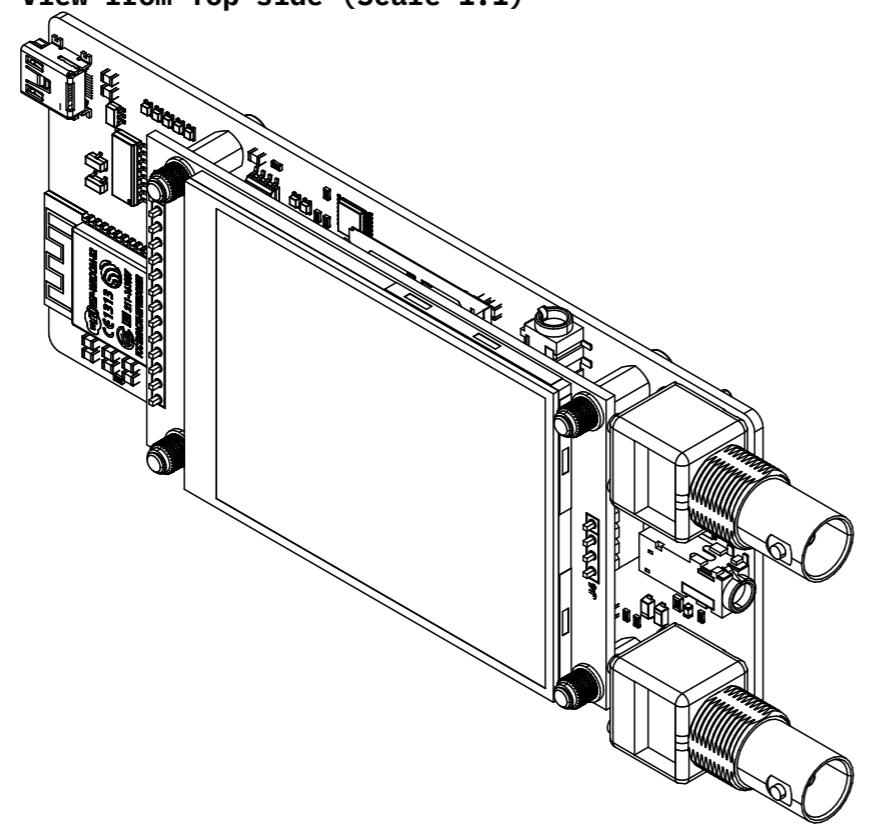
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REV STATUS OF SHEETS	REV							
SHEET								

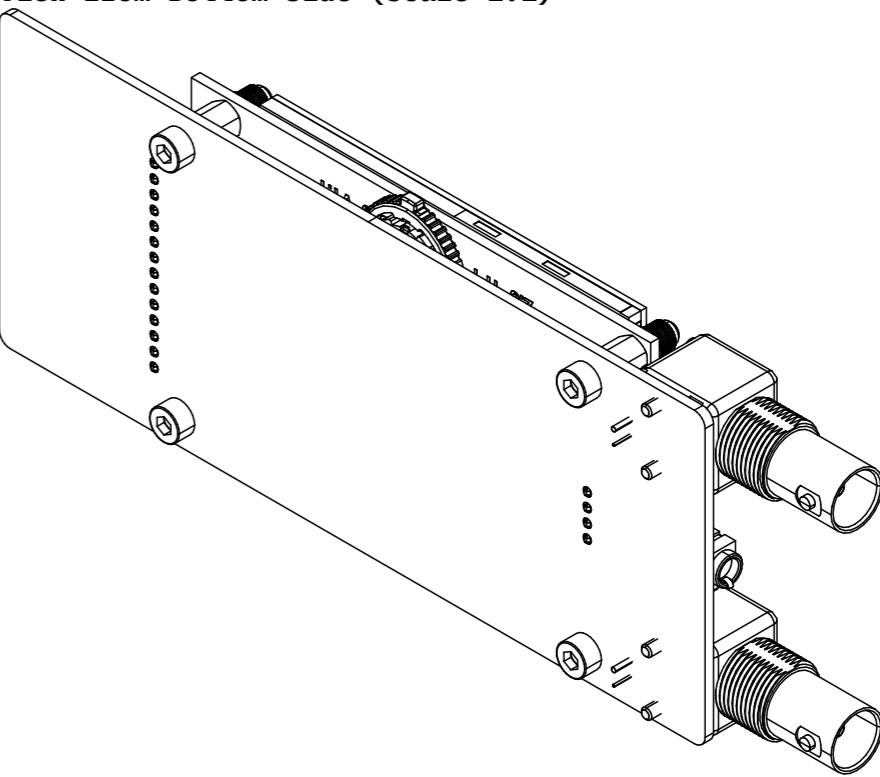
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

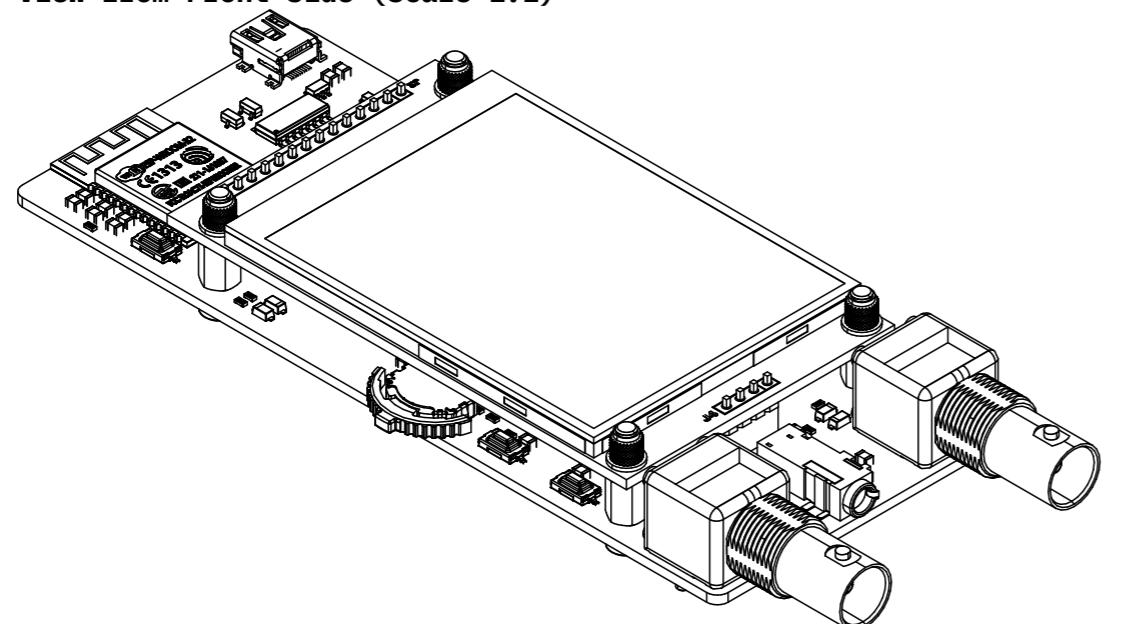
View from Top side (Scale 1:1)



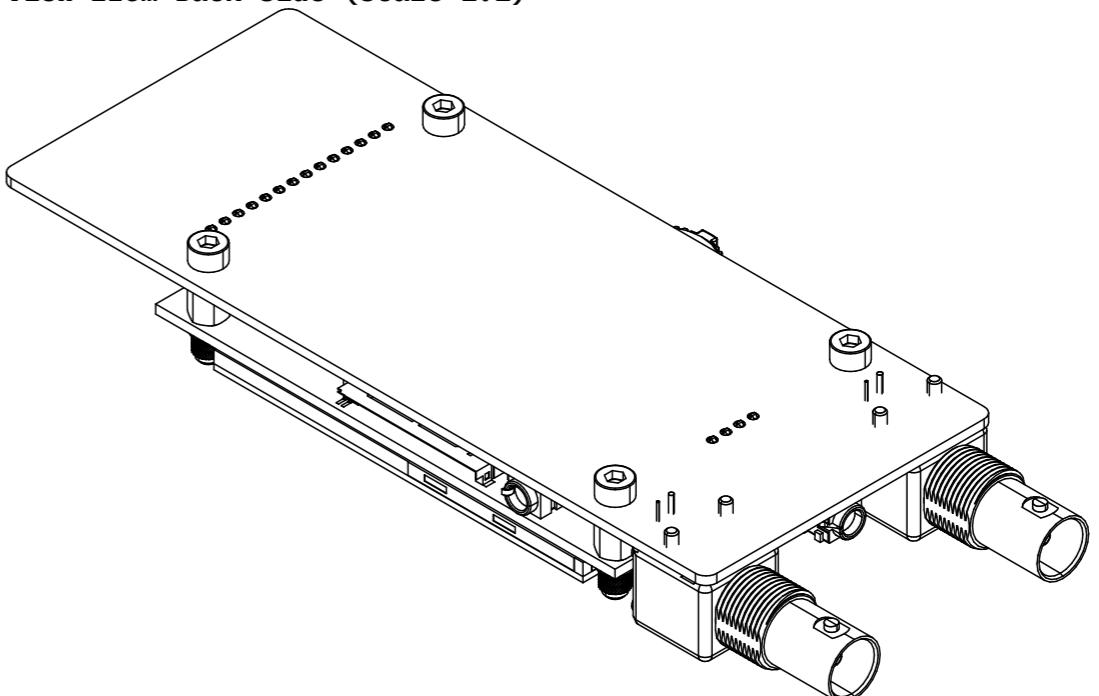
View from Bottom side (Scale 1:1)



View from Front side (Scale 1:1)



View from Back side (Scale 1:1)



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: Juan Del Pino Mena 2022-07-29

DESIGNER: Juan Del Pino Mena 2022-07-29

CHECKER: Andrés M. Roldán 2022-07-29

Reference Documents

BOM DOC: BOM/bill_of_materials

ASSY DOC: --

SCH DOC: SCH/*

NEXT ASSY

USED ON

PCB DOC: PCB/TIK_PCB.PcbDoc

APPLICATION

Dpto. Electrónica y
tecnología de computadores
University of Granada, Spain
C/ Fuente Nueva, s/n, 18001

DESIGN ITEM: Item

DESIGN ITEM REVISION: 6

TITLE: TREE INSPECTION KIT MECHANICAL DRAFTS

SIZE: A3

CAGE CODE: --

DWG NO: 1

SCALE: 1:1

FILE NAME: TIK_PCB.PCDBdwf

SHEET: 1 OF 5

REV: 6

THIRD ANGLE PROJECTION

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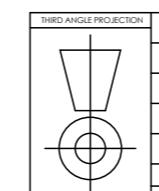
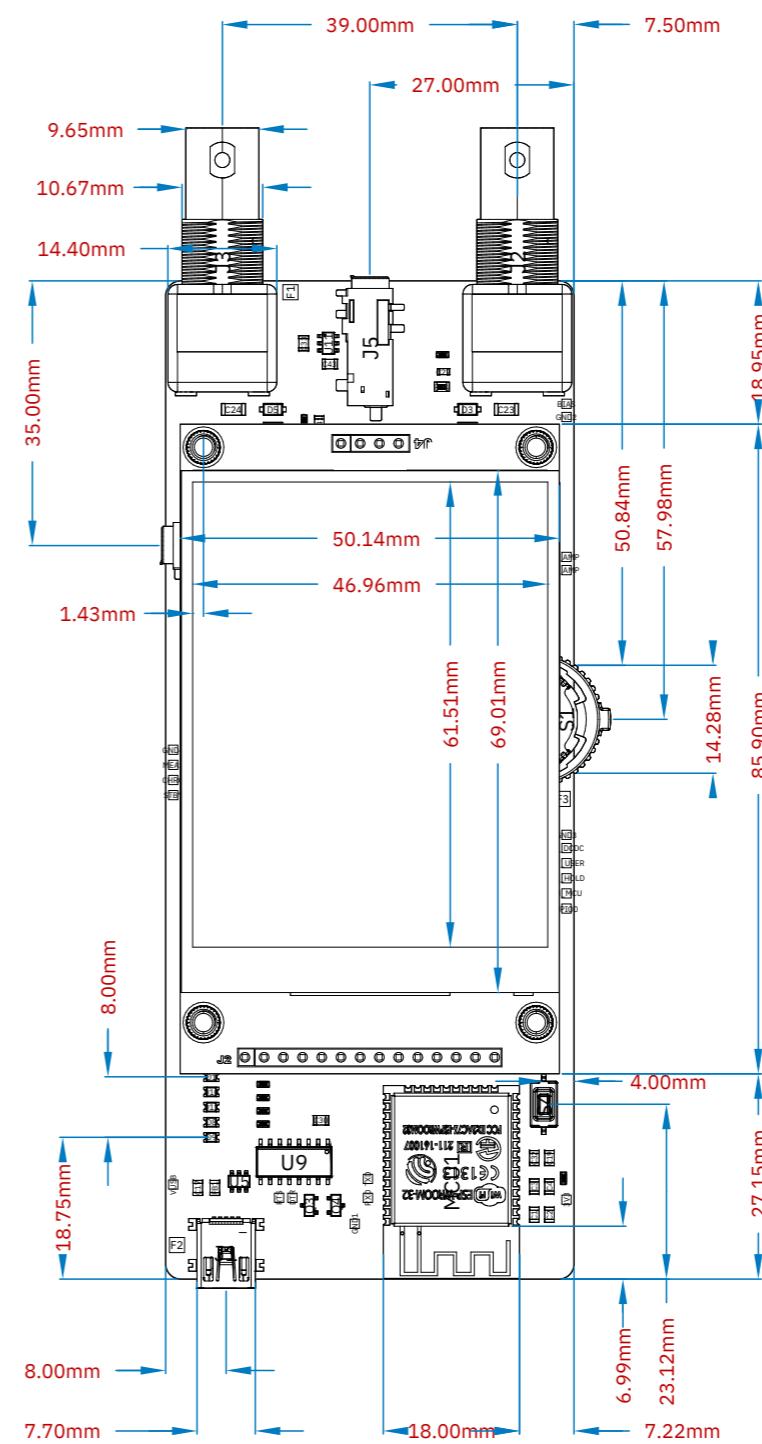
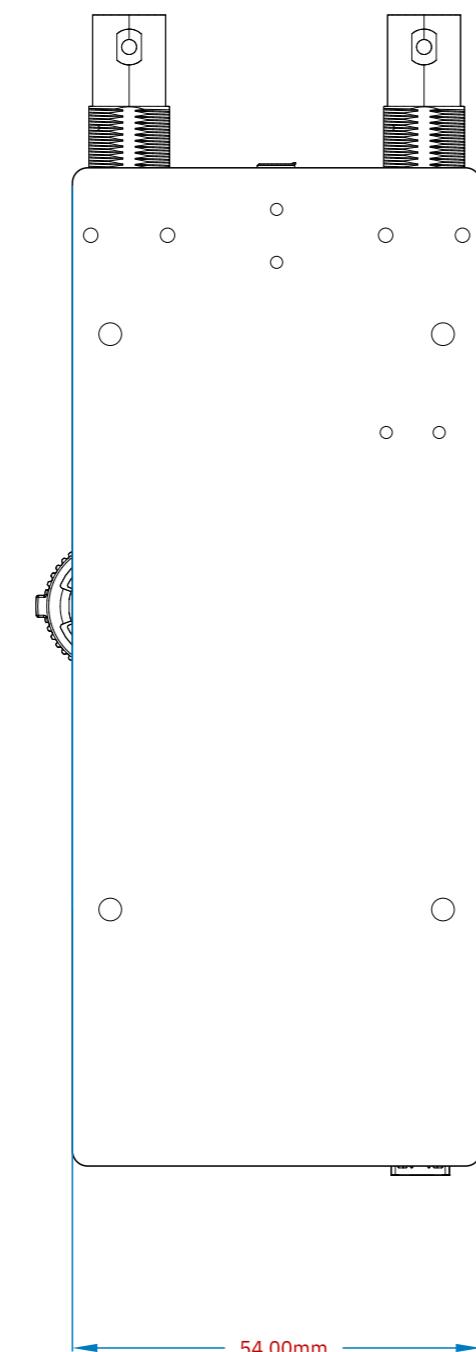
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PART NO:	=PCB_PART_NUMBER
APPROVALS	
ENGINEER:	Juan Del Pino Mena 20
DESIGNER:	Juan Del Pino Mena 20
CHECKER:	Andrés M. Roldán 20
	Reference Documents
BOM DOC:	BOM/bill_of_ma
ASSY DOC:	--
SCH DOC:	SCH/*
PCB DOC:	PCB/TIK_PCB.Pc

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tecnología de computadores
University of Granada, Spain
C/ Fuente Nueva, s/n, 18001

ITEM: .Item DESIGN ITEM REVISION: 6

TREE INSPECTION KIT MECHANICAL DRAFTS

CAGE CODE: DWG NO: R

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FILE NAME: TIK_PCB.PCBDwf SHEET: 2 OF

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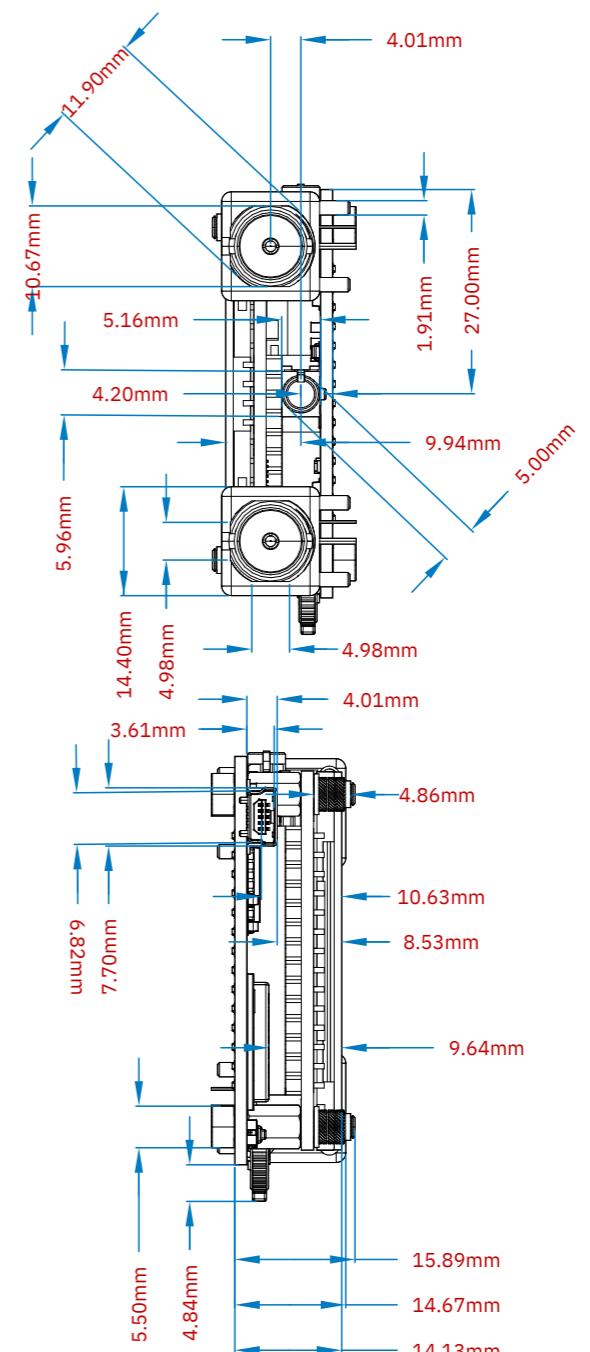
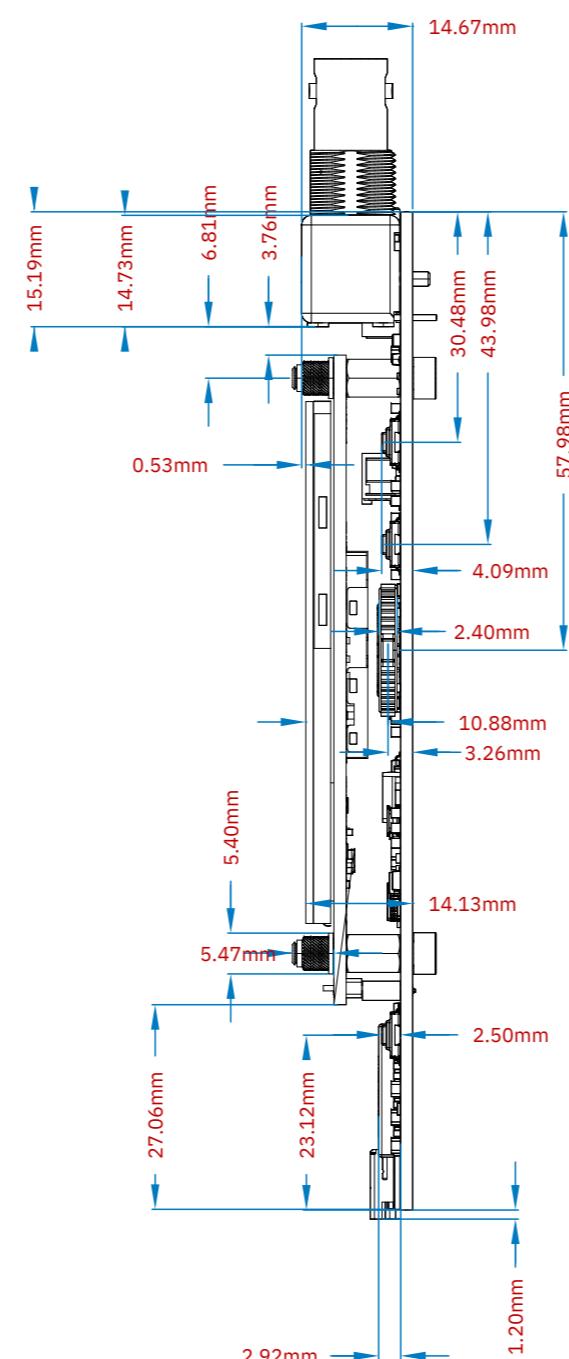
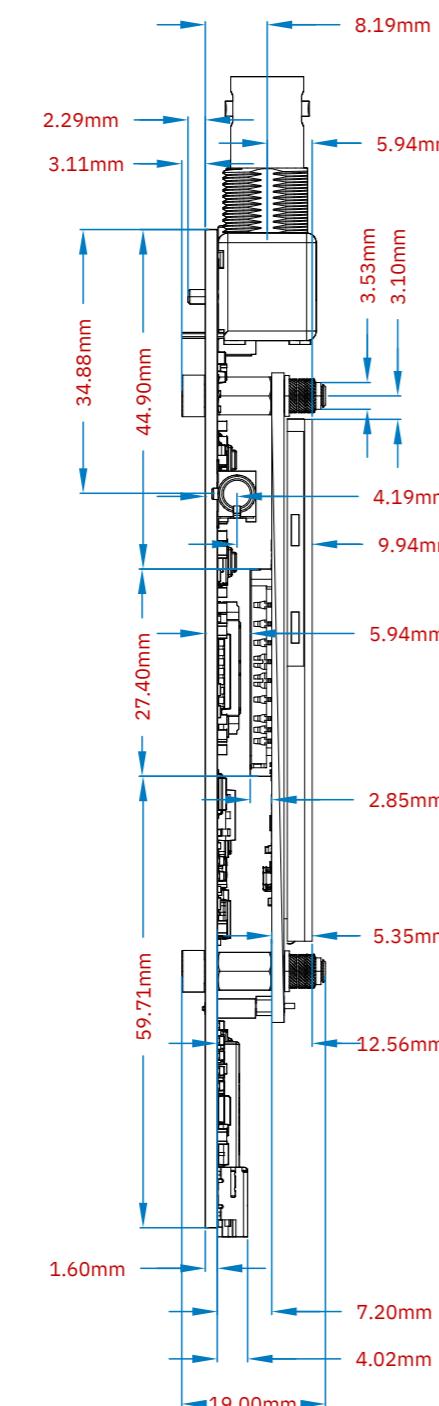
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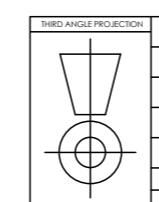
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2								
3								
4								
5								
6								



PART NO: =PCB_PART_NUMBER		APPROVALS	DATE	Dpto. Electrónica y tecnología de computadores University of Granada, Spain C/Fuente Nueva, s/n, 18001		
ENGINEER:	Juan Del Pino Mena	2022-07-29	DESIGNER:	Juan Del Pino Mena	2022-07-29	
CHECKER:	Andrés M. Roldán	2022-07-29	Reference Documents			
BOM DOC:	BOM/bill_of_materials			DESIGN ITEM:	Item	
ASSY DOC:	--			DESIGN ITEM REVISION:	6	
SCH DOC:	SCH/*			TITLE:	TREE INSPECTION KIT MECHANICAL DRAFTS	
PCB DOC:	PCB/TIK_PCB.PcbDoc			SIZE:	CAGE CODE:	DWG NO:
APPLICATION:				A3	--	
NEXT ASSY:	USED ON:	FILE NAME:	TIK_PCB.PCDBdwf			SCALE:
THIRD ANGLE PROJECTION		DWG NO:				3 OF 5
		REV:				6



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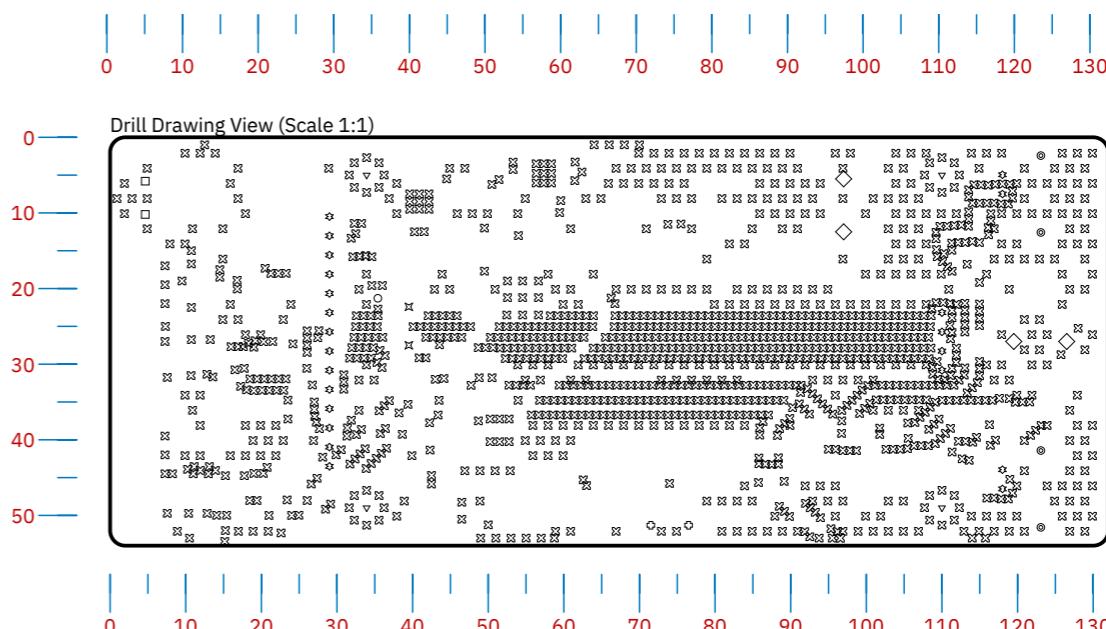
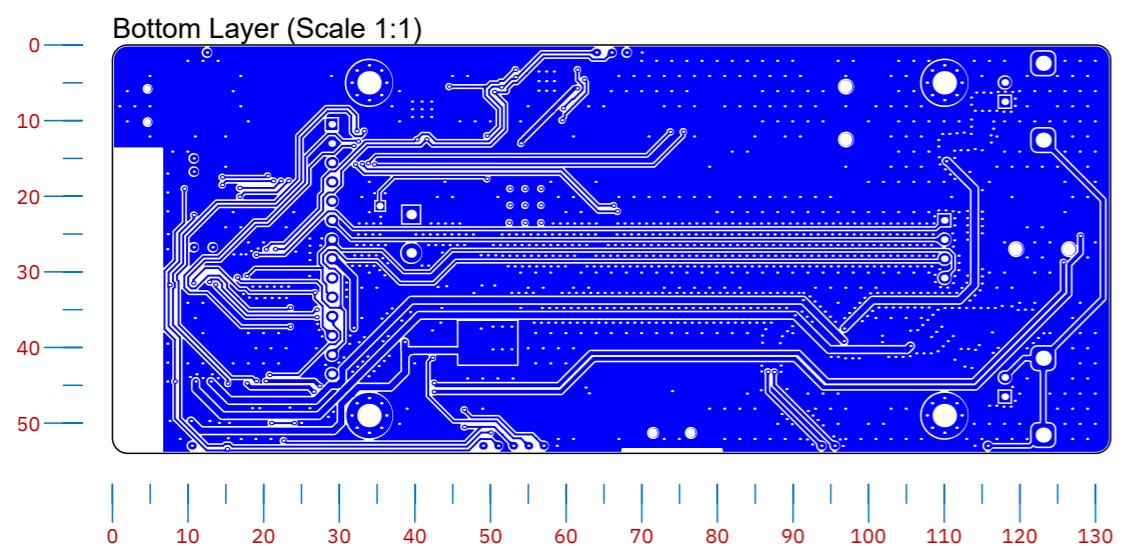
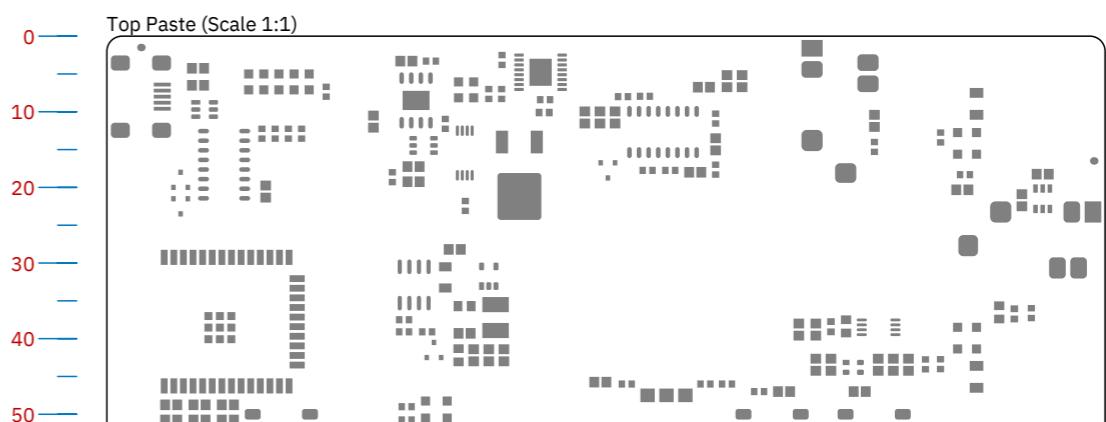
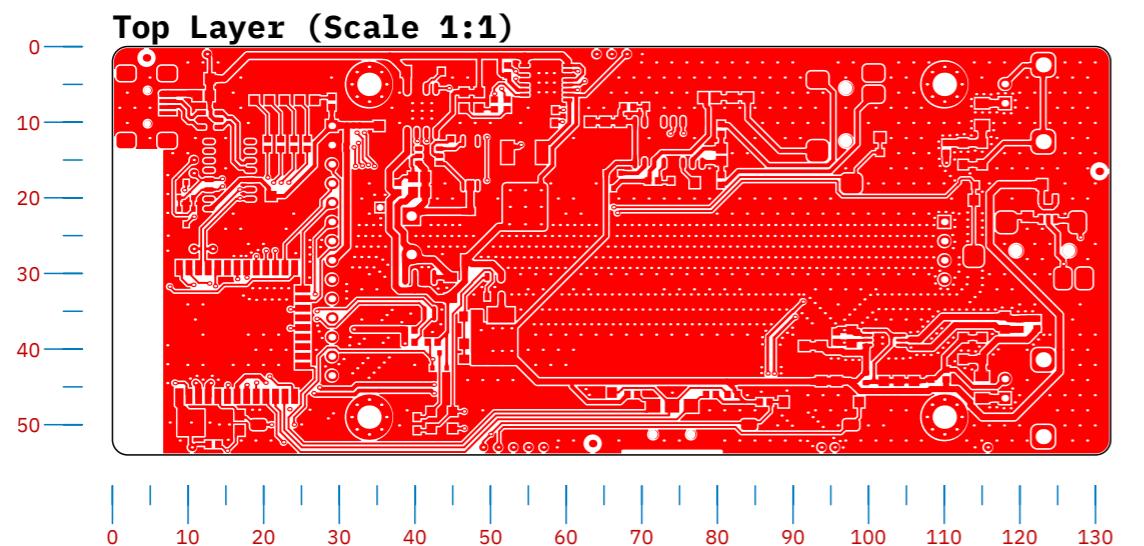
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REV STATUS OF SHEETS		REV				REVISIONS	
SHEET			ZONE	REV	DESCRIPTION	DATE	APPROVED



Layer Stack Legend

Material	Layer	Thickness	Dielectric Material Type	Gerber
Top Overlay			Legend	GTO
Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask GTS
Copper	Top Layer	0.04mm	Signal	GTL
		1.50mm	Dielectric	
Copper	Bottom Layer	0.04mm	Signal	GBL
Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask GBS
	Bottom Overlay		Legend	GBO
Total thickness: 1.59mm				

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
×	1330	0.30mm	Plated	
◊	22	0.89mm	Plated	
□	2	0.90mm	Non-Plated	
○	1	0.90mm	Plated	
◊	2	1.20mm	Non-Plated	
✗	2	1.27mm	Plated	
◇	4	1.70mm	Non-Plated	
◎	4	2.01mm	Plated	
▽	4	3.10mm	Plated	
1371 Total				

PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: Juan Del Pino Mena 2022-07-29

DESIGNER: Juan Del Pino Mena 2022-07-29

CHECKER: Andrés M. Roldán 2022-07-29

Reference Documents

BOM DOC: BOM/bill_of_materials

ASSY DOC: --

SCH DOC: SCH/*

NEXT ASSY USED ON

PCB DOC: PCB/TIK_PCB.PcbDoc

APPLICATION

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University of Granada, Spain
C/ Fuente Nueva, s/n, 18001

DESIGN ITEM: Item DESIGN ITEM REVISION: 6

TITLE: TREE INSPECTION KIT MECHANICAL DRAFTS

SIZE: CAGE CODE: DWG NO:

A3 --

SCALE: FILE NAME: PCB/TIK_PCB.PcbDoc

FILE NAME: TIK_PCB.PCDBdwf

SCALE: SHEET: 4 OF 5

REV: 6

A

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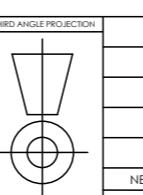
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A	B	C	D	E	F	G	H
					REV STATUS OF SHEETS	REV	REVISIONS
					SHEET		ZONE REV DESCRIPTION DATE APPROVED

Bill Of Materials

Designator	Value	Tolerance	Description	Type	Package Description	Quantity
C22	100pF	5% 10V	Ceramic cap size 0805		0603	1
C23, C24	100nF	10% 100V	Ceramic cap size 1206 C1206C104K1RACTU	X7R	1206	2
C25	22pF	5% 10V	Ceramic cap size 0805		0805	1
FB1, FB2	40mR, 3A 25%		0805, 60Ω, 3A, 25% SMT		0805	2
J5			3.5mm Jack 4-pole with normally closed switches			1
J6			3.5mm Jack 4-pole with normally closed switches		3.5mm Jack 4-pole with normally closed switches	1
L1	2.2uH	20% 2.2A	Shielded Power Inductor 2.2 uH 20% 2.2 A 50.4 mohms 3.11 A (sat) 60MHz 4018: 4x4x1.8mm		4x4x1.8mm	1
Q1			Dual N-channel Enhancement mode power MOSFET	Dual NMOS	TSSOP-8	1
Q2			MJD210 PNP BJT transistor DPAK (decawatt) 5A dc	PNP	DPAK (TO-252)	1
Q6			65 V, 100 mA PNP general-purpose transistor	PNP	SOT23	1
R1	150K	1%	Res size 0805 SMD mounting, low power Yageo-RC0805FR-07150KL		0805	1
R8	1.2K	1%	Res size 0603 SMD mounting, low power		0603	1
R14, R17	1M	1%	Res size 0805 SMD mounting, low power. Yageo-RC0805FR-071ML		0805	2
R23, R24	220	5%	Res size 0603 SMD mounting, low power		0603	2
R26, R27, R28, R29	150	5%	Res size 0603 SMD mounting, low power		0603	4
R36	22K	5%	Res size 0603 SMD mounting, low power		0603	1
RT1	10K		NTC THERMISTOR 10K for soldering a cable from the battery NTC		0603	1
U1			1.0MHZ, 2A STEP-DOWN DC-DC BUCK CONVERTER, with latch-off protection	Buck converter 2A	TSOT-25 (SOT-23-5)	1
U2	LDO 1.8V, 80mA		Fixed output lowdropout linear regulator. 1.8 V 80 mA	LDO	SC82-AB (SC70-4)	1
U6			LMV358IDGKR Dual OpAmp; low voltage rail to rail opamp; 2.7V to 5V Vss; ESD protection; MSOP-8 Package.	Dual OpAmp	MSOP-8	1
U10			HX711 load cell amplifier		SOP 16 L	1
U11			TPD3S014TDBVRQ1 ESD prot. & current limit		SOT-23-6	1
C1, C14, C34	47pF	5% 10V	Ceramic cap size 0805		0805	3
C2, C8, C13, C15, C17, C18, C20, C21, C27, C30, C31, C32, C33, C35, C37, C39, C40, C41, C42	100nF	10% 25V	Ceramic cap size 0805		0805	19
C3, C16, C26, C29, C36, C38	10uF	10% 25V	Ceramic cap size 0805		0805	6
C5	27pF	5% 10V	Ceramic cap size 0805		0805	1
C4, C6, C7, C9, C12, C43	22uF	20% 10V	Ceramic cap size 0805 CC0805MKX5R6BB226 Yageo MLCC 22uF 10V 20% X5R		0805	6
C10, C11, C19	1uF	10% 25V	Ceramic cap size 0805		0805	3
C28	470pF	5% 10V	Ceramic cap size 0805		0603	1
D2, D3, D4, D5, D12, D13			SURFACE MOUNT FAST SWITCHING DIODE	Rectifier, General purpose	SOD123	6
D1, D6, D8, D10			Low power LED color Green		GREEN	4
D7, D9, D11			Low power LED color Red		RED	3
J1			USB-MINI-B Female, Manufacturer PN/ID: 10033526-N3212LF		USB-Mini-B, Female	1
J2, J3			BNC coaxial female connector		BNC Female right angle	2
J4			ILI9341 TFT LCD Jumper pin headers., plus SD card reader pins	PCB Pin headers: F, 1x14 & 1x4	100 mil pitch	1
MCU1			- Transceiver; 802.11 b/g/n _Wi-Fi, WiFi, WLAN_, Bluetooth Smart Ready 4.x Dual Mode For Use With ESP-WROOM-32			1
Q3, Q4				N-Ch	SOT23	2
Q5			PMOS BSS84AK	P-Ch	SOT23	1
R18, R21, R22	4.7K	1%	Res size 0603 SMD mounting, low power		0603	3
R3	33K	1%	Res size 0805 SMD mounting, low power		0805	1
R4, R5, R25	0R	5%	Res size 0603 SMD mounting, zero-ohm OR Yageo RC0603JR-070RL		0603	3
R9, R10, R11, R12, R13, R35, R37, R38, R39, R40	10K	5%	Res size 0603 SMD mounting, low power		0603	10
R2, R6, R33, R34	100R	5%	Res size 0603 SMD mounting, low power		0603	4
R7, R15, R16	1K	5%	Res size 0603 SMD mounting, low power		0603	3
R19	1.5K	1%	Res size 0603 SMD mounting, low power		0603	1
R20	0.2R	1%	Res size 1206 SMD mounting, high power, shunt, current sense.		1206	1
R30, R31, R32	100K	5%	Res size 0603 SMD mounting, low power		0603	3
S1			SWITCH Multidirection Slide Push Button SMD TS-003	Thumb Switch		1
S2, S3, S4			Generic 2 pin button		SMD 2-pin	3
U3			DW01A One cell Li-Po/Li-ion Battery protection IC	Bat protection	SOT-23-6	1
U4			1A Standalone Linear Li-Ion Battery Charger with Thermal Regulation in SOP-8		Li-Po/Li-Ion charger	1
U5			Very low capacitance ESD protection		ESD Protection	1
U7			LTC4060EFE		TSSOP-16	1
U8			Zero-Drift, Bi-Directional CURRENT/POWER MONITOR with I2C. SOIC-8 (D) Package		Current sense	1
U9			USB to serial chip CH340C, integrated oscillator.		USB to UART	1

PART NO: =PCB_PART_NUMBER	APPROVALS	DATE	GRANASAT	Dpto. Electrónica y tecnología de computadores University of Granada, Spain C/ Fuente Nueva, s/n, 18001			
ENGINEER: Juan Del Pino Mena	2022-07-29	DESIGNER: Juan Del Pino Mena		2022-07-29	CHECKER: Andrés M. Roldán	2022-07-29	
Reference Documents				DESIGN ITEM:	Item	DESIGN ITEM REVISION:	6
BOM DOC: BOM/bill_of_materials				TITLE:	TREE INSPECTION KIT MECHANICAL DRAFTS		
ASSY DOC: --				SIZE:	CAGE CODE:	DWG NO:	
SCH DOC: SCH/*				A3	--		REV: 6
PCB DOC: PCB/TIK_PCB.PcbDoc			SCALE:	FILE NAME:	TIK_PCB.PCDBdwf	5 OF 5	
APPLICATION							



Line #	Designator	Value	Description	Quantity	fabGroup	fabOrder
C22		100pF	Ceramic cap size 0805	1		
C23, C24		100nF	Ceramic cap size 1206 C1206C104B226	2		
C25		22nF	Ceramic cap size 0805	1		
F81, F82		40mH, 3A 25%	0805_600_3A_25%_SMI	2		
J5			3.5mm Jack 4-pole with normally closed switches	1		
J6			3.5mm Jack 4-pole with normally closed switches	1		
L1		2.2uH	Resistor Power Inductor 2.2 uH 20%	1	DCDC converter	2
			2.2 A 50.4 ohms 3.11 A (sat) 60MHz 4081-84x18mm			
O1			N-channel Enhancement mode power MOSFET	1		
Q2			IRD210 PNP-BJT transistor DPAK (decawatt) 5A dc	1		
O6			16V, 100 mA PNP general-purpose transistor	1		
R1		150K	Res size 0805 SMD mounting, low power Yageo-R0805FR-07150KL	1		
R8		1.2K	Res size 0603 SMD mounting, low power	1		
R14, R17		1M	Res size 0805 SMD mounting, low power Yageo-R0805FR-071M	2		
R23, R24		220	Res size 0603 SMD mounting, low power	2		
R26, R27, R28, R29		150	Res size 0603 SMD mounting, low power	4		
R36		22K	Res size 0603 SMD mounting, low power	1		
R71		10K	NTC THERMISTOR 10K for soldering a cable from the battery NTC	1		
			1.0MHz, 2A STEP-DOWN DC-DC BUCK CONVERTER, with latch-off protection			
U2		ILO 1.8V, 80mA	High output lowdropout linear regulator 1.8V 80 mA	1		
U5			LMV358IDGKR Dual OpAmp: low voltage rail to rail opamp; 2.7V to 5V low ESD protection MSOP-8 package	1		
U10			HK711 load cell amplifier	1		
U11			TPD03914T0BV(R01) ESD prot. & current limit	1		
4	C1, C14, C34	47pF	Ceramic cap size 0805	3	Microcontroller, ILO Regulator & ILO bypass, [NoParam]	1, 12, [NoParam]
5	C2, C8, C13, C15, C17, C18, C20, C21, C22, C23, C31, C32, C33, C35, C37, C39, C40, C41, C42	100nF	Ceramic cap size 0805	19	Microcontroller, DCDC converter, ILO Regulator & ILO bypass, Charger for Li-Ion, USB Port, Buttons - Reset, Buttons - Boot, Buttons - Multipurpose, Signal conditioning, USB to UART & Programming, LCD TFT Display, Buttons - Powerup button, [NoParam]	1, 2, 12, 4, 11, 10, 9, 13, 3, 15, [NoParam]
6	C3, C16, C26, C29, C36, C38	10uF	Ceramic cap size 0805	4	Microcontroller, Charger for Li-Ion, Signal conditioning, Battery, [NoParam]	1, 4, 13, 7, [NoParam]
7	C5	27pF	Ceramic cap size 0805	1	DCDC converter	2
8	C4, C6, C7, C9, C12, C43	22uF	Ceramic cap size 0805 C00805MK5R6B6226 Yageo MLCC ZL0R 10V 20% X5R	6	[NoParam], DCDC converter, LDO Regulator & ILO bypass	[NoParam], 2, 12
9	C10, C11, C19	1uF	Ceramic cap size 0805	3	LDO Regulator & ILO bypass, Buttons - Reset	12, 11
12	C28	470pF	Ceramic cap size 0805	1	Charger for Ni-Mh	6
13	D2, D3, D4, D5, D12, D13		SURFACE MOUNT FAST SWITCHING DIODE	4	Signal conditioning, Buttons - multipurpose button	13, 3
14	D1, D6, D8, D10		Low power LED color Green	4	DCDC converter, Charging status, USB to UART & Programming	2, 5, 3
15	D7, D9, D11		Low power LED color Red	3	Charging status, USB to UART & Programming	5, 3
18	J1		USB-Mini-B female, Manufacturer PN#ID: 100255A-N24	1	USB Port	2
19	J3		BNC coaxial female connector	2		
20	J4		U9341 TFT LCD Jumper pin headers, plus SD card reader pins	1	LCD TFT Display	15
22	MCU1		+ Transceiver 802.11 b/g/n, Wi-Fi, WiFi, WLAN, Bluetooth Smart Ready & Dual Mode-For Use With ESP-WROOM-32	1	Microcontroller	1
25	Q3, Q4			2	USB to UART & Programming	3
26	Q5		PMOS FETSSAAK	1	Buttons - Powerup button	3
27	R18, R21, R22	4.7K	Res size 0603 SMD mounting, low power	3		
29	R3	33K	Res size 0805 SMD mounting, low power	1		
30	R4, R5, R25	0R	Res size 0603 SMD mounting, zero-ohm OR Yageo-C0603R-070RL	1	LDO Regulator & ILO bypass, Battery	12, 7
31	R9, R10, R11, R12, R13, R35, R37, R38, R39, R40	10K	Res size 0603 SMD mounting, low power	10		
32	R2, R6, R33, R34	100R	Res size 0603 SMD mounting, low power	4		
33	R7, R15, R16	1K	Res size 0603 SMD mounting, low power	3		
38	R19	1.5K	Res size 0603 SMD mounting, low power	1		
39	R20	0.2R	Res size 1206 SMD mounting, high power, shunt current sense	1		
40	R30, R31, R32	100K	Res size 0603 SMD mounting, low power	3		
42	S1		SW100 Multidirection Slide Push Button SMD-TS-003	1	Buttons - Multipurpose	9
43	S2, S3, S4		Generic 2 pin button	3	Buttons - Reset, Buttons - Boot, Buttons - Powerup button	11, 10, 3
46	U3		EN914 One cell Li-Po/Li-ion Battery protection IC	1	Charger for Li-Ion	4
47	U4		1A Standalone Linear Li-Ion Battery Charger with Thermal Regulation in SOP-8	1		
48	U5		Very low capacitance ESD protection	1	USB Port	2
50	U7		LTC4904ETP	1		
51	U8		Zero-Drift, Bi-Directional CURRENT/POWER MONITOR with I2C, SOC-8(D) Package	1		
52	U9		USB to serial chip CH340C, integrated oscillator	1	USB to UART & Programming	3