

A  
BACHELOR'S DEGREE IN TELECOMMUNICATION ENGINEERING

Bachelor's Thesis

ACADEMIC COURSE 2021/2022

# *Tree Inspection Kit*

## *handheld device*

AUTHOR:

Juan Del Pino Mena

SUPERVISED BY:

Sr. Andrés Roldán Aranda

DEPARTMENT:

Electronics and Computer Technology



UNIVERSIDAD  
DE GRANADA



Project title: TIK\_HandheldDevice.PrjPcb

Date: 2022-06-10 Revision: 0.6

Sheet 1 of 20

## A Introduction

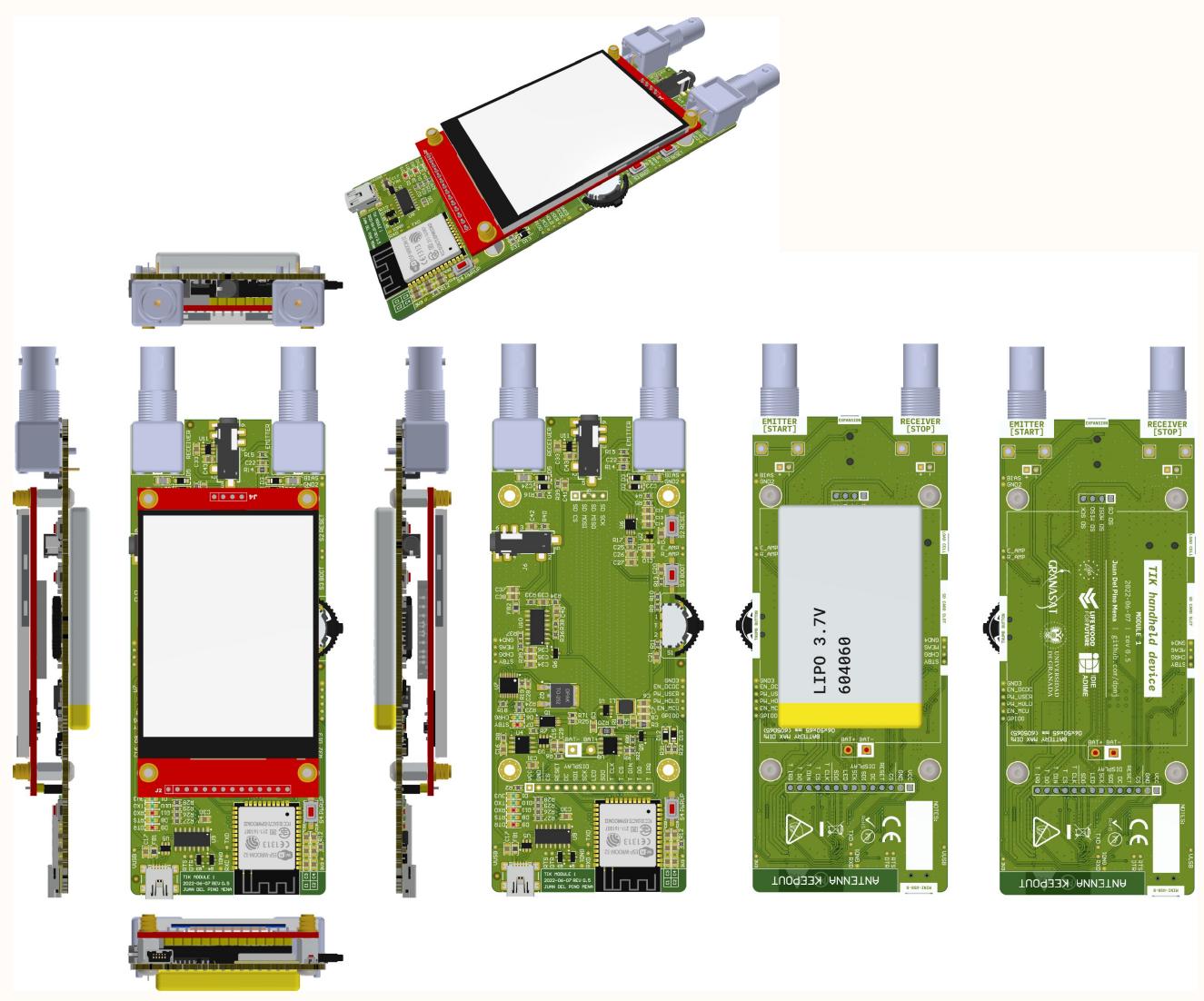
The present project has as main objective the development of a handheld electronic device capable of measuring the MOE of wood from silviculture so its properties can be characterised.

The device is equipped with the electronics needed to measure the delay between two signals which come from two piezoelectric sensors nailed into a piece of wood. It can be a standing tree, a tree trunk or a wood board.

The transit time of a mechanic wave travelling through the longitudinal axis of the wood is related to the material rigidity and consequently with its MOE.

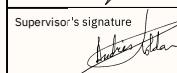
This device can also weight trunks to estimate its density by using a load cell.

At the right side you can see some renders of the PCB (version 0.5) which has been manufactured and tested.



## D Tree Inspection Kit handheld device

A device capable of determining the microsecond delay between 2 signals coming from piezoelectric probes nailed into a tree, trunk or wood board. This allows the indirect calculus of the Modulus of Elasticity in a non-destructive way.

Designer's signature  
  
Supervisor's signature  


Sheet title: **Introduction and PCB renders**

Project title: **TIK\_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

Date: **2022-06-10** Revision: **0.6**

Sheet 2 of 20

Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología  
de Computadores  
University of Granada  
C/Fuente Nueva, s/n, 18001  
Granada, Granada, Spain



## Index

SECTION	SHEET
0. Cover .....	1
1. Introduction & PCB 3D renders .....	2
2. Changelog & Index .....	3
3. PCB characteristics, trace width & vias .....	4
4. System block diagram .....	5
5. ESP32 MCU .....	6
6. Power rails .....	7
7. Battery and current sense .....	8
7.1. Charger variant #1: Ni-MH .....	9
7.2. Charger variant #2: Li-Ion .....	10
8. USB port .....	11
9. Auto programming .....	12
10. Buttons .....	13
10.1. Bootsel, reset, multipurpose .....	13
10.2. Power-up button .....	14
11. TFT LCD Display .....	15
12. Signal conditioning .....	16
12.1. Conditioning circuit .....	16
12.2. Circuit simulations .....	17
14. Expansion port .....	18
13. Load cell amplifier .....	19
15. Power budget & battery selection .....	20
16. Bill of materials .....	21
17. 3D PCB (PDF3D) .....	22
18. PCB layout prints .....	23
18.1. Top .....	23
18.2. Bottom .....	23
19. Mechanical schematics .....	24
19.1 Isometric views .....	24
19.2 Part views & measurements .....	25
19.3 Layer stackup, top/bottom, drills ..	26

## Changelog

### # Revision 0.6 | 2022-06-08

#### NEW

- Completed documentation (final version)
- Added a DCDC converter substitute

#### FIXED

- Changed 3D models to fit the real board.

### # Revision 0.5 | 2022-06-07 [MANUFACTURED VER.]

#### NEW

- Added multilayer connector to the battery
- Added a power budget & battery selection
- Adjusted the charging current resistor value of the TP4056.
- Added a expansion port and load cell connectors footprints. (4-pole jacks).
- Added support for jack plug switches.
- Applied JLCPCB design rules via .rul file.
- Tented vias for avoiding corrosion
- Added detailed explanation of trace design with Saturn PCB toolkit.
- Applied a nice format to the BOM.
- Added an introduction, updated renders.
- Added mechanical drawings with 3D isometric views, part drawing views, measurements, layer stackup, drills, etc.
- Added Gerber and NC Drills fabrication jobs for ordering PCB and its stencil.

#### FIXED

- Corrected LEDs' series resistors values
- Relocated the battery below the PCB. This makes the product wider, but solves a lot of space constraints.
- Removed VBIAS plane to avoid splitting planes, for EMI considerations.
- A lot of cosmetic improvements and corrections on PCB top & bottom overlays.
- Replaced logos and added new ones.
- Improved routing.
- A few cosmetic changes on the schematic sheets and cover.
- Removed rooms.
- NTC connector changed, now it's meant for soldering the NTC cable from a battery.

### # Revision 0.4 | 2022-05-22

#### NEW

- Added parameters for fabrication groups and fabrication order
- Added a Bill of Materials. The one in this document is simple. Refer to the manually configured BOM of this project.
- Added a PCB track legend and description for visible layers.
- Given more info about ESP32 pins.
- Added a precise block diagram.
- Added support for an extension port.
- Added a HX711-based load cell acquisition system.

#### FIXED

- Corrected I2C pins on the ESP32.
- Removed "same length" directive on UART and I2C nets.
- Improved routing.
- Removed via shielding on I2C traces.
- Solved all DRC warnings and errors.
- Avoided disrupting the ESP32's strapping pins default configuration during boot.
- Corrected a pin assignment error between the schematic symbol and the footprint of the MDJ210 PNP BJT transistor.
- Removed PCB cutouts.

### # Revision 0.3 | 2022-04-28

#### NEW

- Changed rotary encoder vertical for horizontal, side-placed, SMD type multipurpose 'thumb button'.
- Added a explanation of PCB trace widths.
- Adopted JLCPCB design rules.
- Full PCB component placement and routing, with no important DRC messages.
- Added silkscreen logos to the back of the PCB, as well as port markings, information and regulatory graphics: CE, WEEE, ESD sensitive warning and RoHS.

#### FIXED

- Changed numerical test point designators to net/rail names, to be quickly identified.
- Changed LEDs footprints.
- Corrected a faulty connection on the DW01A Lithium battery protection IC.
- The MCU has no longer the possibility to stop battery charging. This is because the ENABLE signals required by the chargers work on 5V and this could cause damage to the ESP32.

### # Revision 0.2 | 2022-04-23 [FIRST PCB]

#### NEW

- Schematic hierarchy and block diagram.
- Initial PCB layout
- Added a vertical rotary encoder. PCBLib contains a 90-degree alternative.
- Added an alternative Ni-MH charger.
- Added footprints for all neccessary components to the PCB Library.
- Added explanatory footprints and photos to schematic ICs.
- Added board mounting holes (making use of the TFT LCD module mounting hole positions)
- Added test points
- Added fiducials
- Added a power-up button
- Added net classes and parameter sets to most important nets: power, digital communications, analog signals, etc.

#### FIXED

- Removed errors in the lithium charger
- Removed errors in the adequation circuit
- Changed ESD USB Protection IC.
- Changed some adequation circuit values and made topology more clear.
- Revised all passive components values and sizes to match existing component disponibility.
- Corrected various pin definitions from the ESP32-WROOM-32D symbol

### # REVISION 0.1 | 2022-04-01 [FIRST VERSION]

#### NEW

- TFT LCD / SD card connections.
- First adequation circuit iteration
- LiPo battery charger with TP4056
- Auto programming circuit.

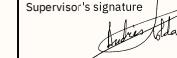
#### FIXED

--

## Revision history and document index

Detailed changelog and complete document sheets index.

All along the schematic pages, a sheet title and description will be written on this corner.

Designer's signature  
  
Supervisor's signature  


Sheet title: **Changelog and document index**  
Project title: **TIK\_HandheldDevice.PxjPcb**  
Desinger: **Juan Del Pino Mena**  
Date: **2022-06-10** Revision: **0.6** Sheet 3 of 20

Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología  
de Computadores  
University of Granada  
C/Fuente Nueva, s/n, 18001  
Granada, Granada, Spain



## SPI traces (@ 80 MHz, digital)

Er Effective  
Conductor Width (W)  
**0,254 mm**  
Conductor Height (H)  
**1,50 mm**  
Frequency (MHz)  
**80**

10-mil "default" trace width

Note:  
This calculator uses a complex formula presented by E. Hammarstad and O. Jensen, not the simplified formula presented by the IEC-2141A.

Wavelength Calculator  
Input Method  
 Frequency  
Frequency  
**80 MHz**  
Er Eff  
**2,8905**

Wavelength Information  
Period  
Speed of Light

Crossstalk Calculator  
Signal Rise Time  
**5 ns**  
Signal Voltage  
**3,3 V**  
Coupled Length  
**80 mm**  
Conductor Spacing (S)  
**0,254 mm**  
Conductor Height (H)  
**1,5 mm**

5 ns as a possible rise time of the SPI signal

$\lambda = \frac{C}{f * \sqrt{(ErEff)}}$

Wavelength Divide  
1/20 Wave Length  
**11.02083 cm**

CrossTalk Coefficient  
**0,24555 dB**  
Coupled Voltage  
**3,20801 Volts**

Er Effective Information

Send to Wavelength Calculator

△ SPI traces should not be longer than this result to avoid a transmission line. Note that this is rather a pessimistic value, as we are dividing the real wavelength by 20. Er Eff has been estimated with the expected fabrication characteristics.

Wavelength Calculator  
Input Method  
 Frequency  
Frequency  
**80 MHz**  
Units  
 MHz  
Er Eff  
**2,8905**

Wavelength Information  
Period  
Speed of Light

Crossstalk Calculator  
Signal Rise Time  
**5 ns**  
Signal Voltage  
**3,3 V**  
Coupled Length  
**80 mm**  
Conductor Spacing (S)  
**0,254 mm**  
Conductor Height (H)  
**1,5 mm**

5 ns as a possible rise time of the SPI signal

$\lambda = \frac{C}{f * \sqrt{(ErEff)}}$

Wavelength Divide  
1/20 Wave Length  
**11.02083 cm**

CrossTalk Coefficient  
**0,24555 dB**  
Coupled Voltage  
**3,20801 Volts**

Er Effective Information

△ As you can clearly see, a 2-layer, 1-6 mm height PCB is not great for signal integrity. We have great crosstalk between SPI lines. A common solution is to include GND copper between SPI lines with good connection to ground. This can be achieved by via shielding.

## Sensor analog signals (1 MHz max BW)

Wavelength Calculator  
Input Method  
 Frequency  
Frequency  
**1 MHz**  
Er Eff  
**3,0260**

Wavelength Information  
Period  
Speed of Light

Conductor Impedance  
Conductor Width (W)  
**0,8 mm**  
Conductor Height (H)  
**1,5 mm**  
Conductor Gap (G)  
**0,254 mm**

Formula Restrictions:  
 $0.1 < W/H < 2.0$   
 $T = 13um$   
? Help

Z<sub>0</sub>  
**60.6257 Ohms**

$\lambda = \frac{C}{f * \sqrt{(ErEff)}}$

Wavelength Divide  
1/20 Wave Length  
**861.70030 cm**

△ Er\_Eff calculated with a 0.8 mm wide trace. Trace length will not be a problem.

CrossTalk Calculator  
Signal Rise Time  
**2000 ns**  
Signal Voltage  
**3,3 V**  
Coupled Length  
**150 mm**  
Conductor Spacing (S)  
**0,254 mm**  
Conductor Height (H)  
**1,5 mm**

Estimated signal rise time. See simulations

CrossTalk Coefficient  
**-0,19079 dB**  
Coupled Voltage  
**0,03228 Volts**

△ Crosstalk and EMI can be a problem given the needed precision. Place these far from high-speed, with via shielding, as well as a good GND/power planes below.

## Via characteristics

Via Characteristics  
Via Hole Diameter  
**0,3 mm**  
Internal Pad Diameter  
**0,6 mm**  
Ref Plane Opening Diam  
**1,016 mm**  
Via Height  
**1,6 mm**  
Via Plating Thickness  
**0,035 mm**

Ref Plane  
Opening  
Via Pad  
Ref Plane  
Via Plating  
Via Height  
Via Plating Thickness

IPC-2152 with modifiers mode

Via Capacitance  
**0,5893 pF**  
Via DC Resistance  
**0,00086 Ohms**  
Power Dissipation  
**0,00326 Watts**

Via Inductance  
**1,2993 nH**  
Resonant Frequency  
**5751.849 MHz**  
Conductor Cross Section  
**0,0368 Sq.mm**

Via Impedance  
**46.956 Ohms**  
Step Response  
**30.4373 ps**  
Via Current  
**1.9514 Amps**

△ We are using only one type of via. We are far from the resonant frequency and the step response is very fast. Parasites are very low. In DC it can stand the required amount of current. Nevertheless, it should be always used various in parallel to ensure a low resistance path for power and returning currents.

## 0.254 mm (10 mil) traces

Conductor Characteristics  
Solve For  
 Amperage  
 Conductive Width  
Plane Present?  
 Yes  
Conductor Width  
**0,254 mm**  
Conductor Length  
**10 mm**  
Parallel Conductors?  
 No  
PCB Thickness  
**1,6 mm**

Options  
Solve For  
 Power Copper Weight  
 Parallel Conductors  
Units  
 Imperial  
 Metric  
Substrate Options  
Material Selection  
**FR-4 STD**

IPC-2152 with modifiers mode  
Etch Factor: 1:1  
Skin Depth  
**7,37972 um**  
Power Dissipation  
**0,03469 Watts**  
Conductor DC Resistance  
**0,01529 Ohms**

Skin Depth Percentage  
**21.08 %**  
Power Dissipation in dBm  
**7,4023 dBm**  
Conductor Cross Section  
**0,0129 Sq.mm**

Frequency  
 DC  
**80 MHz**  
Distance to Plane  
**1,5 mm**

Plating Thickness  
**4,6 µm**  
Temp Rise (°C)  
**10**  
Tg (°C)  
**130**

IPC-2152 with modifiers mode  
Etch Factor: 1:1  
Skin Depth  
**66.00620 um**  
Power Dissipation  
**0,03710 Watts**  
Conductor DC Resistance  
**0,01005 Ohms**

Skin Depth Percentage  
**100 %**  
Power Dissipation in dBm  
**7,6940 dBm**  
Conductor Cross Section  
**0,0196 Sq.mm**

Conductor Layer  
 Internal Layer  
 External Layer  
Information  
Total Copper Thickness  
70 um  
Via Thermal Resistance  
N/A

Print  
Solve!

△ Trace AC/DC characteristics in one centimetre of trace for a given frequency/DC and for a trace temperature increase of 10 °C over a standard ambient temperature of 25°C in a FR-4 dielectric.

0.254 mm (10 mil) is the default trace width. It's thin so we can save space, but has the worst DC characteristics and should not be used for power. These are the kind of traces used by the SPI bus. The skin depth is not optimal but this will depend on frequency and again, AC current is not a critical aspect here. It's a "good enough" approach.

## 0.35 mm traces

Conductor Characteristics  
Solve For  
 Amperage  
 Conductive Width  
Plane Present?  
 No  
Conductor Width  
**0,35 mm**  
Conductor Length  
**10 mm**  
Parallel Conductors?  
 No  
PCB Thickness  
**1,6 mm**

Options  
Solve For  
 Power Copper Weight  
 Parallel Conductors  
Units  
 Imperial  
 Metric  
Substrate Options  
Material Selection  
**FR-4 STD**

IPC-2152 with modifiers mode  
Etch Factor: 1:1  
Skin Depth  
**66.00620 um**  
Power Dissipation  
**0,03710 Watts**  
Conductor DC Resistance  
**0,01005 Ohms**

Skin Depth Percentage  
**100 %**  
Power Dissipation in dBm  
**7,6940 dBm**  
Conductor Cross Section  
**0,0196 Sq.mm**

Frequency  
 DC  
**1 MHz**  
Distance to Plane  
**1,5 mm**

Plating Thickness  
**4,6 µm**  
Temp Rise (°C)  
**10**  
Tg (°C)  
**130**

IPC-2152 with modifiers mode  
Etch Factor: 1:1  
Skin Depth  
**66.00620 um**  
Power Dissipation  
**0,03974 Watts**  
Conductor DC Resistance  
**0,00654 Ohms**

Skin Depth Percentage  
**100 %**  
Power Dissipation in dBm  
**7,9921 dBm**  
Conductor Cross Section  
**0,0301 Sq.mm**

Conductor Layer  
 Internal Layer  
 External Layer  
Information  
Total Copper Thickness  
70 um  
Via Thermal Resistance  
N/A

Print  
Solve!

△ 0.35 mm traces are used by connecting power pins to the power net in low-power components whose pins are very close together and cannot fit a trace of more width without breaking design rules.

This trace width has good properties and can be used even for low-speed analog signals if needed.

## 0.5 mm traces

Conductor Characteristics  
Solve For  
 Amperage  
 Conductive Width  
Plane Present?  
 No  
Conductor Width  
**0,5 mm**  
Conductor Length  
**10 mm**  
Parallel Conductors?  
 No  
PCB Thickness  
**1,6 mm**

Options  
Solve For  
 Power Copper Weight  
 Parallel Conductors  
Units  
 Imperial  
 Metric  
Substrate Options  
Material Selection  
**FR-4 STD**

IPC-2152 with modifiers mode  
Etch Factor: 1:1  
Skin Depth  
**66.00620 um**  
Power Dissipation  
**0,03974 Watts**  
Conductor DC Resistance  
**0,00654 Ohms**

Skin Depth Percentage  
**100 %**  
Power Dissipation in dBm  
**8,0912 dBm**  
Conductor Cross Section  
**0,0301 Sq.mm**

Frequency  
 DC  
**1 MHz**  
Distance to Plane  
**1,5 mm**

Plating Thickness  
**4,6 µm**  
Temp Rise (°C)  
**25**  
Tg (°C)  
**77,0**

IPC-2152 with modifiers mode  
Etch Factor: 1:1  
Skin Depth  
**66.00620 um**  
Power Dissipation  
**0,04325 Watts**  
Conductor DC Resistance  
**0,00385 Ohms**

Skin Depth Percentage  
**100 %**  
Power Dissipation in dBm  
**8,4359 dBm**  
Conductor Cross Section  
**0,0511 Sq.mm**

Conductor Layer  
 Internal Layer  
 External Layer  
Information  
Total Copper Thickness  
70 um  
Via Thermal Resistance  
N/A

Print  
Solve!

△ This is an optimal width in terms of area/specs for power delivery as it can withstand a lot of current (more than the system will continuously need) with low losses.

## 0.8 mm traces

Conductor Characteristics  
Solve For  
 Amperage  
 Conductive Width  
Plane Present?  
 No  
Conductor Width  
**0,8 mm**  
Conductor Length  
**10 mm**  
Parallel Conductors?  
 No  
PCB Thickness  
**1,6 mm**

Options  
Solve For  
 Power Copper Weight  
 Parallel Conductors  
Units  
 Imperial  
 Metric  
Substrate Options  
Material Selection  
**FR-4 STD**

IPC-2152 with modifiers mode  
Etch Factor: 1:1  
Skin Depth  
**66.00620 um**  
Power Dissipation  
**0,04325 Watts**  
Conductor DC Resistance  
**0,00385 Ohms**

Skin Depth Percentage  
**100 %**  
Power Dissipation in dBm  
**8,4359 dBm**  
Conductor Cross Section  
**0,0511 Sq.mm**

Frequency  
 DC  
**1 MHz**  
Distance to Plane  
**1,5 mm**

Plating Thickness  
**4,6 µm**  
Temp Rise (°C)  
**25**  
Tg (°C)  
**77,0**

IPC-2152 with modifiers mode  
Etch Factor: 1:1  
Skin Depth  
**66.00620 um**  
Power Dissipation  
**0,04325 Watts**  
Conductor DC Resistance  
**0,00385 Ohms**

Skin Depth Percentage  
**100 %**  
Power Dissipation in dBm  
**8,4359 dBm**  
Conductor Cross Section  
**0,0511 Sq.mm**

Conductor Layer  
 Internal Layer  
 External Layer  
Information  
Total Copper Thickness  
70 um  
Via Thermal Resistance  
N/A

Print  
Solve!

△ This trace width is employed by the analog signals to maintain good signal integrity at low line impedance.  
It can also be used as a power main bus for ensuring low power losses across a distance and for devices with a pulsed, aggressive power consumption such as the ESP32 and the LCD.

## Trace & via characteristics

Trace width based on results from PCB Toolkit by Saturn PCB Design INC.

Used JLPCB 2-layer, FR-4, 1.6 mm height, 35 um conductor height (1 oz/ft<sup>2</sup>) board characteristics as reference.

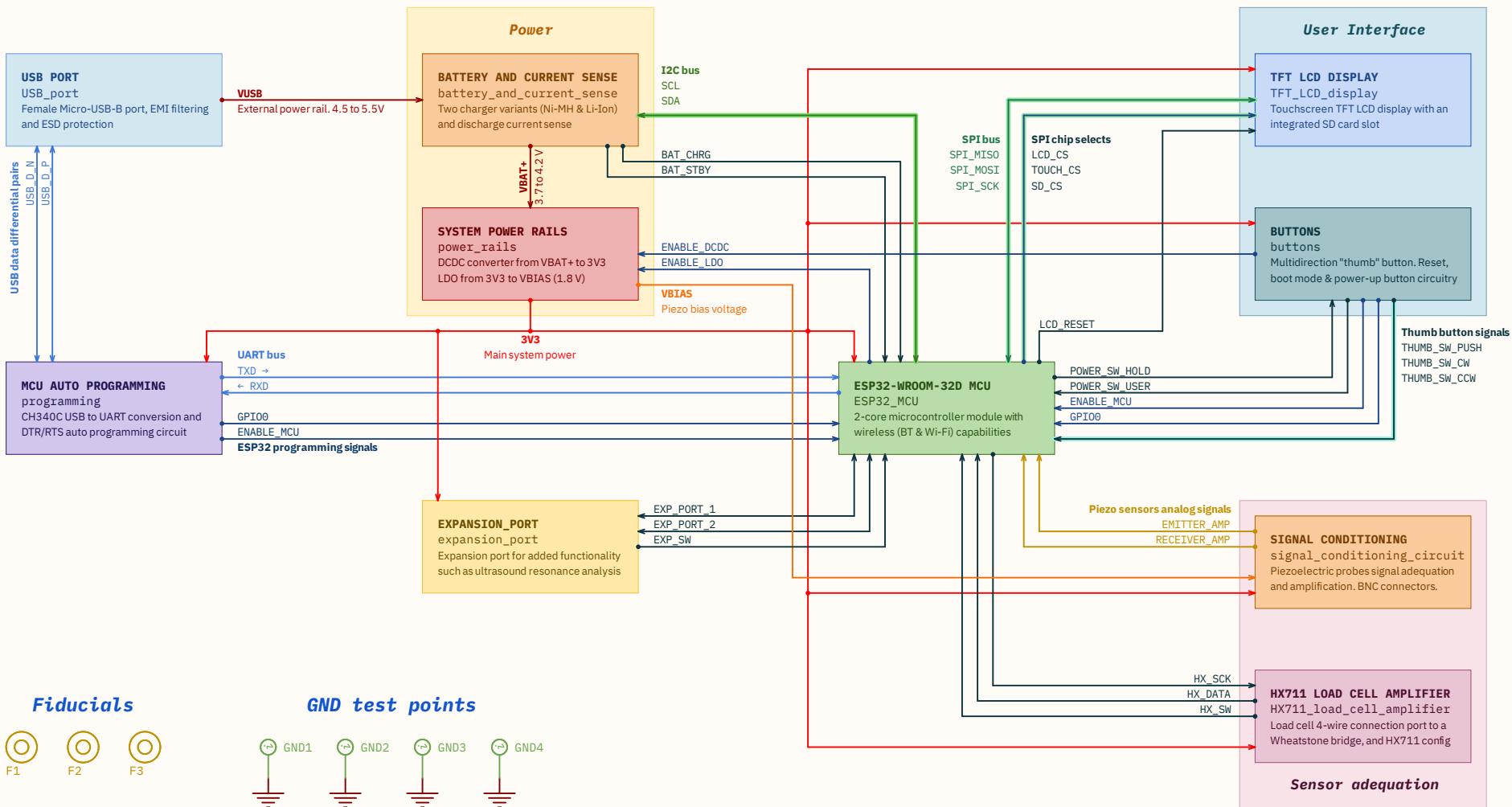
Designer's signature  
Supervisor's signature

Sheet title: **Trace width design**  
Project title: **TIK\_HandheldDevice.PjPcb**  
Designer: **Juan Del Pino Mena**  
Date: **2022-06-10** Revision: **0.6**

Sheet 4 of 20

Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología de Computadores  
University of Granada  
C/Fuente Nueva, s/n, 18001  
Granada, Granada, Spain





## System blocks organization and connections

The project's global block diagram. Arrows show how modules are interconnected and include net names. PCB includes 3 fiducials for fabrication purposes. GND test points are distributed along the PCB for easy access.

Designer's signature  
Supervisor's signature

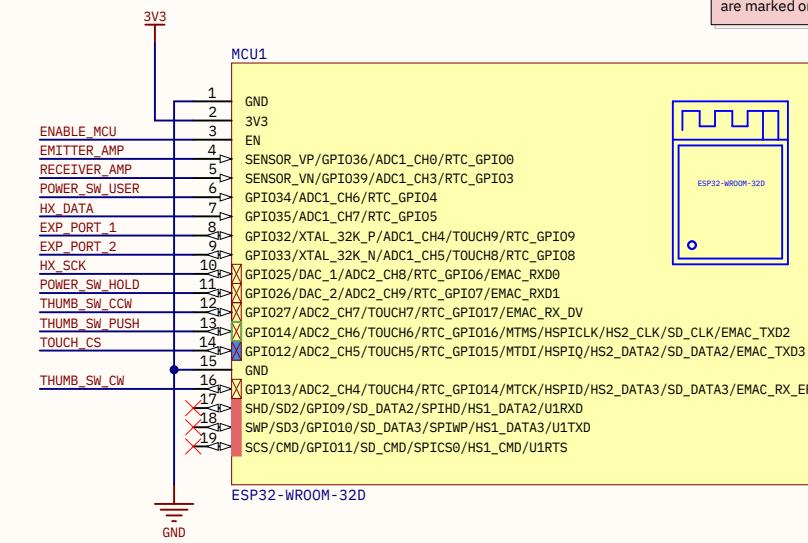
Sheet title: **System blocks organization and connections**  
Project title: **TIK\_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

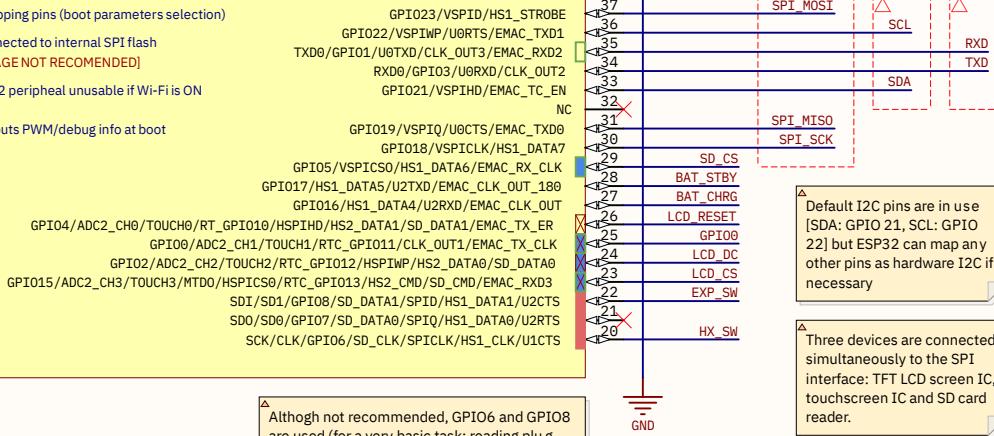
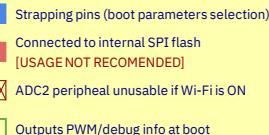
Date: **2022-06-10** Revision: **0.6** Sheet 5 of 20

Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología de Computadores  
University of Granada  
C/Fuente Nueva, s/n, 18001  
Granada, Granada, Spain





Some ESP32's pins behave in a way that prevent using them freely. They are marked on the legend below.



Although not recommended, GPIO6 and GPIO8 are used (for a very basic task: reading plug switches. Should be no problem).

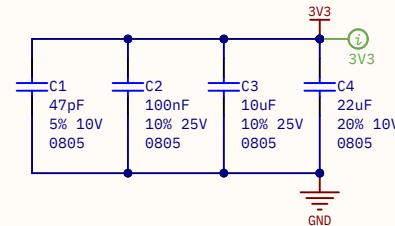
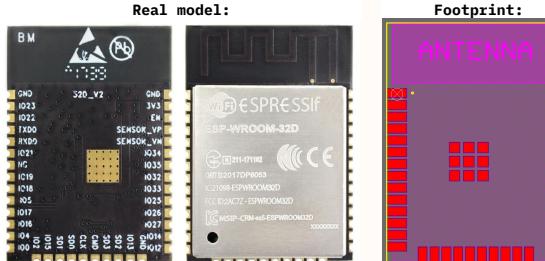
Strapping pins digital state are registered during reset and modify the boot sequence parameters according to the [ESP32 datasheet, table 5, page 21].

We must make sure that if pull-up/down resistors are connected to these pins (i.e for buttons) they do not alter the default configuration unintentionally.

Following the [ESP32-WROOM-32D datasheet, page 9] GPIO6 to GPIO11 (pins 17 to 22) will remain floating as they are connected to the integrated SPI flash memory and its usage is not recommended for other uses.

Also, the ADC2 peripheal is not usable while using Wi-Fi or Bluetooth and should be left unused if not necessary.

Digital I/O on those pins while on Wi-Fi or BT is fine.



Recommended bucket/bypass capacitors are 0.1 µF and 10 µF, ceramic, low ESR. Should be placed close to the chip and with short return paths.  
[ESP32-WROOM-32D datasheet, page 21]

Added one extra MLC 22  $\mu$ F electrolytic cap to filter current spikes during ESP32 RF usage and a small 47pF capacitor to be more effective filtering high frequencies

**ESP32-WROOM-32D MCU - Wi-Fi + Bluetooth module**

This module integrates an ESP32-D0WD chip, a 240 MHz, dual-core processor with Wi-Fi and Bluetooth capabilities. This sheet describes its hardware configuration and I/O pins.

Designer's signature  


---

Supervisor's signature  


Ch. 1000 - FORSÄKURERNA SÖR MÅN

Büro für Wirtschaftswissenschaften und Betriebswirtschaftslehre der Universität Regensburg

Designer: Juan Del Pino Mena

Date: 2022-06-19 Revision:

**Supervisor:**  
Sr. Andrés Roldán Aranda  
*Dpto. Electrónica y Tecnología de Computadores*  
*University of Granada*  
*C/ Fuente Nueva, s/n, 18001*  
*Granada, Granada, Spain*

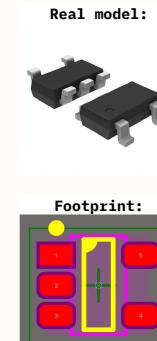
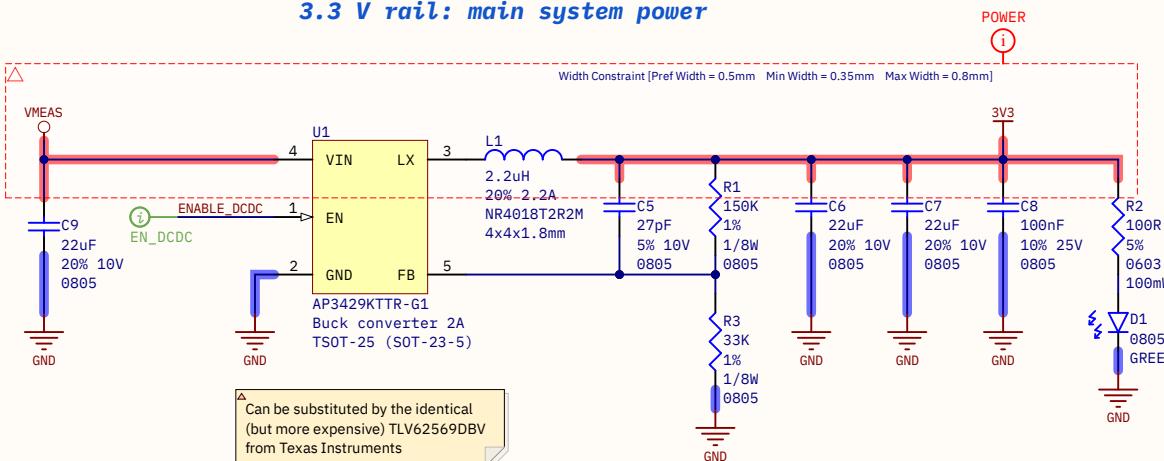


### **3.3 V rail: main system power**

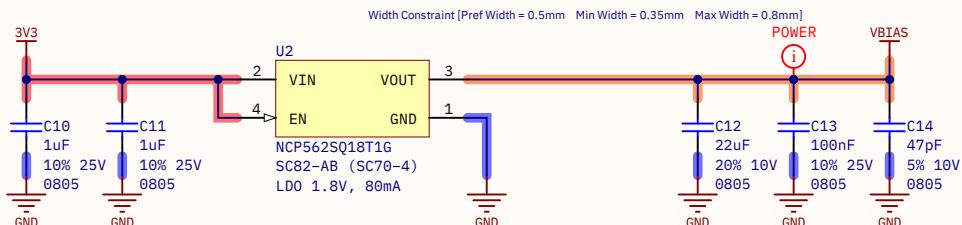
Typical Application Circuit. [AP3429/A  
datasheet, page 2]  
with some values modified as needed and/or  
part availability.  
Capacitors should be placed close to the chip  
and circuit should be traced in short loops.

Feedback voltage  $V_{FB}$  is regulated at 0.6 V.

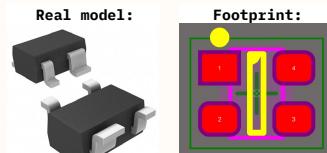
- Resistors are adjusted as a voltage divider. So, if 3.3V are needed at the converter output:
$$V_{FB} = 0.6V = V_{out} \cdot (R2)/(R1+R2)$$
Thus,  $R2 = 2/R1$
- Resistor values must be high (kOhms) in order to maintain a low power consumption on the feedback circuit.



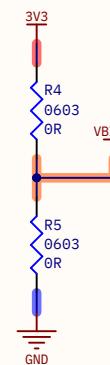
### **1.8 V rail: $V_{bias}$ for signal conditioning circuit**



Usage of multiple input capacitors to reduce ESR and ESL. Recommended  $C_{in}$  is 1  $\mu F$ . There are no recommended values for  $C_{out}$  but these 3 caps should probe more than enough for low ESR and ripple reduction at a wide frequency range. Datasheet specifies a typical 100  $\mu Vrms$  noise on  $V_{out}$ , somewhat high.



#### *Optional 1V8 rail bypass jumpers*



**IMPORTANT:**  
1V8 rail is bypassable by soldering these optional  
0-0HM resistors. This is for experimenting with  
different voltages and if it affects the overall  
performance of the adquisition circuit.

Do NOT connect both OR resistors at the same time or it will jump VCC and GND. And keep the LDO disabled at all times.

▲ This can also be used to insert a voltage divider, i.e.: if you want to reduce the rail voltage to VCC/2 you only have to add two  $>= 10\text{ K}\Omega$  0603 resistors. Just keep in mind that voltage won't be as stable as in a LDO as it will be greatly dependent on the load impedance.

If you do this, populate the LDO's output caps, so VBIAS it behaves as a small-signal GND.

## *Power rails*

Battery DC/DC step-down converter and Vbias for signal conditioning circuit. 3V3 is the main system power and can deliver upto 2 amps. VBIAS is only for polarization of the probes and won't drag much current.

Designer's signature	
Supervisor's signature	

Sheet title: **Power rails**

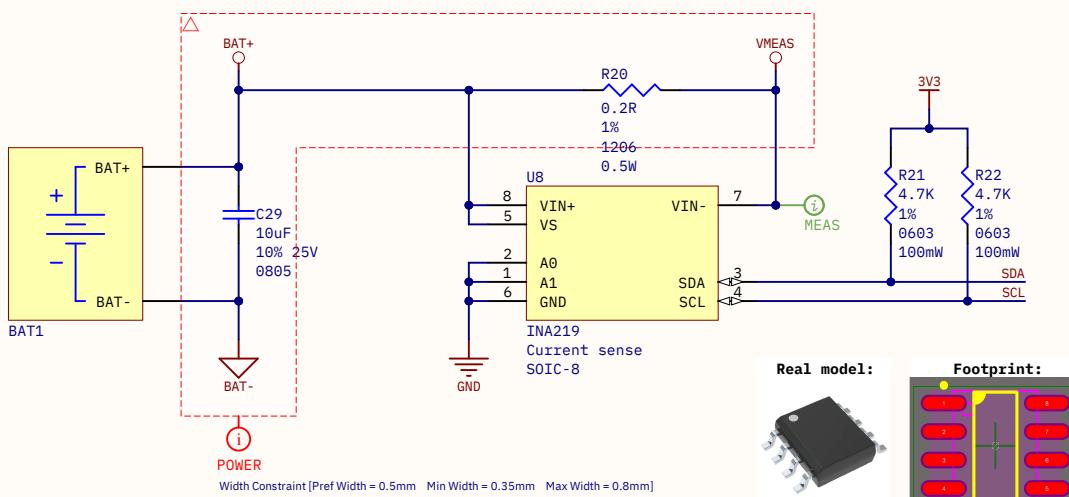
Designer: Juan Del Pino Mena

Date: 2022-06-10 Revision: 0.6

**Supervisor:**  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología de Computadores  
*University of Granada*  
C/ Fuente Nueva, s/n, 18001  
Granada, Granada, Spain



## Battery output current sense and voltage monitor. Charger selection jumper. Battery thermistor

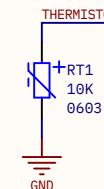


△ I2C bus termination resistors

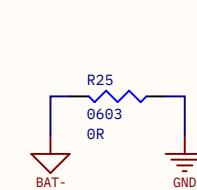
△ Device's I2C address: 100000 (0x20) [INA219 datasheet, page 10, table 2]

△ All the current that passes by the battery also goes through the current sense resistor. When it's positive means that the battery is discharging and when it's negative means that it's charging. INA219 also reports the battery voltage.

This way we can monitor via software the energy the battery receives and supplies, building a BMS (Battery Monitoring System)



△ Battery NTC Thermistor, shared by both chargers. If not integrated onto the battery itself (third cable), short the pads.



△ IMPORTANT: jumper for charger selection.

The battery connector is shared by the two possible chargers. However, on the Lithium charger BAT- is NOT connected to the system's global GND; but in the NiMH charger it is.

So, jump these pads ONLY IF USING THE NiMH charger.

## Battery charging circuit variants

△ Two circuit variants are implemented BUT NOT USED SIMULTENEOSLY. Only one must be populated at a time. The usage of one over the other will come by component disponibility.

**CHARGER VARIANT #1: NiMH**  
**battery\_charger\_Ni\_MH**  
 Charger to populate if battery chemistry is Nickel-Metal Hydride

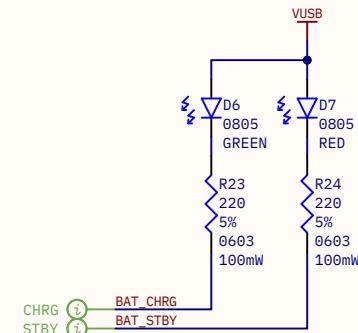
**CHARGER VARIANT #2: Li-Ion**  
**battery\_charger\_Li-Ion**  
 Charger to populate if battery chemistry is Lithium-Ion or Lithium-Polymer

## Charging status indicator

△ These signals come from both charging IC's.

△ They are status outputs that are normally on high impedance and they are pulled LOW when activated.

We can use these pins to turn on some LEDs and to notify the microcontroller of the charging status.



## Battery and current sense

Two circuit variants that will be implemented but not used simultaneously. The usage of one over the other will come by component disponibility. INA219 current sensor is independent and common for both systems.

Designer's signature  
 Supervisor:  
 Sr. Andrés Roldán Aranda  
 Dpto. Electrónica y Tecnología de Computadores  
 University of Granada  
 C/Fuente Nueva, s/n, 18001  
 Granada, Granada, Spain

Project title: TIK\_HandheldDevice.PjPcb  
 Supervisor:  
 Sr. Andrés Roldán Aranda  
 Dpto. Electrónica y Tecnología de Computadores  
 University of Granada  
 C/Fuente Nueva, s/n, 18001  
 Granada, Granada, Spain

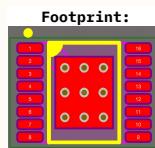
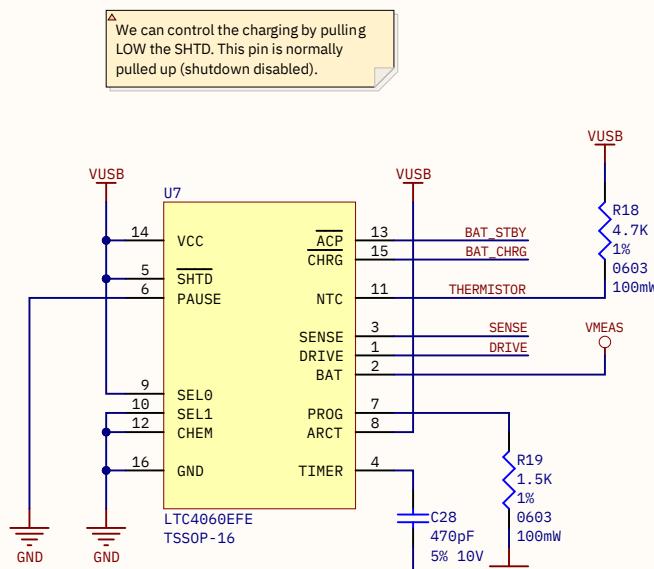
Supervisor's signature  
 Designer: Juan Del Pino Mena  
 Date: 2022-06-10 Revision: 0.6

Sheet title: Battery and current sense  
 Project title: TIK\_HandheldDevice.PjPcb  
 Designer: Juan Del Pino Mena  
 Date: 2022-06-10 Revision: 0.6

Sheet 8 of 20



## NiMH/NiCd battery charger IC



△ TIMER capacitor and PROG resistor program the charge Tmax (maximum charging time, a security measure). [LTC4060 datasheet, page 13]. These values should complete a full charge in at most 1 h 6'.

△ PROG resistor programs the maximum current that the battery will receive while charging. For 1.5 kOhm this is 0.93 A.

△ i.e.: a 1000 mAh battery will charge at approx 1C with this configuration, but can be insufficient time for a 3000 mAh one.

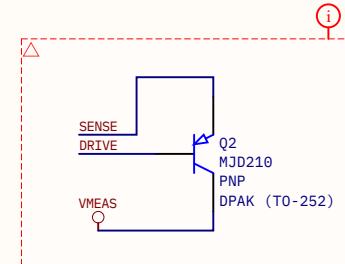
## Battery charging circuitry for Ni-MH

Battery charger circuit variant #1. By default the device uses a Nickel-metal hydride battery which are chemically and thermally more stable (and safer) than Lithium-based ones; at the cost of a lower charge/volume ratio.

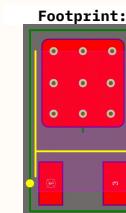
## External PNP BJT current driver

Width Constraint [Pref Width = 0.5mm Min Width = 0.35mm Max Width = 0.8mm]

POWER



△ DRIVE pin on the LTC4060 provides a controlled sink current that drives the PNP base. So, it's not necessary to have a base resistor.



Designer's signature  
Supervisor's signature

Sheet title: **Battery charger**

Project title: **TIK\_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

Date: **2022-06-10** Revision: **0.6**

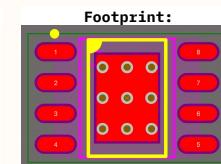
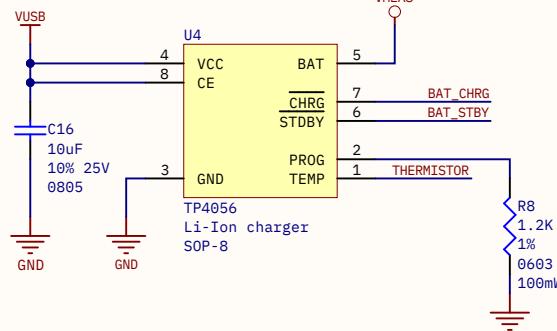
Sheet 9 of 20

Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología  
de Computadores  
University of Granada  
C/Fuente Nueva, s/n, 18001  
Granada, Granada, Spain



## Lithium battery charger IC

- △ The TP4056 datasheet recommends to connect a resistor of 0.2 to 0.5 Ohm between VUSB and its VCC pin. It does not explain why, but probably for chip temperature concerns.
- △ The TP4056 is only specified for charging single-cell Li-Ion batteries on its datasheet. However, many sites, forums and online stores list TP4056-based modules as compatible with both Li-Ion and Li-Po given the chemistry similarity. Take this with caution.
- △ Resistor in PROG regulates the maximum battery charging current. At 2 kOhm, this is 580 mA. At 1 kOhm, it is > 1 A. Change according to battery capacity. [TP4056 english datasheet, page 3]
- △ TEMP expects a NTC thermistor (of unspecified value). On some Lithium-Ion batteries this NTC can be integrated on the package.

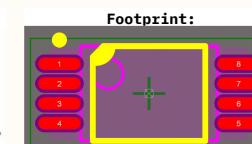
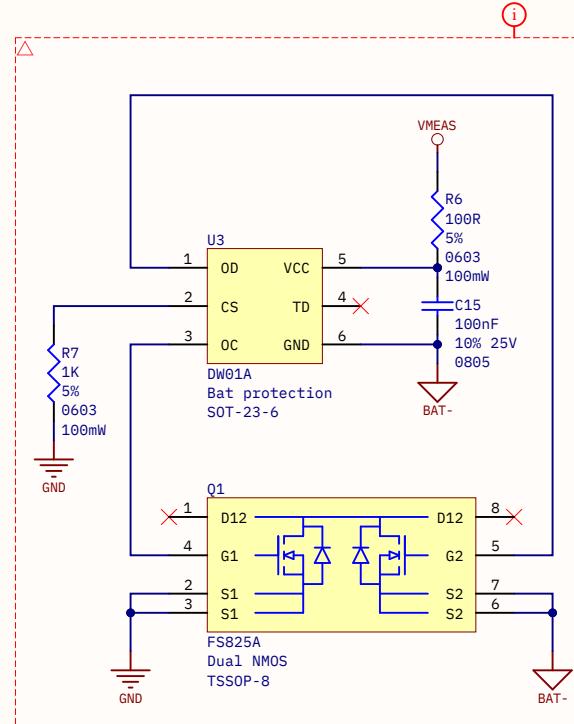


△ This device will get hot, and has a thermal pad to dissipate to PCB GND plane

## Lithium battery protection

Width Constraint [Pref Width = 0.5mm Min Width = 0.35mm Max Width = 0.8mm]

POWER



## Battery charging circuitry for Li-Ion

Battery charger circuit variant #2. Li-Ion and Li-Po batteries offer much more power density at the cost of instability. This circuit must NOT be placed if the Ni-MH charger is present on the board (and vice-versa).

Designer's signature  
Supervisor's signature

Sheet title: **Battery charger**

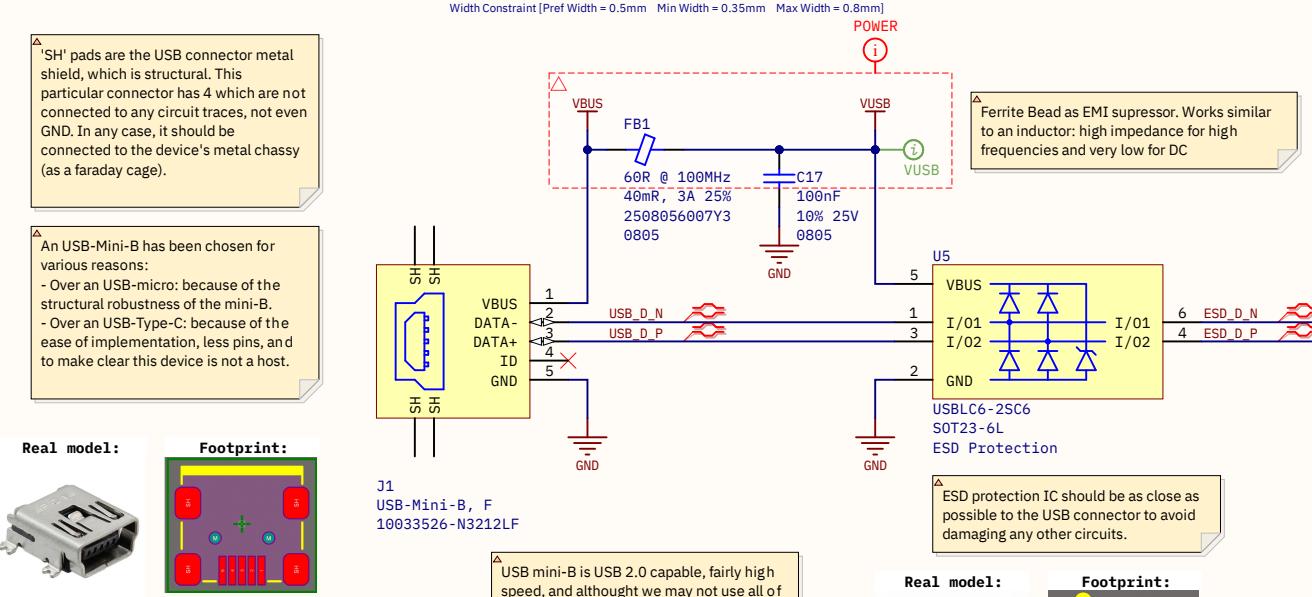
Project title: **TIK\_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

Date: **2022-06-10** Revision: **0.6** Sheet 10 of 20

Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología de Computadores  
University of Granada  
C/Fuente Nueva, s/n, 18001  
Granada, Granada, Spain





## USB connector and ESD protection circuit

USB is used as a programming interface, as well as a power source for the charging circuit. Since it's an external connector, it needs to have a protection circuit against electro-static discharge (ESD) and noise.

Designer's signature

Supervisor's signature

Sheet title: **USB connector and ESD protection circuit**

Project title: **TIK\_HandheldDevice.PxjPcb**

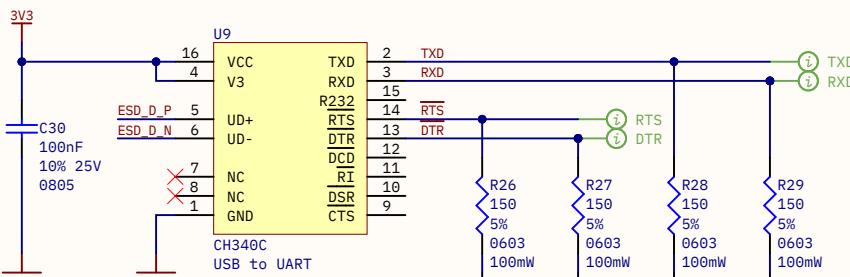
Designer: **Juan Del Pino Mena**

Date: **2022-06-10** Revision: **0.6** Sheet 11 of 20

Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología  
de Computadores  
University of Granada  
C/Fuente Nueva, s/n. 18001  
Granada, Granada, Spain



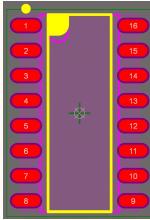
## USB to UART conversion



Real model:



Footprint:

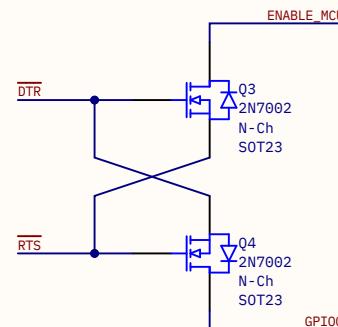


These LEDs serve as a visual testimony of UART communication and help during debugging.

If they drag too much current they can be used with 1 kΩ resistors or be completely disconnected.

Should not be present on a commercial product.

## Auto programming circuit



ESP32 GPIO00 is a Strapping pin. Strapping pins modify the device's boot mode during chip reset. GPIO00 is pulled up during reset by default. ENABLE\_MCU is pulled up by an external pullup resistor

When GPIO00 is HIGH, it boots from internal SPI memory, but when it's LOW the boot sequence changes to 'Download' and we can upload a program to the MCU.

[ESP32 Datasheet, section 2.4, pages 19-20]

## Circuit truth table

DTR	RTS	ENABLE_MCU	GPIO00
0	0	1	1
0	1	1	0
1	0	0	1
1	1	1	1

\*(DTR, RTS active low)

## USB to UART and MCU programming

This circuit allows a computer to reprogram the ESP32 via USB so it can be reprogrammed. This is possible by sending RTS and DTR signals with a determined timing so the device enters an alternative boot mode.

Designer's signature  
Supervisor's signature

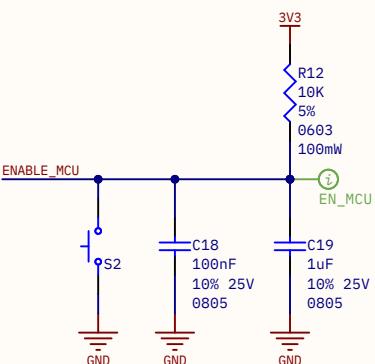
Sheet title: **USB to UART and MCU programming**  
Project title: **TIK\_HandheldDevice.PxjPcb**  
Desinger: **Juan Del Pino Mena**  
Date: **2022-06-10** Revision: **0.6**

Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología  
de Computadores  
University of Granada  
C/Fuente Nueva, s/n, 18001  
Granada, Granada, Spain



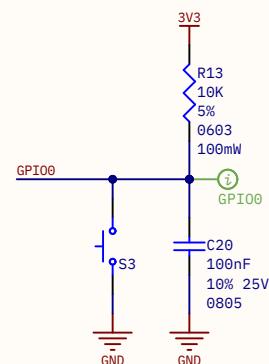
## Reset

To ensure power stability to the microcontroller during powerup, this RC filter introduces a delay on the ENABLE pin. Usual values are  $10\text{ k}\Omega$ ,  $1\text{ }\mu\text{F}$  ( $\tau = 10\text{ ms}$ ,  $t_{\{10-90\}} = 22\text{ ms}$ ). [ESP32-WROOM-32D datasheet, page 22]



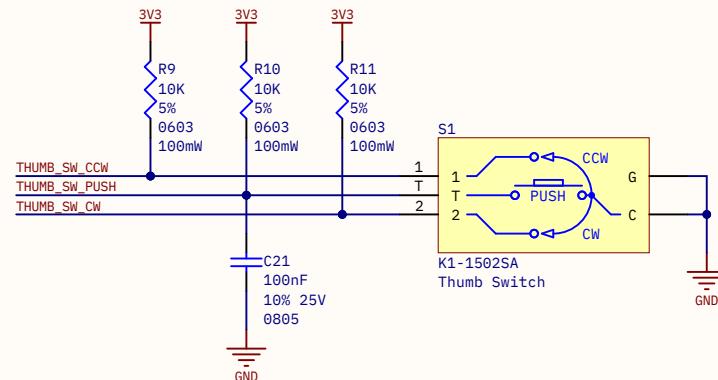
## Boot mode selection (debug)

Allows to force 'Download' boot sequence  
Same design as in ESP32 DevKit boards.  
100 nF cap are for debouncing and should be placed close to the buttons



## Multidirection 'thumb' button (UI navigation)

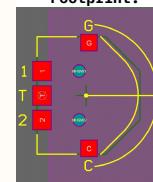
Horizontal SMD device, multi-directional / muti-function rotary slider button.  
Accessed from the right side.



Real model:



Footprint:



## Buttons

TIK buttons. Some of them are meant for debugging like boot mode selection and reset, and will not be accessible to the end user. The power-up button and the "thumb" button are meant to be part of the UI.

Designer's signature  
Supervisor's signature

Sheet title: **Buttons**  
Project title: **TIK\_HandheldDevice.PjPcb**

Desinger: **Juan Del Pino Mena**

Date: **2022-06-10** Revision: **0.6** Sheet 13 of 20

Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología  
de Computadores  
University of Granada  
C/Fuente Nueva, s/n. 18001  
Granada, Granada, Spain



A

B

C

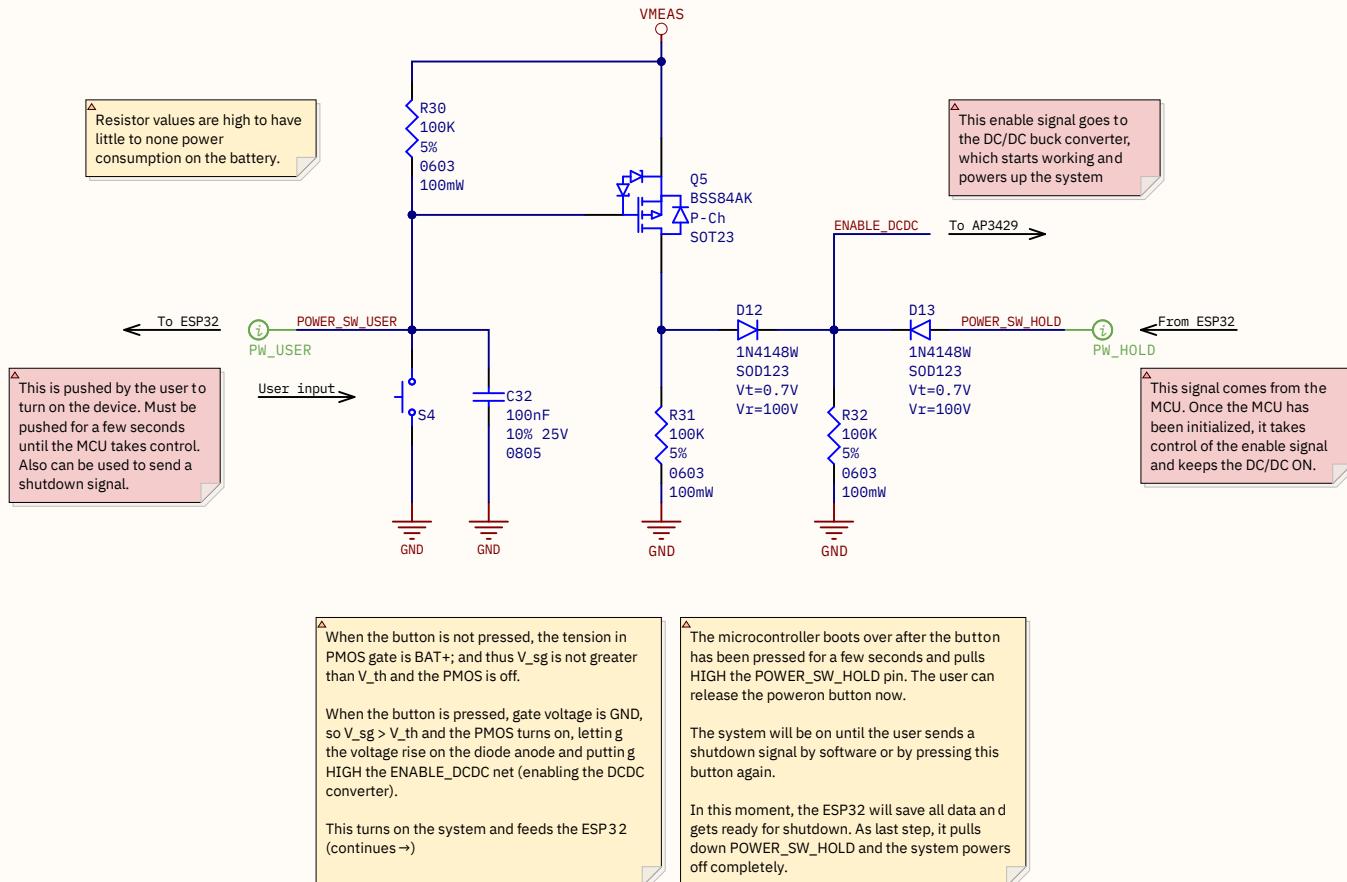
D

A

B

C

D



## Powerup button

This circuit avoids using a power-up switch, which can shutdown the device without prior warning. The user pushes a button during a couple of seconds, in which the ESP32 will boot and keep the system on until a shutdown signal is sent.

Designer's signature  
Supervisor's signature

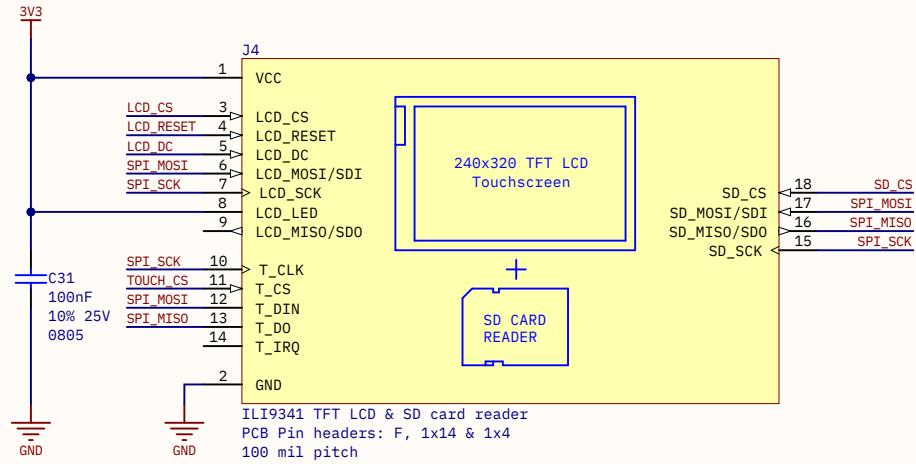
Sheet title: **Powerup button**  
Project title: **TIK\_HandheldDevice.PjPcb**

Desinger: **Juan Del Pino Mena**

Date: **2022-06-10** Revision: **0.6** Sheet 14 of 20

Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología de Computadores  
University of Granada  
C/Fuente Nueva, s/n, 18001  
Granada, Granada, Spain





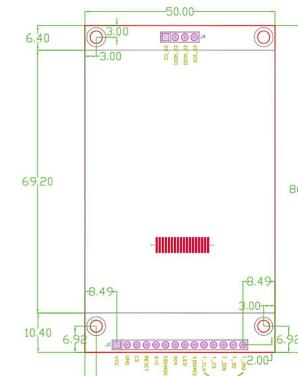
Real model:



Footprint:



As ILI9341 2.8" TFT LCD module has the bigger footprint t and needs mechanical support. Our PCB inherits its mounting holes position.



## LCD TFT touchscreen & SD card reader

TIK uses an ILI9341 2.8" TFT LCD display module as a graphic user interface. This module has touchscreen capabilities and also integrates a SD card reader on one of its sides. All three elements are managed via SPI.

Designer's signature  
Supervisor's signature

Sheet title: **LCD TFT touchscreen & SD card reader**

Project title: **TIK\_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

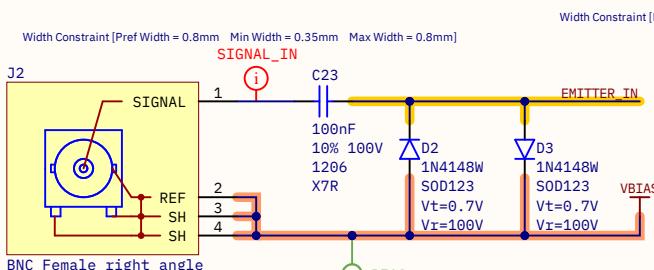
Date: **2022-06-10** Revision: **0.6**

Sheet 15 of 20

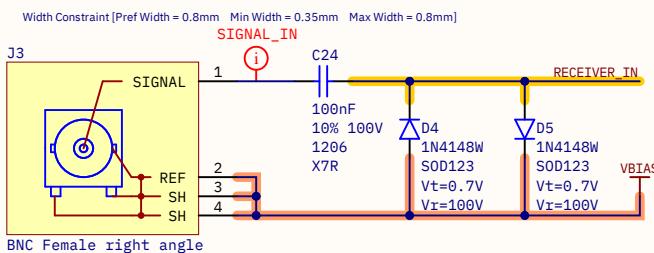
Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología de Computadores  
University of Granada  
C/Fuente Nueva, s/n. 18001  
Granada, Granada, Spain



A



Width Constraint [Pref Width = 0.8mm Min Width = 0.35mm Max Width = 0.8mm]  
Matched Net Lengths [Tolerance = 25mm]

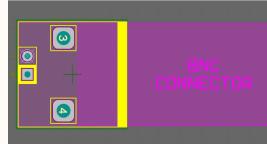


Width Constraint [Pref Width = 0.8mm Min Width = 0.35mm Max Width = 0.8mm]

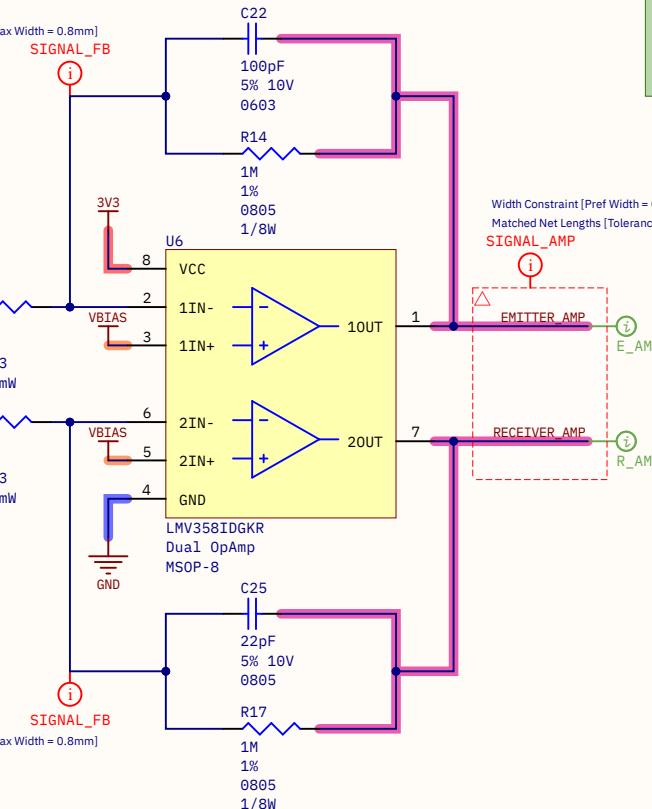
**Real model:**



**Footprint:**



Emitter signal will be in the range of 15 V to 100 V and need to be clipped by the diodes. Then, the OpAmp will amplify to saturation so the emitter can be perceived by the instrument as a flank; whereas the receiver signal will most likely be amplified without any clipping.

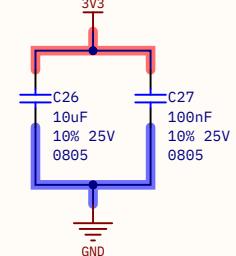


**SIGNAL\_CONDITIONING\_SIMULATIONS**  
**signal\_conditioning\_simulations**  
Results of simulating the adequation circuit with SPICE and realistic input waveforms

These are two charge mode amplifiers. This circuit is meant for sensors which are physically far from the acquisition system. It mitigates the effect of cables' capacitance.  
[James Karki (Texas Instruments)  
"Signal Conditioning Piezoelectric Sensors". Application Report  
SLOA033A. September 2000]

This OpAmp is meant for low voltages, low power, single-supply and it has its own ESD protection.

Bypass caps for the OpAmp, should be physically close to its power pins.



## Piezoelectric sensors conditioning circuit

Two analog signals come from two piezoelectric sensors nailed into a tree or trunk. The way piezos work force us to use this circuit to convert charge into voltage. The piezo sensors used generated up to -100 V peak, so it needs clipping

Designer's signature  
Supervisor's signature

Sheet title: **Piezoelectric sensors conditioning circuit**

Project title: **TIK\_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

Date: **2022-06-10**

Revision: **0.6**

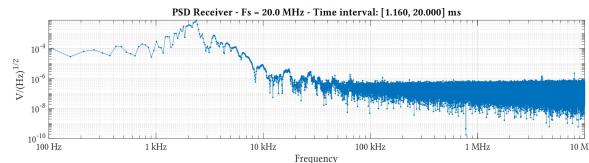
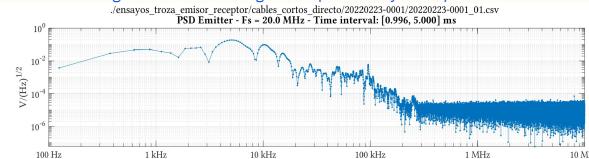
Sheet 16 of 20

Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología de Computadores  
University of Granada  
C/Fuente Nueva, s/n, 18001  
Granada, Granada, Spain



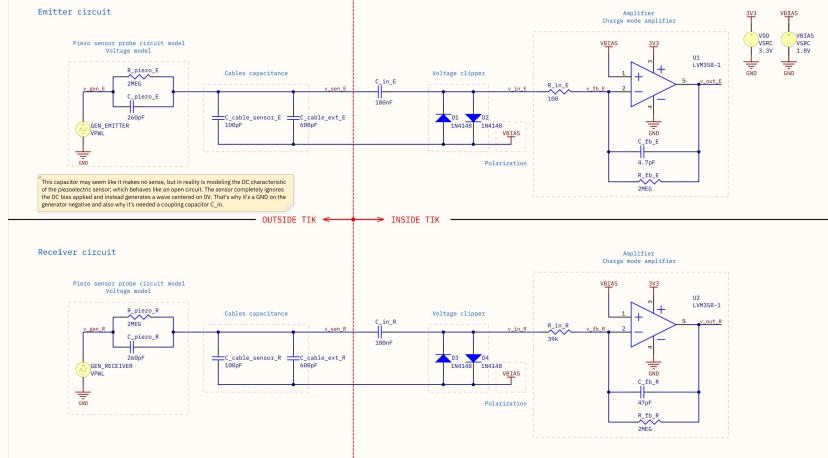
## Trunk signal's Voltage Spectral Density

Example VSD of a generic trunk signal captured by the piezoelectric sensors



## Simulated circuit

Circuit from a subproject inside ./SIMULATIONS

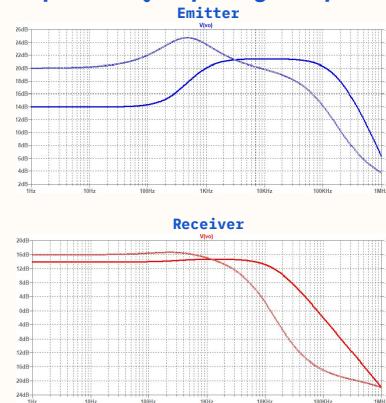


[TOPOLOGY DOES NOT CHANGE, BUT COMPONENT VALUES MAY NOT BE UP TO DATE]

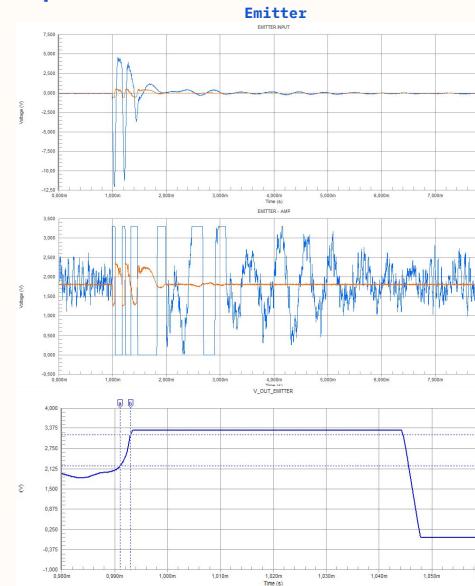
A piezoelectric is commonly modeled as a charge source in parallel with a resistor and a capacitor (charge model). This, however, is not practical for simulated analysis. Instead, we resorted to the voltage model, which is a voltage source in series with a resistor and a capacitor in parallel.

Nevertheless, in empirical analysis we found that our probes are far more complex than this simple model: They behave like an open circuit for DC (thus ignoring VBIAS). They have a great resistance and capacitance dependency on frequency, and a resonance around 100 kHz.

## Expected frequency response



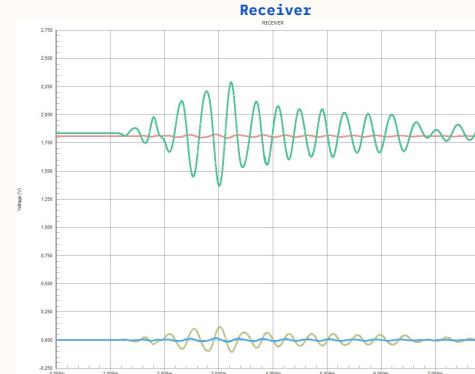
## Expected transient behavior



The emitter input signal can be of 10 to 20 V if the piezoelectric probe is hit very hard. This voltage can damage electronics. As a countermeasure we use two 4148 diodes on the input that clip the signal to ±0.7 volts around VBIAS, allowing us to manipulate it without risk.

The adequate circuit for the emitter has more gain than it needs, so the output of the OpAmp is saturated. This gives us a very step flank where the signal clearly begins and it's very easy to identify. In this simulation it's clear that maybe it's not needed so much gain as the output is very noisy and could be easily false-triggered.

Zoom over the first pulse. The expected rise time will be around 2 us, so the delay is of 1 sample (Fs = 500 kHz)



The receiver on the other hand has a very weak signal that needs to be amplified and centered over 1.8V. We have to be more cautious in this case so we don't distort it as we have to sample and process it with precision.

The adequate circuit for the emitter has more gain than it needs, so the output is saturated. This gives us a very step flank where the signal clearly begins and it's very easy to identify.

## Signal conditioning circuit simulations

SPICE simulations of the adequation circuit. These are only the results. You can find the simulation circuit and models on the ./SIMULATIONS/ folder inside this project.

Designer's signature  
Supervisor's signature

Sheet title: **Signal Conditioning Theoreticals**  
Project title: **TIK\_HandheldDevice.PjPcb**

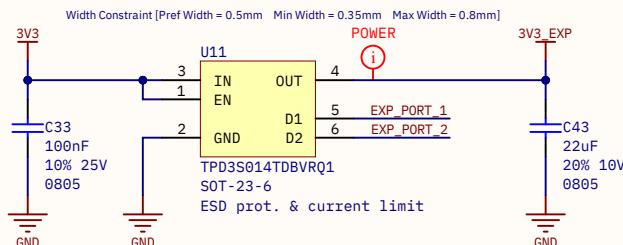
Designer: **Juan Del Pino Mena**

Date: **2022-06-10** Revision: **0.6** Sheet 17 of 20

Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología de Computadores  
University of Granada  
C/Fuente Nueva, s/n, 18001  
Granada, Granada, Spain

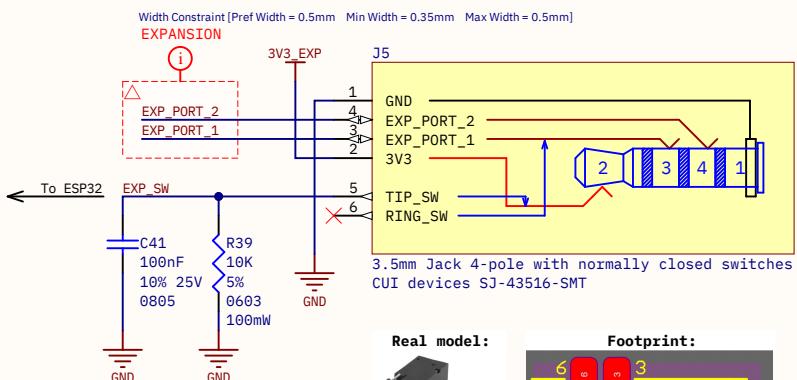


### Current limiter and ESD protection



### Expansion port connector

Expansion port pins are both Input/Output and are connected to the ADC1 so we give the maximum amount of functionality available to the expansion card.



Plug detection switch circuitry operation: The switch is normally closed. So, normally EXP\_SW is HIGH. When plugged in, the switch opens and EXP\_SW will be LOW

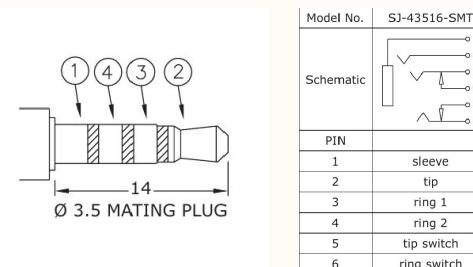
### 3.5mm jack connector considerations

For both the expansion port and the load cell connector

We are using the 3.5mm jack connector in a non-standard application, as we are not transferring audio but power and/or analog and digital signals of different nature.

Nevertheless, we have adjusted the connector to somewhat fit the OMPT convention (GND in sleeve, signals in rings).

The mating socket and plug are connected as follows. In this connector series there is the possibility of up to 6 pads, the additional 2 pads being connected to switches for detecting the plug insertion. We only use the tip switch (pin 5) to allow using both the SJ-43516 as well as the SJ-43515 models. We prefer the 6-pad version as it offers more mechanical integrity.  
[CUI Devices SJ-4351X-SMT Datasheet, page 2]



To avoid shorting GND and VCC, the 3V3 rail is located at the tip, so it will make contact last. This also allows us to easily add the tip switch circuitry.

Nevertheless, since this is an external connector, this will have a current limit switch and ESD protection IC to avoid damaging the device.

### Expansion port & jack connector

Expansion port for added functionality, such as an ultrasound resonance analysis for wood boards. Also, this sheet includes a description of the jack connector properties.

Designer's signature

Sheet title: Expansion port

Project title: TIK\_HandheldDevice.PrtPcb

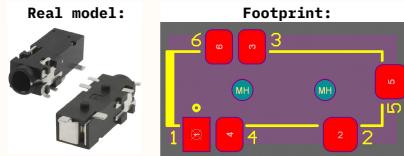
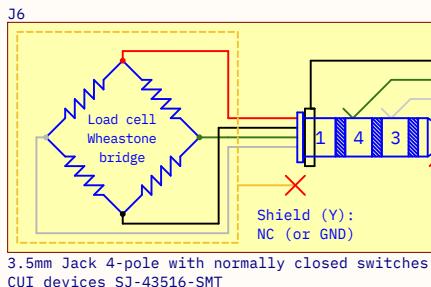
Supervisor's signature

Desinger: Juan Del Pino Mena

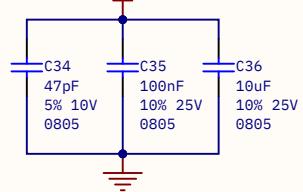
Date: 2022-06-10 Revision: 0.6 Sheet 18 of 20

Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología de Computadores  
University of Granada  
C/Fuente Nueva, s/n. 18001  
Granada, Granada, Spain





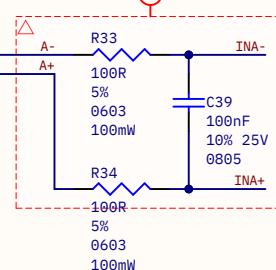
There's no "standard load cell connector". We have selected a 3.5mm jack 4-pole connector and organized the pins in the usual order and with usual colors. Note that the shield is unconnected. A more appropriate alternative could be a RJ-11 6-pin connector, but was discarded because of the large socket size.



VCC/VDD bypass caps for noise filtering and voltage stabilization for the HX711.

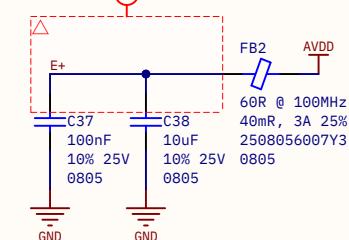
Width Constraint [Pref Width = 0.5mm Min Width = 0.35mm Max Width = 0.5mm]

LOAD\_CELL\_SIGNAL



Width Constraint [Pref Width = 0.5mm Min Width = 0.35mm Max Width = 0.5mm]

POWER



Noise/EMI filtering on AVDD. Sparkfun's design uses a 2.2 uH chip inductor. Instead we use a ferrite bead.

Plug detection switch circuitry

GND GND

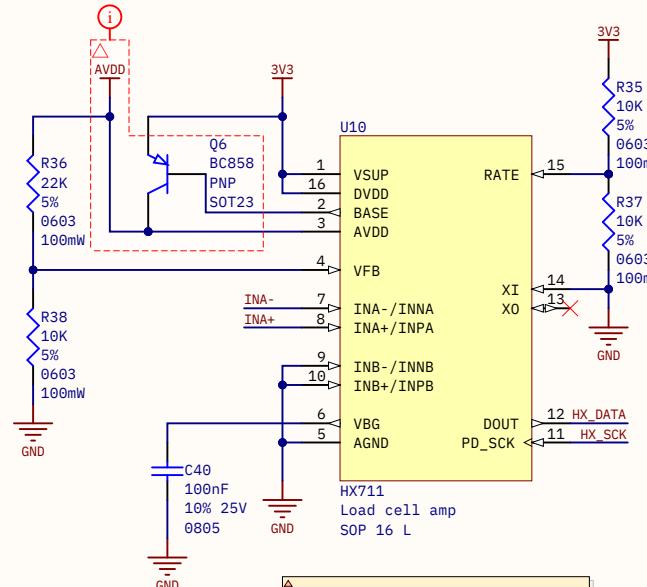
GND GND

GND GND

GND GND

Width Constraint [Pref Width = 0.5mm Min Width = 0.35mm Max Width = 0.5mm]

POWER

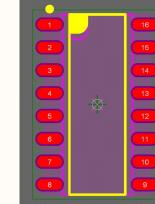


RATE pin config:  
- Pulled down: normal mode, 10 SpS  
- Pulled up: fast mode, 80 SpS, noisier

Real model:

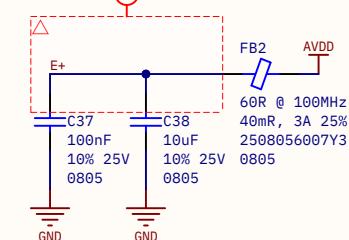


Footprint:



Width Constraint [Pref Width = 0.5mm Min Width = 0.35mm Max Width = 0.5mm]

POWER



Noise/EMI filtering on AVDD. Sparkfun's design uses a 2.2 uH chip inductor. Instead we use a ferrite bead.

Resistors serve as a short circuit protection since A+ and A- are exposed pins and also input impedance. Capacitor prevents noise and rapid change. Signals from load cells are slow.

VBG = VFB is a reference bypass output. It stays fixed at 1.25 V.

AVDD is the analog voltage source with is generated by the HX711's internal regulator with the aid of the PNP BJT.

$AVDD = VBG \cdot (R1 + R2) / R1$   
It should always be less than (VSUP - 100 mV)  
[HX711 datasheet, page 4]

In this design:  
 $AVDD = 1.25 V \cdot (22 k\Omega + 10 k\Omega) / 20 k\Omega = 1.82 V$   
HX711 will serve 24 bit, 2's complement raw ADC data.  
The system needs a software calibration with a known weight for extracting a correction factor for this design.

"Reference PCB Board schematic" from the [HX711 Datasheet, figure 4, page 6]

## HX711 load cell amplifier

This circuit is used to get weight measurements out from load cells in order to estimate the density of a trunk or board.  
This design is based on the Sparkfun HX711 module by N. Seidle and A. Wende.

Designer's signature

Sheet title: **HX711 load cell amplifier**

Project title: **TIK\_HandheldDevice.PjPcb**

Supervisor's signature

Desinger: **Juan Del Pino Mena**

Date: **2022-06-10**

Revision: **0.6**

Sheet 19 of 20

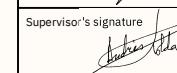
Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología de Computadores  
University of Granada  
C/Fuente Nueva, s/n, 18001  
Granada, Granada, Spain



A	Block	Component	Description/Conditions	Units	Supply voltage (V)	Current consumption per unit ( $\mu$ A)		Total dissipated power ( $\mu$ W)		Notes
						Typical	Maximum	Typical	Maximum	
	MCU	ESP32-WROOM-32D	MCU + wireless comm. Module	1	3.3	500 mA		1.7 W		Current spikes during wireless TX
Power rails		AP3429	DC/DC Buck converter IC	1	4.2	90 $\mu$ A		378 $\mu$ W		
		NCP562SQ18T1G	Low-Dropout regulator IC	1	3.3	3 $\mu$ A		9.9 $\mu$ W		
		150 k $\Omega$ + 33 k $\Omega$ voltage divider	FB pin feedback. Fixed consumption	1	3.3	18 $\mu$ A		59.4 $\mu$ W		
		[Optional] bypass voltage divider	Assuming 3V3/2 with 10 k $\Omega$ resistors	1	3.3	165 $\mu$ A		544.5 $\mu$ W		Consider only if populated
		Generic 0805 green LED	Assuming Vf = 3V & 39 $\Omega$ series resistor	1	3.3	7.7 mA		25.4 mW		Consider only if populated
Battery & current sense		INA219	Voltage & current sense IC	1	4.2	0.7 mA	1 mA	3 mW	4.2 mW	
		Generic 0805 green LED	Assuming Vf = 3V & 220 $\Omega$ series resistor	1	5.5	11.4 mA		62.5 mW		Consider only if populated
		Generic 0805 red LED	Assuming Vf = 2V & 470 $\Omega$ series resistor	1	5.5	7.5 mA		41 mW		Consider only if populated
		I2C pull-up resistor	Assuming line level is LOW, with 4.7k $\Omega$ resistors	2	3.3	0.7 mA		4.6 mW		
B		LTC4060EFE	NiMH/NiCd charger IC	1	5.5	2.9 mA	4.3 mA	16 mW	23.7 mW	
	[Optional] NiMH charger	MDJ201	Power PNP BJT. Ice=0.95 A, Ibe=120mA, Vce=1.8V, Vbe=0.7 V	1	--	--		1.71 W + 84 mW $\approx$ 1.8 W		Consider only if populated. For charging ICs and BJT: consider only when charging the battery (else they are off). In this case power consumption comes from external supply not from the internal battery.
		4.42 k $\Omega$ + NTC voltage divider	NTC pin. Assuming NTC at 50°C (3.54 k $\Omega$ )	1	5.5	691 $\mu$ A		3.8 mW		
[Optional] Li-Ion/Li-Po charger		TP4056	Li-Ion/LiPo charger IC, Vbus-Vbat=1.8 V, Ibat=1 A	1	5.5	150 $\mu$ A	500 $\mu$ A	1.8 W + 2.8 mW $\approx$ 1.8 W		
	DW01A	Battery protection IC		1	4.2	3 $\mu$ A	6 $\mu$ A	12.6 $\mu$ W	25.6 $\mu$ W	
	FS825A	Dual power NMOS, Rds(on)=25 m $\Omega$ , Ibat=1 A		1	--	--		50 mW (both NMOS)		
USB connector	USBLC6-2SC6	USB ESD protection IC		1	5.5	10 nA	150 nA	55 nW	825 nW	Consider only when USB is plugged
	CH340C	USB to UART converter IC		1	3.3	12 mA	30 mA	39.6 mW	99 mW	Worst case when programming
Programming	2N7002	G.P. NMOS. Ib=0 A, Vds=3.3 V, Ids=330 $\mu$ A (during conmutation)		2	--	--		1 mW		Consider only when programming
	Generic 0805 green LED	Assuming Vf = 3V & 39 $\Omega$ series resistor		2	3.3	7.7 mA		50.8 mW		Consider when programming, using UART and if populated.
	Generic 0805 red LED	Assuming Vf = 2V & 150 $\Omega$ series resistor		2	3.3	8.7 mA		57.4 mW		
Buttons	Pull-up resistors	Assuming line level is LOW, 10k $\Omega$ resistors		5	3.3	0 (not pushed)	330 $\mu$ A	0 (not pushed)	5.4 mW	Worst case: all pressed at once
	BSS84AK	G.P. PMOS. Rsd(on) = 7.5 $\Omega$ , Ib=0, Isd = 77 $\mu$ A		1	--	--		45 nW		
Power-up button	1N4148W	Small signal diode. Vf=0.7 V, If=26 $\mu$ A		2	--	--		36.4 $\mu$ W		Worst case: both ON
	100 k $\Omega$ pull-up resistor	100 k $\Omega$ pull-up resistor		1	4.2	42 $\mu$ A		176.4 $\mu$ W		
TFT LCD display	LCD TFT ILI9341 module	320x240p LCD (Measured)		1	3.3					Worst case: all pixels white, 60 FPS
Signal conditioning	LMV358DGKR	General purpose dual OpAmp, with no load		1	3.3	140 $\mu$ A	340 $\mu$ A	462 $\mu$ W	1.1 mW	Both OpAmps, high Z load
	1N4148W	Small signal diode. Vf=0.7 V, If= $\mu$ A (Measured)		4	--					Consider only when measuring
Load cell amplifier	HX711	Load cell amplifier & ADC IC		1	3.3	1.4 mA		4.6 mW		Enters sleep if the data clock stops
	BC858	General purpose PNP BJT. Vce=1.8V, Ice=? $\mu$ A (Measured)		1	--					Consider only when HX711 is awake
	22 k $\Omega$ + 10 k $\Omega$ voltage divider	VFB pin feedback for AVDD=1.82 V regulation.		1	1.82	57 $\mu$ A		103.7 $\mu$ W		Consider only when HX711 is awake

## Power budget

Detailed estimation of typical and worst-case power consumption per component in order to define battery requirements. Choosing a battery.

Designer's signature  
  
Supervisor's signature  


Sheet title: **Power budget**  
Project title: **TIK\_HandheldDevice.PjPcb**  
Desinger: **Juan Del Pino Mena**  
Date: **2022-06-10** Revision: **0.6** Sheet 20 of 20

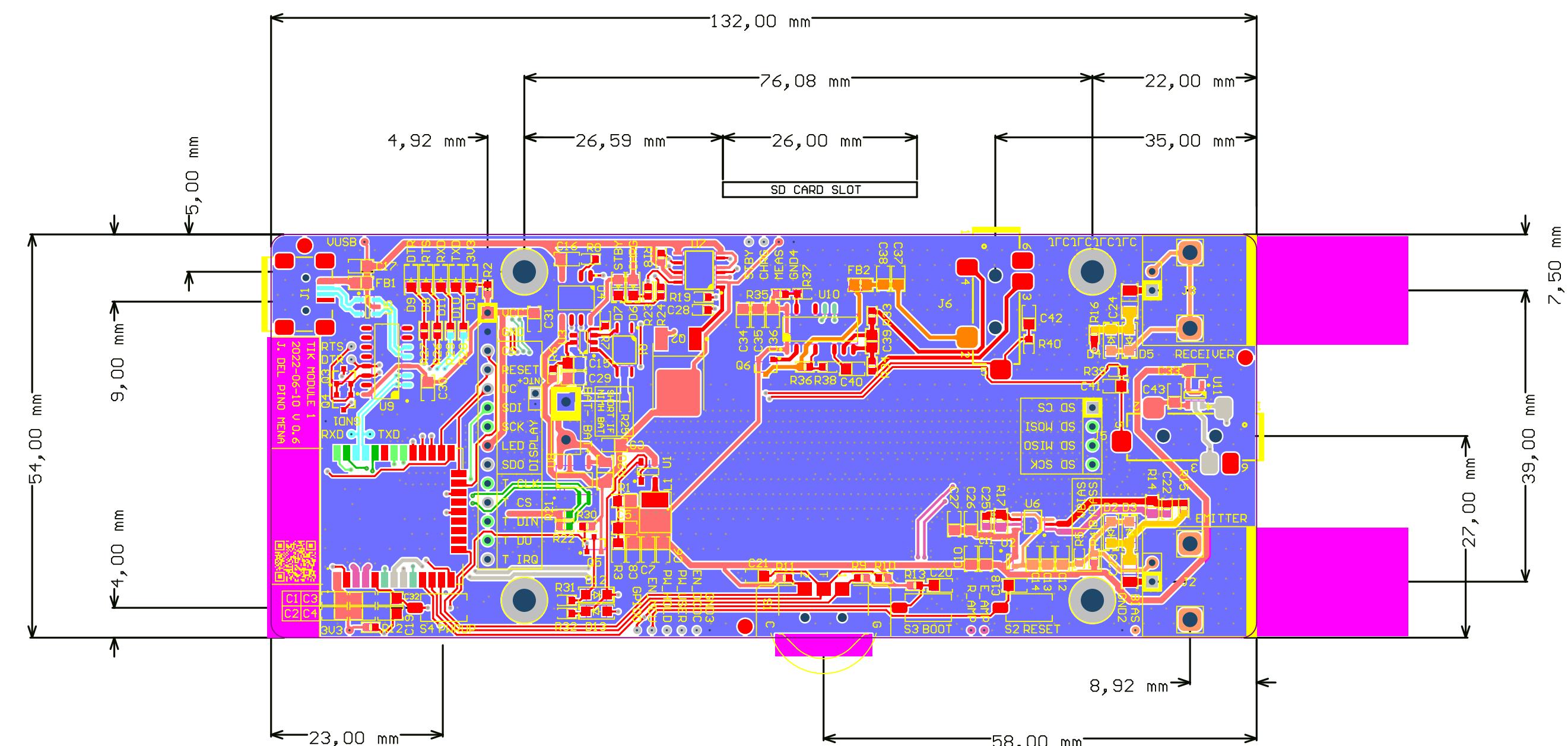
Supervisor:  
Sr. Andrés Roldán Aranda  
Dpto. Electrónica y Tecnología de Computadores  
University of Granada  
C/Fuente Nueva, s/n, 18001  
Granada, Granada, Spain





A

A



## VISIBLE LAYERS

Board outline + Multilayer + Top  
overlay + Top layer + Keep-out  
dimensions

**TRACKS & POLYGONS COLOR LEGEND:**

 Emitter/Receiver Analog Signals	 Power Reference GND/BAT-	 SPI
 Generic Net on Top Layer	 Power Rail 3V3/BAT+/VUSB/ VMEAS/VSENSE	 I2C
 Generic Net on Bottom Layer	 Power Rail VBIAS	 SERIAL UART/USB

# ***TIK handheld device PCB***

PCB orientation: vertical. Screen facing front, BNCs on top, USB at the bottom, SD Card reader at the left, powerup button at the bottom front right, and multipurpose button on the right side.

Designer's signature

Sheet title: TIK Handheld Device PCB

Dpto. Electronica y Tecnologia  
de Computadores  
University of Granada  
C/ Fuente Nueva, s/n, 18001  
Granada, Granada, Spain  
Sr. Andres Roldan Aranda

Supervisor's signature

Designer: Juan Pol Rincón Mena

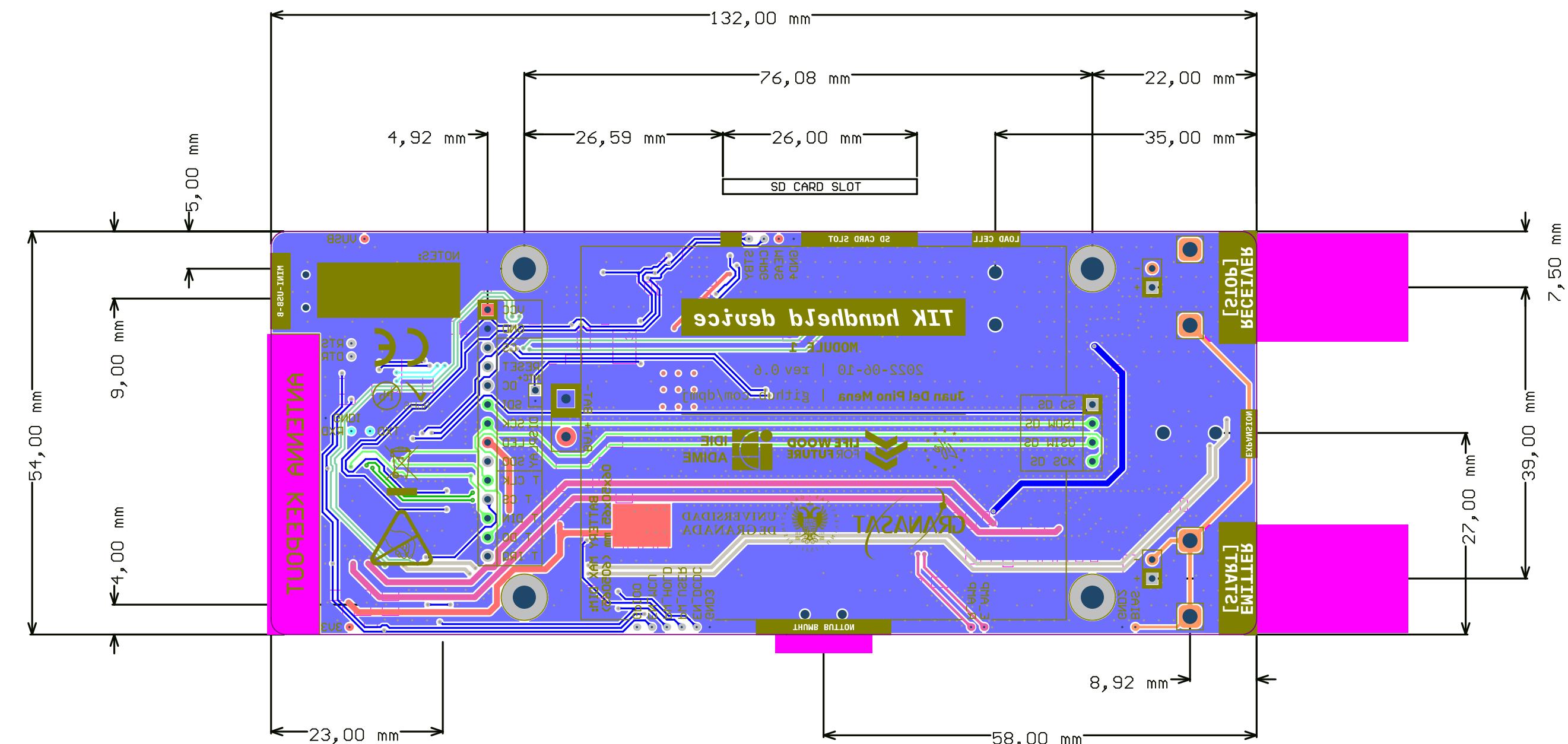
---

Date: 2022-06-10  
Revision: 0.6 Sheet 1 of 1



A

A



## **VISIBLE LAYERS**

Board outline + Multilayer + Bottom  
overlay + Bottom layer + Keep-out  
dimensions

**TRACKS & POLYGONS COLOR LEGEND:**

 Emitter/Receiver Analog Signals	 Power Reference GND/BAT-	 SPI
 Generic Net on Top Layer	 Power Rail 3V3/BAT+/VUSB/ VMEAS/VSENSE	 I2C
 Generic Net on Bottom Layer	 Power Rail VBIAS	 SERIAL UART/USB

# ***TIK handheld device PCE***

PCB orientation: vertical. Screen facing front, BNCs on top, USB at the bottom, SD Card reader at the left, powerup button at the bottom front right, and multipurpose button on the right side.

Designer's signature

Sheet title: TIK Handheld Device PCB

Dpto. Electronica y Tecnologia  
de Computadores  
University of Granada  
C/ Fuente Nueva, s/n, 18001  
Granada, Granada, Spain  
Sr. Andres Roldan Aranda

Supervisor's signature

Designer: Juan Del Rincón Mesa

*Andresolda*

Supervisor: Andres Roldan Aranda

Date: 2022-06-10  
Revision: 0.6 Sheet 1 of 1



A

B

C

D

E

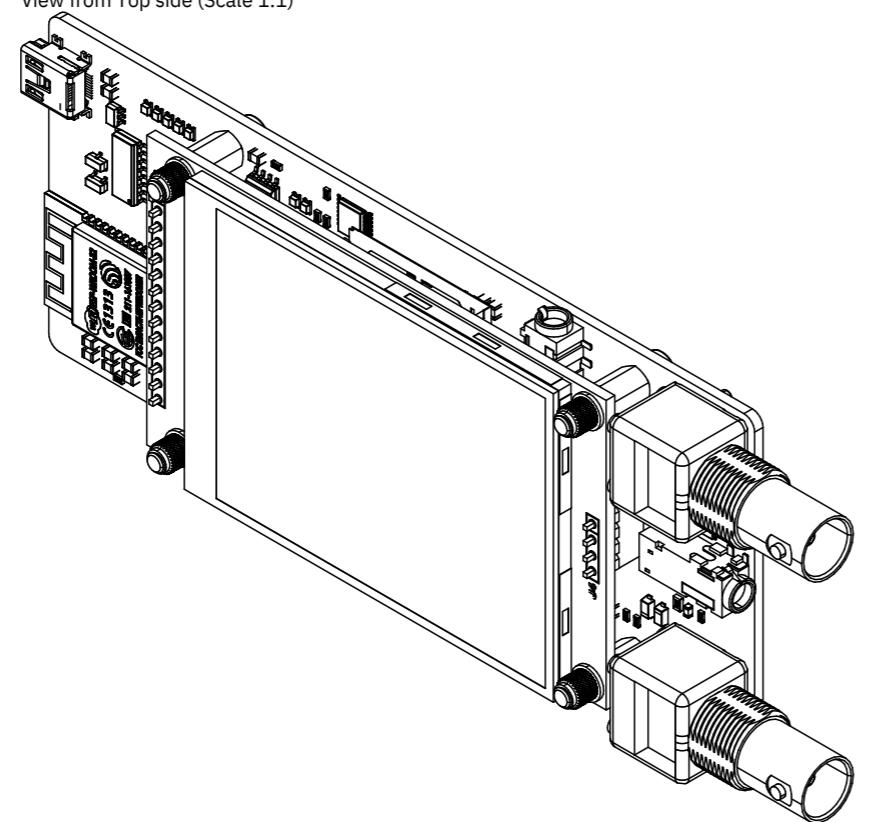
F

G

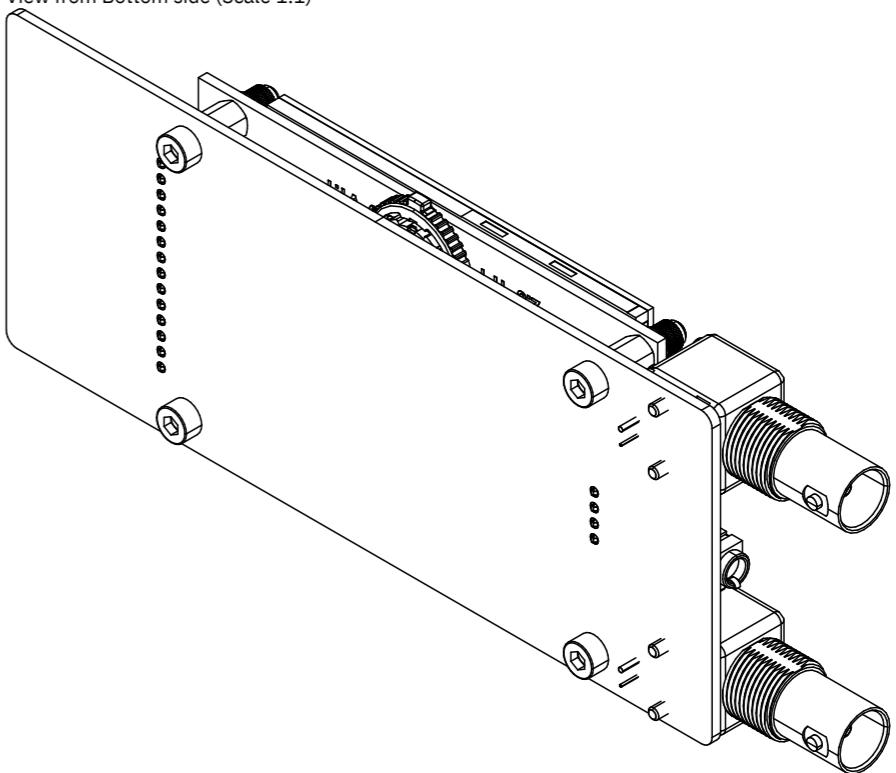
H

REV STATUS OF SHEETS		REV					DWG NO.		G	REV	REVISIONS		
SHEET									ZONE	REV	DESCRIPTION	DATE	APPROVED

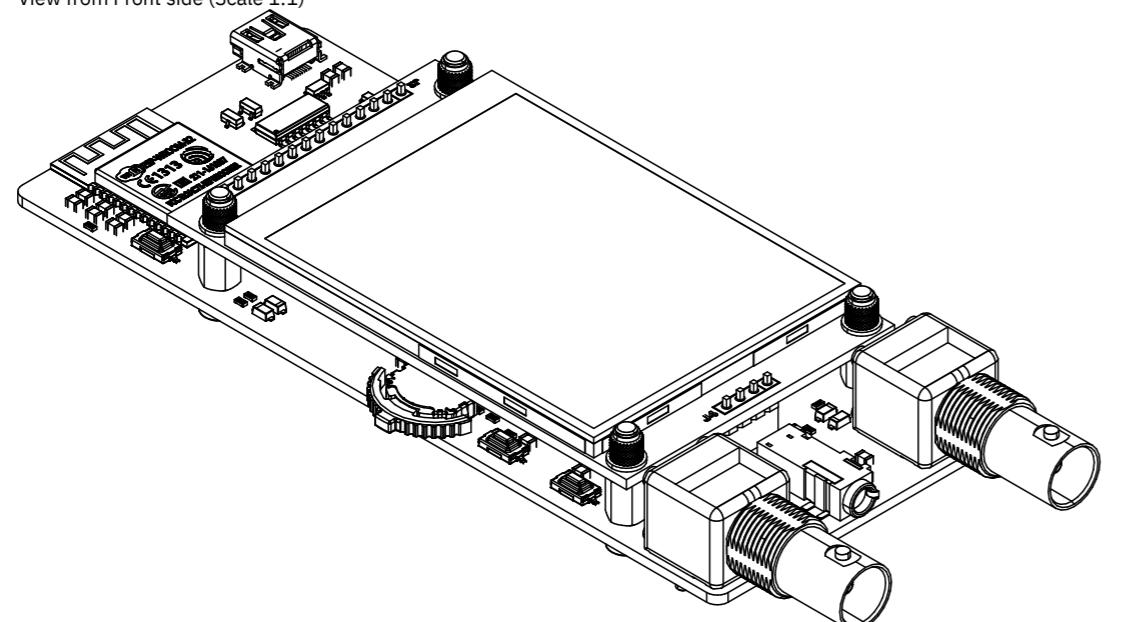
View from Top side (Scale 1:1)



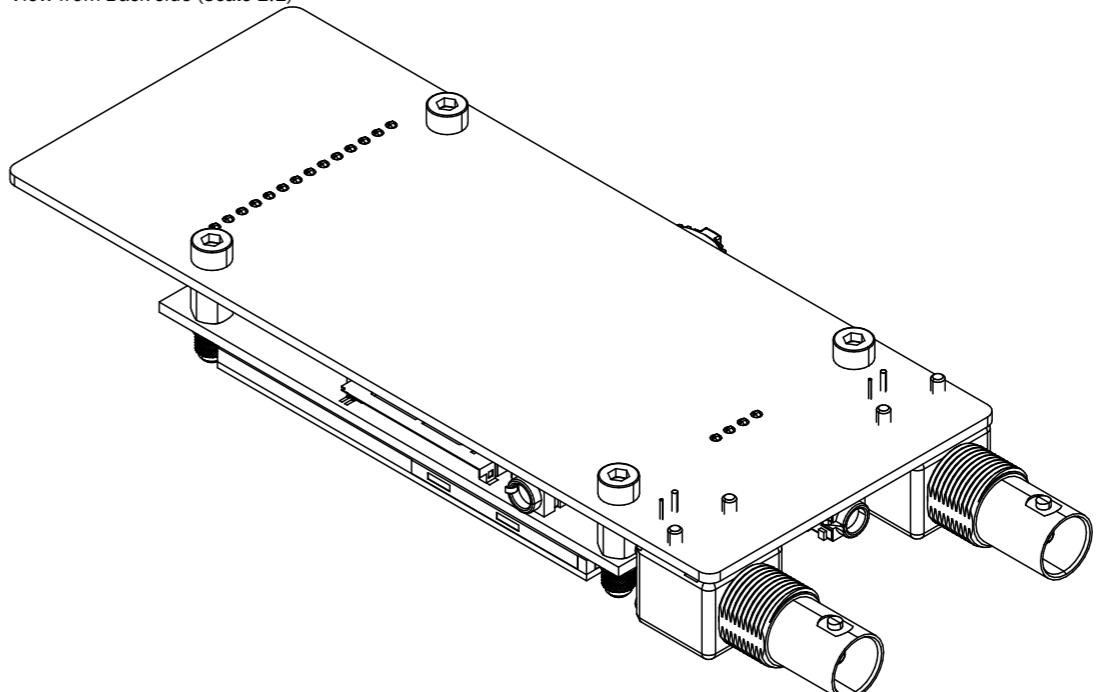
View from Bottom side (Scale 1:1)



View from Front side (Scale 1:1)



View from Back side (Scale 1:1)



PART NO: =PCB\_PART\_NUMBER

APPROVALS DATE

ENGINEER: Juan Del Pino Mena 2022-05-14

DESIGNER: Juan Del Pino Mena 2022-05-14

CHECKER: Juan Del Pino Mena 2022-05-14

Reference Documents

BOM DOC: BOM/bill\_of\_materials

ASSY DOC: --

SCH DOC: SCH/\*

NEXT ASSY

USED ON

PCB DOC: PCB/TIK\_PCB.PcbDoc

APPLICATION

**GRANASAT**  
 Dpto. Electrónica y  
 tecnología de computadores  
 University of Granada, Spain  
 C/ Fuente Nueva, s/n, 18001

DESIGN ITEM: Item

DESIGN ITEM REVISION: 6

TITLE: TREE INSPECTION KIT MECHANICAL DRAFTS

SIZE: A3

CAGE CODE: --

DWG NO: 1

REV: 6

SCALE: 1:1

FILE NAME: TIK\_PCB.PCDBdwf

SHEET: 1 OF 3

A

B

C

D

E

F

G

H

A

B

C

D

E

F

G

H

REV STATUS  
OF SHEETS

REV

1

SHEET

DWG NO:

1

REV:

6

REVISIONS

ZONE

REV:

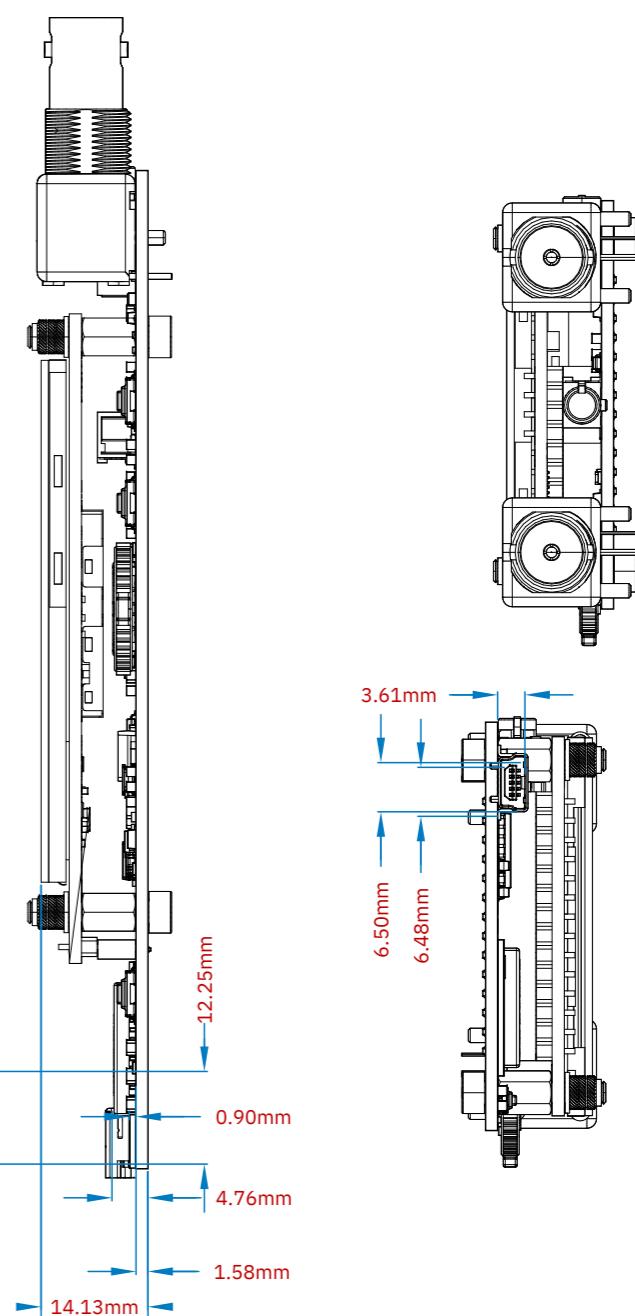
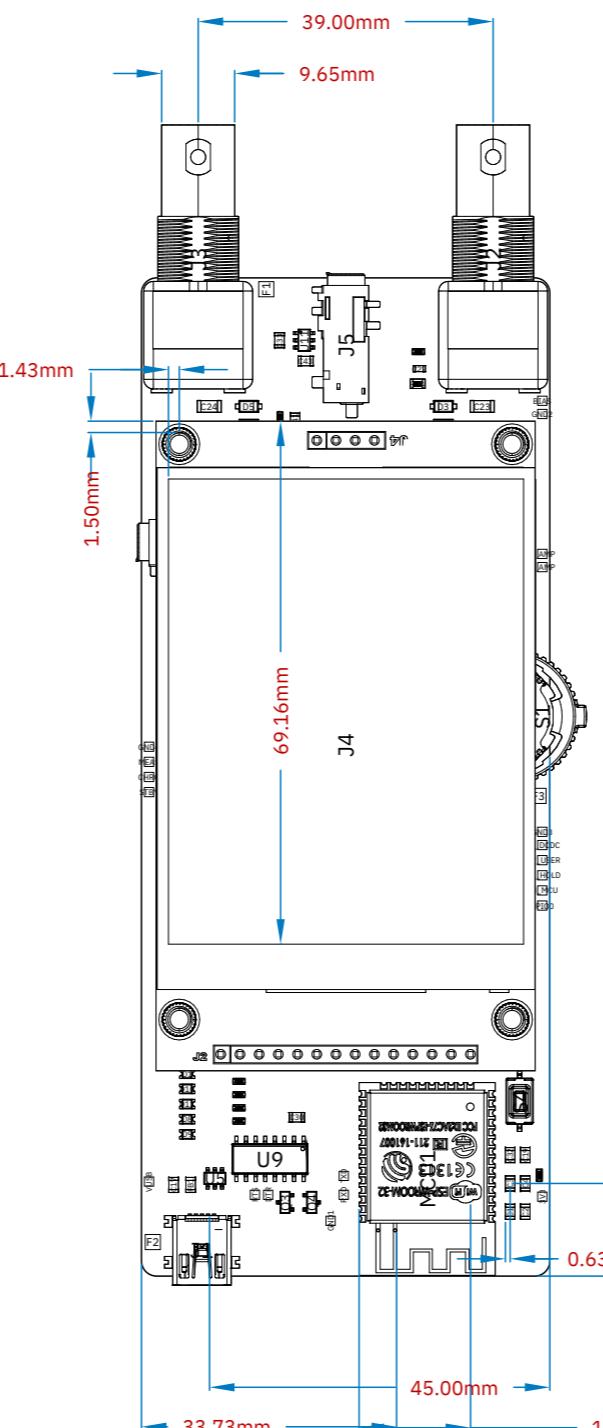
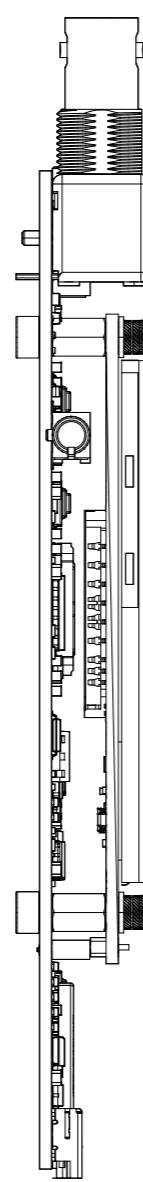
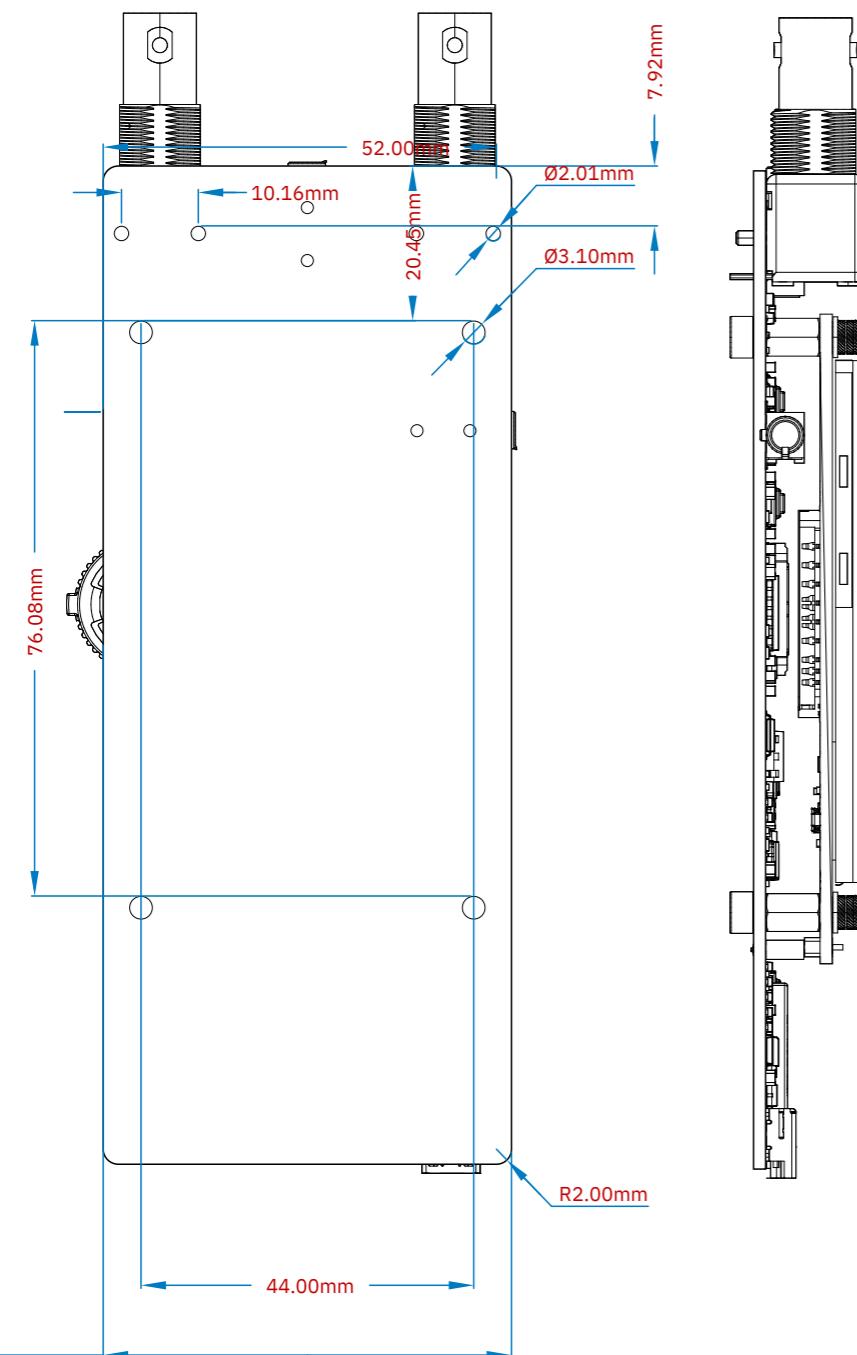
1

DESCRIPTION

DATE

1

APPROVED



PART NO: =PCB\_PART\_NUMBER

APPROVALS DATE

ENGINEER: Juan Del Pino Mena 2022-05-14

DESIGNER: Juan Del Pino Mena 2022-05-14

CHECKER: Juan Del Pino Mena 2022-05-14

Reference Documents

BOM DOC: BOM/bill\_of\_materials

ASSY DOC: --

SCH DOC: SCH/\*

NEXT ASSY: USED ON

PCB DOC: PCB/TIK\_PCB.PcbDoc

APPLICATION

**GRANASAT**  
 Dpto. Electrónica y  
 tecnología de computadores  
 University of Granada, Spain  
 C/ Fuente Nueva, s/n, 18001

DESIGN ITEM: Item

TITLE: TREE INSPECTION KIT MECHANICAL DRAFTS

DESIGN ITEM REVISION: 6

SIZE: A3

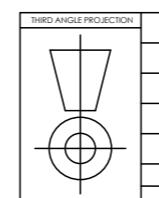
CAGE CODE: --

DWG NO: --

SCALE: FILE NAME: TIK\_PCB.PCDBdwf

HEET: 2 OF 3

REV: 6



APPROVALS	DATE
ENGINEER: Juan Del Pino Mena	2022-05-14
DESIGNER: Juan Del Pino Mena	2022-05-14
CHECKER: Juan Del Pino Mena	2022-05-14
Reference Documents	
BOM DOC: BOM/bill_of_materials	
ASSY DOC: --	
SCH DOC: SCH/*	
NEXT ASSY: USED ON	
PCB DOC: PCB/TIK_PCB.PcbDoc	
APPLICATION	

A

B

C

D

E

F

G

H

A

B

C

D

E

F

DWG NO: 1 G REV: 6

REVISIONS

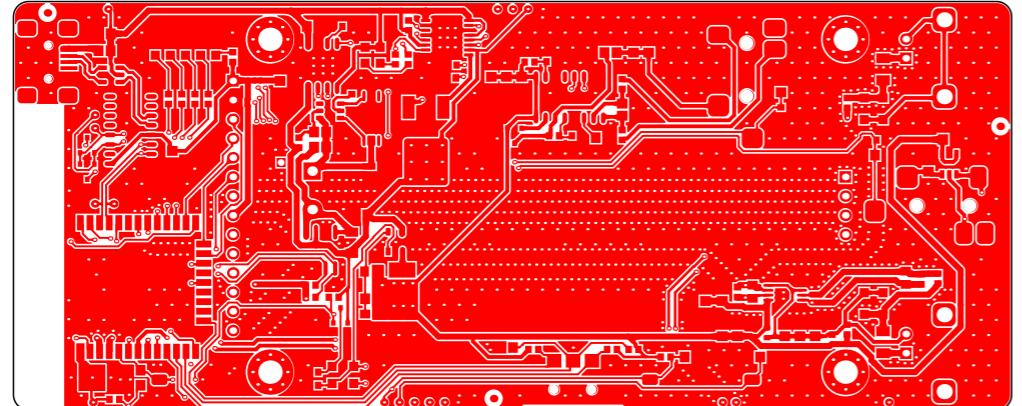
REV STATUS OF SHEETS

REV

1

1

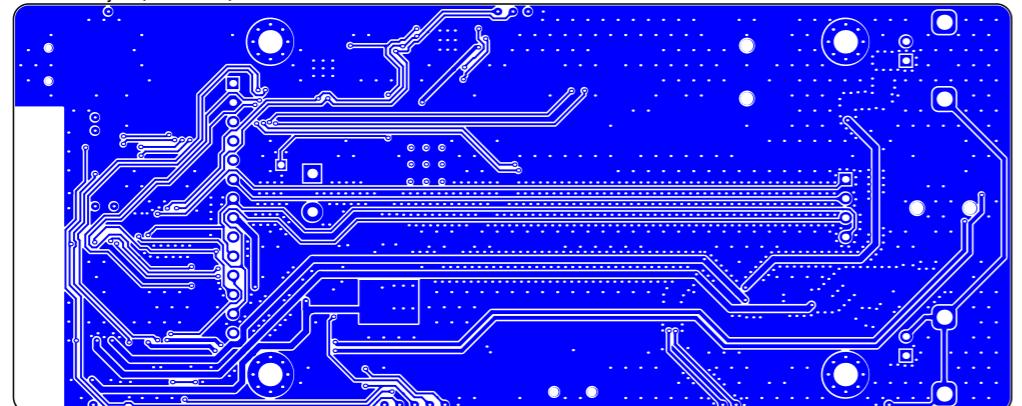
Top Layer (Scale 1:1)



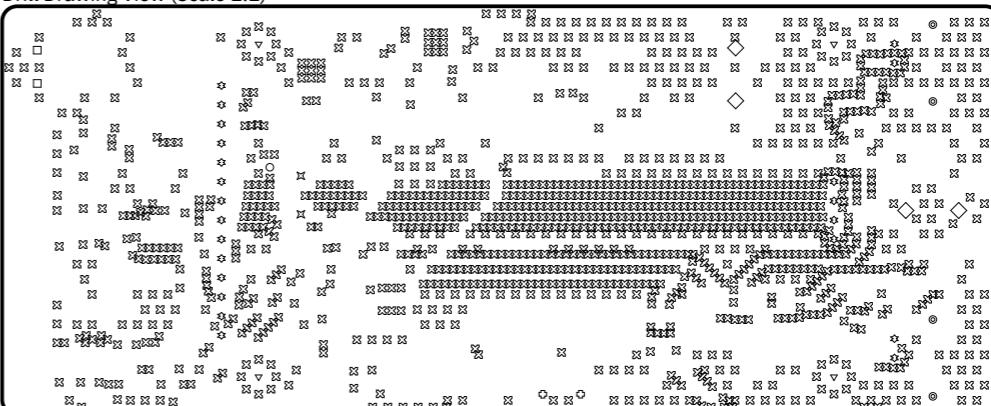
Top Paste (Scale 1:1)



Bottom Layer (Scale 1:1)



Drill Drawing View (Scale 1:1)



Layer Stack Legend



Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
x	1330	0.30mm	Plated	
*	22	0.89mm	Plated	
□	2	0.90mm	Non-Plated	
○	1	0.90mm	Plated	
○	2	1.20mm	Non-Plated	
☒	2	1.27mm	Plated	
◇	4	1.70mm	Non-Plated	
●	4	2.01mm	Plated	
▽	4	3.10mm	Plated	
1371 Total				

PART NO: =PCB_PART_NUMBER	APPROVALS	DATE	 Dpto. Electrónica y tecnología de computadores University of Granada, Spain C/ Fuente Nueva, s/n, 18001
ENGINEER: Juan Del Pino Mena	2022-05-14		
DESIGNER: Juan Del Pino Mena	2022-05-14		
CHECKER: Juan Del Pino Mena	2022-05-14		
Reference Documents			
BOM DOC: BOM/bill_of_materials	ASSY DOC: --	SCH DOC: SCH/*	
Design Item Information			
DESIGN ITEM: Item		DESIGN ITEM REVISION: 6	
TITLE: TREE INSPECTION KIT MECHANICAL DRAFTS			
SIZE: A3	CAGE CODE: --	DWG NO: --	
SCALE: 1:1	FILE NAME: TIK_PCB.PCDBdwf	HEET: 3 OF 3	

A

B

C

D

E

F

DWG NO: 1 G REV: 6

REVISIONS

1

1

