

A
BACHELOR'S DEGREE IN TELECOMMUNICATION ENGINEERING

Bachelor's Thesis

ACADEMIC COURSE 2021/2022

Tree Inspection Kit handheld device

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SUPERVISED BY:

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DEPARTMENT:

Electronics and Computer Technology



UNIVERSIDAD
DE GRANADA



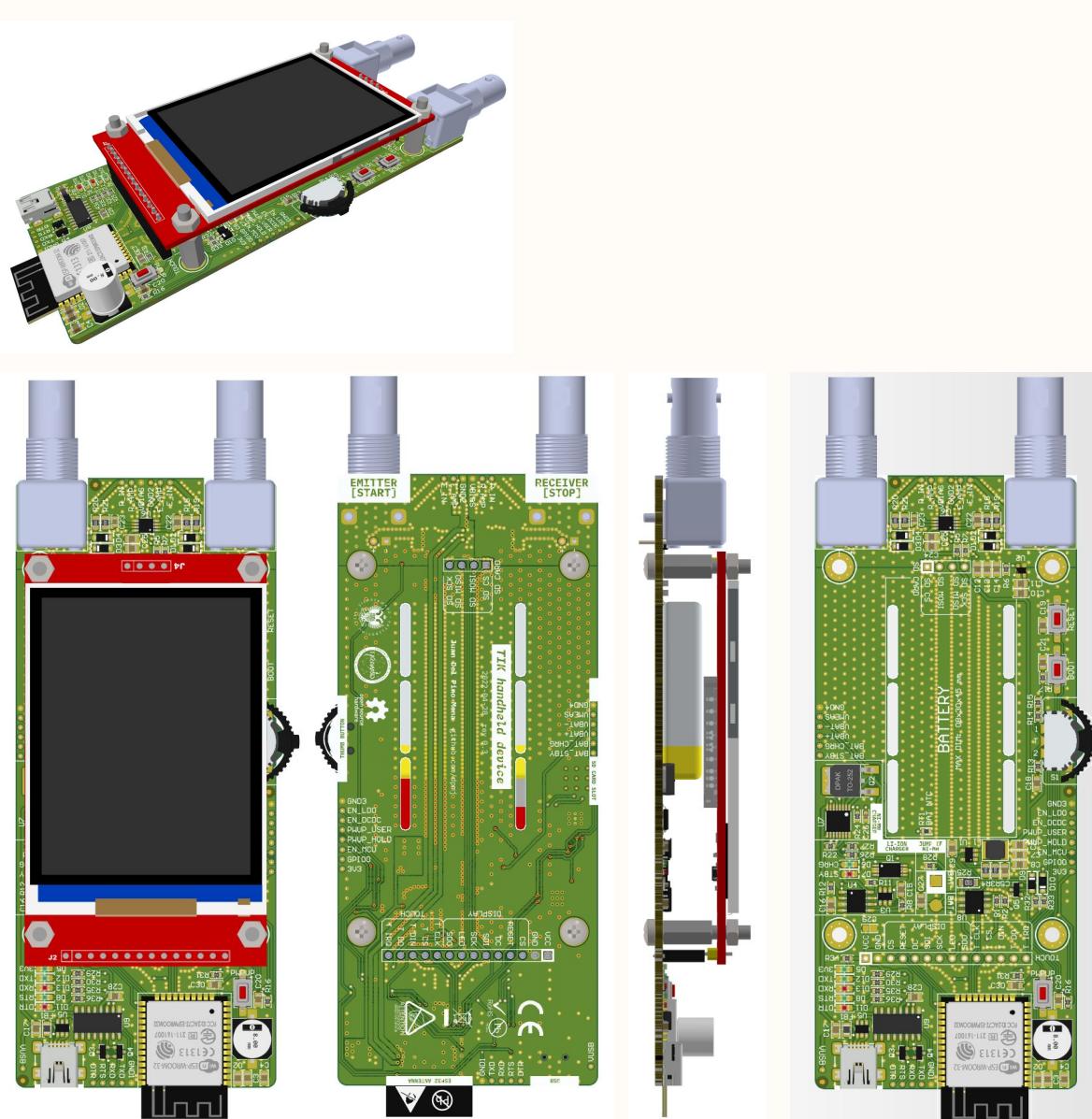
Project title: **TIK_HandheldDevice.PjPcb**

Date: **2022-05-12** Revision: **0.4-WIP**

Sheet 1 of 20

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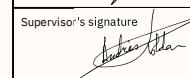
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Tree Inspection Kit handheld device

A device capable of determining the microsecond delay between 2 signals coming from piezoelectric probes pounded into a tree or trunk, for indirectly measuring the Modulus of Elasticity.

Designer's signature

Supervisor's signature


Sheet title: **Introduction and PCB renders**
Project title: **TIK_HandheldDevice.PxjPcb**

Designer: **Juan Del Pino Mena**

Date: **2022-05-12** Revision: **0.4-WIP** Sheet 2 of 20

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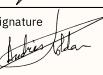
<p># Revision 0.4 2022-05-11 [MOST RECENT] [WIP]</p> <table border="1"> <thead> <tr> <th>NEW</th><th>FIXED</th></tr> </thead> <tbody> <tr> <td> <ul style="list-style-type: none"> - Added fabrication groups and fabrication order parameters - Added a Bill of Materials. The one in this document is simple. Refer to the manually configured BOM of this project. - Added a PCB track legend and description for visible layers on every PDF exported sheet. - Given more information about the ESP32 pin behaviour. - Added a precise block diagram. - Added support for an extension port. - Added a HX711-based load cell acquisition system. </td><td> <ul style="list-style-type: none"> - Corrected I2C pins on the ESP32. - Removed "same length" directive on UART and I2C nets. - Improved routing. - Removed I2C traces' via shielding. - Solved all DRC warnings and errors. - The ESP32's strapping pins default configuration is respected: modified pull-up/down resistors when needed to be according to the default boot setting. - Corrected a pin assignment error between the schematic symbol and the footprint of the MDJ210 PNP BJT transistor. </td></tr> </tbody> </table>	NEW	FIXED	<ul style="list-style-type: none"> - Added fabrication groups and fabrication order parameters - Added a Bill of Materials. The one in this document is simple. Refer to the manually configured BOM of this project. - Added a PCB track legend and description for visible layers on every PDF exported sheet. - Given more information about the ESP32 pin behaviour. - Added a precise block diagram. - Added support for an extension port. - Added a HX711-based load cell acquisition system. 	<ul style="list-style-type: none"> - Corrected I2C pins on the ESP32. - Removed "same length" directive on UART and I2C nets. - Improved routing. - Removed I2C traces' via shielding. - Solved all DRC warnings and errors. - The ESP32's strapping pins default configuration is respected: modified pull-up/down resistors when needed to be according to the default boot setting. - Corrected a pin assignment error between the schematic symbol and the footprint of the MDJ210 PNP BJT transistor. 	<p># Revision 0.2 2022-04-23</p> <table border="1"> <thead> <tr> <th>NEW</th><th>FIXED</th></tr> </thead> <tbody> <tr> <td></td><td> <ul style="list-style-type: none"> - New schematic hierarchy and system's block diagram. - Initial PCB layout - Added a rotary encoder (vertical). Library contains a 90-degree rotary encoder alternative. - Added a new alternative Ni-MH charger circuit. - Added footprints for all necessary components to the PCB Library. - Added explanatory footprints and photos to schematic ICs. - Added board mounting holes (making use of the TFT LCD module mounting hole positions) - Added test points - Added fiducials - Added a power-up button </td></tr> </tbody> </table>	NEW	FIXED		<ul style="list-style-type: none"> - New schematic hierarchy and system's block diagram. - Initial PCB layout - Added a rotary encoder (vertical). Library contains a 90-degree rotary encoder alternative. - Added a new alternative Ni-MH charger circuit. - Added footprints for all necessary components to the PCB Library. - Added explanatory footprints and photos to schematic ICs. - Added board mounting holes (making use of the TFT LCD module mounting hole positions) - Added test points - Added fiducials - Added a power-up button 	
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Revision history

Detailed changelog.

All along the schematic sheets, a sheet title and description will be written on this corner.

Designer's signature

Supervisor's signature


Sheet title: **Changelog**

Project title: **TIK_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

Date: **2022-05-12** Revision: **0.4-WIP** Sheet 3 of 20

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Maximum SPI @ 80 MHz traces length

Wavelength Calculator

Input Method
 Period
 Frequency

Frequency
 80 **MHz**
 Er Eff
 2,8905
 kHz
 Hz

Units
 MHz
 kHz
 Hz

Wavelength Information
 Er Effective Information
 Speed of Light

Y-axis diagram showing a sine wave with wavelength λ indicated.

$$\lambda = \frac{C}{f * \sqrt{(ErEff)}}$$

Wavelength Divide:

1/20 Wave Length: **11.02083 cm**

Note: Enter an Er Eff of 1 for wavelength in air.

Bandwidth & Max Conductor Length

Input Method
 Signal Risetime
 Frequency

f Units
 MHz
 kHz
 Hz

Frequency
 80 **MHz**

Speed of Light

Frequency Domain Method

Full Wavelength (In Air)
374.74057 cm

Lambda Divide by Factor

Maximum Conductor Length
18.73703 cm

Maximum Analog traces length

Wavelength Calculator

Input Method
 Period
 Frequency

Frequency
 100 **KHz**
 Er Eff
 3,0832
 kHz
 Hz

Units
 MHz
 kHz
 Hz

Wavelength Information
 Er Effective Information
 Speed of Light

Y-axis diagram showing a sine wave with wavelength λ indicated.

$$\lambda = \frac{C}{f * \sqrt{(ErEff)}}$$

Wavelength Divide:

1/20 Wave Length: **8536.69684 cm**

Note: Enter an Er Eff of 1 for wavelength in air.

Analog signal trace impedance

Conductor Impedance

Conductor Width (W)
0,8 mm

Conductor Height (H)
1,5 mm

Conductor Gap (G)
0,254 mm

Formula Restrictions:
 $0.1 < W/H < 2.0$
 $T = 53\mu m$

W/H = **0.533**

Zo
60.6257 Ohms

Power traces conductor characteristics (DC)

0.5 mm wide traces

Conductor Characteristics

Solve For
 Amperage
 Conductor Width

Plane Present?
 No
 Yes

Conductor Width
0,5 mm

Conductor Length
1 mm

PCB Thickness
1,6 mm

Frequency DC

Distance to Plane
1,5 mm

Plating Thickness
 Bare PCB
 18um
 35um
 53um
 70um
 88um
 106um
 124um
 142um
 178um

Units
 Imperial
 Metric

Substrate Options
 FR-4 STD
 FR-4 Epoxy

Material Selection
 FR-4 STD
 FR-4 Epoxy

Parallel Conductors?
 No
 Yes

Temp Rise (°C)
10

Ergo Tg (°C)
130

Temp in (°F) = 18.0

Ambient Temp (°C)
25

Temp in (°F) = 77.0

IPC-2152 with modifiers mode

Etch Factor: 1:1

Power Dissipation
0.00397 Watts

Conductor DC Resistance
0.00065 Ohms

Power Dissipation in dBm
5.9921 dBm

Conductor Cross Section
0.0301 Sq.mm

Voltage Drop
0.0016 Volts

Conductor Current
2.4647 Amps

Information
 Total Copper Thickness 70 um
 Via Thermal Resistance N/A

0.35 mm wide traces

Conductor Characteristics

Solve For
 Amperage
 Conductor Width

Plane Present?
 No
 Yes

Conductor Width
0,35 mm

Conductor Length
1 mm

PCB Thickness
1,6 mm

Frequency DC

Distance to Plane
1,5 mm

Plating Thickness
 Bare PCB
 18um
 35um
 53um
 70um
 88um
 106um
 124um
 178um

Units
 Imperial
 Metric

Substrate Options
 FR-4 STD
 FR-4 Epoxy

Material Selection
 FR-4 STD
 FR-4 Epoxy

Parallel Conductors?
 No
 Yes

Temp Rise (°C)
10

Ergo Tg (°C)
130

Temp in (°F) = 18.0

Ambient Temp (°C)
25

Temp in (°F) = 77.0

IPC-2152 with modifiers mode

Etch Factor: 1:1

Power Dissipation
0.00371 Watts

Conductor DC Resistance
0.00100 Ohms

Power Dissipation in dBm
5.6940 dBm

Conductor Cross Section
0.0196 Sq.mm

Voltage Drop
0.0019 Volts

Conductor Current
1.9218 Amps

Information
 Total Copper Thickness 70 um
 Via Thermal Resistance N/A

Via characteristics

Via Characteristics

Via Hole Diameter
0,3 mm

Internal Pad Diameter
0,6 mm

Ref Plane Opening Diam
1,016 mm

Via Height
1,6 mm

Via Plating Thickness
0,035 mm

IPC-2152 with modifiers mode

Via Capacitance
0.5893 pF

Via DC Resistance
0.00086 Ohms

Via Inductance
1.2993 nH

Via Impedance
46.956 Ohms

Via Resonant Frequency
5751.849 MHz

Via Step Response
30.4373 ps

Via Current
1.9514 Amps

Trace & via characteristics

Trace width based on results from PCB Toolkit by Saturn PCB Design INC.

*

TO-DO: EXPLAIN DATA.
CROP SOME
SCREENSHOTS

Designer's signature

Sheet title: **Trace width design**
 Project title: **TIK_HandheldDevice.PjPcb**

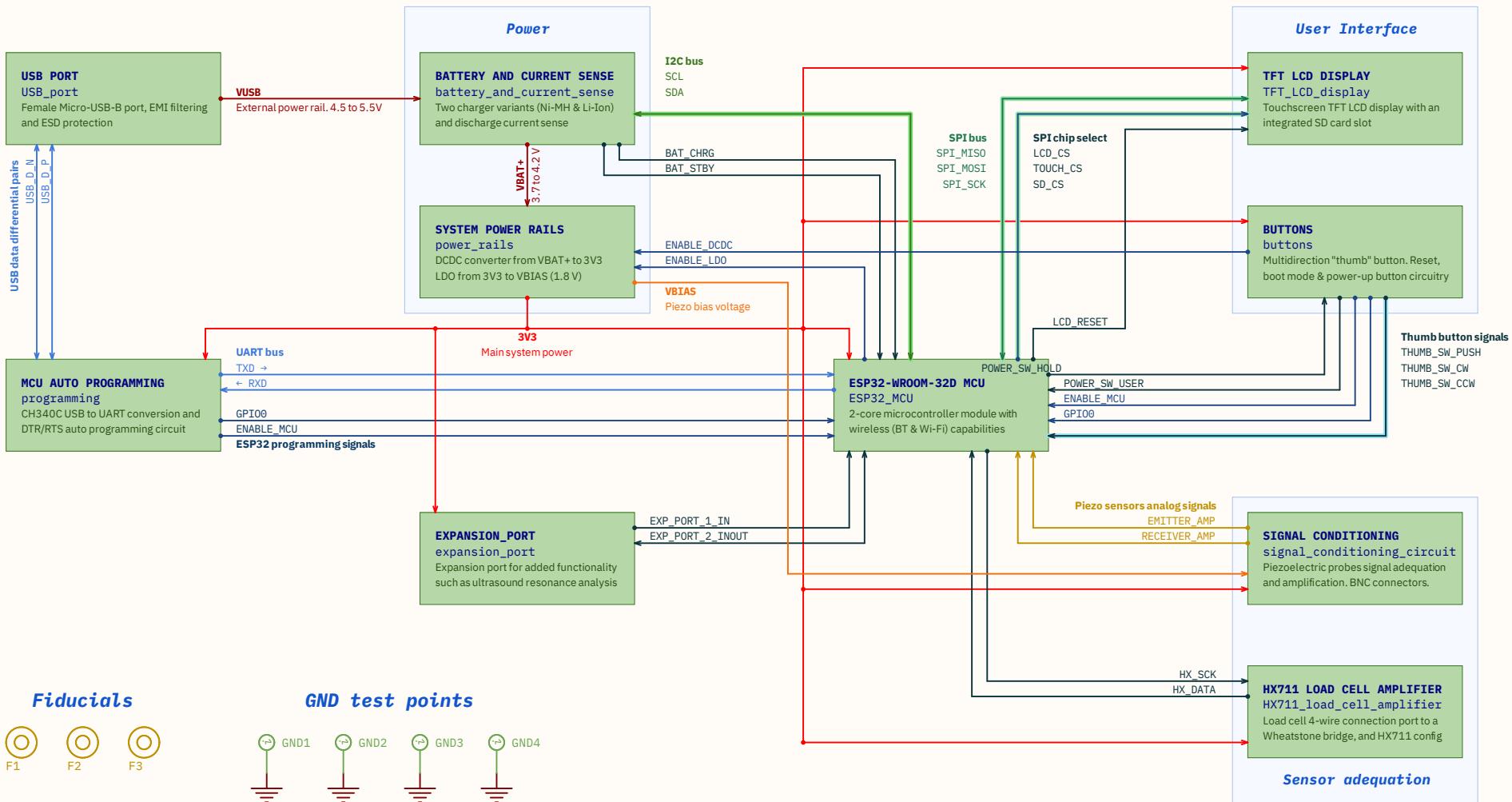
Supervisor's signature

Desinger: **Juan Del Pino Mena**

Date: **2022-05-12** Revision: **0.4-WIP**

Sheet 4 of 20

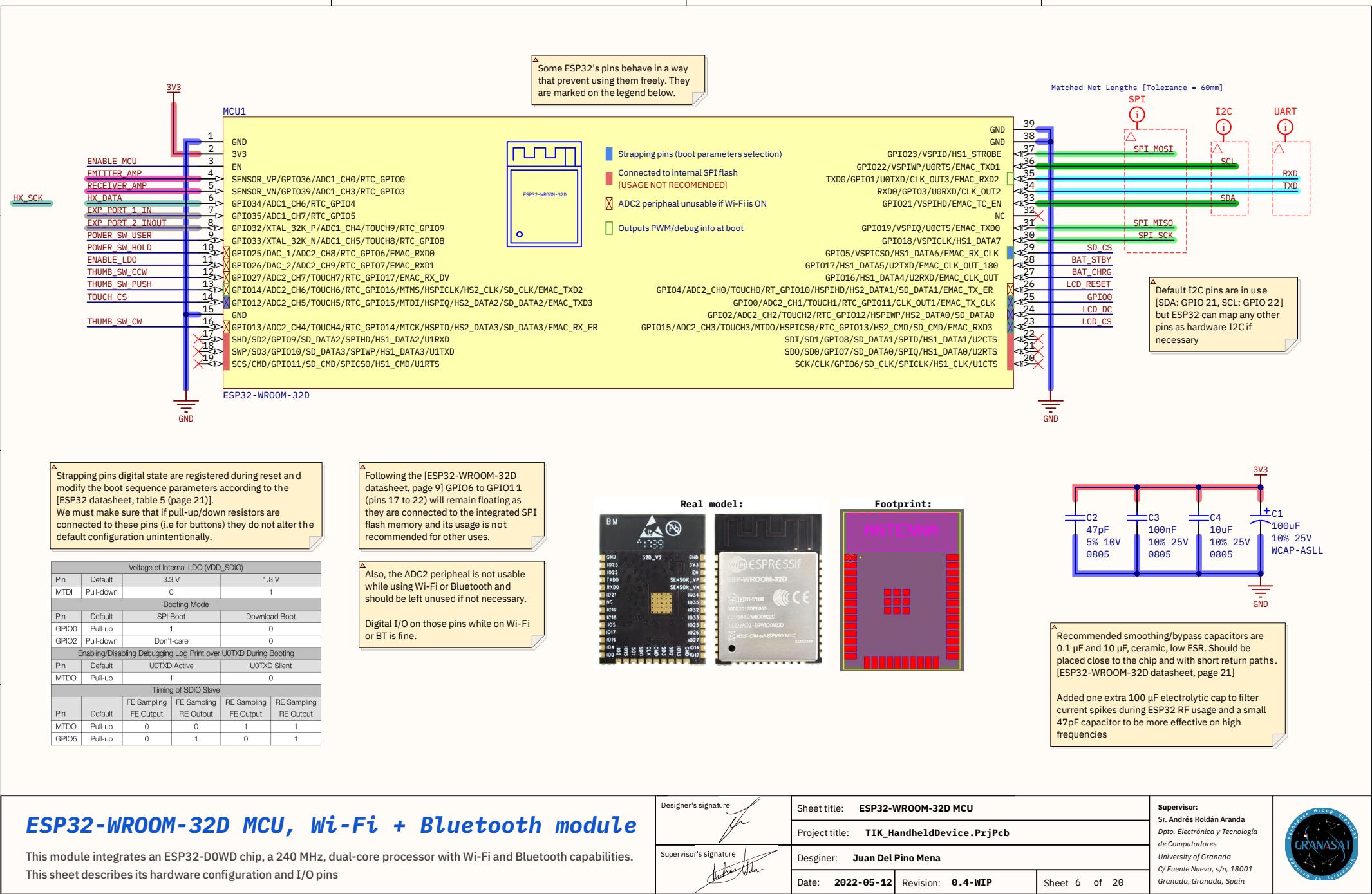




Designer's signature
Supervisor's signature
Project title: **TIK_HandheldDevice.PjPcb**
Desinger: **Juan Del Pino Mena**
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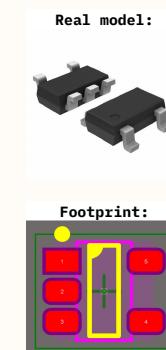
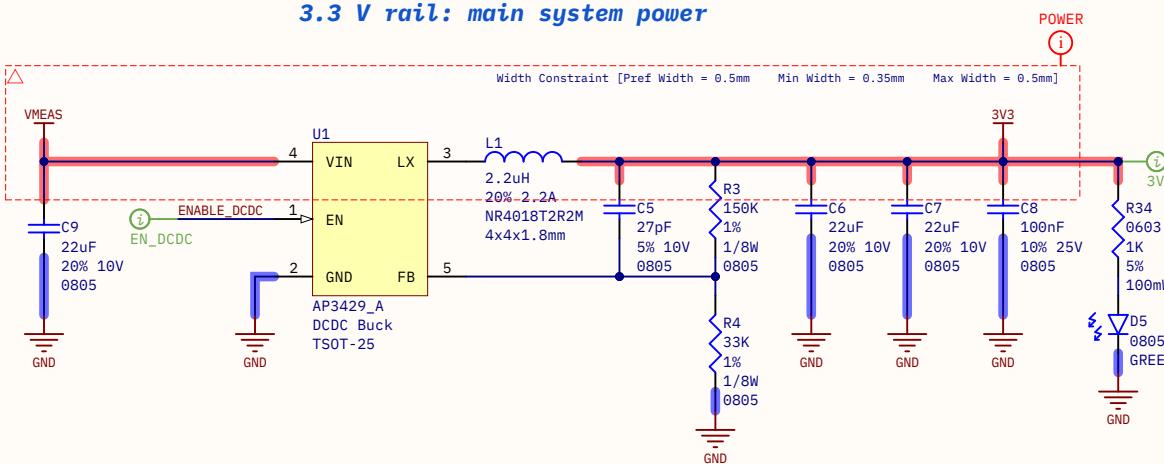
Sheet title: **System blocks organization and connections**
Supervisor:
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University of Granada
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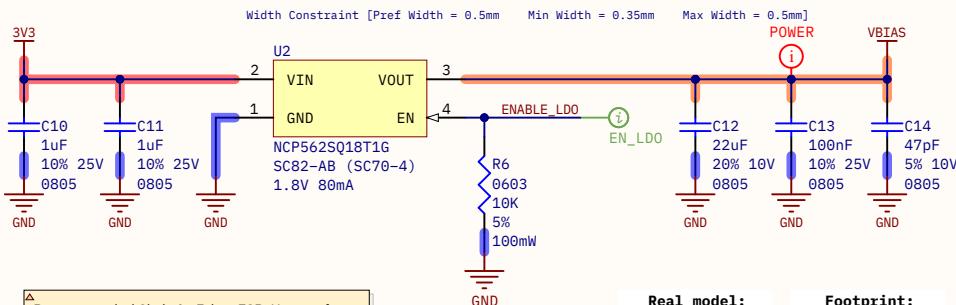


Typical Application Circuit. [AP3429/A datasheet, page 2] with some values modified as needed and/or part availability. Capacitors should be placed close to the chip and circuit should be traced in short loops. Feedback voltage V_{FB} is 0.6 V const.

Resistors are adjusted as a voltage divider. So, if 3.3V are needed at the converter output: $V_{FB} = 0.6V = V_{out} \cdot (R2)/(R1+R2) \rightarrow R2 = 2/9 \cdot R1$. Resistor values must be high (kOhms) in order to maintain a low power consumption on the feedback circuit.



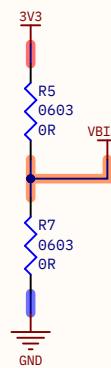
1.8 V rail: Vbias for signal conditioning circuit



Recommended C_{in} is 1 μ F, low ESR. Usage of multiple input capacitors to reduce ESR and ESL. There are no recommended values for C_{out} but these caps should probe more than enough to have low ESR and reduce ripple at a wide frequency range. Datasheet specifies a typical 100 μ Vrms noise on V_{out} , somewhat high.

Optional 1V8 rail bypass jumpers

IMPORTANT: 1V8 rail is bypassable by soldering these optional 0-Ohm resistors. This is for experimenting with different voltages and if it affects the overall performance of the acquisition circuit. Do NOT connect both OR resistors at the same time or it will jump VCC and GND. And keep the LDO disabled at all times.



This can also be used to insert a voltage divider. i.e.: if you want to reduce the rail voltage to $V_{CC}/2$ you only have to add two ≥ 10 KOhm 0603 resistors. Just keep in mind that voltage won't be as stable as in a LDO as it will be greatly dependent on the load impedance.

If you do this, populate the LDO's output caps, so VBIAS it behaves as a small-signal GND.

Power rails

Battery DC/DC step-down converter and Vbias for signal conditioning circuit.

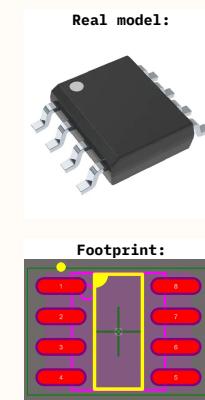
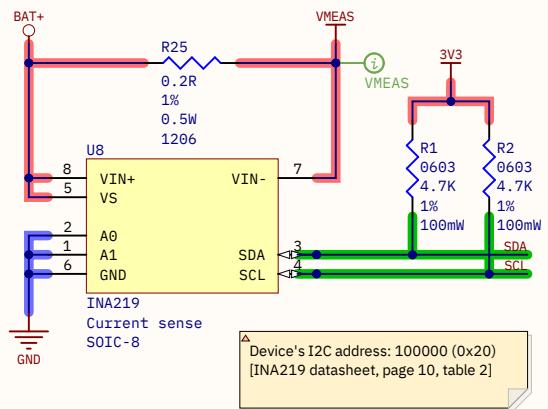
Designer's signature Supervisor: Sr. Andrés Roldán Aranda
Project title: TIK_HandheldDevice.PjPcb
Supervisor's signature Designer: Juan Del Pino Mena
Date: 2022-05-12 Revision: 0.4-WIP Sheet 7 of 20



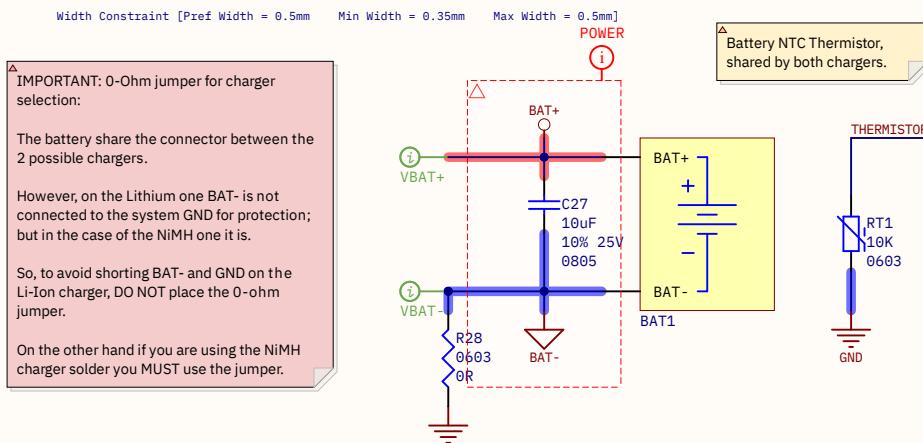
Battery charging circuit variants



Battery output current sense and voltage monitor

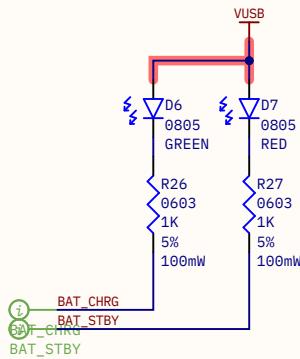


Battery connector. Charger selection jumper. Battery thermistor



Charging status indicator

These signals come from both charging IC's.
They are status outputs that are normally on high impedance and they are pulled LOW when activated.
We can use these pins to turn on some LEDs and to notify the microcontroller of the charging status.



Battery and current sense

Two circuit variants that will be implemented but not used simultaneously. The usage of one over the other will come by component disponibility. INA219 current sensor is independent and common for both systems.

Designer's signature
Supervisor's signature

Sheet title: **Battery and current sense**
Project title: **TIK_HandheldDevice.PjPcb**

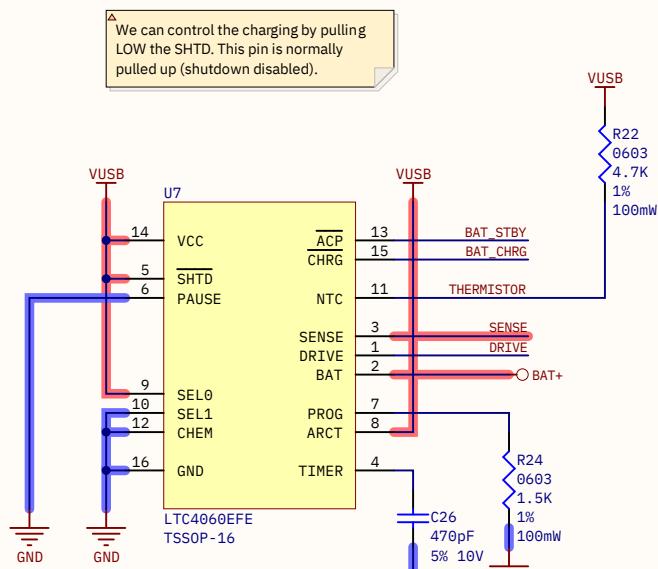
Designer: **Juan Del Pino Mena**

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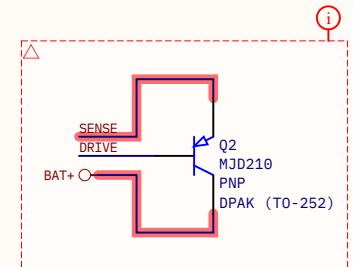


NiMH/NiCd battery charger IC



Width Constraint [Pref Width = 0.5mm Min Width = 0.35mm Max Width = 0.5mm]

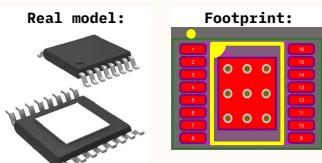
POWER



Following the [LTC4060 datasheet, page 13], if using a 10 K NTC thermistor, Its RHOT should be 4.42 k Ω , 1% to trigger the temperature warning at 45 °C. However, this value being too much specific is problematic.

This can be disabled by connecting a 0-ohm resistor in place of the thermistor.

[NOT IMPLEMENTED] This IC has the possibility of implementing a power path control (power the load from external source while charging)



TIMER capacitor and PROG resistor program the charge Tmax (maximum charging time, a security measure). [LTC4060 datasheet, page 13]. These values should complete a full charge in at most 1 h 6'

PROG resistor programs the maximum current that the battery will receive while charging. For 1.5 k Ω this is 0.93 A.
i.e.: a 1000 mAh battery will charge at approx 1C with this configuration, but can be insufficient time for a 3000 mAh one.

Battery charging circuitry for Ni-MH

Battery charger circuit variant #1. By default the device uses a Nickel-metal hydride battery which are chemically and thermally more stable (and safer) than Lithium-based ones; at the cost of a lower charge/volume ratio.

Designer's signature

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Sheet title: **Battery charger**
Project title: **TIK_HandheldDevice.PjPcb**

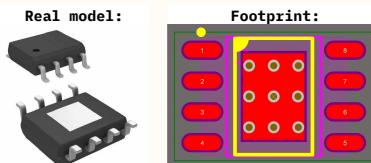
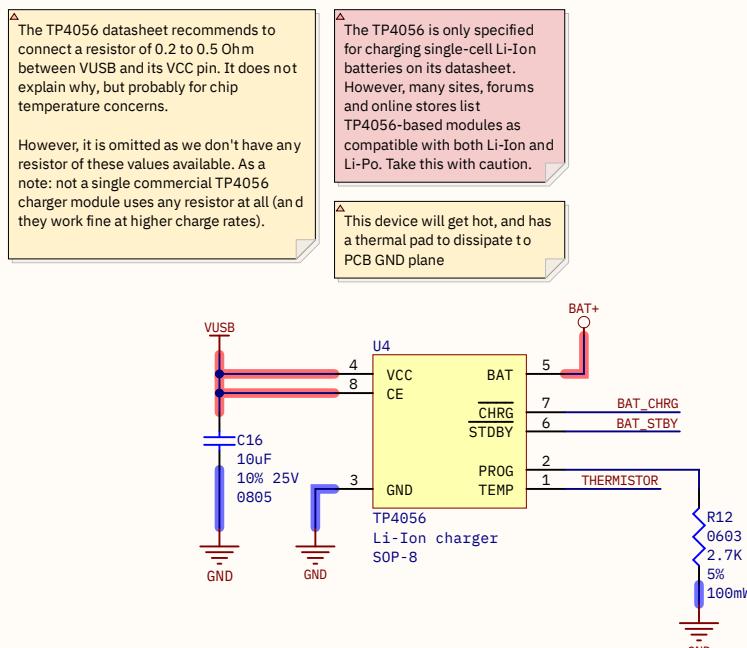
Desinger: **Juan Del Pino Mena**

Date: **2022-05-12** Revision: **0.4-WIP** Sheet 9 of 20

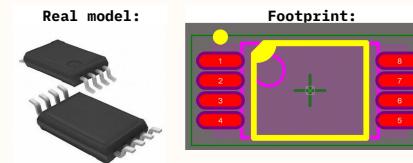
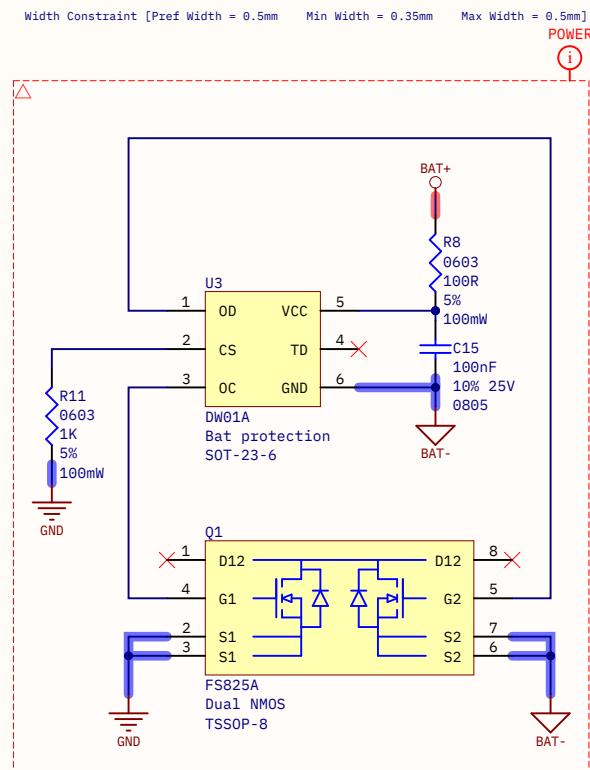
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Lithium battery charger IC



Lithium battery protection



Battery charging circuitry for Li-Ion

Battery charger circuit variant #2. Li-Ion and Li-Po batteries offer much more power density at the cost of instability. This circuit must NOT be placed if the Ni-MH charger is present on the board (and vice-versa).

Designer's signature

Supervisor's signature

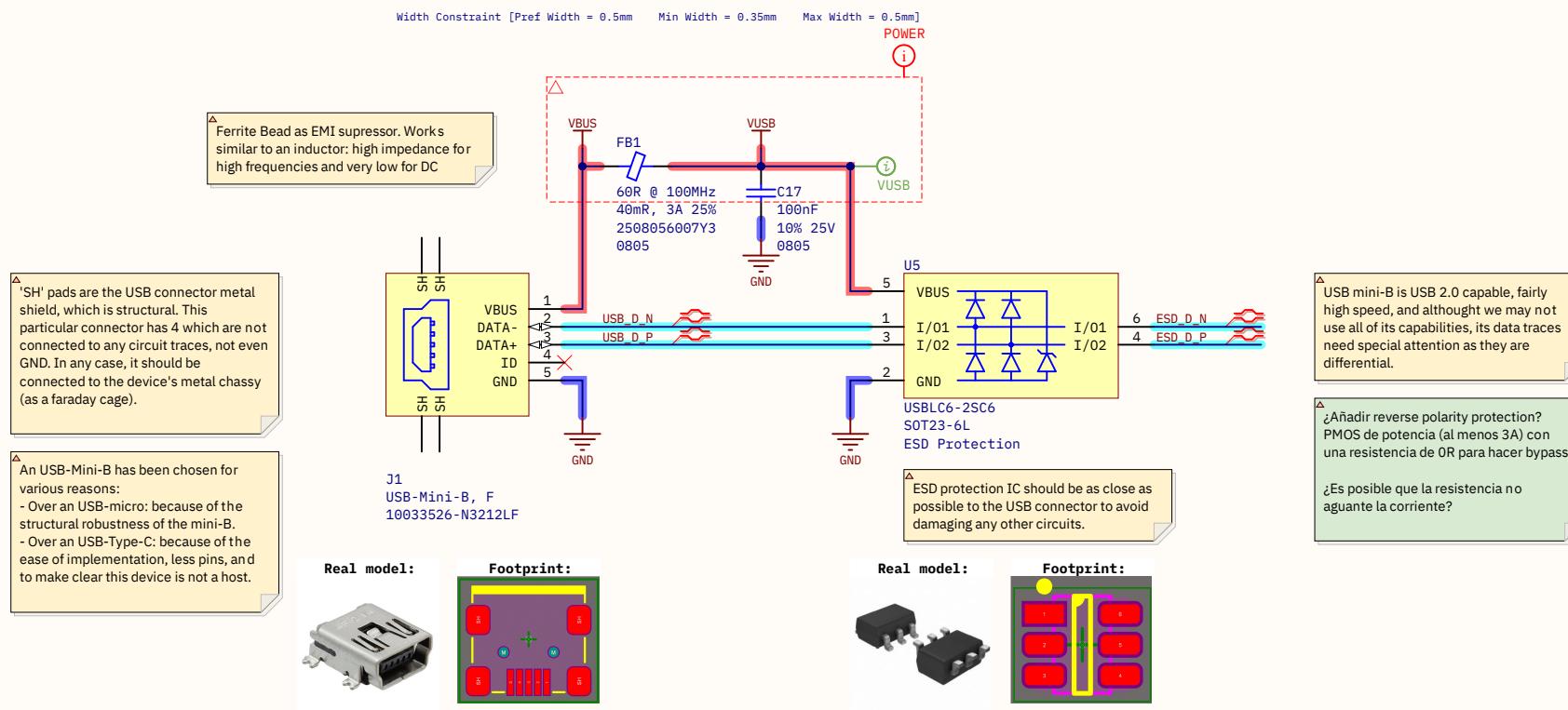
Sheet title: **Battery charger**
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Granada, Granada, Spain





USB connector and ESD protection circuit

USB is used as a programming interface, as well as a power source for the charging circuit. Since it's an external connector, it needs to have a protection circuit against electro-static discharge (ESD) and noise.

Designer's signature

Supervisor's signature

Sheet title: **USB connector and ESD protection circuit**

Project title: **TIK_HandheldDevice.PxjPcb**

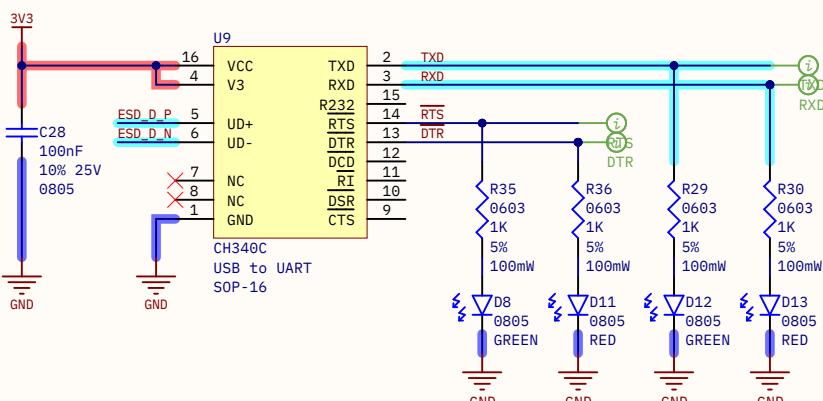
Designer: **Juan Del Pino Mena**

Date: **2022-05-12** Revision: **0.4-WIP** Sheet 11 of 20

Supervisor:
 Sr. Andrés Roldán Aranda
 Dpto. Electrónica y Tecnología
 de Computadores
 University of Granada
 C/Fuente Nueva, s/n. 18001
 Granada, Granada, Spain



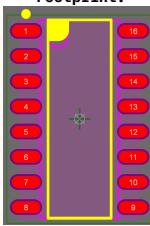
USB to UART conversion



Real model:



Footprint:



These LEDs serve as testimonies of
UART communication and help
during debugging process

USB to UART and MCU programming

*

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Designer's signature
Supervisor's signature

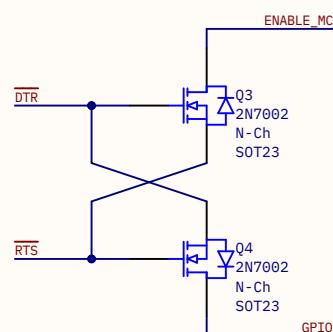
Sheet title: **USB to UART and MCU programming**Project title: **TIK_HandheldDevice.PjPcb**Designer: **Juan Del Pino Mena**Date: **2022-05-12**Revision: **0.4-WIP**

Sheet 12 of 20

Supervisor:
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Auto programming circuit



ESP32 GPIO0 is a Strapping pin. Strapping pins modify the device's boot mode during chip reset (enable pin pulled down)
GPIO0 is pulled up during reset. ESP_ENABLE is pulled up by an external pullup resistor

When GPIO0 is HIGH, it boots from internal SPI memory, but when it's LOW the boot sequence changes to 'Download' and we can upload a program to the MCU.

[ESP32 Datasheet, section 2.4, pages 19-20]

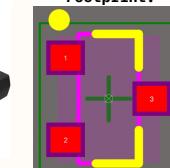
DTR	RTS	ENABLE_MCU	GPIO0	EFFECT
0	0	1	1	Download boot
0	1	1	0	SPI boot
1	0	0	1	
1	1	1	1	

*(DTR, RTS active low)

Real model:

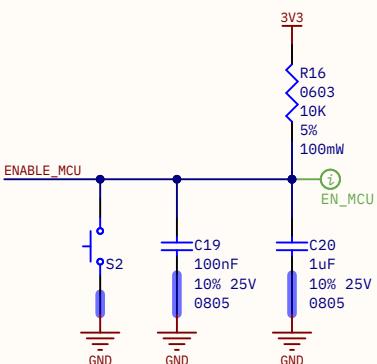


Footprint:



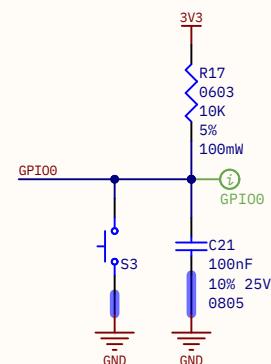
Reset

To ensure power stability to the microcontroller during powerup, this RC filter introduces a delay on the ENABLE pin. Usual values are $10\text{ k}\Omega$, $1\text{ }\mu\text{F}$ ($\tau = 10\text{ ms}$, $t_{\{10-90\}} = 22\text{ ms}$). [ESP32-WROOM-32D datasheet, page 22]



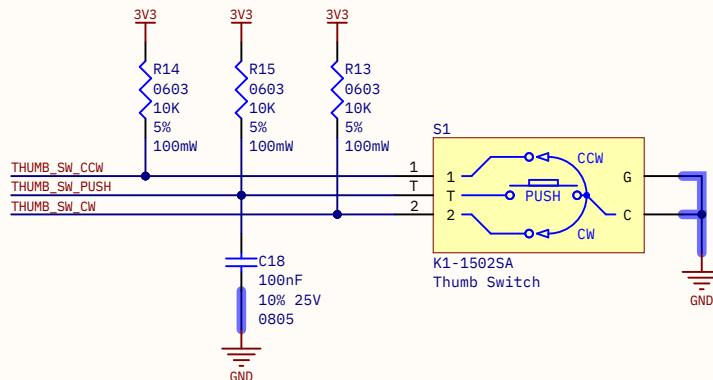
Boot mode selection (debug)

Allows to force 'Download' boot sequence
Same design as in ESP32 DevKit boards.
100 nF cap are for debouncing and should be placed close to the buttons



Multidirection 'thumb' button (UI navigation)

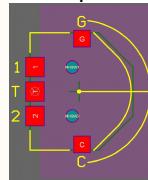
Horizontal SMD device, multi-directional / muti-function rotary slider button. Accessed from the right side.



Real model:



Footprint:



Buttons

TIK buttons. Some of them are meant for debugging like boot mode selection and reset, and will not be accessible to the end user. The power-up button and the "thumb" button are meant to be part of the UI.

Designer's signature
Supervisor's signature

Sheet title: **Buttons**
Project title: **TIK_HandheldDevice.PjPcb**

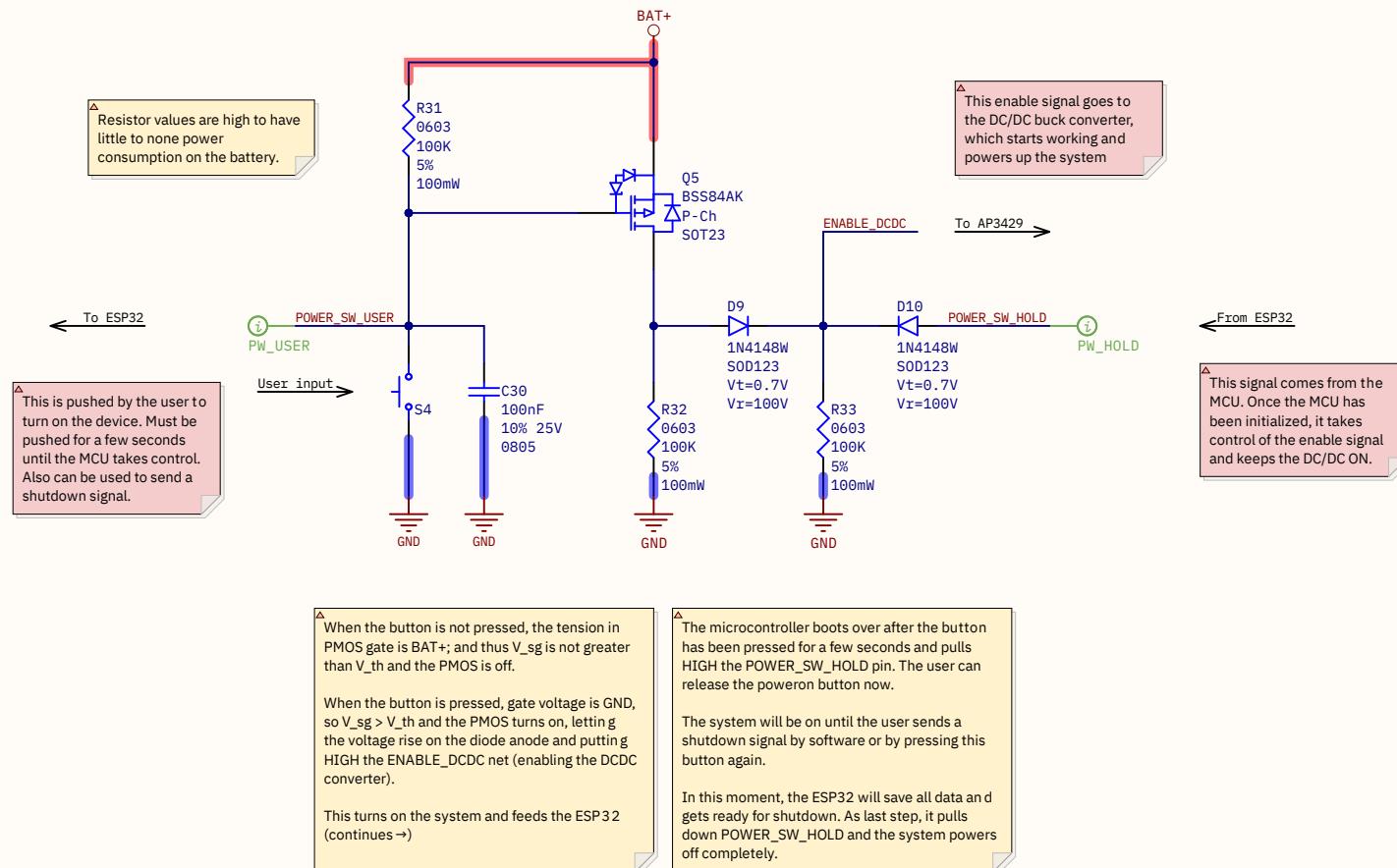
Designer: **Juan Del Pino Mena**

Date: **2022-05-12** Revision: **0.4-WIP** Sheet 13 of 20

Supervisor:
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A



Powerup button

This circuit avoids using a power-up switch, which can shutdown the device without prior warning. The user pushes a button during a couple of seconds, in which the ESP32 will boot and keep the system on until a shutdown signal is sent.

Designer's signature
Supervisor's signature

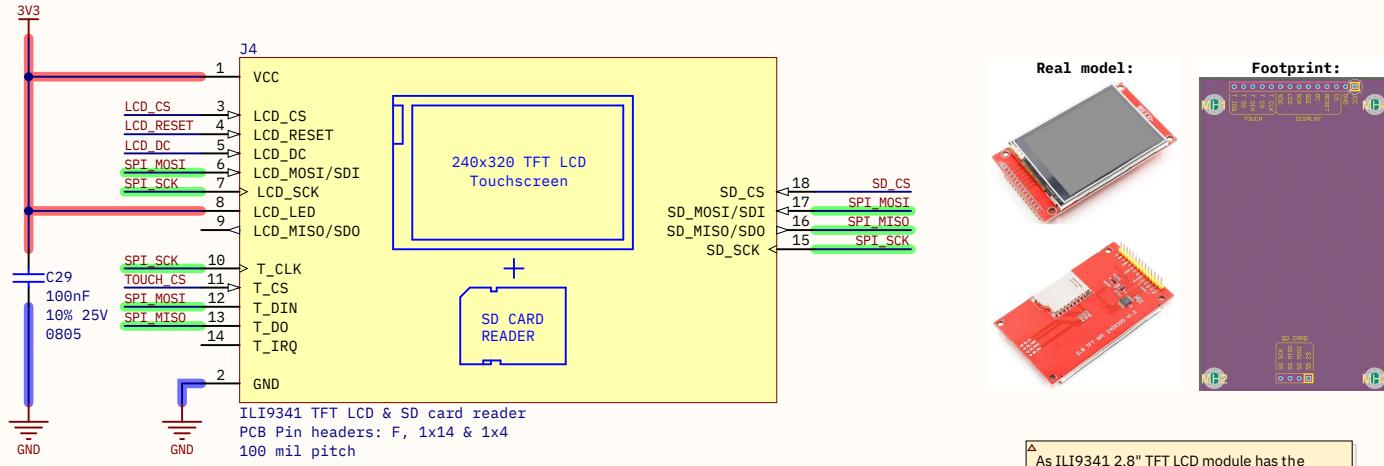
Sheet title: **Powerup button**
Project title: **TIK_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

Date: **2022-05-12** Revision: **0.4-WIP** Sheet 14 of 20

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LCD TFT touchscreen & SD card reader

TIK uses an ILI9341 2.8" TFT LCD display module as a graphic user interface. This module has touchscreen capabilities and also integrates a SD card reader on one of its sides. All three elements are managed via SPI.

Designer's signature
Supervisor's signature

Sheet title: **LCD TFT touchscreen & SD card reader**

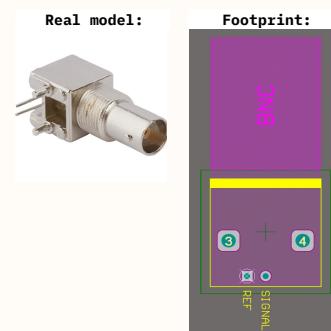
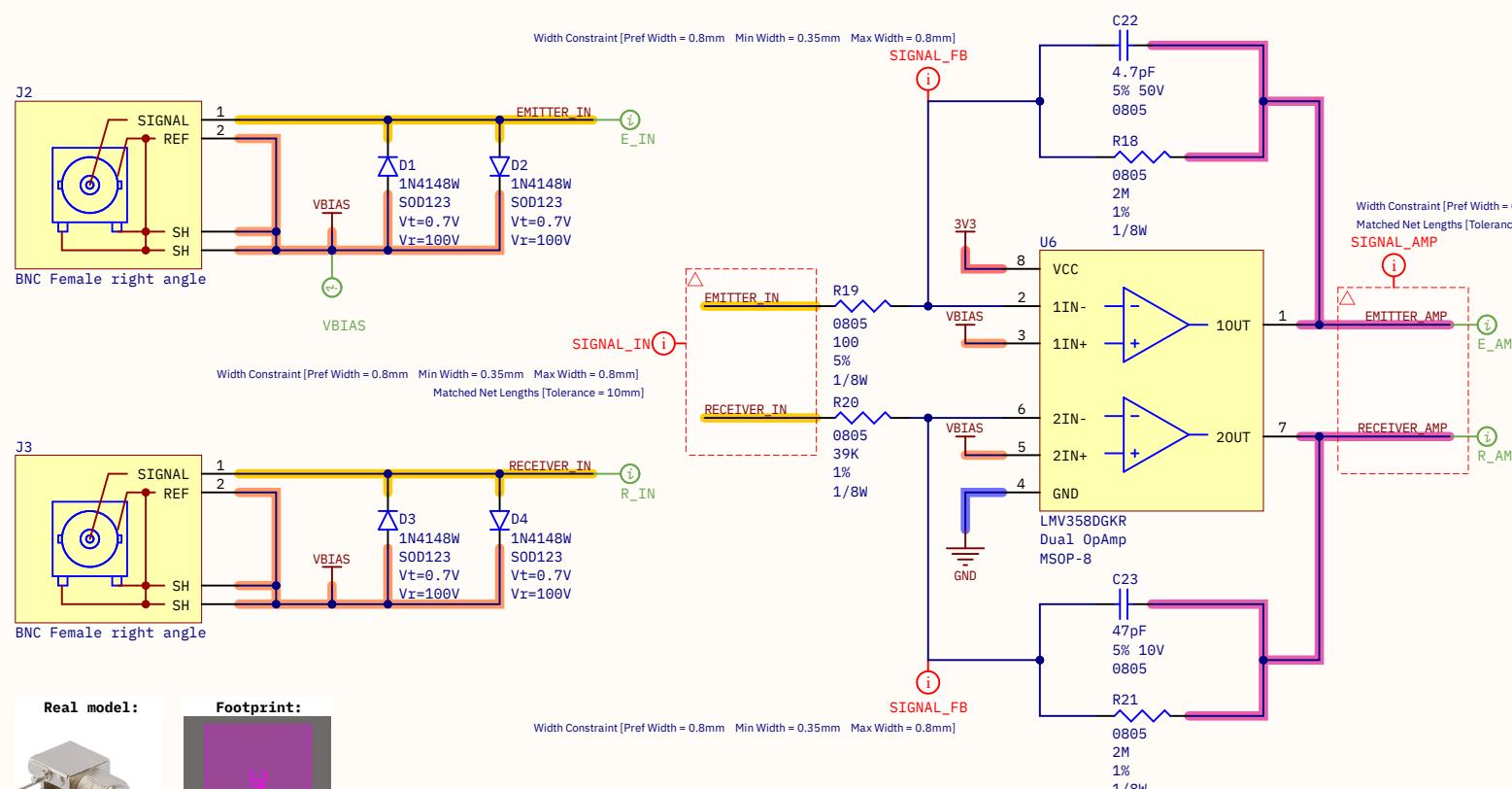
Project title: **TIK_HandheldDevice.PjPcb**

Designer: **Juan Del Pino Mena**

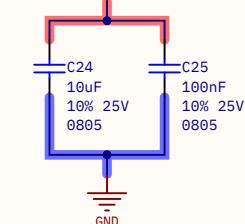
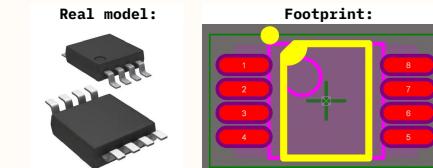
Date: **2022-05-12** Revision: **0.4-WIP** Sheet 15 of 20

Supervisor:
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Emitter signal will be in the range of 15 V to 100 V and need to be clipped. Then, the OpAmp will amplify by perceived by the instrument as a flank; whereas receiver signal most likely will be amplified without any clipping.



Piezoelectric sensors conditioning circuit

Two analog signals come from two piezoelectric sensors nailed into a tree or trunk. The way piezos work force us to use this circuit to convert charge into voltage. The piezo sensors used generated upto -100 V peak, so it needs clipping

Designer's signature
Supervisor's signature

Sheet title: Piezoelectric sensors conditioning circuit

Project title: TIK_HandheldDevice.PjPcb

Designer: Juan Del Pino Mena

Date: 2022-05-12

Revision: 0.4-WIP

Sheet 16 of 20

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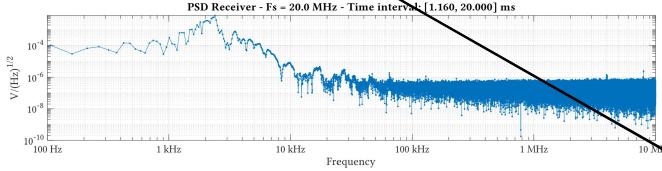
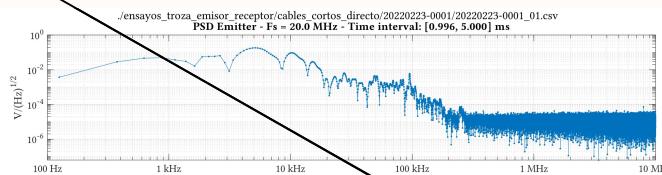
SIGNAL_CONDITIONING_SIMULATIONS
signal_conditioning_simulations

These are two charge mode amplifiers. This circuit is meant for sensors which are physically far from the acquisition system. It mitigates the effect of cables' capacitance.
[James Karki (Texas Instruments)
"Signal Conditioning Piezoelectric Sensors". Application Report
SLOA033A. September 2000]

This OpAmp is meant for low voltages, low power, single-supply and it has its own ESD protection.

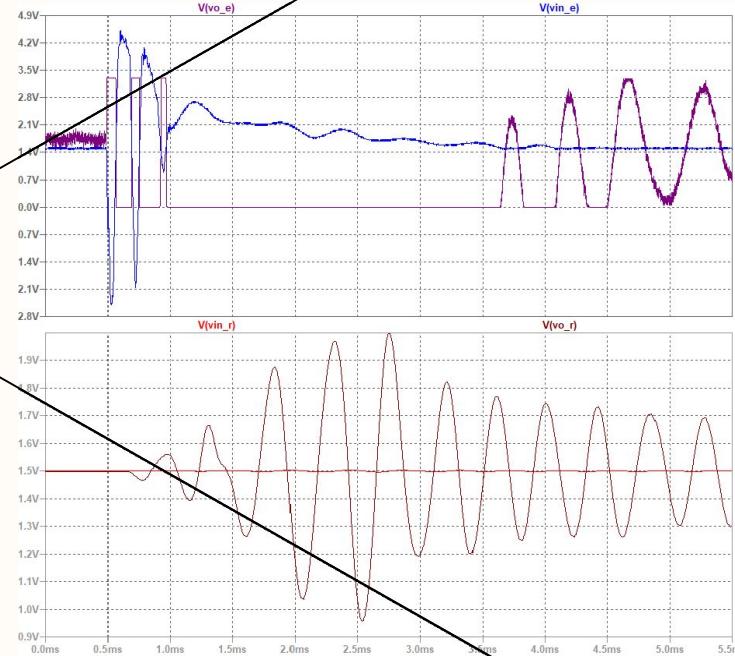
Bypass caps for the OpAmp, should be physically close to its power pins.

Example of a Voltage Spectral Density of trunk signals

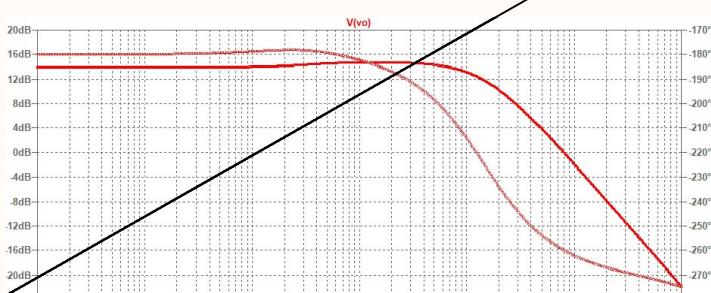
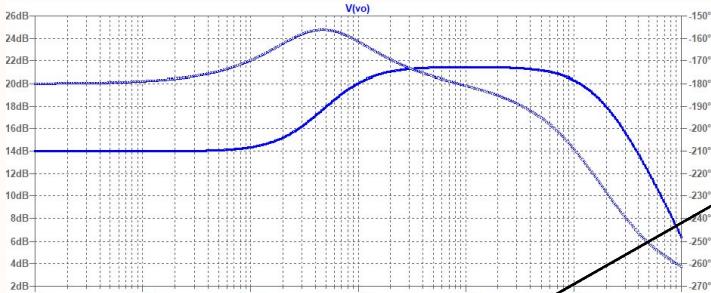


A REVISAR Y REPETIR EN ALTIUM

Time behavior



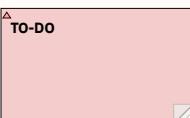
Conditioning circuit theoretical frequency response



Respuesta en frecuencia teórica, con el modelo UniversalOpAmp, cable con 700 pF y R del piezo 2 M Ω
¿Afecta en algo la fase?

Signal conditioning theorecticals

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*



Designer's signature
Supervisor's signature

Sheet title: Signal Conditioning Theorecticals

Project title: TIK_HandheldDevice.PxjPcb

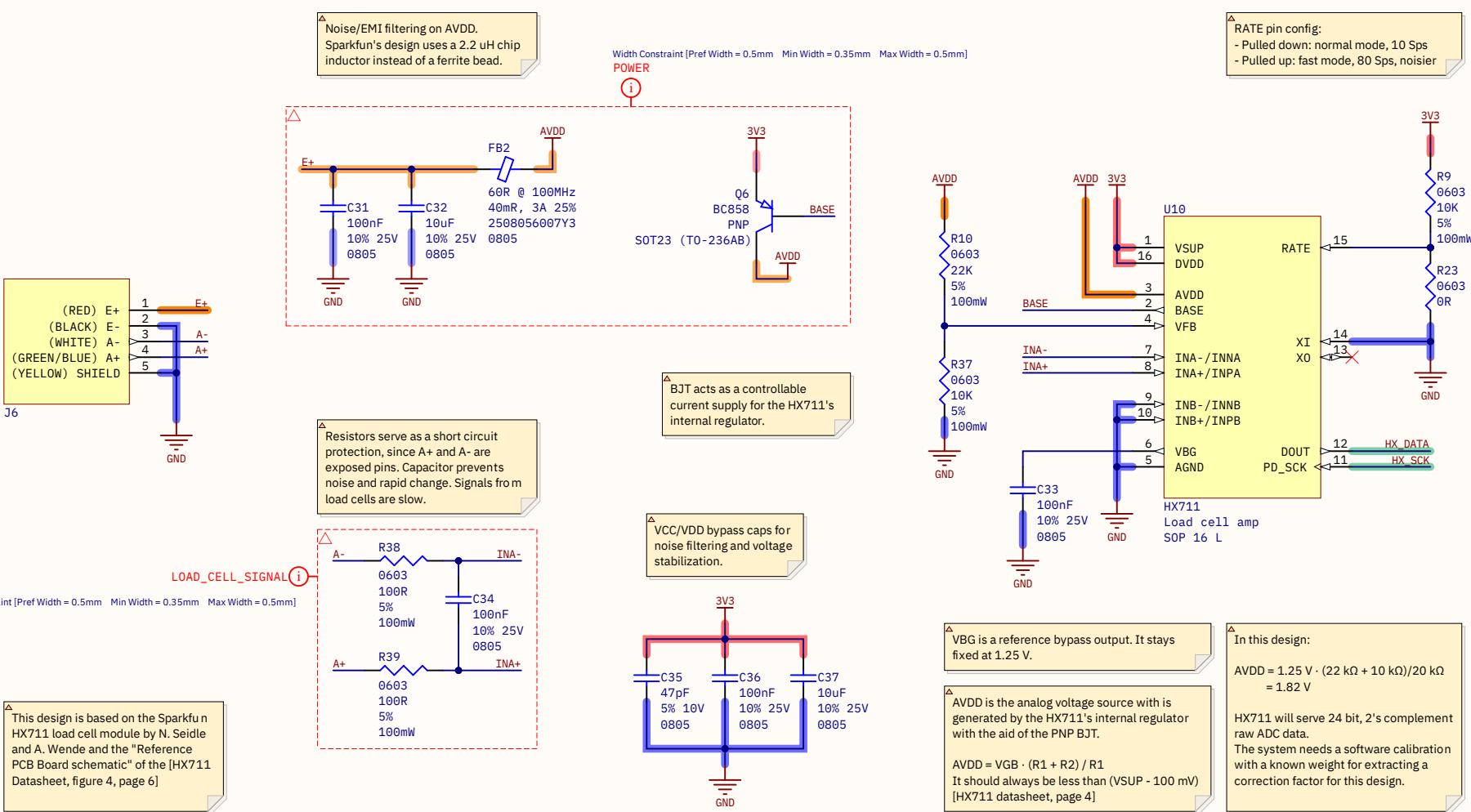
Desinger: Juan Del Pino Mena

Date: 2022-05-12 Revision: 0.4-WIP Sheet 17 of 20

Supervisor:
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A



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Supervisor's signature

Sheet title: **HX711 load cell amplifier**
Project title: **TIK_HandheldDevice.PjPcb**
Designer: **Juan Del Pino Mena**
Date: **2022-05-12** Revision: **0.4-WIP** Sheet 18 of 20

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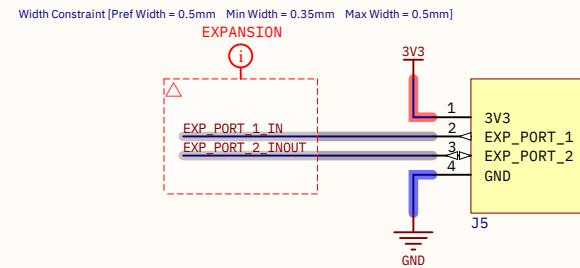
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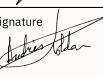
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D



Expansion port

Expansion port for added functionality, such as an ultrasould resonance analysis for wood boards.

Designer's signature 
Supervisor's signature 

Sheet title: Expansion port
Project title: TIK_HandheldDevice.PjPcb

Designer: Juan Del Pino Mena

Date: 2022-05-12 Revision: 0.4-WIP Sheet 19 of 20

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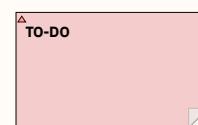
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Power budget

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Designer's signature

Supervisor's signature

Sheet title: **Power budget**

Project title: **TIK_HandheldDevice.PxjPcb**

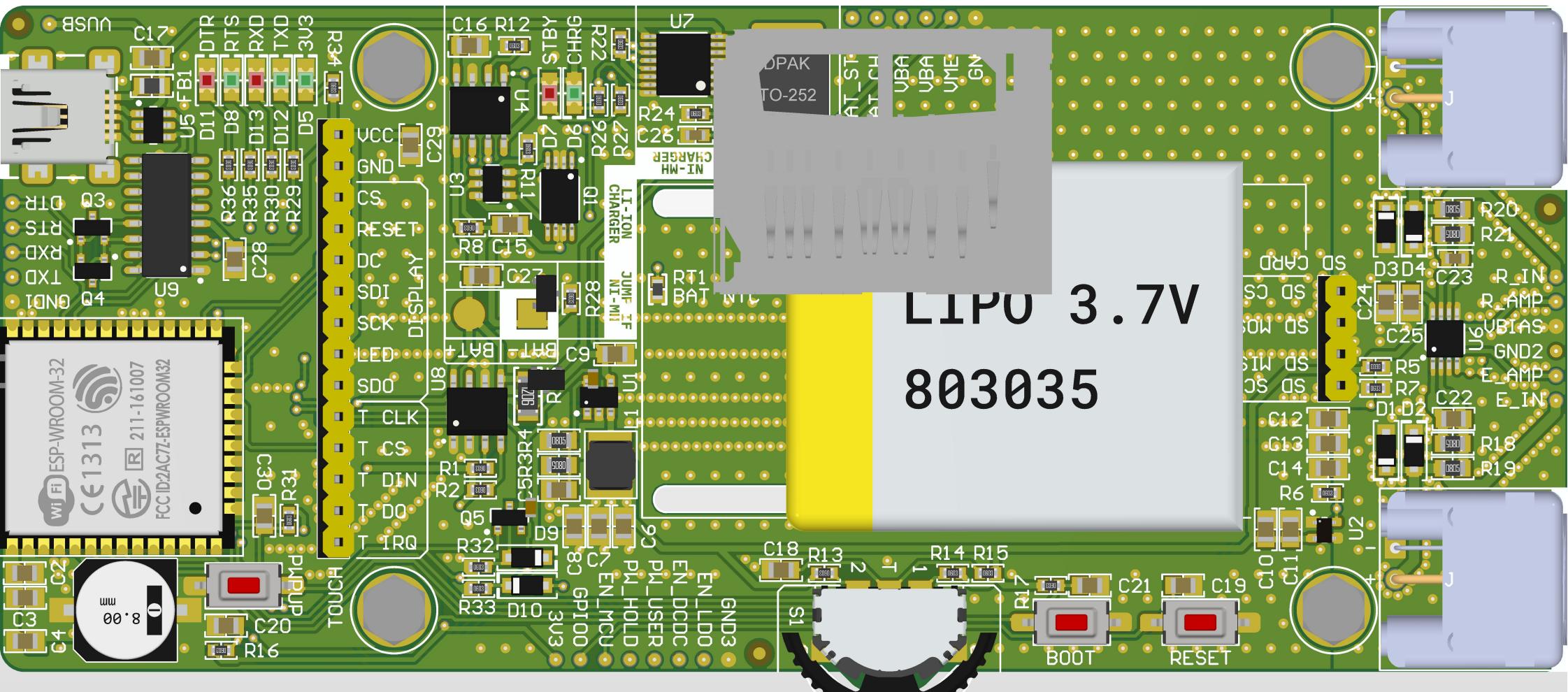
Designer: **Juan Del Pino Mena**

Date: **2022-05-12** Revision: **0.4-WIP** Sheet 20 of 20

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LITPO 3.7V
803035



**RECEIVER
[STOP]**

**EMITTER
[START]**

TIK handheld device

2022-05-12 rey 0.4-WIP

Juan Del Pino Mena github.com/dpmj



THUMB BUTTON

SD CARD SLOT

BAT_STBY
BAT_CHRG
UBAT+
UBAT-
UIMEAS
GND4

R_IN
R_AMP
UBIAS
GND2
E_AMP
E_IN
SD_CARD
SD_CS
SD_MOSI
SD_MISO
SD_SCK



GND3

EN_LDO

EN_DCDC

PUL_USER

PUL_HOLD

EN MCU

GP100

3V3

DISPLAY

Touch

UCC
GND

CS
RESET
DC
SDI
SCK
LED

SDO
T_CLK
T_CS
T_DIN
T_DO
T_IRQ



✓ RoHS
Pb-free

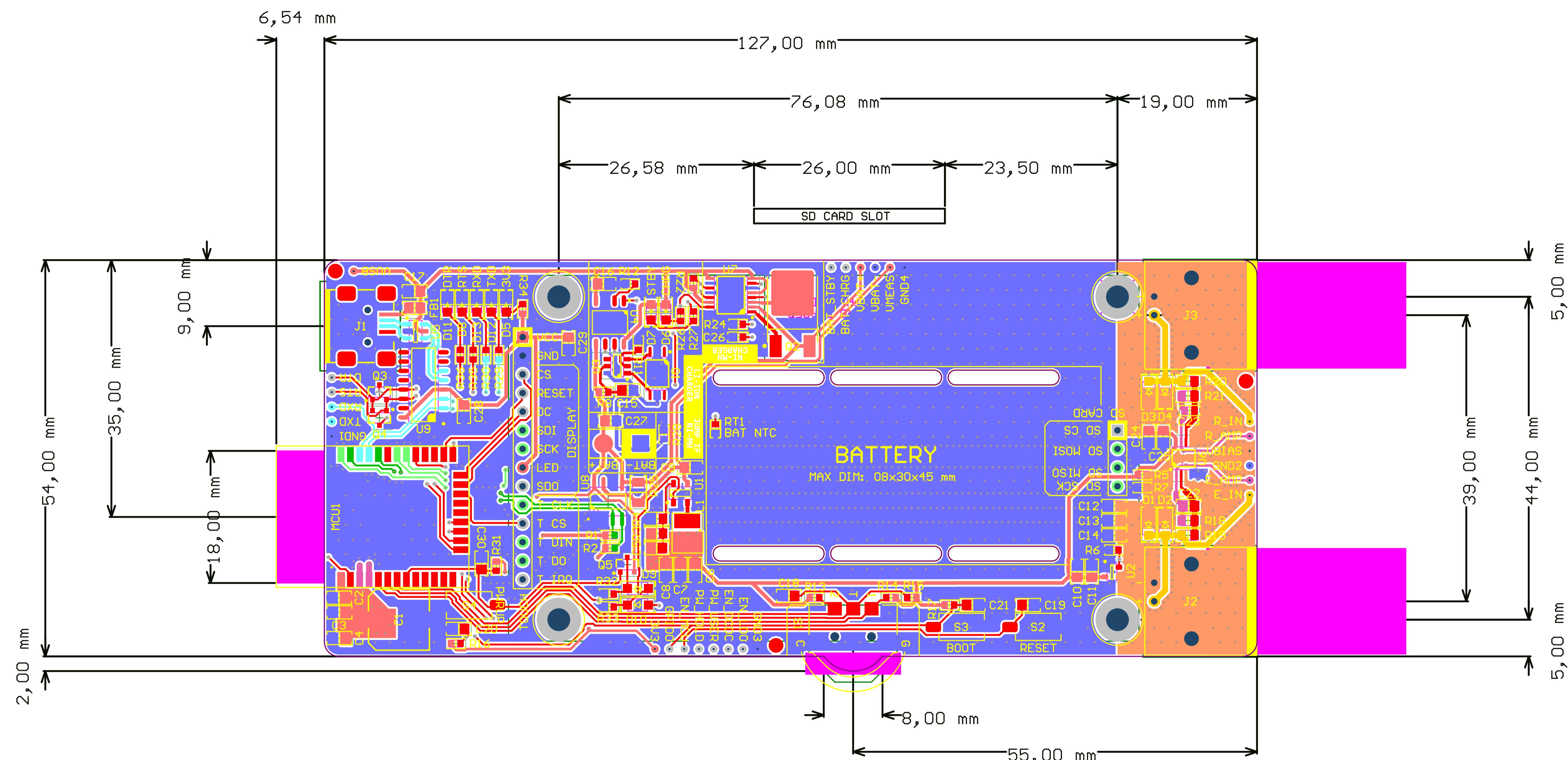


USB

USB

ESP32 ANTENNA

A

**VISIBLE LAYERS:**

Board outline + Multilayer + Top overlay + Mechanical 15 + Top layer + Keep-out + dimensions

TRACKS & POLYGONS COLOR LEGEND:

EMITTER/RECEIVER ANALOG SIGNALS	POWER REFERENCE GND/BAT-	SPI
GENERIC NET ON TOP LAYER	POWER RAIL 3V3/BAT+/VUSB/VMEAS/VSENSE	I2C
GENERIC NET ON BOTTOM LAYER	POWER RAIL VBIAS	SERIAL UART/USB

TIK handheld device PCB

PCB orientation: vertical. Screen facing front, BNCs on top, USB at the bottom, SD Card reader at the left, powerup button at the bottom front right, and multipurpose button on the right side.

Designer's signature:

Sheet title: TIK Handheld Device PCB

Supervisor's signature:

Project title: TIK_HandheldDevice

Designer: Juan Del Pino Mena

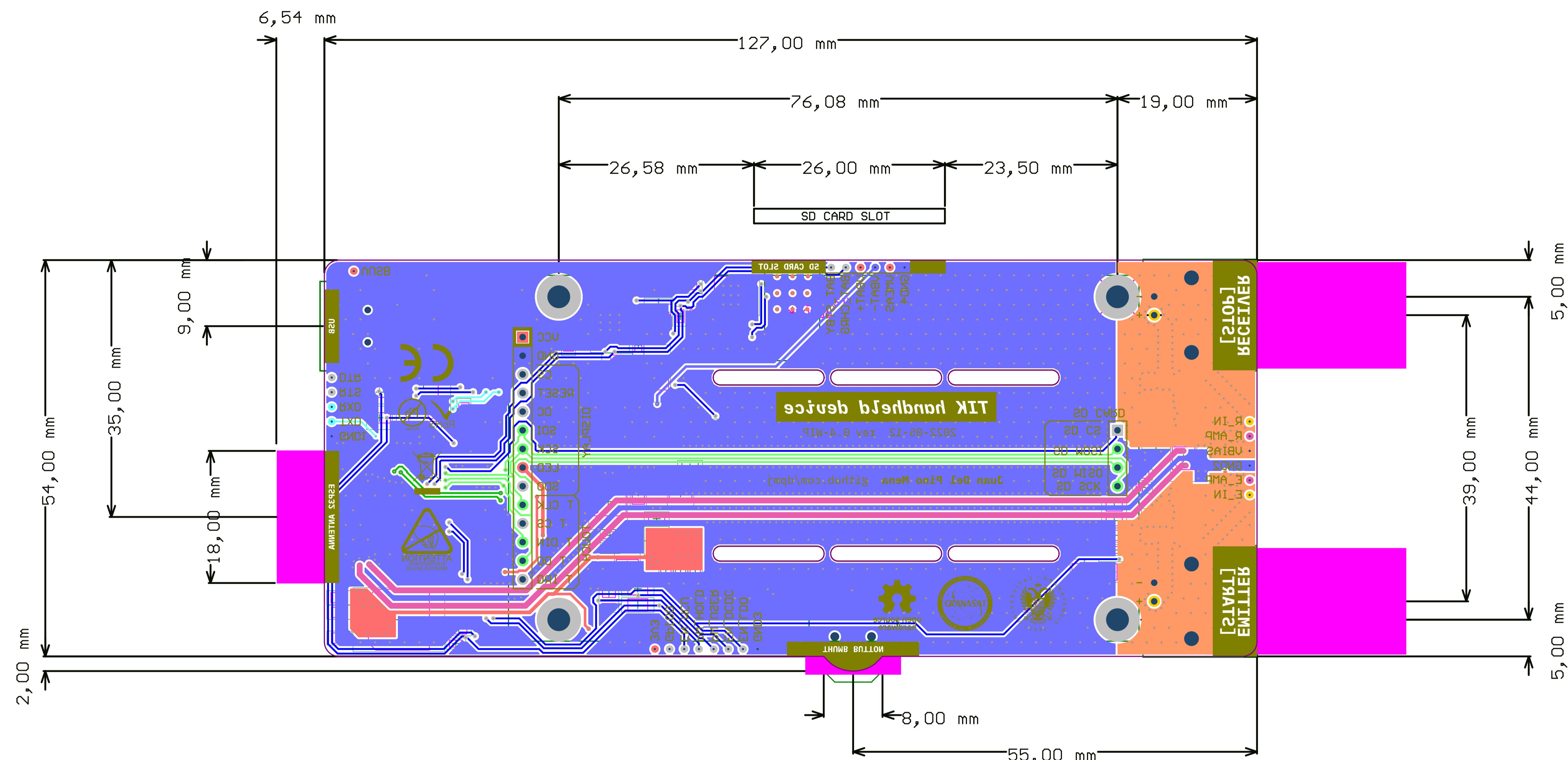
Supervisor: Andres Roldan Aranda

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Sr. Andres Roldan Aranda

Date: 2022-05-12
Revision: 0.4-WIP Sheet 1 of 1



A

**VISIBLE LAYERS:**

Board outline + Multilayer + Bottom overlay + Bottom layer + Keep-out + dimensions

TRACKS & POLYGONS COLOR LEGEND:

EMITTER/RECEIVER ANALOG SIGNALS	POWER REFERENCE GND/BAT-	SPI
GENERIC NET ON TOP LAYER	POWER RAIL 3V3/BAT+/VUSB/VMEAS/VSENSE	I2C
GENERIC NET ON BOTTOM LAYER	POWER RAIL VBIAS	SERIAL UART/USB

TIK handheld device PCB

PCB orientation: vertical. Screen facing front, BNCs on top, USB at the bottom, SD Card reader at the left, powerup button at the bottom front right, and multipurpose button on the right side.

Designer's signature:

Sheet title: TIK Handheld Device PCB

Supervisor's signature:

Project title: TIK_HandheldDevice

Designer: Juan Del Pino Mena

Supervisor: Andres Roldan Aranda

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Date: 2022-05-12
Revision: 0.4-WIP Sheet 1 of 1



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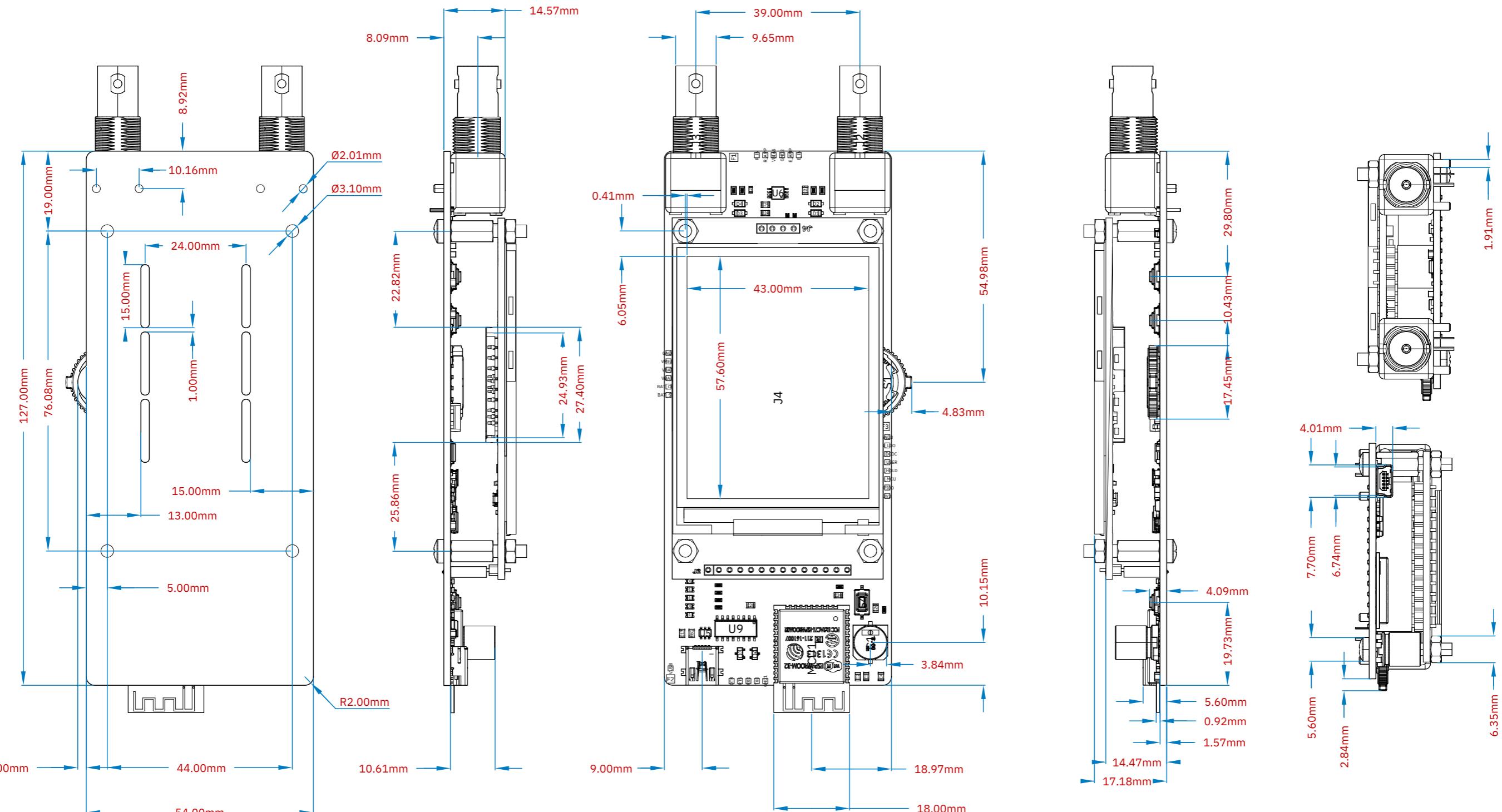
D

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PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: Juan Del Pino Mena 2022-05-14

DESIGNER: Juan Del Pino Mena 2022-05-14

CHECKER: Juan Del Pino Mena 2022-05-14

Reference Documents

BOM DOC: BOM/bill_of_materials

ASSY DOC: --

SCH DOC: SCH/*

NEXT ASSY: PCB/TIK_PCB.PcbDoc

PCB DOC: PCB/TIK_PCB.PcbDoc

APPLICATION

Dpto. Electrónica y
tecnología de computadores
University of Granada, Spain
C/ Fuente Nueva, s/n, 18001

GRANASAT

Design Item: Item
Design Item Revision: 4
Title: TREE INSPECTION KIT MECHANICAL DRAFTS

Size: A3
Cage Code: --
DWG NO: 1
Rev: 4

Scale: 1:1
File Name: TIK_PCB.PCDBdwf
Sheet: 1 OF 1

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