

Submission of course activities

Mixed-Signal Hardware Design with KiCad
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Lesson 3 Part Selection

3.1 Part Selection For Your Own Design

Try to follow the part selection steps ('basics') outlined in this video to perform the part selection for your own, previous electronics project. Have your part selections changed from what you previously chose? Did you require additional components?

Last year, for my bachelor's thesis, I developed a portable device to capture and process signals from two piezoelectric sensors and display the result on an LCD screen. It was my first 'serious' PCB design. Due to my lack of experience and the limited stock in the lab I was working in, I chose some components that I would not use now:

- The microcontroller was an Espressif ESP32-WROOM-32D, not the latest, but a very popular μ C in the DIY world, and it had the processing power and wireless capabilities needed for the project. However, it's not very well maintained and documented (especially on the software side) and is not recommended for new designs (NRND).
- As the ESP32-WROOM-32D has no USB peripherals, a USB-to-UART converter was needed. Again, due to various constraints, I ended up using a CH340C, which proved to be very problematic. The USB port was a mini-USB, which is robust but discontinued.
- To save costs, the idea was to use the two ADC peripherals integrated in the ESP32-WROOM-32D to acquire from both sensors simultaneously. However, in order to sample at the required speed (about 200 kSps) it was essential to use DMA, but only one of the peripherals was capable of using it, so the sampling rate had to be reduced. I also found the acquisition period to be inconsistent.
- The device was powered by a Li-Po battery, and the charging circuitry was based on a TP4056. Although simple, it's a linear charger –so very inefficient– and had no power path control.

Today, I think an adequate replacement would be the ESP32-S3-WROOM-1 for both the ESP32-WROOM-32D and CH340C. If I ever needed a USB-to-UART converter, I would choose a Silicon Labs CP2102N or similar. As for the ADCs, a more reliable alternative is the ADS78XX series from Texas Instruments. The battery charger could be replaced by a switched mode charger such as the BQ25629 from TI. And the USB port should be updated to a Type-C.

3.2 Distributor Part Search

Go to other electronics distributor websites (DigiKey, Farnell, ...) and try out their part search using the example from the video. How do the part searches compare? Which one do you prefer?

They are very similar. For electronic components, I personally prefer Mouser and DigiKey to shops with a wider product range such as Farnell and RS Components because the search filters are more precise. However, for specialised products such as microcontrollers, DC/DC converters, sensors or ADCs, I prefer to select them directly from the manufacturer's website (STM, Analog, Microchip, TI...) and then search for stock and prices in online shops.

3.3 Microcontroller Choice

What microcontroller alternatives would you choose for this design? Are there any pin-to-pin compatible microcontrollers that could be used as a replacement?

In Mouser, setting the filter to: Manufacturer = STM, Data bus width = 32 bits, Clock Frequency = 48 MHz onwards, RAM = at least 20 kB, ROM = greater or equal than 128 kB and Power supply = from 2.4 to 3.6 V. Leaving the package and number of pins unchosen and sorting by price, the first microcontroller that appears in stock is the STM32F030CCT6. However, this μC lacks USB. Looking for similar chips on the manufacturer's website but with USB support, reveals the STM32F302C series, which are optimized for mixed-signal applications and could even replace the ADCs.

A pin-to-pin compatible, drop-in replacement for the STM32F103CBT6 would be any of the F1 or F3 series [1] with the same LQFP-48 package, like the STM32F302CBT6. The ability to reconfigure the STM32 pins helps to find alternatives in the same manufacturer. Also, there are clones of the popular STM32F103, e.g. the AIR32F103.

3.4 Data Converters

What alternative data converters (ADCs and DACs) would you choose that are suitable for this application?

ADC The basic requirements are: single-channel (or more if price is not affected), single-ended or differential, 12 bits, and at least 40 kSps, with SPI interface and support for 3.3 V. Some $\leq 2\text{ €}$ options gathered from Mouser:

- Microchip MCP33141D / MCP33151D
- OnSemi NCD98010 / NCD98011
- Texas Instruments ADS7826 / ADS7827 / ADS7829

DAC The requirements are identical to those of the ADC. Some inexpensive options are listed below:

- Analog Devices AD5601 / AD5611 / AD5621
- Microchip MCP48FVB2X / MCP48CXB2X
- Texas Instruments DAC7512

3.5 Power Supplies

If we use a linear, LDO regulator with a dropout voltage of +1V1 for all +3V3 rails in our design, what power loss would we suffer?

To calculate the dissipated power P_D in a LDO, it is necessary to consider the dropout voltage V_{DO} and the current passing through it I . In our case, $V_{DO} = 1.1\text{ V}$, but the current is undefined. Assuming $I = 0.1\text{ A}$:

$$P_D = V_{DO} \cdot I = 1.1\text{ V} \cdot 0.1\text{ A} = 0.11\text{ W} \quad (1)$$

3.6 Analogue Circuitry

Compare the Johnson noise of the three following resistors: 100 Ohms, 1k, and 10k. What is the combined Johnson noise of two resistors in parallel, and two resistors in series?

Johnson noise, also known as thermal noise, arises due to the thermal agitation of charge carriers in a resistive medium. It is characterized by its root mean square (RMS) voltage:

$$V_{\text{rms}} = \sqrt{4 \cdot k_B \cdot T \cdot R \cdot B} \quad (2)$$

- k_B is Boltzmann's constant ($\approx 1.38 \times 10^{-23}$ J/K).
- T is the temperature in Kelvin.
- R is the resistance in Ohms.
- B is the bandwidth in Hertz.

Assuming a room temperature of $T = 25^\circ\text{C} \equiv 298$ K and a normalized bandwidth ($B = 1$ Hz), the noise RMS voltage is 1.28 nV for 100 Ω , 4.06 nV for 1 k Ω , and 12.83 nV for 10 k Ω .

When combining two resistors, the noise will depend on their total resistance:

Series $R_S = R_1 + R_2$, so that $V_{\text{rms},S} = \sqrt{4 \cdot k_B \cdot T \cdot (R_1 + R_2) \cdot B}$. The sum of two resistances greater than zero will always be greater than either part, and since the noise is directly dependent on the resistance, it will also be greater.

Parallel $R_P = R_1 || R_2 = \frac{R_1 \cdot R_2}{R_1 + R_2}$, and so, $V_{\text{rms},P} = \sqrt{4 \cdot k_B \cdot T \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot B}$. As we know, the value resulting from the parallel of two resistors (non-zero and non-infinite) is less than the value of the resistors themselves, so the noise will be lower.

3.7 Surrounding Circuitry

Look up the differences between various ceramic capacitor types (X5R, Y5V, C0G, and so on). What are each's benefits and drawbacks?

There are different classes of capacitor dielectrics [2]:

Class 1 Temperature compensating capacitors. They have a predictable temperature coefficient and do not tend to suffer with aging.

Class 2 General purpose ceramic capacitors. They offer high capacitance values in a small size, but can be severely affected by temperature, voltage (both AC and DC), frequency and aging.

In a MLCC capacitor, the first character of the code indicates the lowest temperature that the capacitor can handle, the second character the maximum temperature, and the third character the maximum amount of capacitance change over the part's temperature range. A qualitative comparison between several common types of capacitors is shown below:

X5R Relatively high capacitance per unit volume and are cost-effective. Suitable for applications where moderate capacitance are needed. However, X5R capacitors have a significant capacitance change with temperature and voltage.

- Y5V** High capacitance. Commonly used for decoupling, where their capacitance shift with temperature and voltage are not critical. Their temperature operation range is reduced.
- Z5U** Similar to Y5V, but with narrowed operating temperature range.
- X7R** Good balance between temperature stability and capacitance values. Still not suitable for high-precision applications.
- C0G** Also called NP0 (Class 1). Very low capacitance drift over temperature variations and voltage biases. Low losses and high Q factors, suitable for precision applications. However, they tend to have lower capacitance values compared to class 2 capacitors. They can also be more expensive.

Lesson 4 How To Read A Datasheet and Circuit Design Introduction

Open the datasheet for the DAC IC used in this design. Is the datasheet arranged in a similar way? What are the key sections?

The datasheet of the DACxx6x series [3] is organised identically to the TLV62569 DC/DC converter one. This is partly because all IC datasheets follow a similar structure, and mainly because they are from the same manufacturer, Texas Instruments, which has very standardised documents. The key sections are:

1. Features
2. Applications
3. Description
4. Revision history
5. Device comparison table
6. Pin configuration and functions
7. Specifications
8. Detailed description
9. Application and implementation
10. Power supply recommendations
11. Layout
12. Device and documentation support
13. Mechanical, packaging and orderable information

Lesson 5 Schematic Design - Power Supply

5.1 RLC Filters

Using the online RLC filter tool, design an RLC low-pass filter that has a cut-off frequency of 100 kHz and damping ratio of 1.25. Inspect the frequency response, and note the inductor and resistor values. What capacitor size did you choose?

The data from above is entered in the RLC Low-pass Filter Design Tool hosted in Okawa Electric Design website [4]: cutoff frequency 100 kHz and damping ratio 1.25. The capacitor value is chosen as $C = 100 \text{ nH}$. Forcing the value of the coil and the resistor to be from commercial series, $R = 39 \Omega$ and $L = 22 \mu\text{H}$ are obtained, which are adequate values. The frequency response obtained is shown in Figure 1. Due to the constraint to stick to commercial values, the cut-off frequency has slightly shifted to 107.3 kHz.

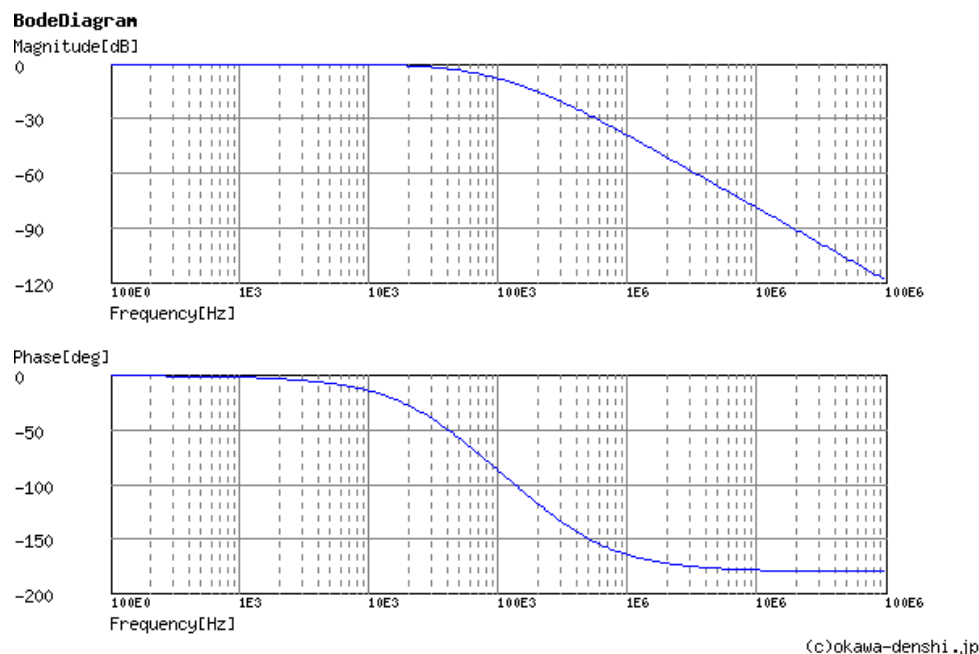


Figure 1 – Frequency response of the 100 kHz RLC filter designed in Okawa Electric Design website [4].

5.2 RC Filters

Cascade a high-pass RC filter with a low-pass RC filter, and set $R=1k$ for both and $C=1nF$ for both. What type of filter is the combined structure? What is the input impedance vs frequency?

Instead of using the online tool, it has been decided to use LTSpice in order to have more control over the information obtained from the circuit.

The filter resulting from the cascade of the two proposed high-pass and low-pass filters is a band-pass (see Figure 3). Due to the overlap of their cut-off frequencies, the passband attenuates the signal considerably (6 dB). The figure also depicts the input impedance as a function of frequency, which corresponds almost to that of the first stage: the high pass.

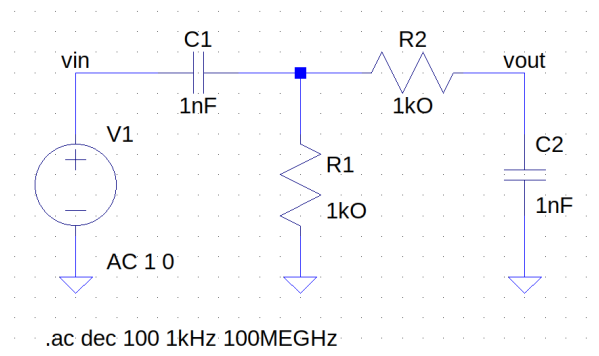


Figure 2 – Cascade of the high-pass CR and low-pass RC filters.

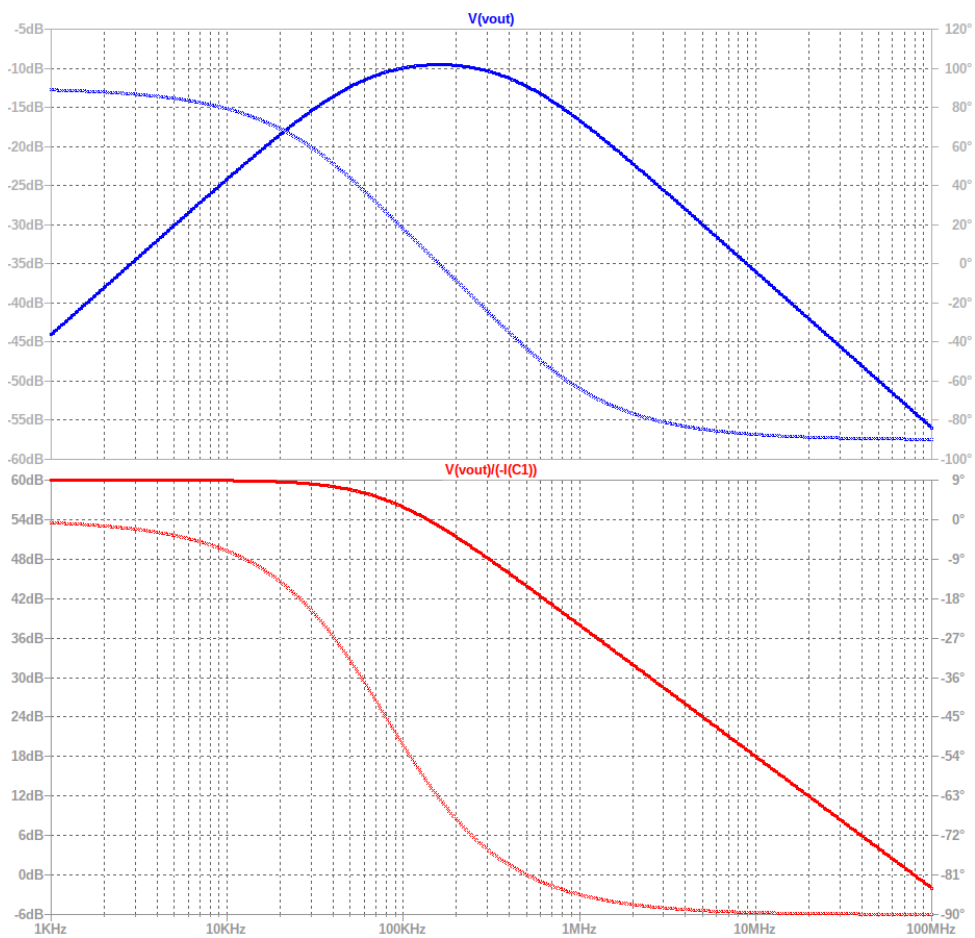


Figure 3 – Frequency response of the cascade CR-RC filters: Bode plot and input impedance.

Lesson 6 Schematic Design - Microcontroller, USB, SWD, and ESD Protection

Try to select a different STM32 microcontroller, download STM32CubeIDE, and do a rough pin-out planning given the constraints of this project.

In [subsection 3.3](#) we already discussed the STM32F302CBT6 as a suitable replacement for the STM32F103CBT6, since it comes in the same LQFP-48 package and has similar characteristics. After installing the STM32CubeIDE and creating a new project based on the STM32F302CBT6 microcontroller, the pin allocation takes place. See [Figure 4](#) for the result, which is pin-to-pin compatible with the pinout assignment performed in lesson 6.

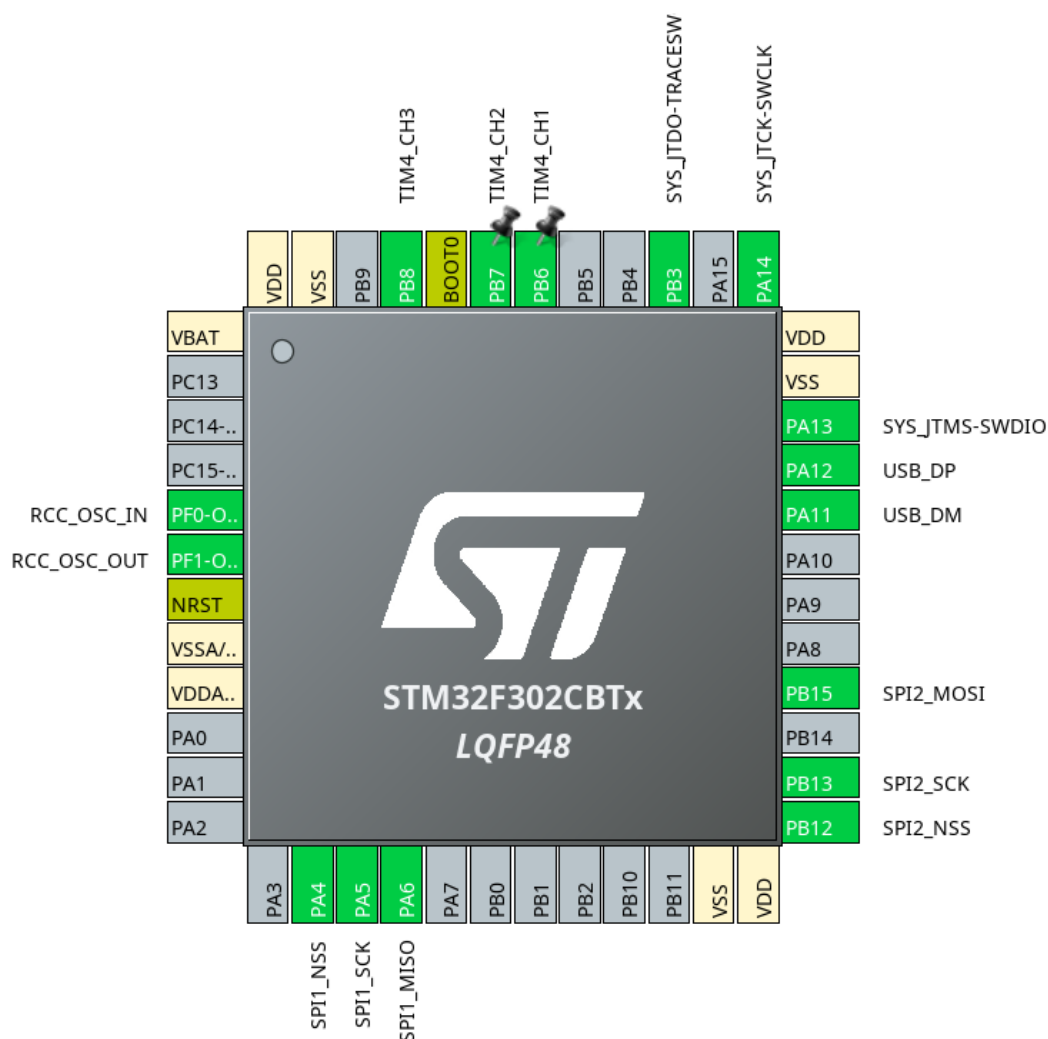


Figure 4 – STM32F302CBT6 rough pin planning.

Lesson 8 Final Schematic Tips, Footprint Selection, and Footprint Creation

Have a go at trying to make your own footprint for a different part (e.g. the buck converter IC) in KiCad using the datasheet as a guide.

Using the dimensions for the SOT-23-6 package in the TLV62569 DC/DC converter datasheet [5], KiCad's footprint wizard for SOIC packages, and the 3D model from Kirk Jess on 3DContentCentral [6], the footprint of the component has been synthesised, as shown in [Figure 5](#).

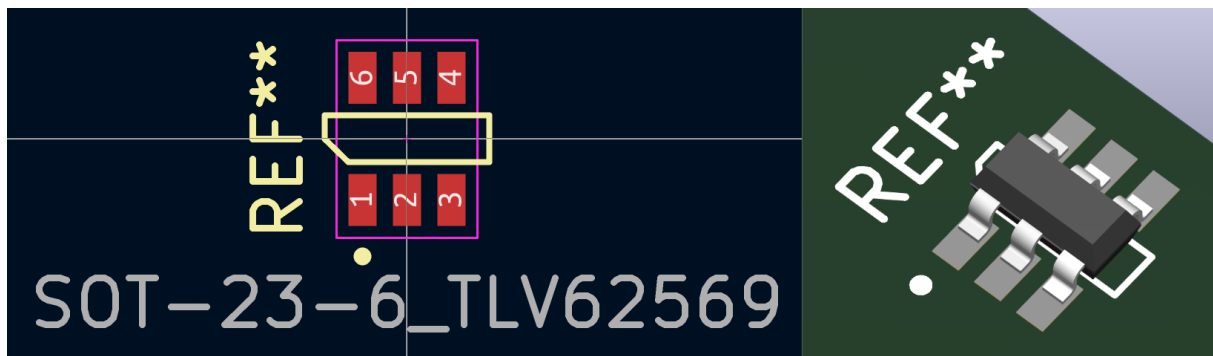


Figure 5 – 2D and 3D view of the TLV62569 footprint.

Lesson 9 Circuit Simulation with LTSpice

Download and install LTSpice, then try and perform a frequency response analysis of the 3rd order Butterworth anti-aliasing filter.

The simulated circuit comprises from the decoupling capacitor / high-pass filter at the input of the follower, up to the balanced output (Figure 6). The resulting frequency response is plotted in Figure 7. We can first observe the cutoff frequency of the high pass filter (which differs from the schematic, since it is 0.723 Hz and not 1.4 Hz). The passband extends up to its cut-off frequency of approximately 24 kHz. At 20 kHz there is an attenuation of about 1 dB. This filter is suitable for audio applications.

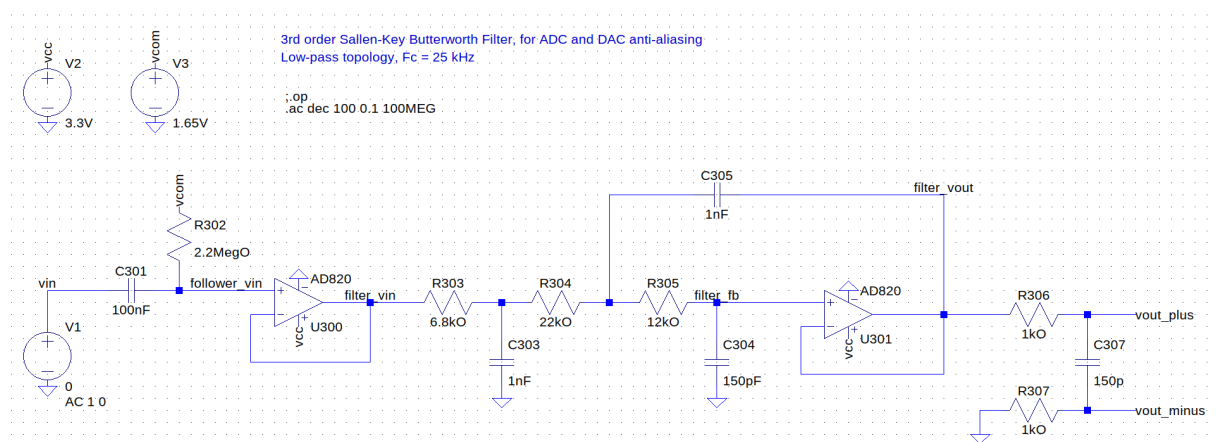


Figure 6 – Sallen-Key third-order butterworth filter circuit in LTSpice.

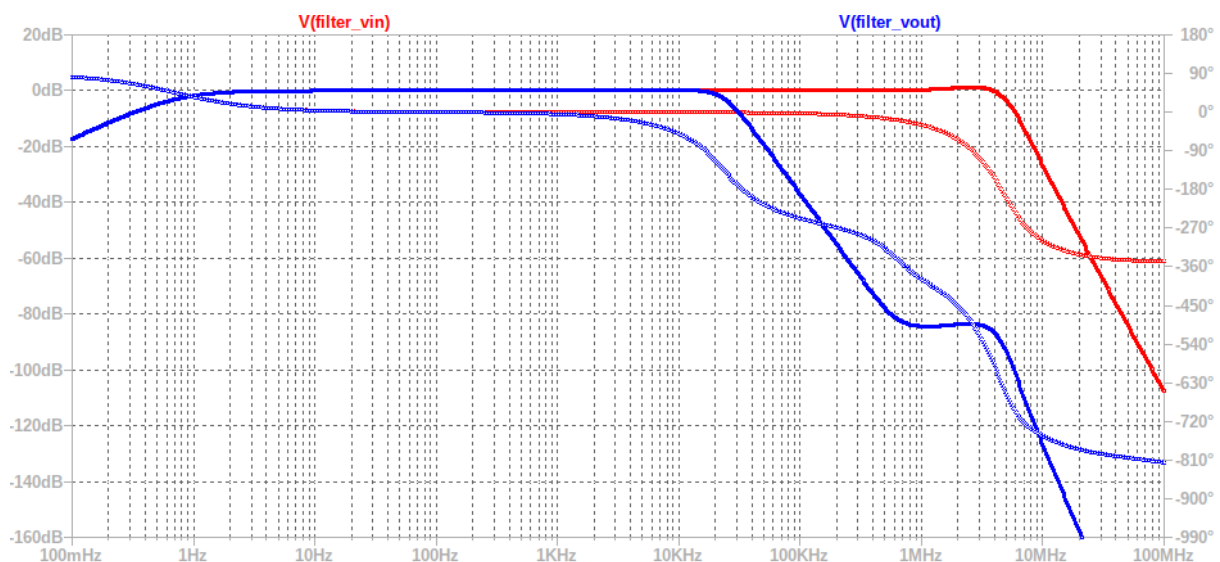


Figure 7 – Sallen-Key third-order butterworth filter frequency response in LTSpice.

Lesson 11 PCB - Design Rules and Set-Up

Using your own preferred PCB manufacturer's website, try and fill in all of the required design rules, as shown in the video, in KiCad.

I have decided to use EuroCircuits as the PCB manufacturer, being one that I have not used previously. Based on their documentation [7], [8], the 4-layer stackup from the Defined Impedance Pool has been chosen, and a pattern class 6 and drill class C PCB has been selected. The stackup and design rules have been specified in the KiCAD configuration as shown in the screenshots in Figure 8 and Figure 9. The board finish is ENIG. With the chosen stackup, a 90 Ω differential pair at the USB high-speed frequency has the dimensions shown in Figure 10.

Category	Parameter	Value	Unit
Copper	Minimum clearance:	0.15	mm
	Minimum track width:	0.2	mm
	Minimum connection width:	0	mm
	Minimum annular width:	0.13	mm
	Minimum via diameter:	0.4	mm
	Copper to hole clearance:	0.3	mm
	Copper to edge clearance:	0.25	mm
Holes	Minimum through hole:	0.3	mm
	Hole to hole clearance:	0.5	mm
uVias	Minimum uVia diameter:	0.2	mm
	Minimum uVia hole:	0.1	mm
Silkscreen	Minimum item clearance:	0	mm
	Minimum text height:	0.8	mm
	Minimum text thickness:	0.08	mm

Parameter	Value	Unit
Arc/circle approximated by segments		
Max allowed deviation:	0.005	mm
Note: zone filling can be slow when < 0.005 mm.		
Zone fill strategy		
<input type="checkbox"/> Allow fillets outside zone outline		
<input checked="" type="checkbox"/> Min thermal relief spoke count:	2	
Length tuning		
<input checked="" type="checkbox"/> Include stackup height in track length calculations		

Figure 8 – KiCAD board setup - Constraints

Copper layers: 4 ☒ Impedance controlled Add Dielectric Layer... Remove Dielectric Layer...

Layer	Id	Type	Material	Thickness	Color	Epsilon R	Loss Tan
F.Silkscreen		Top Silk Screen	Direct Printing		White		
F.Paste		Top Solder Paste					
F.Mask		Top Solder Mask	Liquid Ink	0.01 mm	Green	3.3	0
F.Cu		Copper		0.035 mm			
Dielectric 1		PrePreg	PR2116	0.12 mm	PTFE natural	3.69	0.02
In1.Cu		Copper		0.035 mm			
Dielectric 2		Core	FR4	1.2 mm	FR4 natural	4.5	0.02
In2.Cu		Copper		0.035 mm			
Dielectric 3		PrePreg	PR2116	0.12 mm	PTFE natural	3.69	0.02
B.Cu		Copper		0.035 mm			
B.Mask		Bottom Solder Mask	Liquid Ink	0.01 mm	Green	3.3	0
B.Paste		Bottom Solder Paste					
B.Silkscreen		Bottom Silk Screen	Direct Printing		White		

Board thickness from stackup: 1.6 mm Adjust Dielectric Thickness Export to Clipboard

Figure 9 – KiCAD board setup - Physical stackup configuration

Transmission Line Type

- ☐ Microstrip Line
- ☐ Coplanar wave guide
- ☐ Coplanar wave guide w/ ground plane
- ☐ Rectangular Waveguide
- ☐ Coaxial Line
- ☒ Coupled Microstrip Line
- ☐ Stripline
- ☐ Twisted Pair

Substrate Parameters

er: 3.69

tan δ: 0.02

p: 1.72e-08

H: 0.12 mm

H_t: 1e+20 mm

T: 0.035 mm

Roughness: 0 mm

μ(conductor): 1

Physical Parameters

W: 0.26 mm

S: 0.19 mm

L: 100 mm

Analyze ↓ Synthesize ↑

Electrical Parameters

Zeven: 54.8199 Ω

Zodd: 45.1094 Ω

Ang.L: 1.77411 rad

Results

Effective er (even): 3.00525

Effective er (odd): 2.73354

Conductor losses (even): 0.232704 dB

Conductor losses (odd): 0.282696 dB

Dielectric losses (even): 0.144421 dB

Dielectric losses (odd): 0.130913 dB

Skin depth: 2.95188 μm

Differential Impedance (Zd): 90.2519 Ω

Component Parameters

Frequency: 0.5 GHz

Odd Even

Figure 10 – KiCAD board setup - 90 Ω differential pair calculus

Lesson 12 PCB - Layout

I would strongly encourage you to start from the finished schematic (project files included in 'Lesson 1'), and follow along with the layout process - or even try to improve on the layout shown in the video. This step is needed to be eligible for a course certificate.

The missing 3D models from the BNC connectors, USB Type-C, ADC, DAC, buck converter inductor, and common-mode choke have been added. Some have been obtained from the built-in KiCAD library at \$KICAD7_3DMODEL_DIR/ whereas others are in \$KIPRJMOD/Juan_Footprints_Lib/3D/

Rather than following the video step by step and doing it exactly the same, I have decided to follow the recommendations but varying the layout by constraining the design to a PCB that fits a Hammond Manufacturing 1457C802EBK enclosure [9]. Clearance zones have been defined to prevent components from colliding with the housing and its rails.

The early layout is shown in Figure 11. A 3D view of the board is shown in Figure 12. The layout is divided into zones according to the schematic sheets, with enough space between them for easy routing.

Note: As the 1457C802EBK case is EMC/EMI shielded, an extra earth net has been added to the design to connect the mounting holes and the shield of the USB connector. Unfortunately, the BNC connectors can't benefit from this earth, as the metal structure is directly connected to GND.

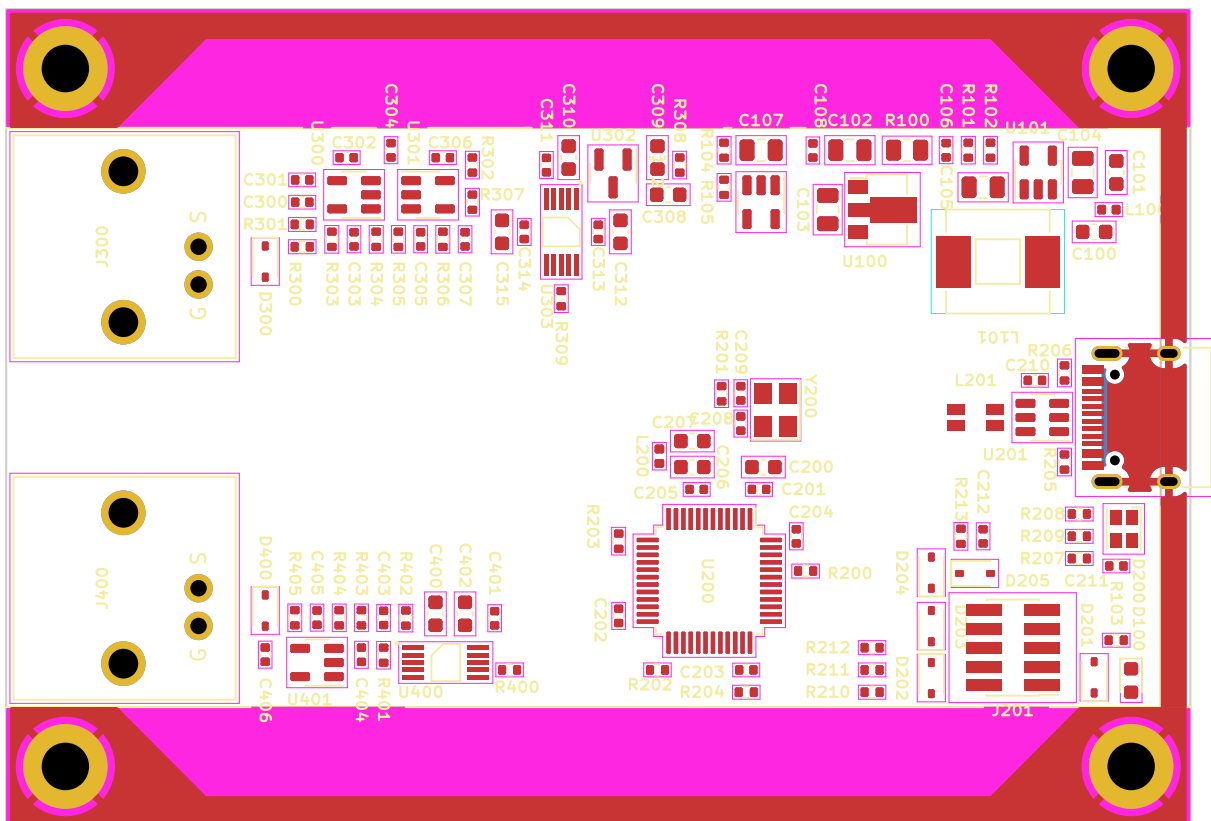


Figure 11 – Preliminary layout of the board – 2D view

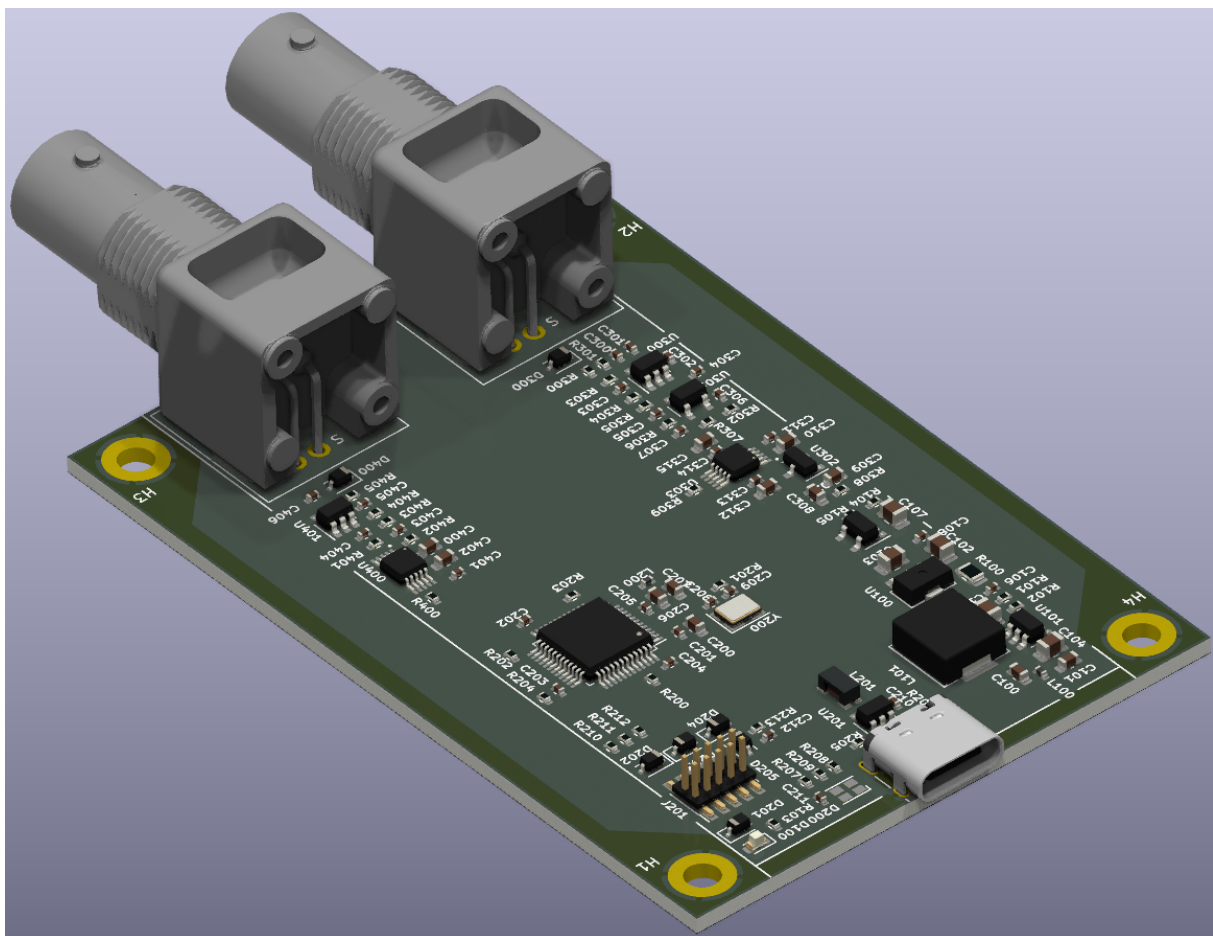


Figure 12 – Preliminary layout of the board – 3D view

Lesson 13 PCB - Routing

You should now try to route out the complete PCB by yourself, following the guidelines in this video. This step is needed to be eligible for a course certificate.

The layout of the board has undergone minimal change from previous lesson. The top layer accommodates the majority of signal traces and routing, while the bottom layer provides additional signal bridges and power distribution. Polygon pours are widely used, to optimise for lower voltage drops –even for lower current circuits– given that there is plenty of space.

To ensure signal integrity, return path vias are placed for all signals undergoing layer changes. In addition, via stitching is performed on both the ground and earth planes. Earth features exposed copper to make a connection to the metal housing.

The board has no Design Rule Check errors. Some footprints had to be updated to solve warnings. Only a handful of non-critical warnings remain, due to the silkscreen of the USB being cropped by the board outline.

In [Figure 13](#) an updated 3D view of the board is shown. On the following pages are several prints of the board layers.

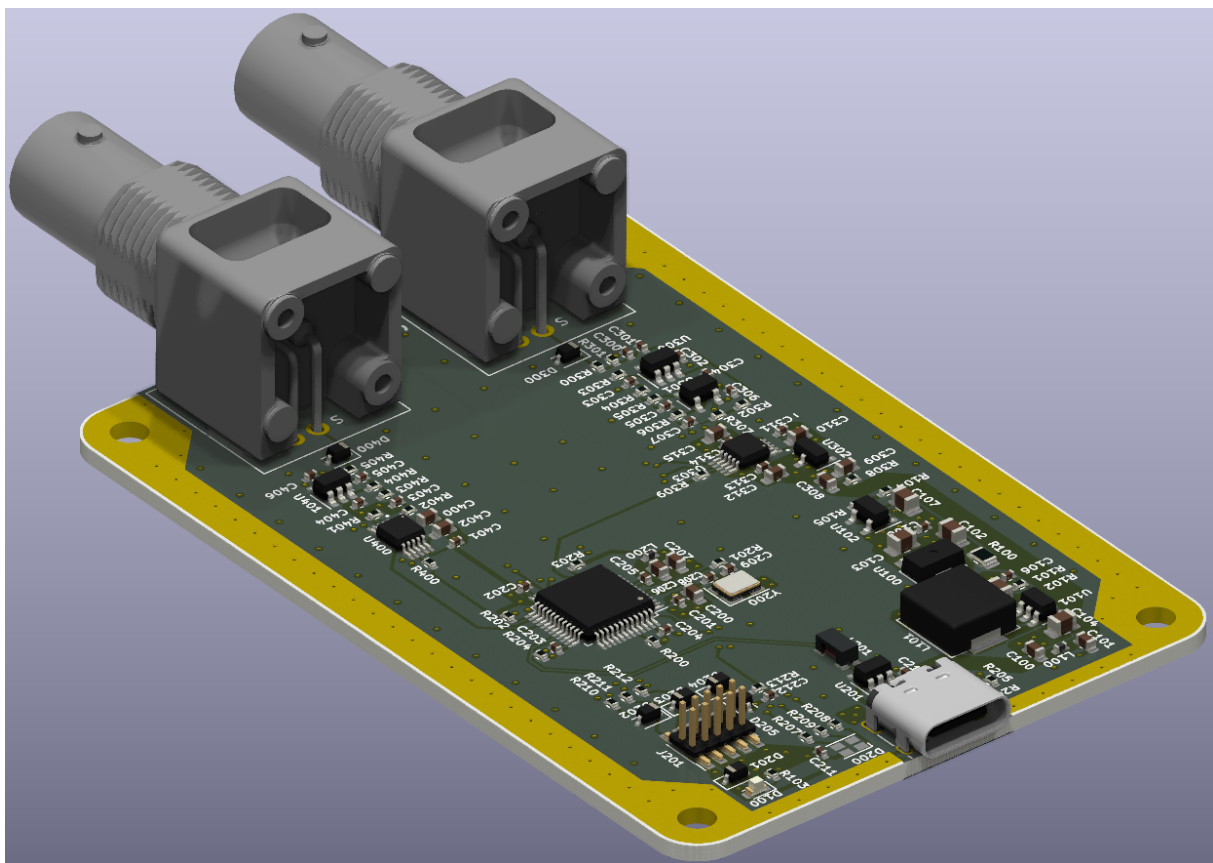
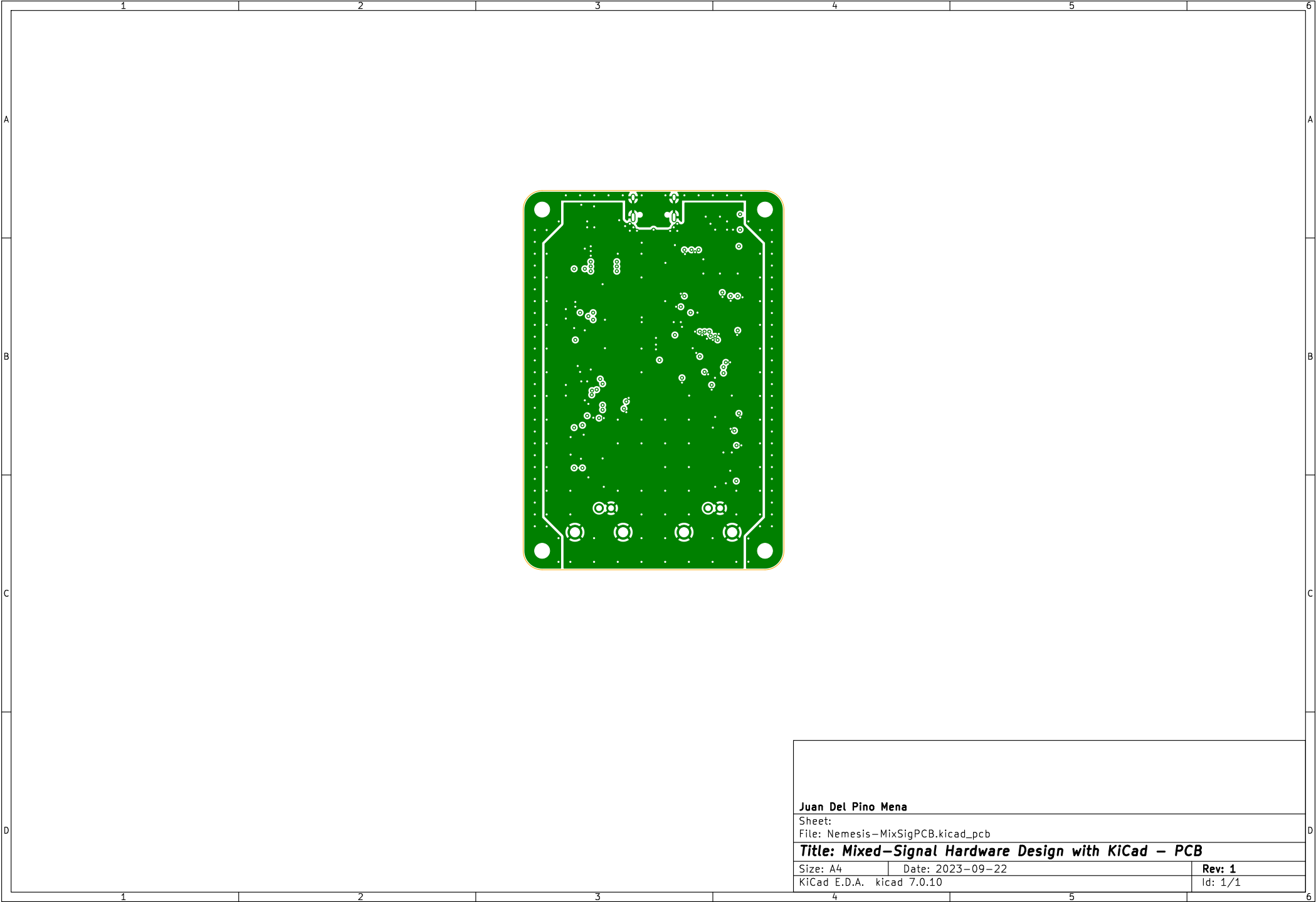


Figure 13 – 3D view of the board, finished layout and routing

Id: 1/1



Juan Del Pino Mena

Sheet:

File: Nemesis-MixSigPCB.kicad_pcb

Title: Mixed-Signal Hardware Design with KiCad - PCB

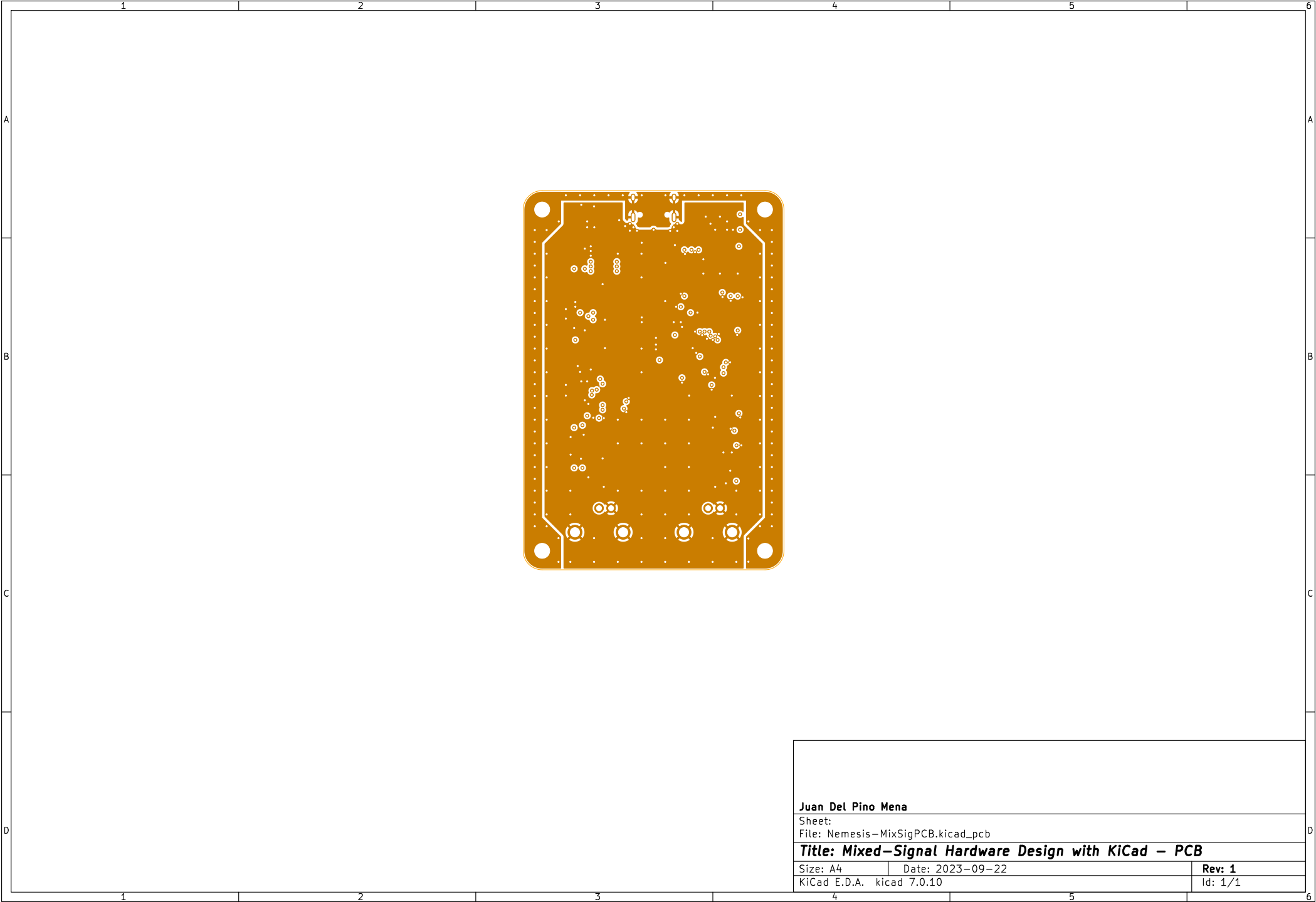
Size: A4

Date: 2023-09-22

Rev: 1

KiCad E.D.A. kicad 7.0.10

Id: 1/1



Juan Del Pino Mena

Sheet:

File: Nemesis-MixSigPCB.kicad_pcb

Title: Mixed-Signal Hardware Design with KiCad - PCB

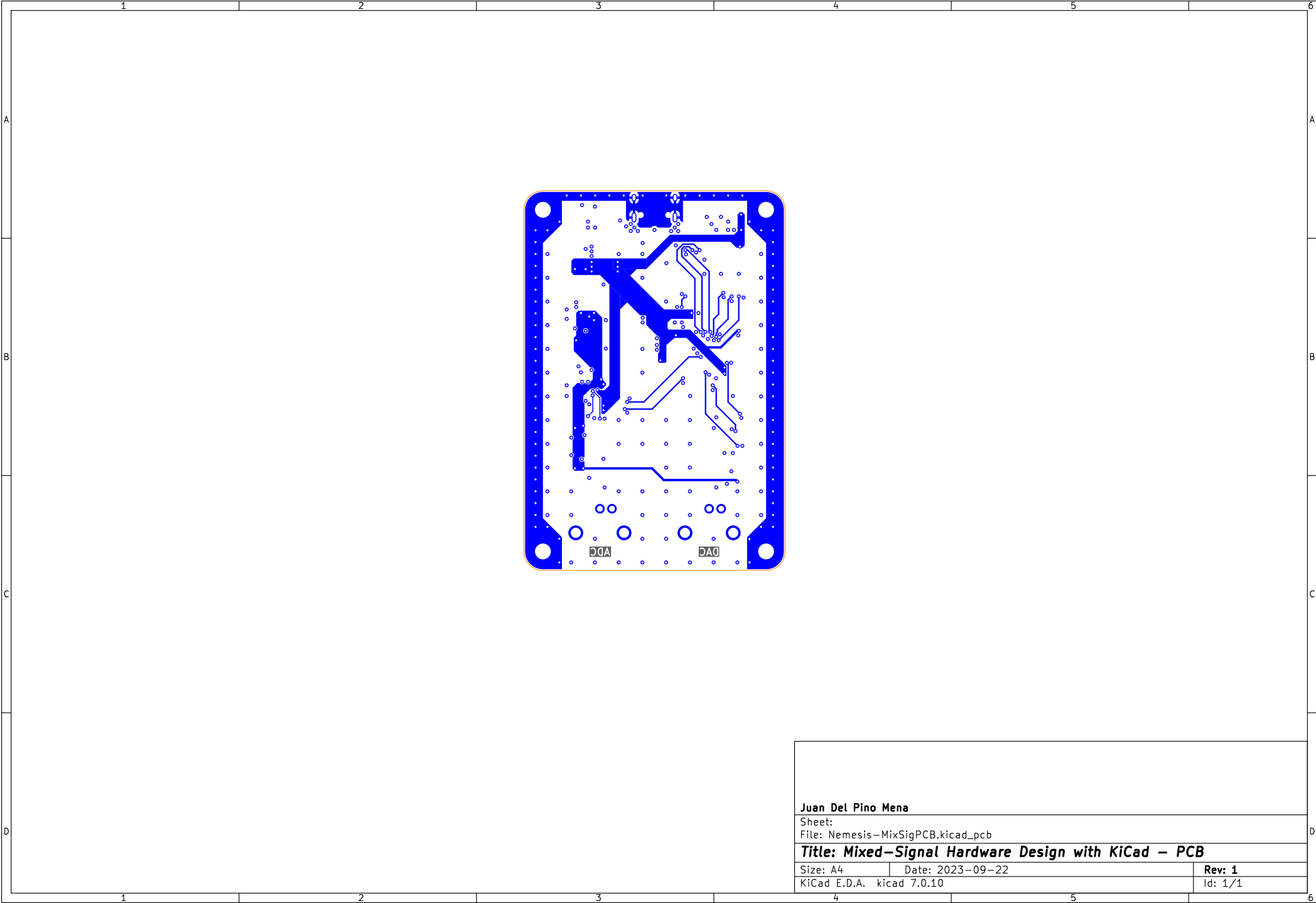
Size: A4

Date: 2023-09-22

Rev: 1

KiCad E.D.A. kicad 7.0.10

Id: 1/1



Juan Del Pino Mena		
Sheet:		
File: Nemesis-MixSigPCB.kicad_pcb		
Title: Mixed-Signal Hardware Design with KiCad - PCB		
Size: A4	Date: 2023-09-22	Rev: 1
KiCad E.D.A. kicad 7.0.10		Id: 1/1

Lesson 14 PCB - Finishing touches

Try to add your own logo and silkscreen to your PCB design. How would you go about adding tooling holes for assembly?

Some decorative silkscreen has been added in the bottom layer.

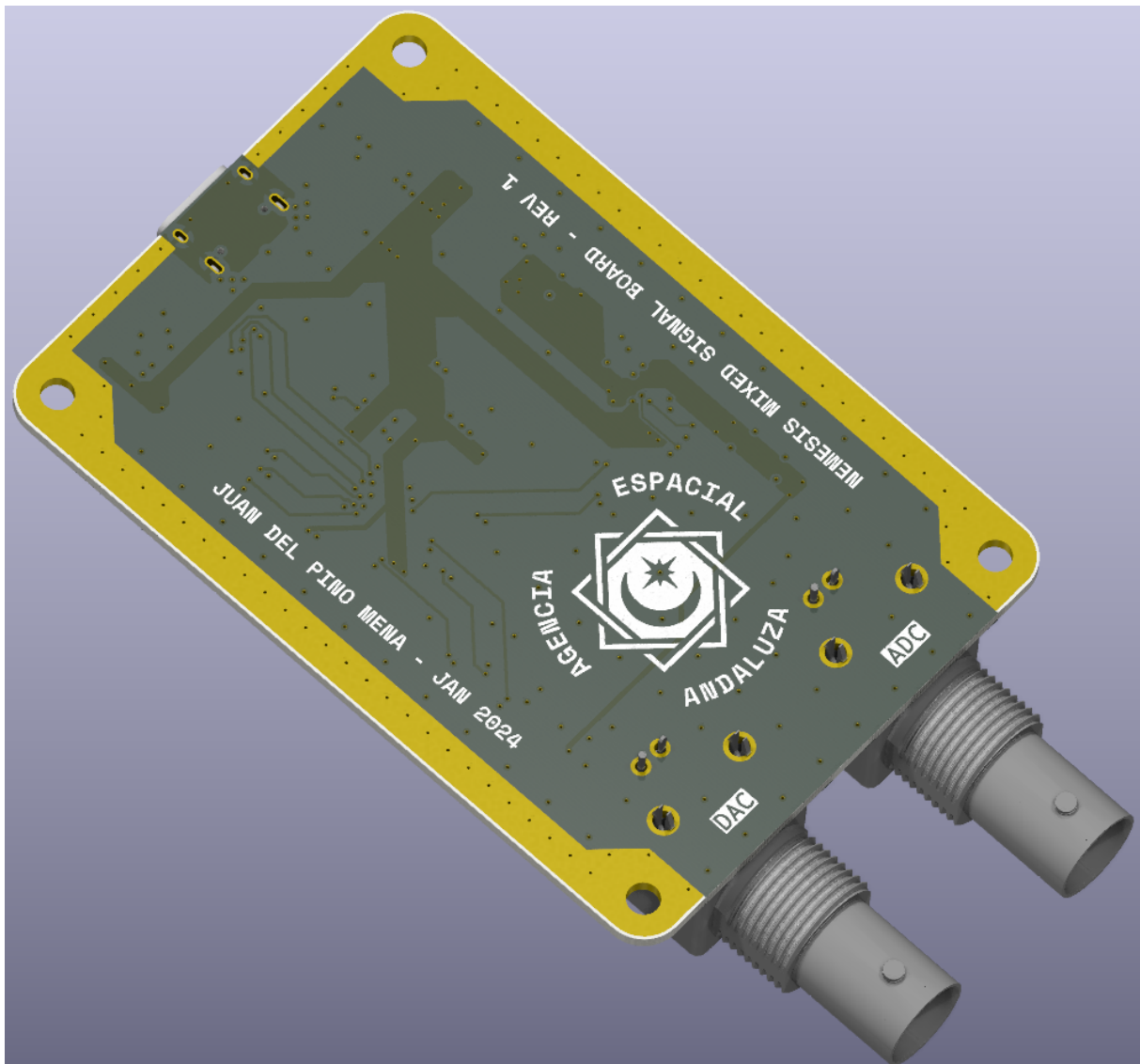


Figure 14 – 3D view of the board, bottom view.

Lesson 15 Getting The Product Manufactured

Try to export Gerber and Drill files, as well as assembly files (footprint position and BOM) for yourself in KiCad.

A manufacturer and part number has been provided for every component in the design. Gerber and Drill files are exported to the Gerber/ folder inside the project. Gerber files have been checked. Assembly files (placement and bill of materials) are placed in the Assembly/ folder.

JLCPCB automatically detects all features of the board when the gerbers are uploaded. Selected specs are: 4 layers, controlled impedance (stackup JLC0416H-7628), green solder mask, white silkscreen, FR-4 TG 155°C, ENIG surface finish, 1 oz/ft² in external layers, 0.5 oz/ft² in internal layers, plugged vias, 0.3 mm minimum via hole, 0.2 mm tolerance in board cutout, and assembly of 5 boards. The price is \$ 37.39.

In Eurocircuits both the gerbers and the assembly files are correctly identified. For the controlled impedance pool (which is the one actually this project is designed for), and selecting similar specs to those selected in JLCPCB, the total price is € 220.70.

Conclusions

I found this course quite complete. The explanations were clear, sufficient and practical, highlighting the key aspects needed to develop intuition when designing boards. I already had some experience, but I found all the details explained in the schematics, topology and component selection very helpful.

Giving the students basic materials is a double-edged sword: on the one hand, it gives everyone a common starting point, abstracts some of the design process and speeds up progress towards completion. But on the other hand, we lose part of the experience. I think I would have done an extra lesson on how to create a new schematic sheet from scratch. It would also have been nice to take advantage of the extensive and high quality symbol, footprint and 3D libraries that come with KiCAD.

I found some problems with the resources provided, such as outdated PCB footprints and schematic symbols, which were annoying. But on the positive side, these problems made me look for solutions on my own, and I became more confident with KiCAD.

Also, this was my first project in KiCAD and I found it very fast, convenient and extensible. In some ways I think it puts bloated software like Altium Designer to shame. Thank you for introducing me to this wonderful piece of open source software!

References

- [1] ST Microelectronics Inc., *Migrating from STM32F1 Series to STM32F3 Series microcontrollers*, Application Note AN4228. DocID024110, Rev 6, Feb 2017. Available online: https://www.st.com/resource/en/application_note/dm00024853-migration-and-compatibility-guidelines-for-stm32-microcontroller-applications-stmicroelectronics.pdf.
- [2] C. Kaiser, *The Capacitor Handbook*. Springer Netherlands, 2012, ISBN: 9789401180900.
- [3] T. I. Inc., *DACxx6x series datasheet*, Document number SLAS719E, August 2010, Revised June 2015. Available online: <https://www.ti.com/lit/gpn/DAC7563>.
- [4] O. E. Design, *Engineering design utilities*, Available online: <http://sim.okawa-denshi.jp/en/>.
- [5] T. I. Inc., *TLV62569 datasheet*, Document number SLVSDG1C. December 2016, Revised October 2017. Available online: <https://www.ti.com/lit/gpn/tlv62569>.
- [6] K. Jess, *SOT-23-6 3D model*, Available online: <https://www.3dcontentcentral.es/download-model.aspx?catalogid=171&id=93222>.
- [7] Eurocircuits, *PCB configurator: Services, pool, technology, buildup*, Available online: <https://be.eurocircuits.com/shop/assembly/configurator.aspx>.
- [8] Eurocircuits, *PCB design guidelines: Classification*, Available online: <https://www.eurocircuits.com/pcb-design-guidelines/classification/>.
- [9] Hammond Manufacturing Ltd., *EMI/RFI shielded extruded aluminum enclosure, pn 1457c802ebk datasheet*, Available online: <https://www.hammfg.com/files/parts/pdf/1457C802EBK.pdf>.