

PROJECT:

LoRa Comms Payload: Electrical Ground Support Equipment

PART OF THE MASTER'S THESIS:

"Development of a LoRa-based communications payload for CubeSat"

MASTER'S DEGREE IN ELECTRONIC SYSTEMS ENGINEERING
 POLYTECHNIC UNIVERSITY OF VALENCIA
 ACADEMIC COURSE 2023/2024

AUTHOR:

Juan Del Pino Mena

SUPERVISORS:

Jorge Daniel Martínez Pérez

DEPARTMENT OF ELECTRONIC ENGINEERING

Vicente Enrique Boria Esbert

DEPARTMENT OF COMMUNICATIONS



DEVELOPED IN PROUD COLLABORATION WITH:

UNIVERSITAT
POLITECNICA
DE VALÈNCIAGENERACIÓN
ESPONTÁNEA— TELECOM
UPV VLCDEPARTAMENTO
DE INGENIERÍA
ELECTRÓNICAiTEAM
Instituto de Telecomunicaciones
y Aplicaciones MultimediaMICROWAVE
APPLICATIONS
GROUP

A

A

B

B

C

C

D

D

Notes:

This project consists of an Electrical Ground Support Equipment board. It is used to program, power and test the payload. It contains a microcontroller symmetrical to the carrier, a PCI-104 bus interface to emulate communication with an OBC, and an RF sink with a LoRa transceiver and variable attenuators, simulating propagation losses.

Title: **Cover and block diagram**

Prj: Estigia Comms Payload - EGSE

Date: 2024-08-31 22:21:01 Last modified: 2024-08-11

Size: A4 Sheet 1 of 12

File: 1_cover.SchDoc

Author: Juan Del Pino Mena

Approved: *

Prj. revision: 0.4

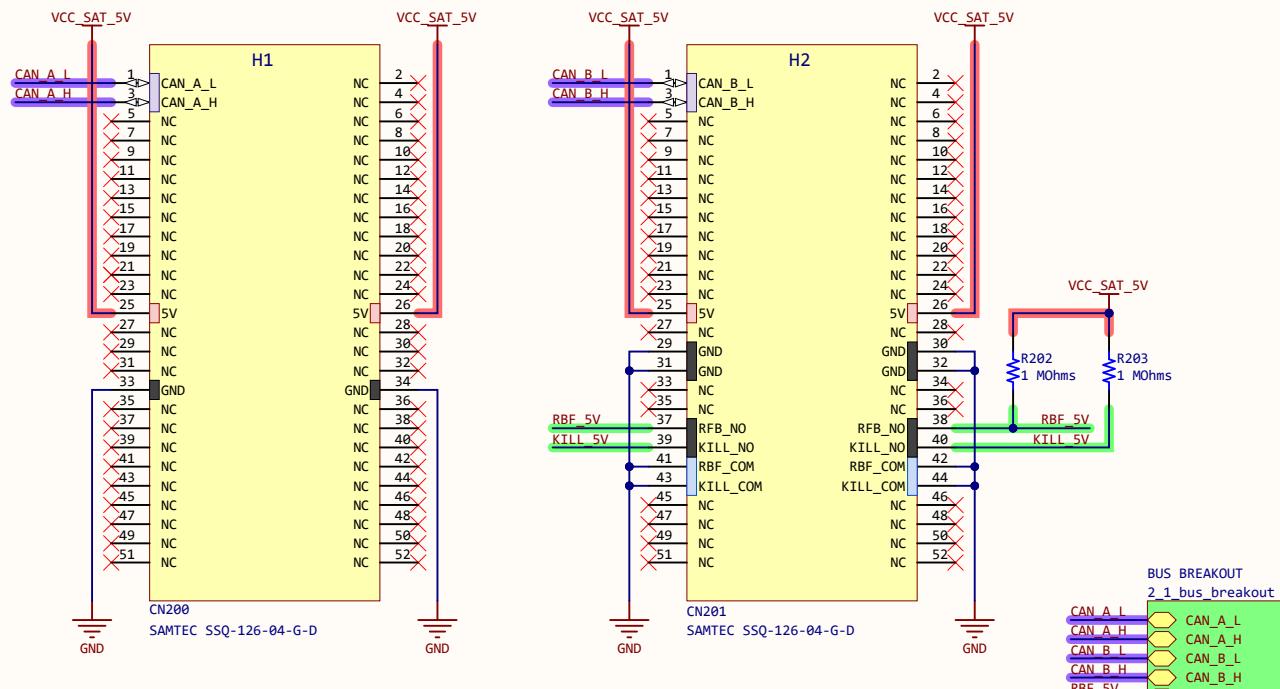
Variant: [No Variations]

Altium version: 24.3.1.35

License: --

 Pluton UPV
 Universitat Politècnica
 de València (UPV)
 Camí de Vera, València
 Spain
 Git Hash: 8abeee9f714978f94ec7b6e07c6d5a44a4eb353b6


CubeSat Bus PCI-104 connectors

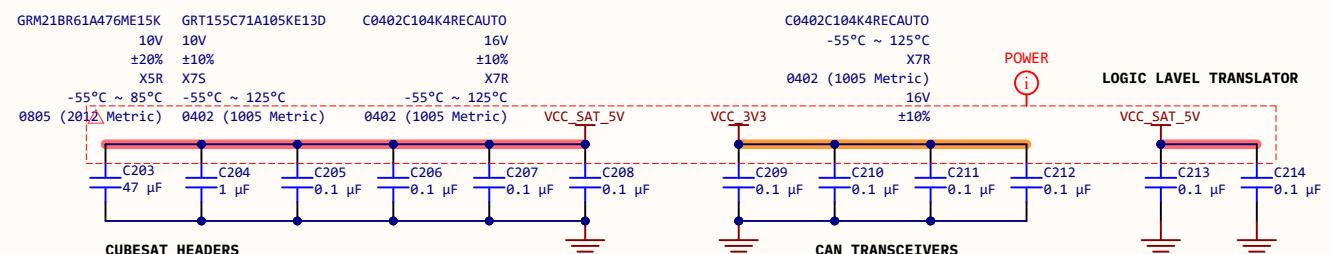


KILL: Global killswitch (NORMAL_OP=1, SHUTDOWN=0)

RBF: Remove Before Flight switch (NORMAL_OP=1, SHUTDOWN=0)

KILL_COM, RFB_COM: The respective switch common voltage

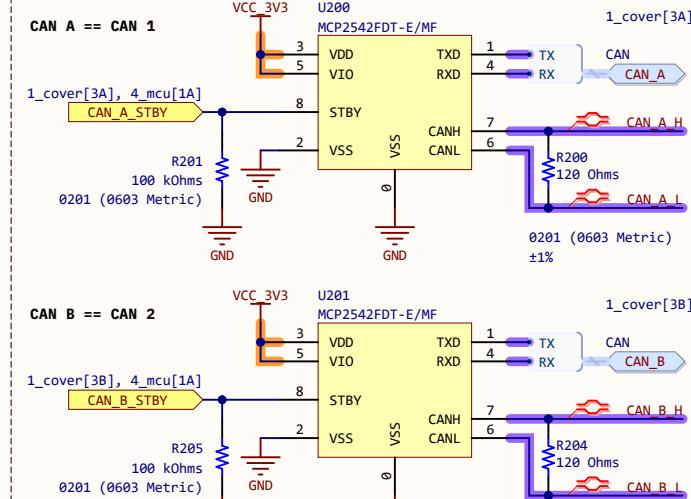
Decoupling capacitors



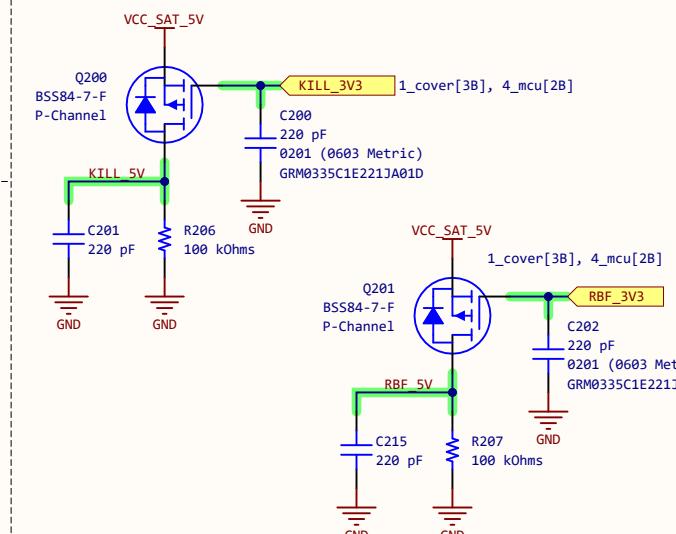
Notes:

- [1] LibreCube Board Spec. https://librecube.gitlab.io/standards/board_specification/ (04-2024)
- [2] LibreCube SpaceCAN Spec. <https://librecube.gitlab.io/standards/spacecan/> (04-2024)
- [3] LibreCube PCI104 pinout spreadsheet <https://docs.google.com/spreadsheets/d/1N1JiXR-5huo--XefjsvC9CI1hi59xMNs0TZhUcxiQ0> (04-2024)
- [4] Microchip Inc. MCP2542FD/4FD MCP2542WFD/4WF Datasheet, DS20005514C, 2020

CAN transceivers



Logic level translator



Title: **CubeSat Bus interface**

Prj: Estigia Comms Payload - EGSE

Date: 2024-08-31 22:21:02

Size: A4

File: 2_cubesat_bus.SchDoc

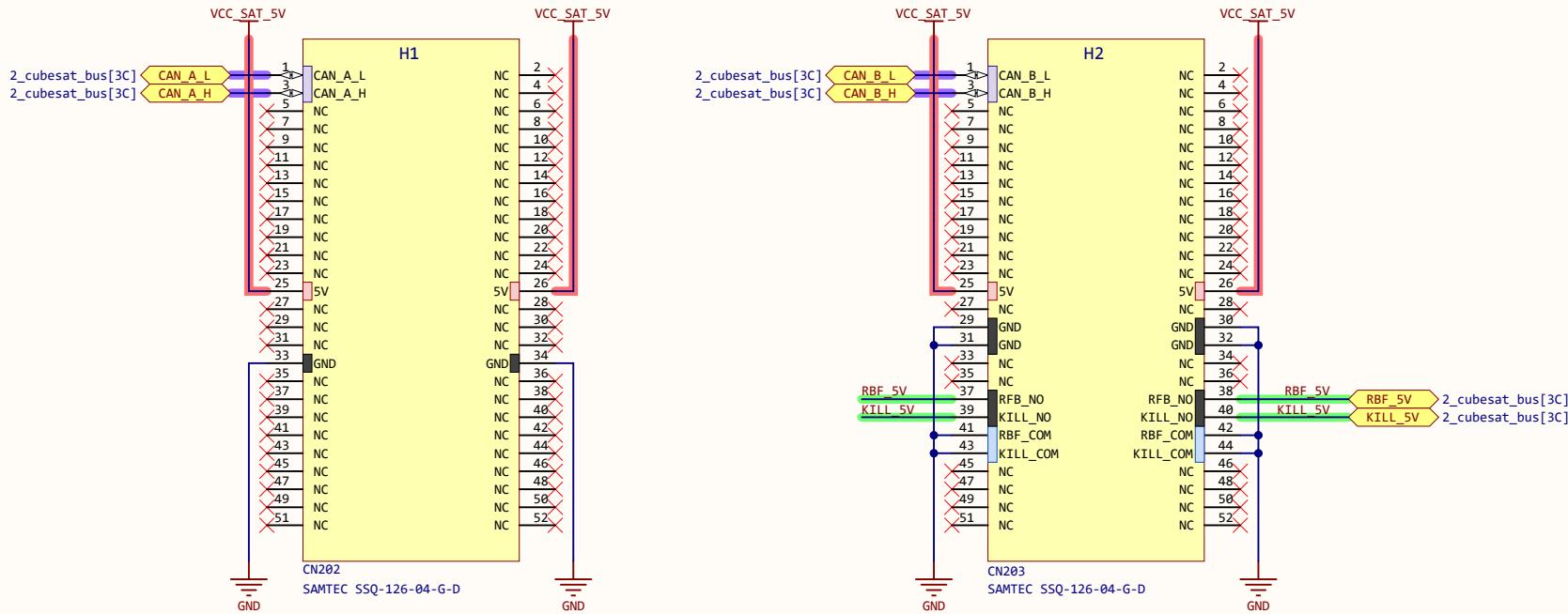
Author: Juan Del Pino Mena
Approved: *
Prj. revision: 0.4
Variant: [No Variations]

Pluton UPV
Universitat Politècnica
de València (UPV)
Camí de Vera, València
Spain

Altium version: 24.3.1.35
License: --

Git Hash: 8abef9f714978f94ec7b6e07c6d5a44a4eb353b6





A

A

B

B

C

C

Notes:

Title: **CubeSat Bus Breakout**

Prj: Estigia Comms Payload - EGSE

Date: 2024-08-31 22:21:03 Last modified: 2024-08-11

Size: A4 Sheet 3 of 12

File: 2_1_bus_breakout.SchDoc

Author: Juan Del Pino Mena

Approved: *

Prj. revision: 0.4

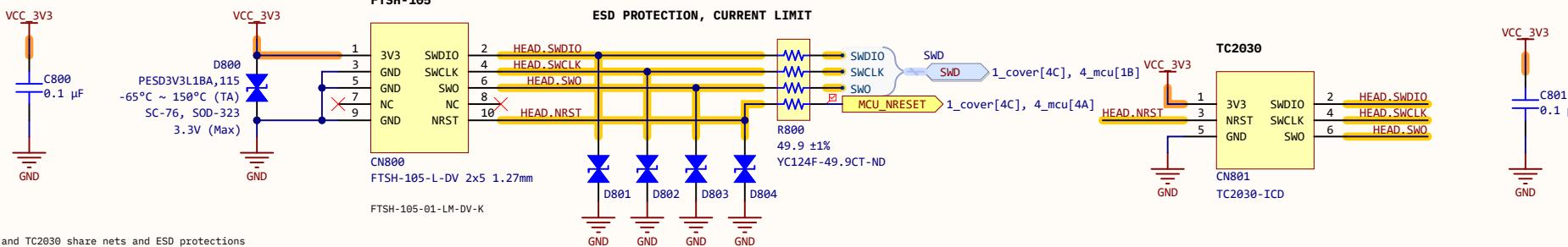
Variant: [No Variations]

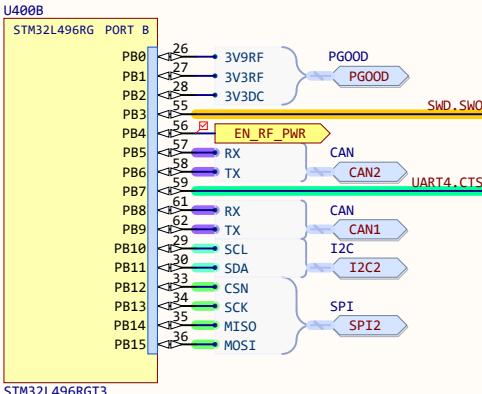
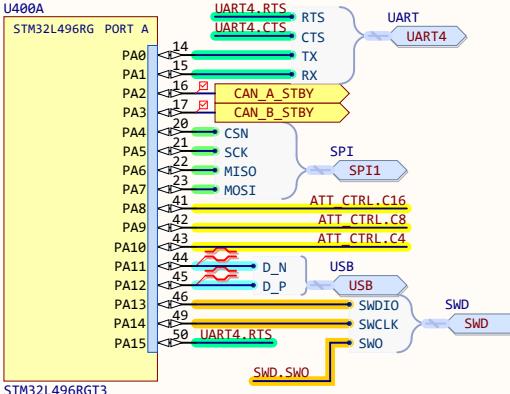
Altium version: 24.3.1.35

License: --

Pluton UPV
 Universitat Politècnica
 de València (UPV)
 Camí de Vera, València
 Spain



SWD

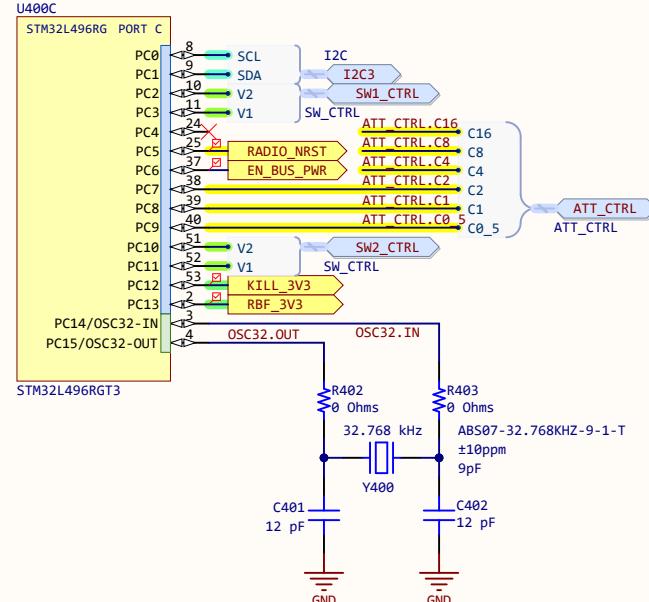


CAN A = CAN 1

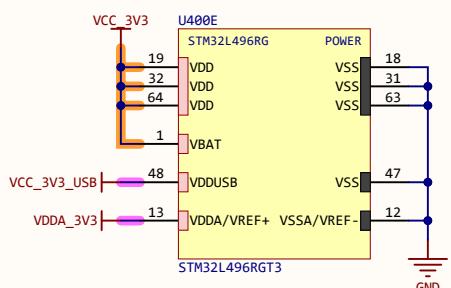
CAN B = CAN 2

Altium warns about "net connection problems" when a bi-directional pin is connected to a input or output port. Ignore warning.

Many interfaces are defined and made available into the sheet symbol, so this sheet can be re-used easily between designs. Some peripherals are used both by the Carrier and EGSE, whereas others are only used in one of them.

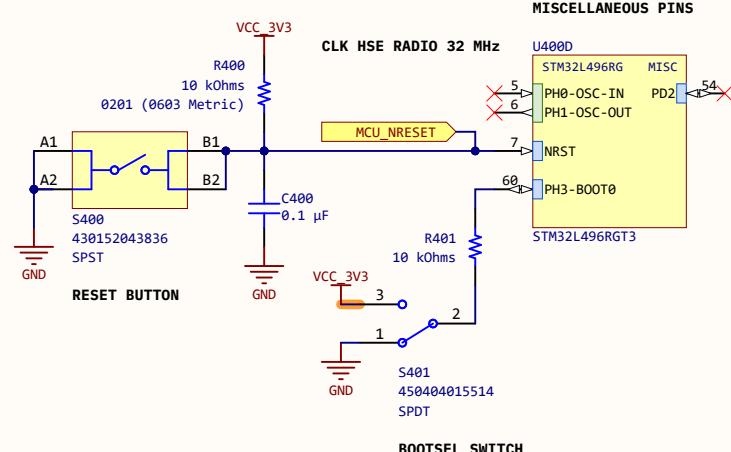


POWER PTE

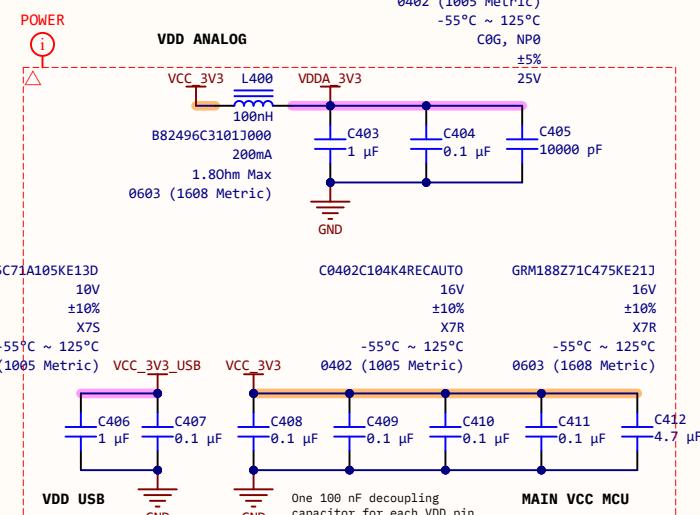


CLK LSE 32.768 kHz

Reset button and boot selection dip switch

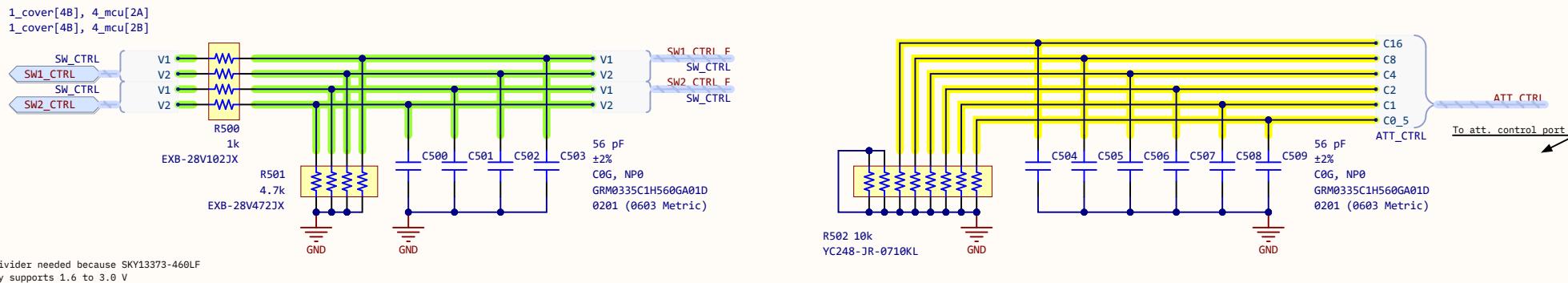


Filtering & decoupling



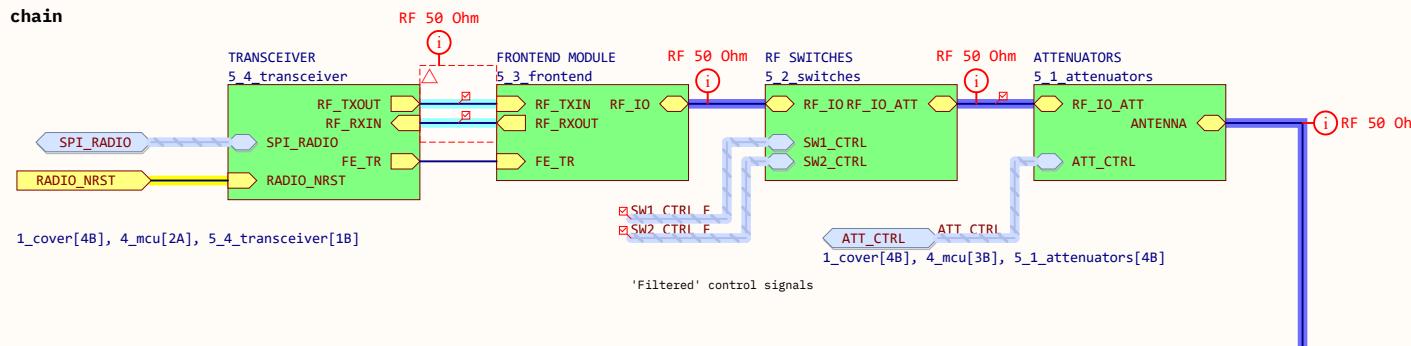
 PLUTON

Filtering of control signals

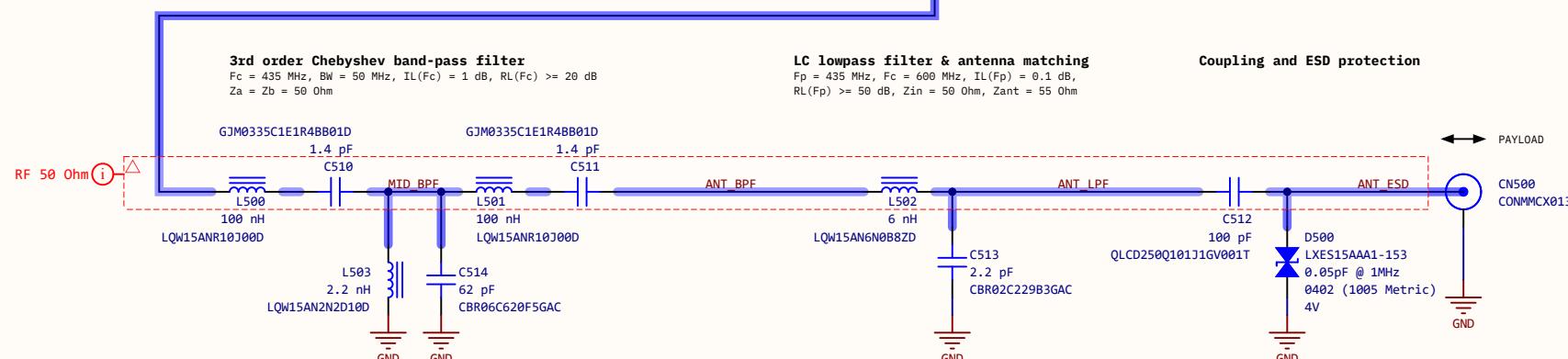


Voltage divider needed because SKY13373-460L logic only supports 1.6 to 3.0 V

RF chain



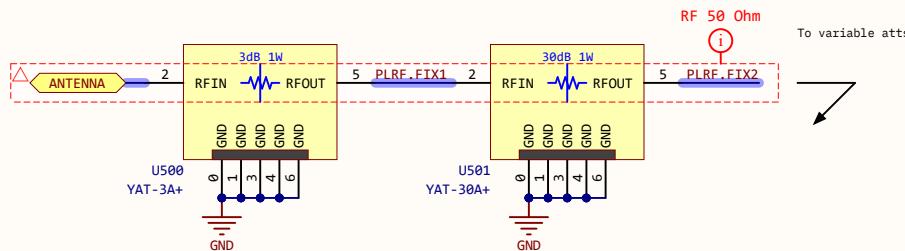
'Filtered' control signal



Notes:	Title: RF path and LoRa transceiver	Author: Juan Del Pino Mena	Pluton UPV Universitat Politècnica de València (UPV) Camí de Vera, València Spain
	Approved: *	Prj. revision: 0.4	
	Prj: Estigia Comms Payload - EGSE	Variant: [No Variations]	
	Date: 2024-08-31 22:21:05	Last modified: 2024-08-11	
	Size: A4	Altium version: 24.3.1.35	
	Sheet 6 of 12	License: --	
	File: 5_rf_path.SchDoc	Git Hash:	

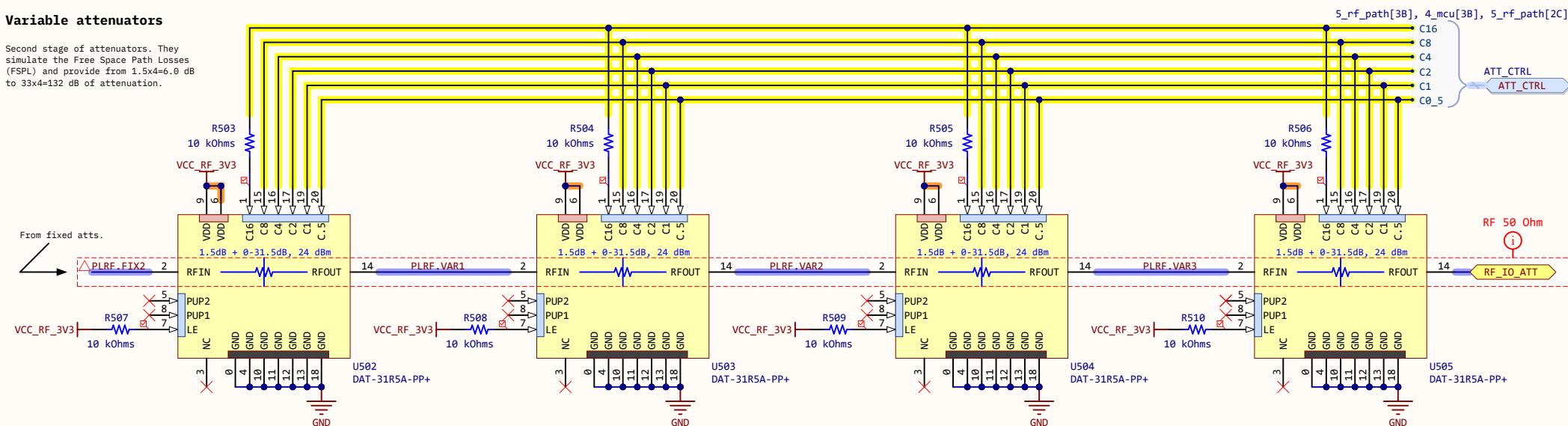
Fixed attenuators

First stage of attenuators. They dissipate the most power in the chain (up to 2W), and protect the RF ICs limiting the input RF power to a safe level.

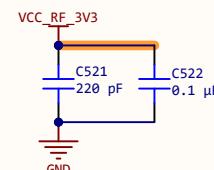
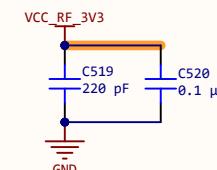
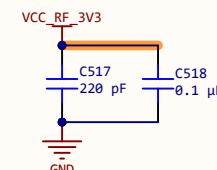
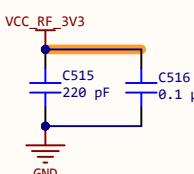


Variable attenuators

Second stage of attenuators. They simulate the Free Space Path Losses (FSPL) and provide from 1.5x4=6.0 dB to 33x4=132 dB of attenuation.



Decoupling caps



Notes:

- [1] Mini-Circuits Inc. YAT-30A+ datasheet, ECO-011434, REV. A, 01-2022
- [2] Mini-Circuits Inc. YAT-3A+ datasheet, ECO-011434, REV. A, 01-2022
- [3] Mini-Circuits Inc. DAT-31R5A-PP+ datasheet, M164761, REV. C, 05-2020

Title: RF Attenuators

Prj: Estigia Comms Payload - EGSE

Date: 2024-08-31 22:21:05 Last modified: 2024-08-11

Size: A4 Sheet 7 of 12

File: 5_1_attenuators.SchDoc

Author: Juan Del Pino Mena

Approved: *

Prj. revision: 0.4

Variant: [No Variations]

Altium version: 24.3.1.35

License: --

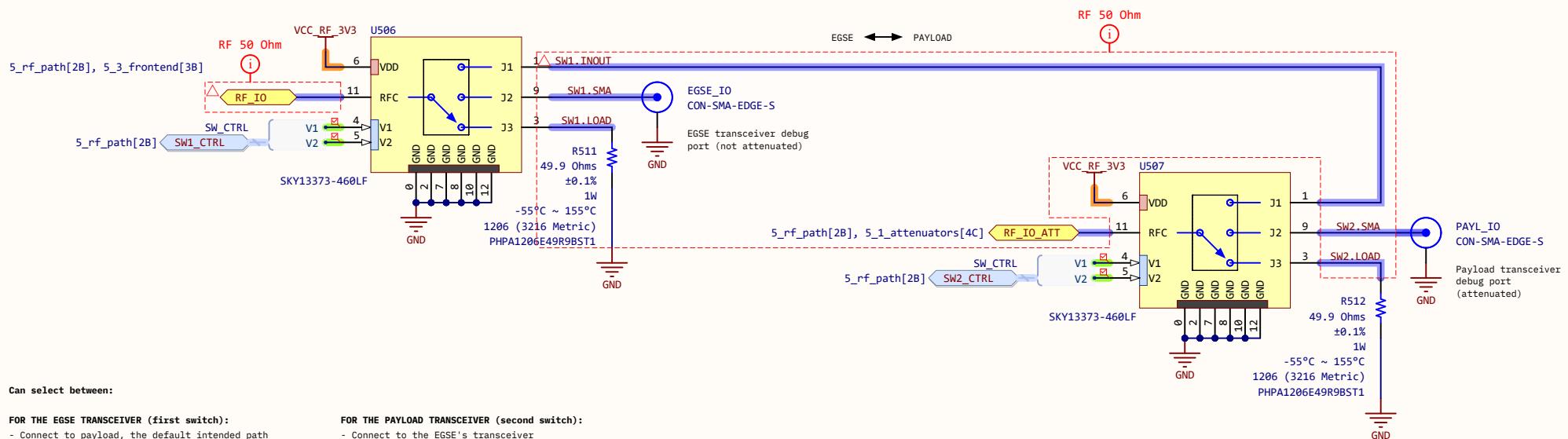
Git Hash:

Pluton UPV

Universitat Politècnica
de València (UPV)
Camí de Vera, València
Spain

PLUTON

RF path selection switches



Can select between:

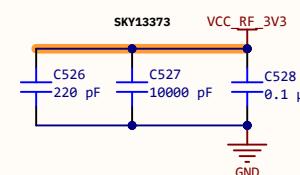
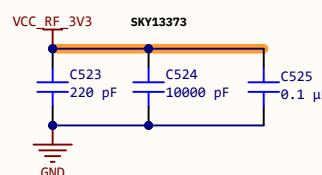
FOR THE EGSE TRANSCEIVER (first switch):

- Connect to payload, the default intended path through the attenuators to the payload's transceiver
- Connect to a SMA connector, rendering the transceiver output available for an antenna, an analyzer, etc.
- Connect to 50-ohm load, to sink the rf signal if not used.
- Connect to 50-ohm load, to sink the rf signal if not used.

FOR THE PAYLOAD TRANSCEIVER (second switch):

- Connect to the EGSE's transceiver
- Connect to a SMA connector (after attenuation!), rendering the transceiver output available for an antenna, an analyzer, etc.
- Connect to 50-ohm load, to sink the rf signal if not used.

Decoupling capacitors



Notes:
 [1] Skyworks Inc. SKY13373-460LF Datasheet, 2012640, 05-2016

Title: RF Switches

Prj: Estigia Comms Payload - EGSE

Date: 2024-08-31 22:21:05 **Last modified:** 2024-08-11

Size: A4 **Sheet:** 8 of 12

File: 5_2_switches.SchDoc

Author: Juan Del Pino Mena
Approved: *

Prj. revision: 0.4

Variant: [No Variations]

Altium version: 24.3.1.35

License: --

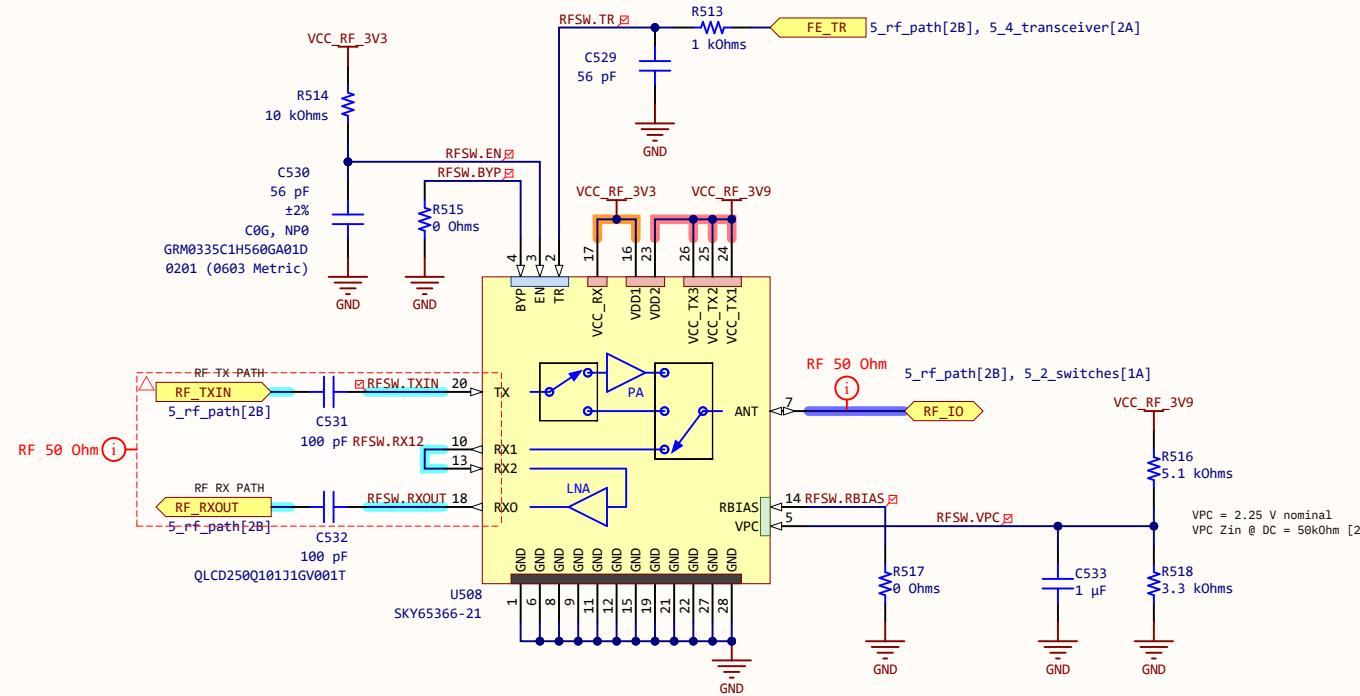
Git Hash:

Pluton UPV
 Universitat Politècnica
 de València (UPV)
 Camí de Vera, València
 Spain

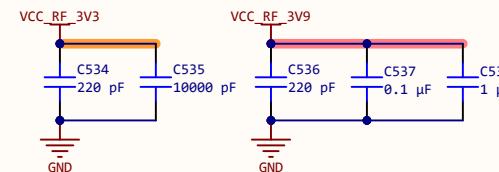
PLUTON

RF Front-End module (Switch + LNA + PA)

Front-end module always enabled, never bypassed.



Decoupling capacitors



Notes:

[1] Semtech Inc. SX1302 Corecell Reference Design with SX1250 RF Front-Ends, PCB_E539V01A, 01-2020
[2] Skyworks Inc. SKY65366-21 400 MHz Tx/Rx Front-End Module, 203146E, 10-2020

Title: **RF Front-end module**

Prj: Estigia Comms Payload - EGSE

Date: 2024-08-31 22:21:05 Last modified: 2024-08-11

Size: A4 Sheet 9 of 12

File: 5_3_frontend.SchDoc

Author: Juan Del Pino Mena
Approved: *

Prj. revision: 0.4

Variant: [No Variations]

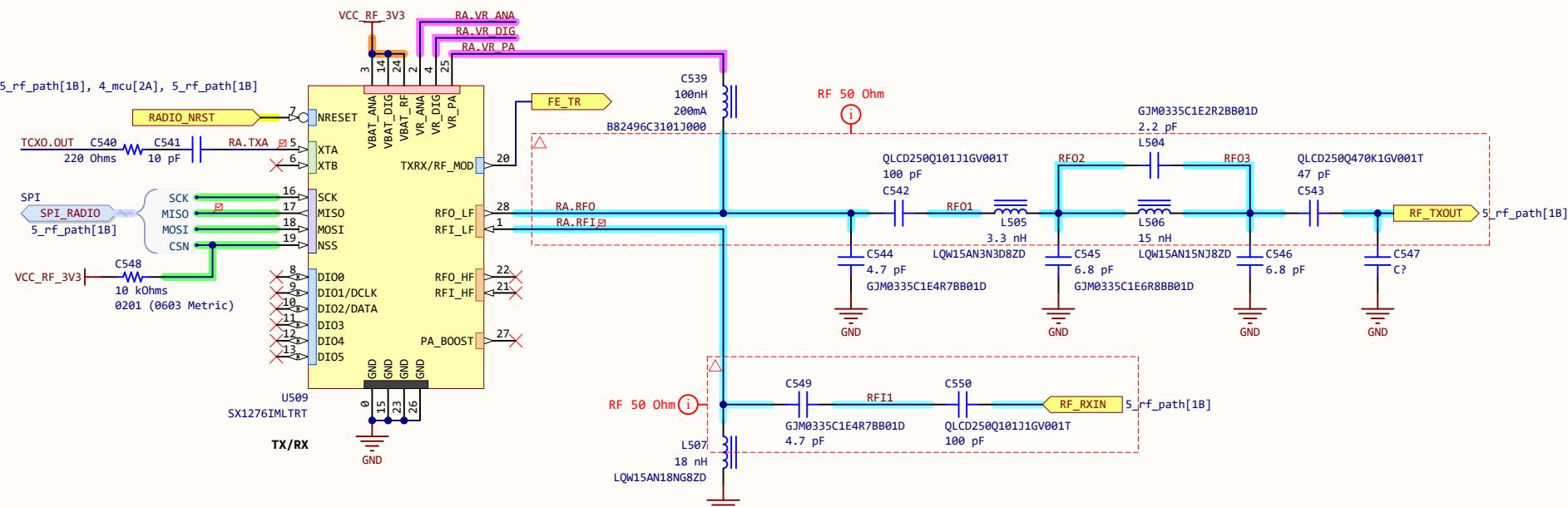
Altium version: 24.3.1.35

License: --

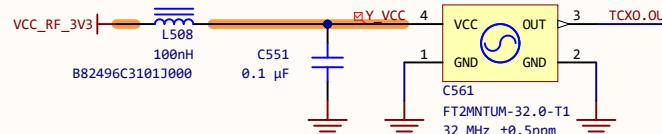
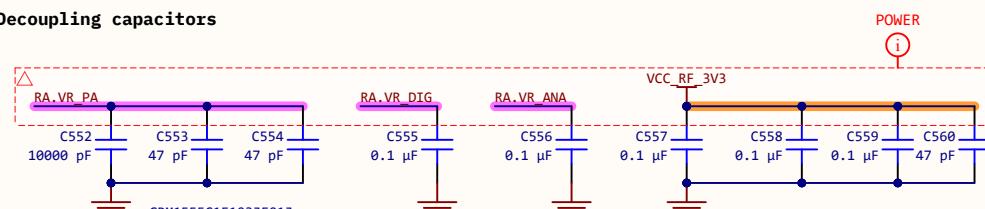
Git Hash:

Pluton UPV
Universitat Politècnica
de València (UPV)
Camí de Vera, València
Spain



LoRa Node Transceiver**Xtal oscillator**

Clipped-sine output TCXO are required, $V_{out_pp} \leq 1.2$ V. Recommended a GPS-precision TCXO (0.5 ppm). A TCXO should be connected to pin XTA through a 220-ohm res and a 10 pF DC-cut cap to reduce the amplitude [4]. Pin XTB should be left open [1].

**Decoupling capacitors****Notes:**

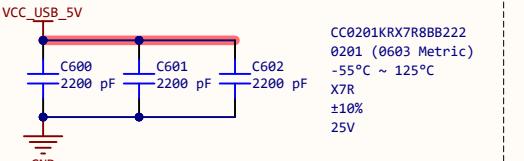
- [1] Semtech Inc. SX127x datasheet, Rev 7, 05-2020
- [2] Semtech Inc. SX127x reference design overview, AN1200.19, 12-2014
- [3] Semtech Inc. SX1276 433/915 MHz reference design SX1276MB1LAS, PCB_E311V02A, v1a, 02-2015

Title: LoRa node transceiver**Prj:** Estigia Comms Payload - EGSE**Date:** 2024-08-31 22:21:06 **Last modified:** 2024-08-31**Size:** A4 **Sheet 10 of 12****File:** 5_4_transceiver.SchDoc

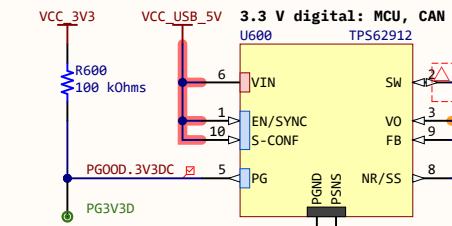
Author: Juan Del Pino Mena
Approved: *
Prj. revision: 0.4
Variant: [No Variations]
Altium version: 24.3.1.35
License: --
Git Hash:

Pluton UPV
Universitat Politècnica
de València (UPV)
Camí de Vera, València
Spain

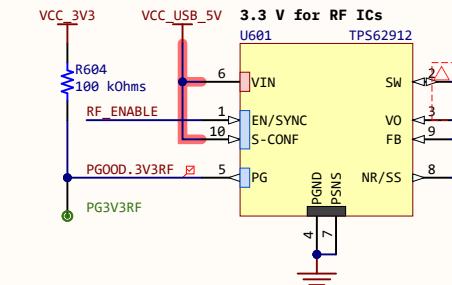


Decoupling capacitors

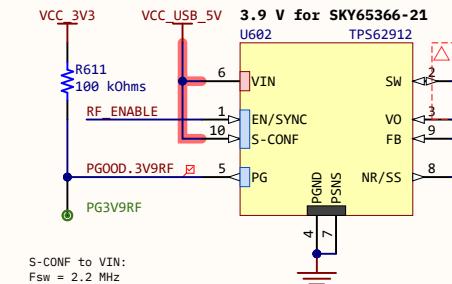
A

Low noise DC/DC converters

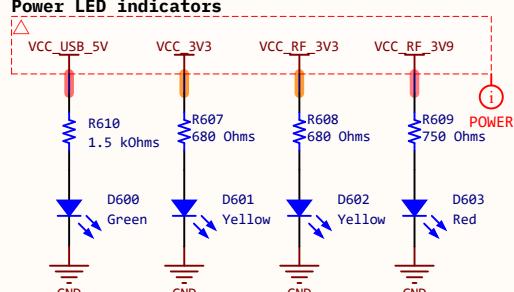
EN/SYNC pin: Open-drain, pull-down (500k, 100k pull-up to 1V2 (instead of 5VIN) to avoid unwanted power-up



BLE18PS080SN1D
8.5 Ohms @ 100 MHz



S-CONF to VIN:
Fsw = 2.2 MHz
Spread-Spectrum OFF
Output Discharge OFF
Sync OFF

Power LED indicators

The TPS62912 PG pin is in high Z when V(FB) >= 95%, and driven low when V(FB) <= 90%. The open-drain pin requires a pullup. The PG signal is used for sequencing of multiple rails by connecting to the EN pin of other converters [1].

To ensure control of all digital IOs during the power-up/down of the SX1302 V rail and avoid an inrush current, the 1.2 V rail shall be enabled before 3.3 V at start-up [2].

Notes:

Power supply based on low-noise DC/DC converters.

[1] Texas Instruments Inc. TPS62912/3 datasheet, SLVSP4B, 03-2021

[2] Semtech Inc. Errata Note Corecell PCB #e539v0le Reference Design, Rev 1.0, 03-2020

Title: Power management

Prj: Estigia Comms Payload - EGSE

Date: 2024-08-31 22:21:06

Last modified: 2024-08-31

Size: A4

File: 6_power_dcdc.SchDoc

Author: Juan Del Pino Mena

Approved: *

Prj. revision: 0.4

Variant: [No Variations]

Altium version: 24.3.1.35

License: --

Git Hash:

Pluton UPV

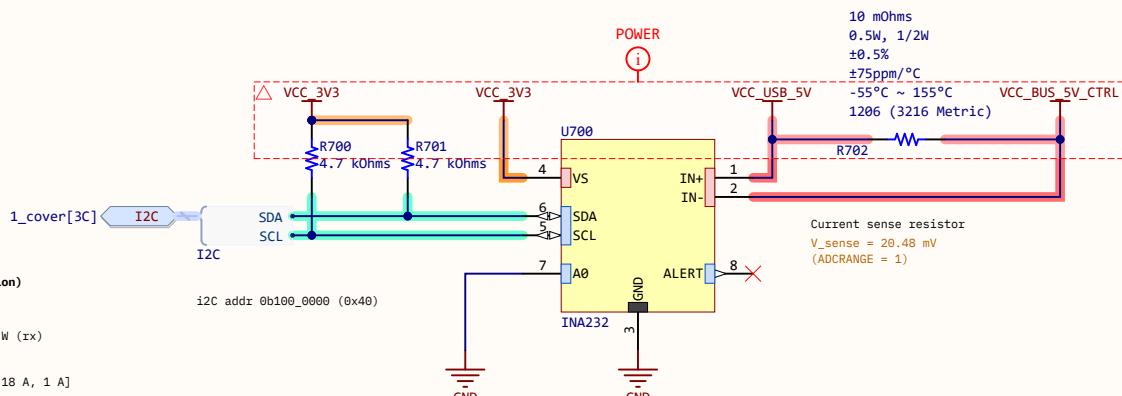
Universitat Politècnica
de València (UPV)
Camí de Vera, València
Spain



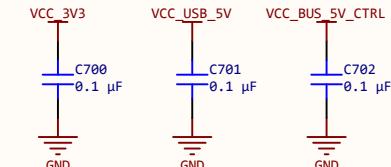
Voltage, current and power monitor

Power measurement excludes EGSE's own consumption. It only monitors the payload's.

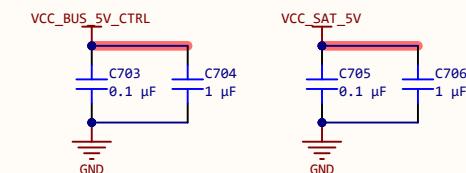
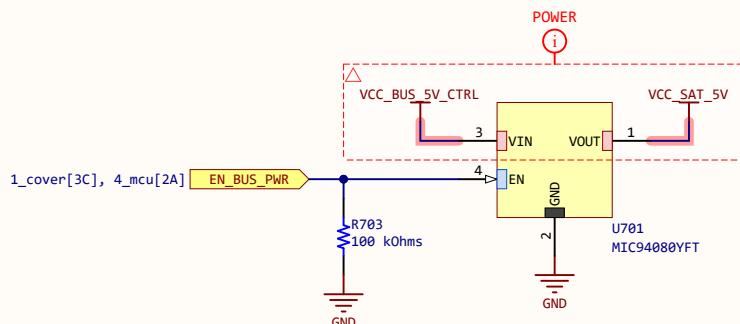
A



Decoupling capacitors



Load power switch


Notes:

- [1] Texas Instruments Inc. INA232 datasheet, SBOSAA2, 12-2022
- [2] Semtech Inc. Errata Note Corecell PCB #e539v01e Reference Design, Rev 1.0, 03-2020
- [3] Microchip Inc. MIC94080/1/2/3/4/5 datasheet, DS20006118A, 2019

Title: Bus power control & monitoring	Author: Juan Del Pino Mena
Approved: *	
Prj. revision: 0.4	
Variant: [No Variations]	
Date: 2024-08-31 22:21:06	Last modified: 2024-08-11
Size: A4	Altium version: 24.3.1.35
File: 7_power_prot_mon.SchDoc	License: --
	Git Hash:

Pluton UPV
Universitat Politècnica
de València (UPV)
Camí de Vera, València
Spain

PLUTON