PROJECT:

LoRa Comms Payload: Electrical Ground Support Equipment

PART OF THE MASTER'S THESIS:

"Development of a LoRa-based communications payload for CubeSat"

MASTER'S DEGREE IN ELECTRONIC SYSTEMS ENGINEERING
POLYTECHNIC UNIVERSITY OF VALENCIA
ACADEMIC COURSE 2023/2024

AUTHOR:

Juan Del Pino Mena

SUPERVISORS:

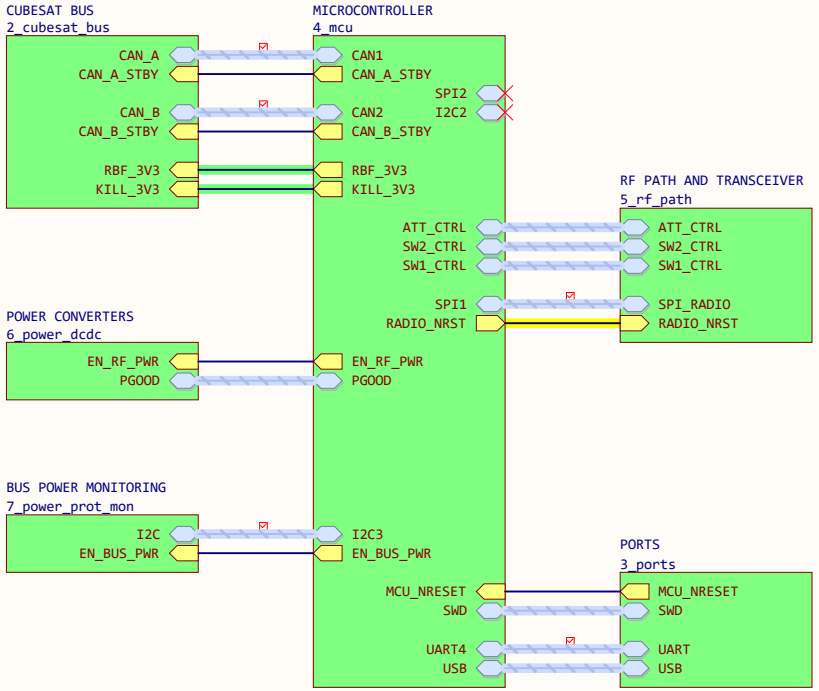
Jorge Daniel Martínez Pérez
DEPARTMENT OF ELECTRONIC ENGINEERING

Vicente Enrique Boria Esbert
DEPARTMENT OF COMMUNICATIONS

LOG100 LOGO Pluton
LOG101 LOGO Pluton isotype
LOG102 LOGO Pluton iso small
LOG103 LOGO AEA
LOG104 LOGO UPV
LOG105 LOGO MAG large

FID100 FID101 FID102

MH100 M3 MH101 M3 MH102 M3 MH103 M3
MH104 M3 MH105 M3 MH106 M3 MH107 M3



DEVELOPED IN PROUD COLLABORATION WITH:

UNIVERSITAT POLITÈCNICA DE VALÈNCIA
GENERACIÓN ESPONTÁNEA
TELECOM UPV VLC
DEPARTAMENTO DE INGENIERÍA ELECTRÓNICA
iTEAM Instituto de Telecomunicaciones y Aplicaciones Multimedia
MICROWAVE APPLICATIONS GROUP

Notes:

This project consists of an Electrical Ground Support Equipment board. It is used to program, power and test the payload. It contains a microcontroller symmetrical to the carrier, a PCI-104 bus interface to emulate communication with an OBC, and an RF sink with a LoRa transceiver and variable attenuators, simulating propagation losses.

Title: *Cover and block diagram*		**Author:** Juan Del Pino Mena	**Pluton UPV**
Prj: Estigia Comms Payload - EGSE		**Approved:** *	*Universitat Politècnica de València (UPV)*
Date: 03/09/2024 19:56:42	**Last modified:** 03/09/2024	**Prj. revision:** 0.4	*Camí de Vera, València*
Size: A4	Sheet 1 of 12	**Variant:** [No Variations]	*Spain*
File: 1_cover.SchDoc		**Altium version:** 24.3.1.35	
		License: --	
		Git Hash:	

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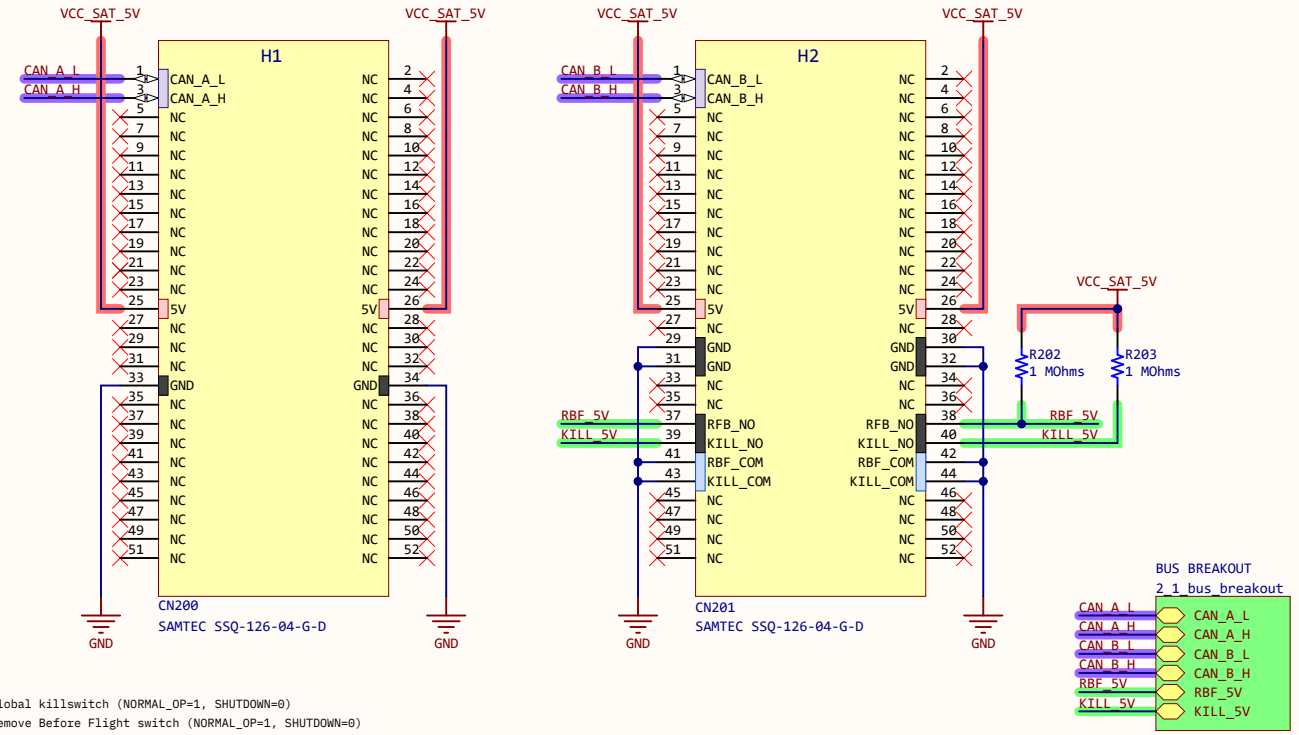
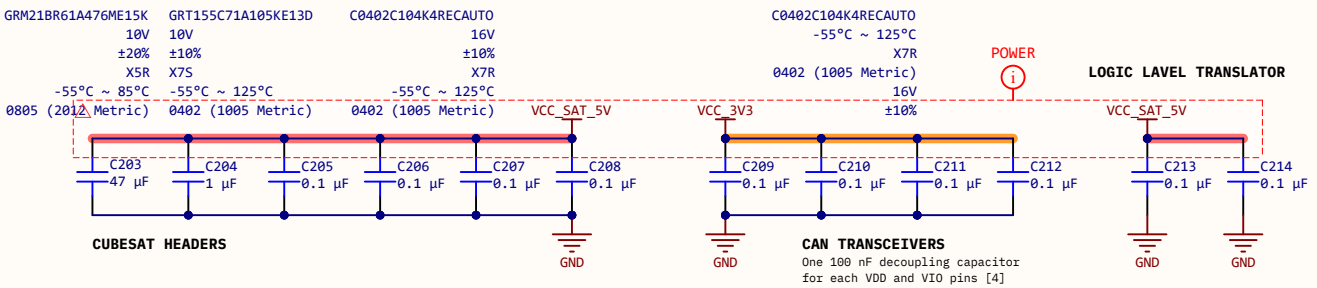
CubeSat Bus PCI-104 connectors

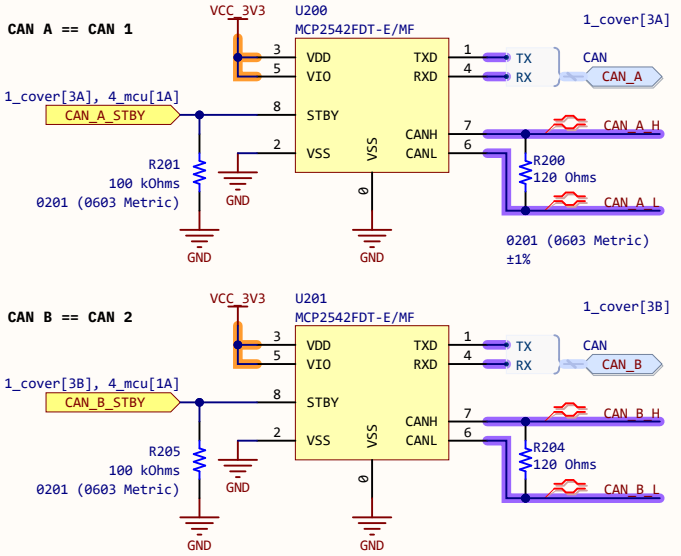


KILL: Global killswitch (NORMAL_OP=1, SHUTDOWN=0)
RBF: Remove Before Flight switch (NORMAL_OP=1, SHUTDOWN=0)
KILL_COM, RBF_COM: The respective switch common voltage

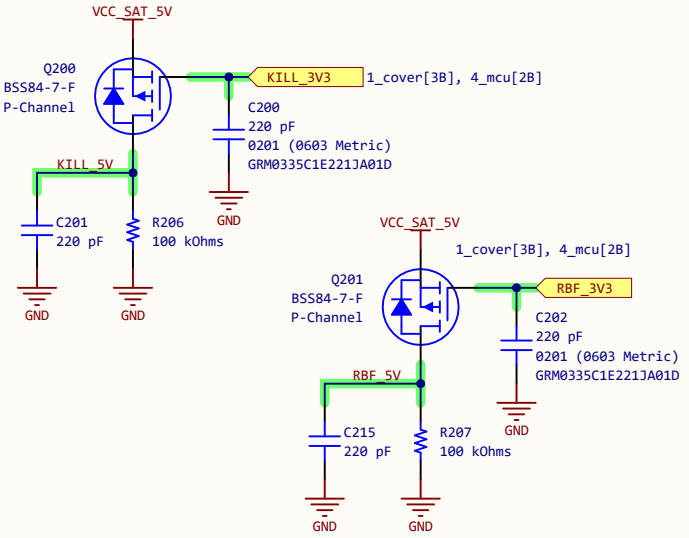
Decoupling capacitors



CAN transceivers



Logic level translator



Notes:

[1] LibreCube Board Spec. https://librecube.gitlab.io/standards/board_specification/ (04-2024)
[2] LibreCube SpaceCAN Spec. https://librecube.gitlab.io/standards/spacecan/ (04-2024)
[3] LibreCube PC104 pinout spreadsheet
https://docs.google.com/spreadsheets/d/1N1JiXR-5huo--XefjsvC9CI1hiS9xMNosTZhUcuxiQ0 (04-2024)
[4] Microchip Inc. MCP2542FD/4FD MCP2542WFD/4WFD datasheet, DS20005514C, 2020

Title: *CubeSat Bus interface*		**Author:**	Juan Del Pino Mena
		Approved:	*
Prj: Estigia Comms Payload - EGSE		**Prj. revision:**	0.4
		Variant:	[No Variations]
Date: 03/09/2024 19:56:43	**Last modified:** 11/08/2024	**Altium version:**	24.3.1.35
Size: A4	Sheet 2 of 12	**License:**	--
File: 2_cubesat_bus.SchDoc		**Git Hash:**	

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Camí de Vera, València
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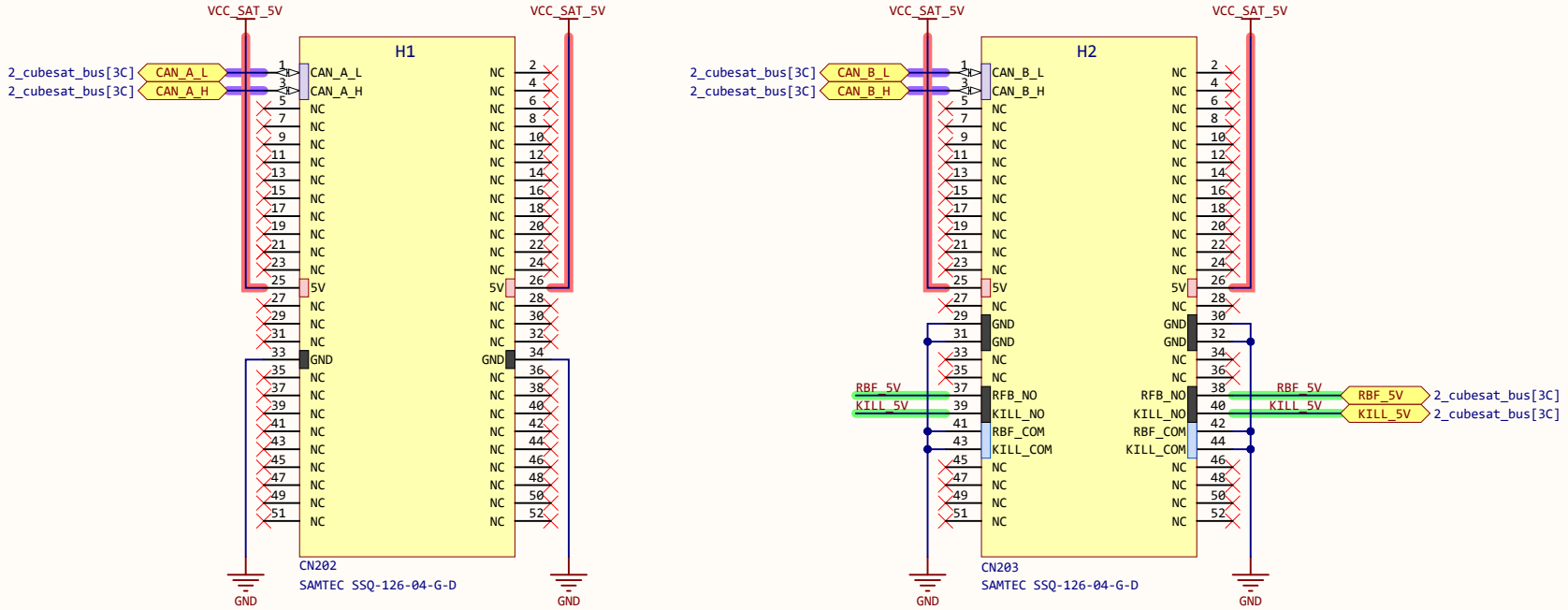
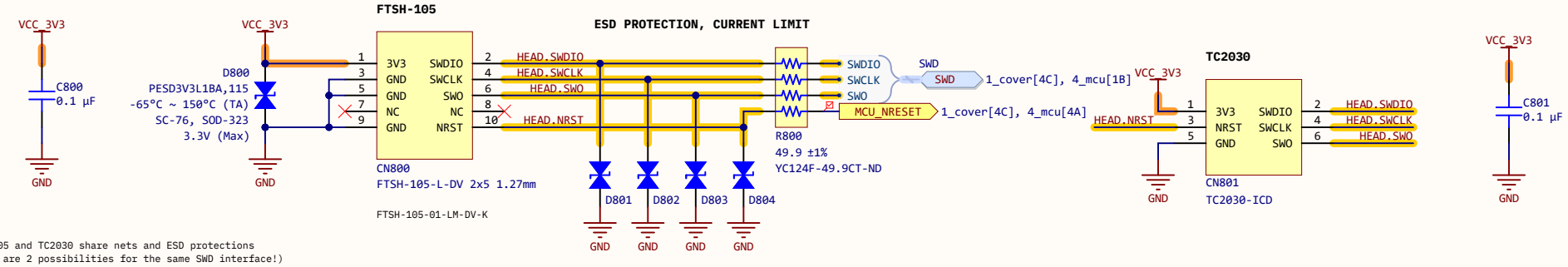


Notes:

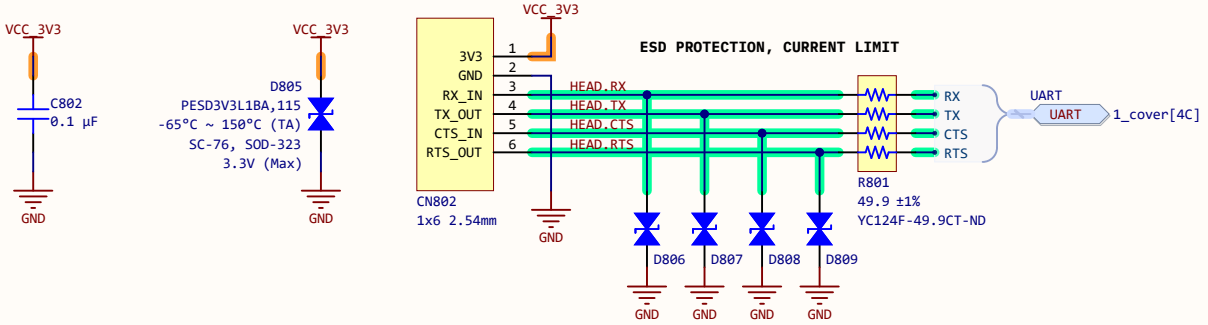
Title: *CubeSat Bus Breakout*		**Author:** Juan Del Pino Mena	**Pluton UPV**
Prj: Estigia Comms Payload - EGSE		**Approved:** *	*Universitat Politècnica de València (UPV)*
		Prj. revision: 0.4	*Camí de Vera, València*
Date: 03/09/2024 19:56:44	**Last modified:** 11/08/2024	**Variant:** [No Variations]	*Spain*
Size: A4	Sheet 3 of 12	**Altium version:** 24.3.1.35	
File: 2_1_bus_breakout.SchDoc		**License:** --	
		Git Hash:	

SWD



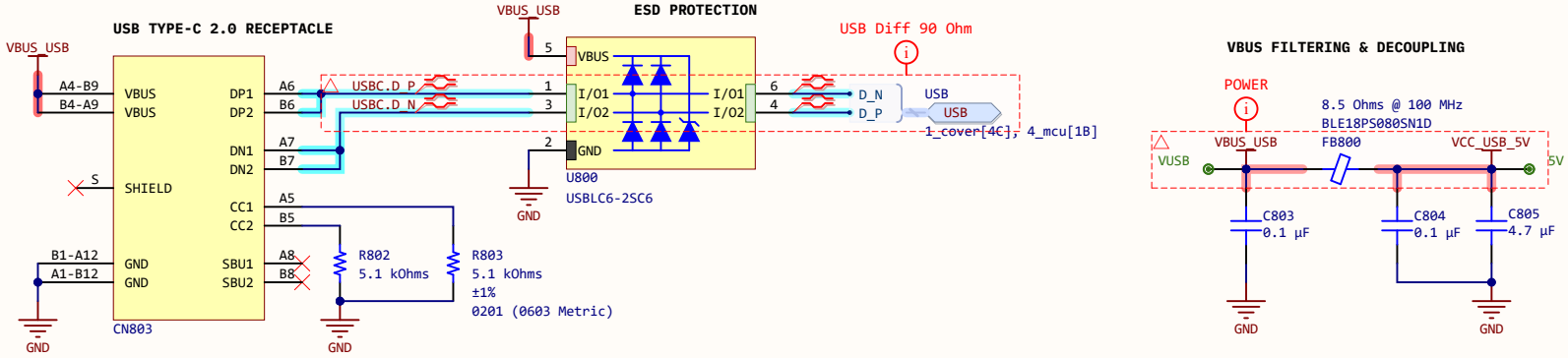
FTSH-105 and TC2030 share nets and ESD protections
(there are 2 possibilities for the same SWD interface!)

UART



CAUTION: UART SIGNALS ALREADY CROSSED!
Compatible serial adapter pinout:
1:3V3, 2:GND, 3:TXD, 4:RXD, 5:RTS, 6:CTS

USB



USB-C 2.0 interface. Pull down resistors on CC pins make the connector behave electrically as an USB type B, device only, which sinks up to 15 W (5V, 3A max).

This USB is used for both power and comms

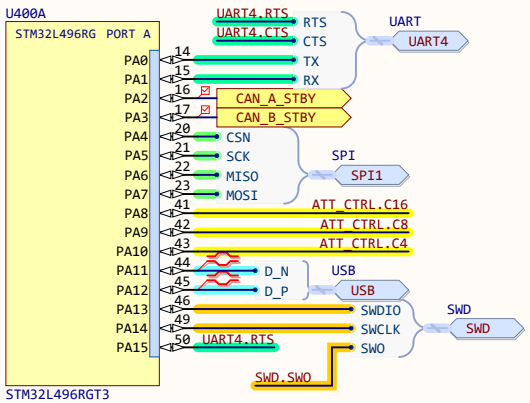
Notes:

Miscellaneous connectors: Debug, UART, USB. With ESD protections.
[1] STMicroelectronics Inc. STLINK-V3MINIE debugger/programmer User Manual, UM2910, Rev 3, 04-2024
[2] Tag-connect, ARM-CTX (20-pin ARM to TC2030) adapter for SWD datasheet.
[3] Tag-connect, TC2030-IDC datasheet, Rev B, 05-2019
[4] STMicroelectronics Inc. AN4879, Rev 6,

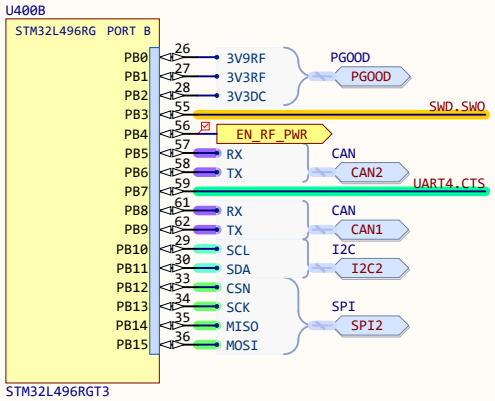
Title: *Ports*		**Author:** Juan Del Pino Mena	**Pluton UPV**
Prj: Estigia Comms Payload - EGSE		**Approved:** *	*Universitat Politècnica de València (UPV)*
		Prj. revision: 0.4	*Camí de Vera, València*
Date: 03/09/2024 19:56:44	**Last modified:** 02/09/2024	**Variant:** [No Variations]	*Spain*
Size: A4	Sheet 4 of 12	**Altium version:** 24.3.1.35	
File: 3_ports.SchDoc		**License:** --	
		Git Hash:	

I/O Ports

PORT A



PORT B

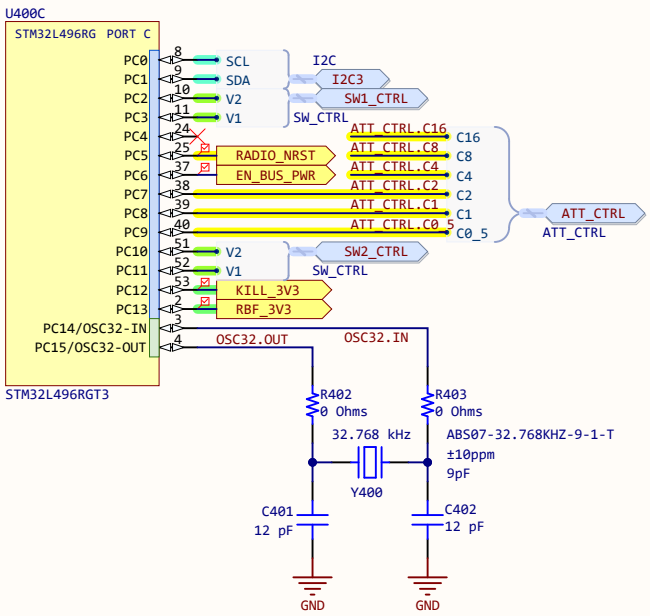


CAN A = CAN 1
CAN B = CAN 2

Altium warns about "net connection problems" when a bi-directional pin is connected to a input or output port. Ignore warning.

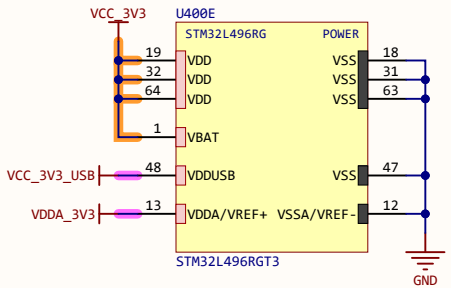
Many interfaces are defined and made available into the sheet symbol, so this sheet can be re-used easily between designs. Some peripherals are used both by the Carrier and EGSE, whereas others are only used in one of them.

PORT C

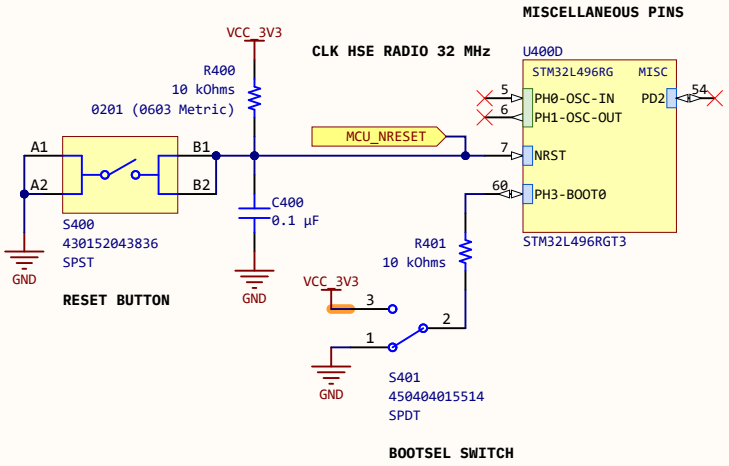


CLK LSE 32.768 kHz
This MCU should use the MSI clock

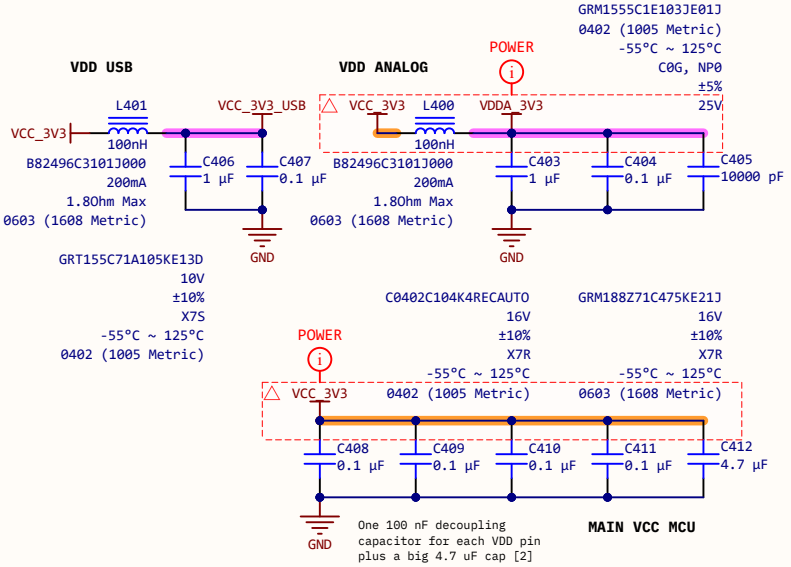
POWER PINS



Reset button and boot selection dip switch



Filtering & decoupling

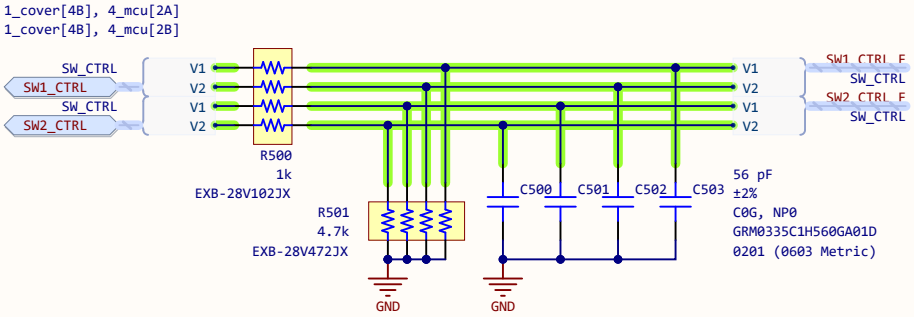


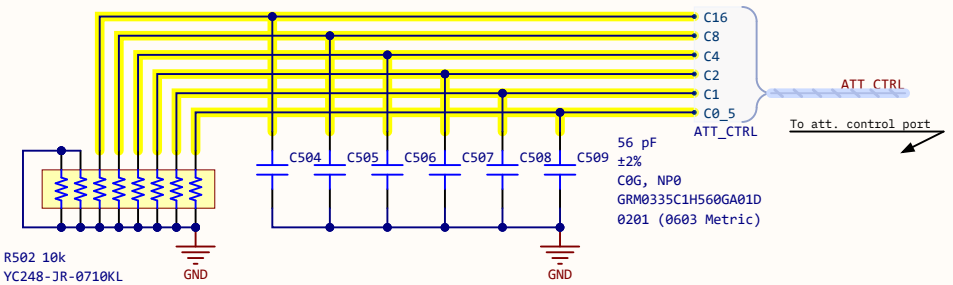
Notes:

[1] STMicroelectronics Inc. STM32L496xx Datasheet, DS11585, Rev 17, 11-2022
[2] STMicroelectronics Inc. Getting started with STM32L4/L4+ hardware dev., AN4555, Rev 9, 11-2022
[3] STMicroelectronics Inc. Oscillator design guide for STM32 MCUs, AN2687, Rev 19, 04-2023

Title: *Microcontroller*		**Author:** Juan Del Pino Mena	**Pluton UPV**
Prj: Estigia Comms Payload - EGSE		**Approved:** *	*Universitat Politècnica de València (UPV)*
Date: 03/09/2024 19:56:44	**Last modified:** 03/09/2024	**Prj. revision:** 0.4	*Camí de Vera, València*
Size: A4	Sheet 5 of 12	**Variant:** [No Variations]	*Spain*
File: 4_mcu.SchDoc		**Altium version:** 24.3.1.35	
		License: --	
		Git Hash:	

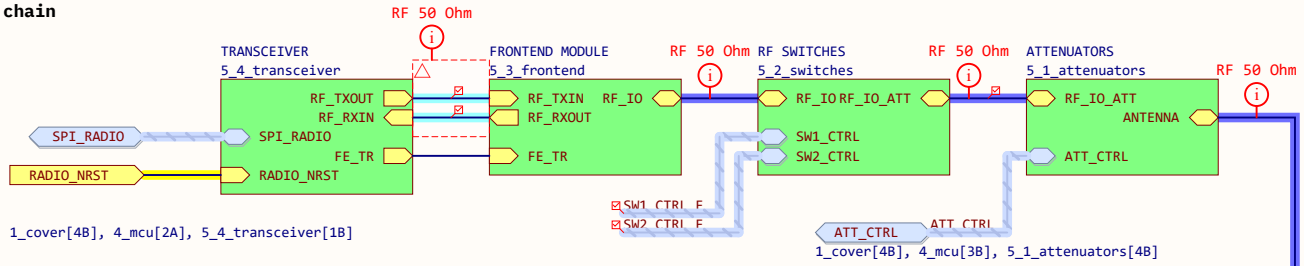
Filtering of control signals





Voltage divider needed because SKY13373-460LF
logic only supports 1.6 to 3.0 V

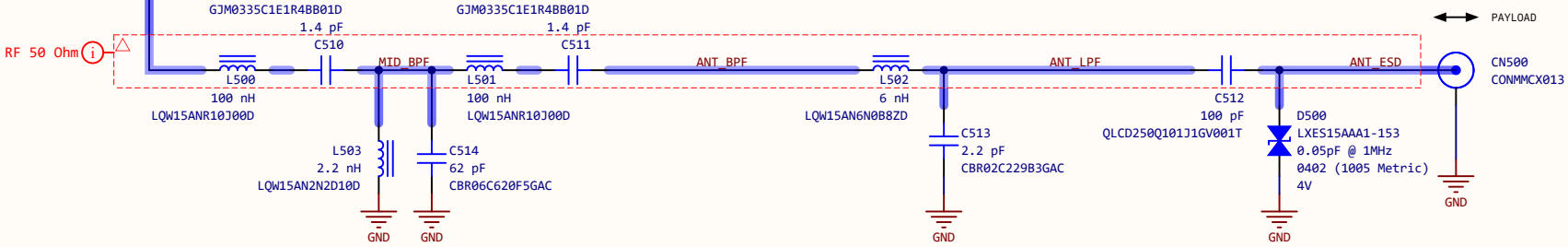
RF chain



3rd order Chebyshev band-pass filter
Fc = 435 MHz, BW = 50 MHz, IL(Fc) = 1 dB, RL(Fc) >= 20 dB
Za = Zb = 50 Ohm

LC lowpass filter & antenna matching
Fp = 435 MHz, Fc = 600 MHz, IL(Fp) = 0.1 dB,
RL(Fp) >= 50 dB, Zin = 50 Ohm, Zant = 55 Ohm

Coupling and ESD protection

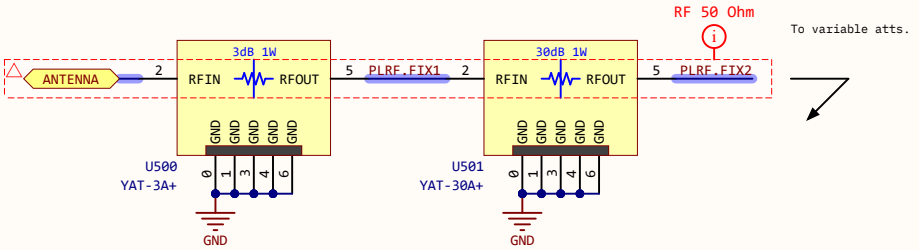


Notes:

Title: *RF path and LoRa transceiver*		**Author:** Juan Del Pino Mena	**Pluton UPV** *Universitat Politècnica de València (UPV) Camí de Vera, València Spain*
Prj: Estigia Comms Payload - EGSE		**Approved:** *	
		Prj. revision: 0.4	
		Variant: [No Variations]	
Date: 03/09/2024 19:56:44	**Last modified:** 02/09/2024	**Altium version:** 24.3.1.35	
Size: A4	Sheet 6 of 12	**License:** --	
File: 5_rf_path.SchDoc		**Git Hash:**	

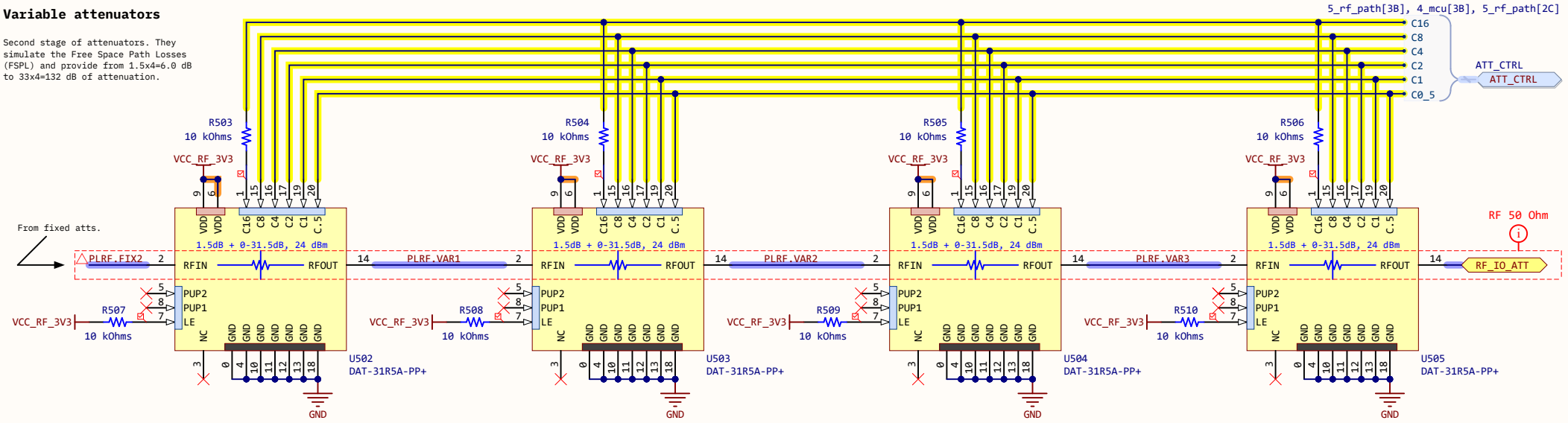
Fixed attenuators

First stage of attenuators. They dissipate the most power in the chain (up to 2W), and protect the RF ICs limiting the input RF power to a safe level.



Variable attenuators

Second stage of attenuators. They simulate the Free Space Path Losses (FSPL) and provide from 1.5x4=6.0 dB to 33x4=132 dB of attenuation.



Decoupling caps

Notes:

[1] Mini-Circuits Inc. YAT-30A+ datasheet, ECO-011434, REV. A, 01-2022
[2] Mini-Circuits Inc. YAT-3A+ datasheet, ECO-011434, REV. A, 01-2022
[3] Mini-Circuits Inc. DAT-31R5A-PP+ datasheet, M164761, REV. C, 05-2020

Title: *RF Attenuators*		**Author:**	Juan Del Pino Mena
		Approved:	*
Prj: Estigia Comms Payload - EGSE		**Prj. revision:**	0.4
		Variant:	[No Variations]
Date: 03/09/2024 19:56:44	**Last modified:** 02/09/2024	**Altium version:**	24.3.1.35
Size: A4	Sheet 7 of 12	**License:**	--
File: 5_1_attenuators.SchDoc		**Git Hash:**	

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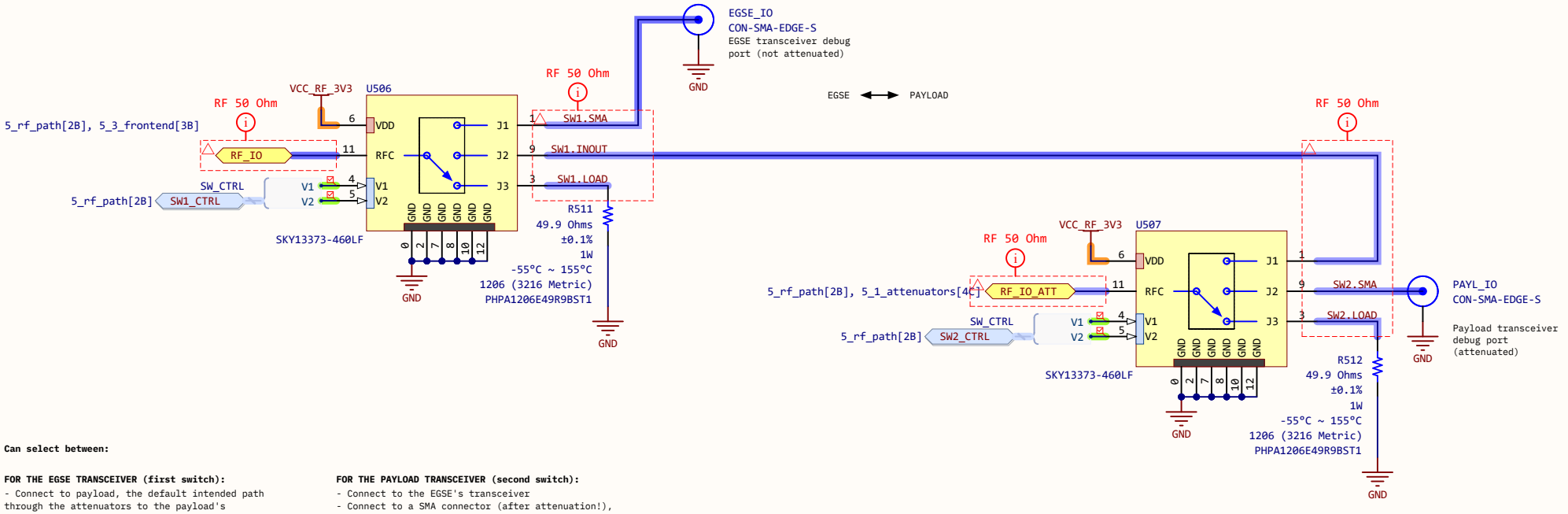
RF path selection switches



Can select between:

FOR THE EGSE TRANSCEIVER (first switch):
- Connect to payload, the default intended path through the attenuators to the payload's transceiver
- Connect to a SMA connector, rendering the transceiver's signal available for debugging purposes.
- Connect to 50-ohm load, to sink the rf signal if not used.

MMCX to payload, general-purpose SMA, 50-ohm load

FOR THE PAYLOAD TRANSCEIVER (second switch):
- Connect to the EGSE's transceiver
- Connect to a SMA connector (after attenuation!), rendering the transceiver output available for an antenna, an analyzer, etc.
- Connect to 50-ohm load, to sink the rf signal if not used.

Decoupling capacitors

Notes:

[1] Skyworks Inc. SKY13373-460LF Datasheet, 2012640, 05-2016

Title: *RF Switches*		**Author:** Juan Del Pino Mena	**Pluton UPV** *Universitat Politècnica de València (UPV) Camí de Vera, València Spain*
Prj: Estigia Comms Payload - EGSE		**Approved:** *	
		Prj. revision: 0.4	
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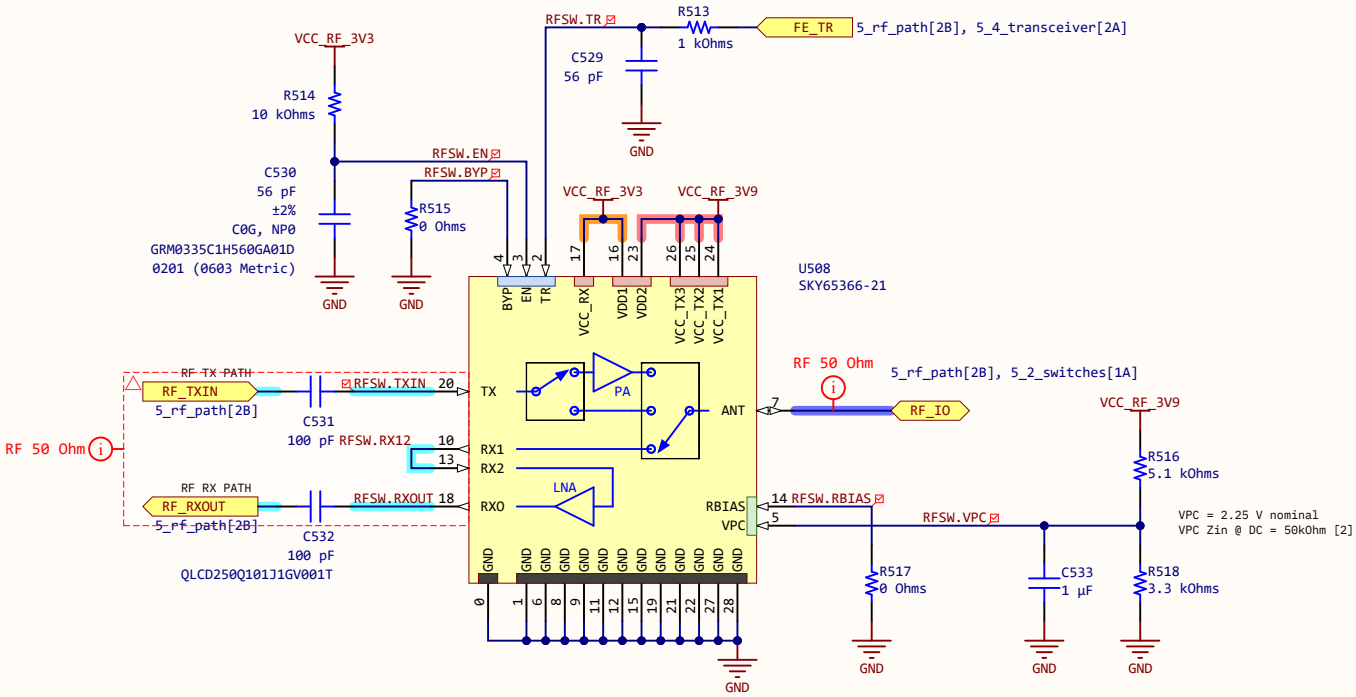
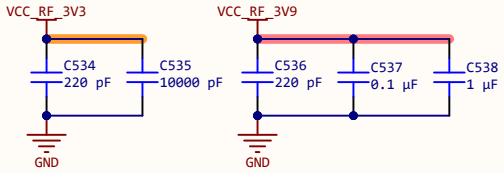
Date: 03/09/2024 19:56:45	**Last modified:** 03/09/2024	**Altium version:** 24.3.1.35	
Size: A4	Sheet 8 of 12	**License:** --	
File: 5_2_switches.SchDoc		**Git Hash:**	

RF Front-End module (Switch + LNA + PA)

Front-end module always enabled, never bypassed.



Decoupling capacitors



Notes:

[1] Semtech Inc. SX1302 Corecell Reference Design with SX1250 RF Front-Ends, PCB_E539V01A, 01-2020
[2] Skyworks Inc. SKY65366-21 400 MHz Tx/Rx Front-End Module, 203146E, 10-2020

Title: *RF Front-end module*		**Author:** Juan Del Pino Mena	**Pluton UPV** *Universitat Politècnica de València (UPV) Camí de Vera, València Spain*
Prj: Estigia Comms Payload - EGSE		**Approved:** *	
		Prj. revision: 0.4	
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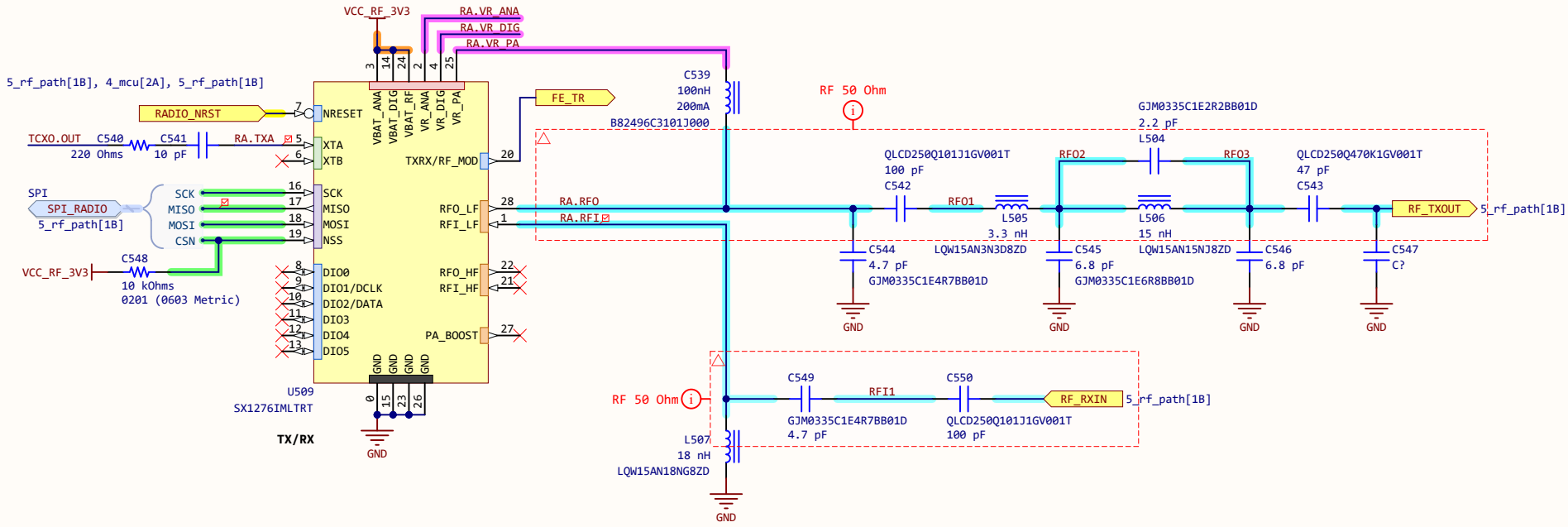
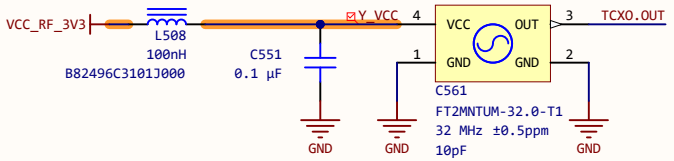
Date: 03/09/2024 19:56:45	**Last modified:** 03/09/2024	**Altium version:** 24.3.1.35	
Size: A4	Sheet 9 of 12	**License:** --	
File: 5_3_frontend.SchDoc		**Git Hash:**	

LoRa Node Transceiver

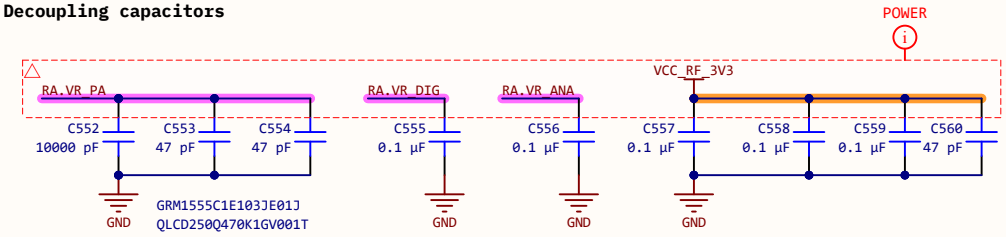


Xtal oscillator

Clipped-sine output TCXO are required, Vout_pp <= 1.2 V. Recommended a GPS-precision TCXO (0.5 ppm). A TCXO should be connected to pin XTA through a 220-ohm res and a 10 pF DC-cut cap to reduce the amplitude [4]. Pin XTB should be left open [1].



Decoupling capacitors



Notes:

[1] Semtech Inc. SX127x datasheet, Rev 7, 05-2020
[2] Semtech Inc. SX127x reference design overview, AN1200.19, 12-2014
[3] Semtech Inc. SX1276 433/915 MHz reference design SX1276MB1LAS, PCB_E311V02A, v1a, 02-2015

Title: *LoRa node transceiver*		**Author:** Juan Del Pino Mena	**Pluton UPV** *Universitat Politècnica de València (UPV) Camí de Vera, València Spain*
Prj: Estigia Comms Payload - EGSE		**Approved:** *	
		Prj. revision: 0.4	
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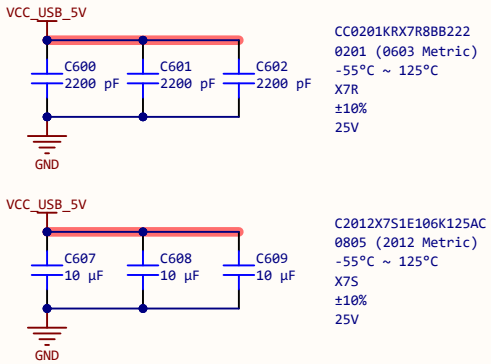
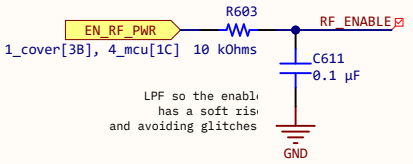
Date: 03/09/2024 19:56:45	**Last modified:** 02/09/2024	**Altium version:** 24.3.1.35	
Size: A4	Sheet 10 of 12	**License:** --	
File: 5_4_transceiver.SchDoc		**Git Hash:**	

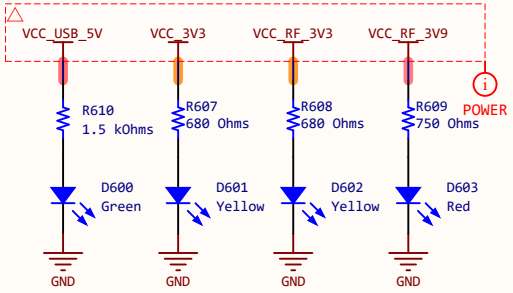
Decoupling capacitors



Enable RF supply



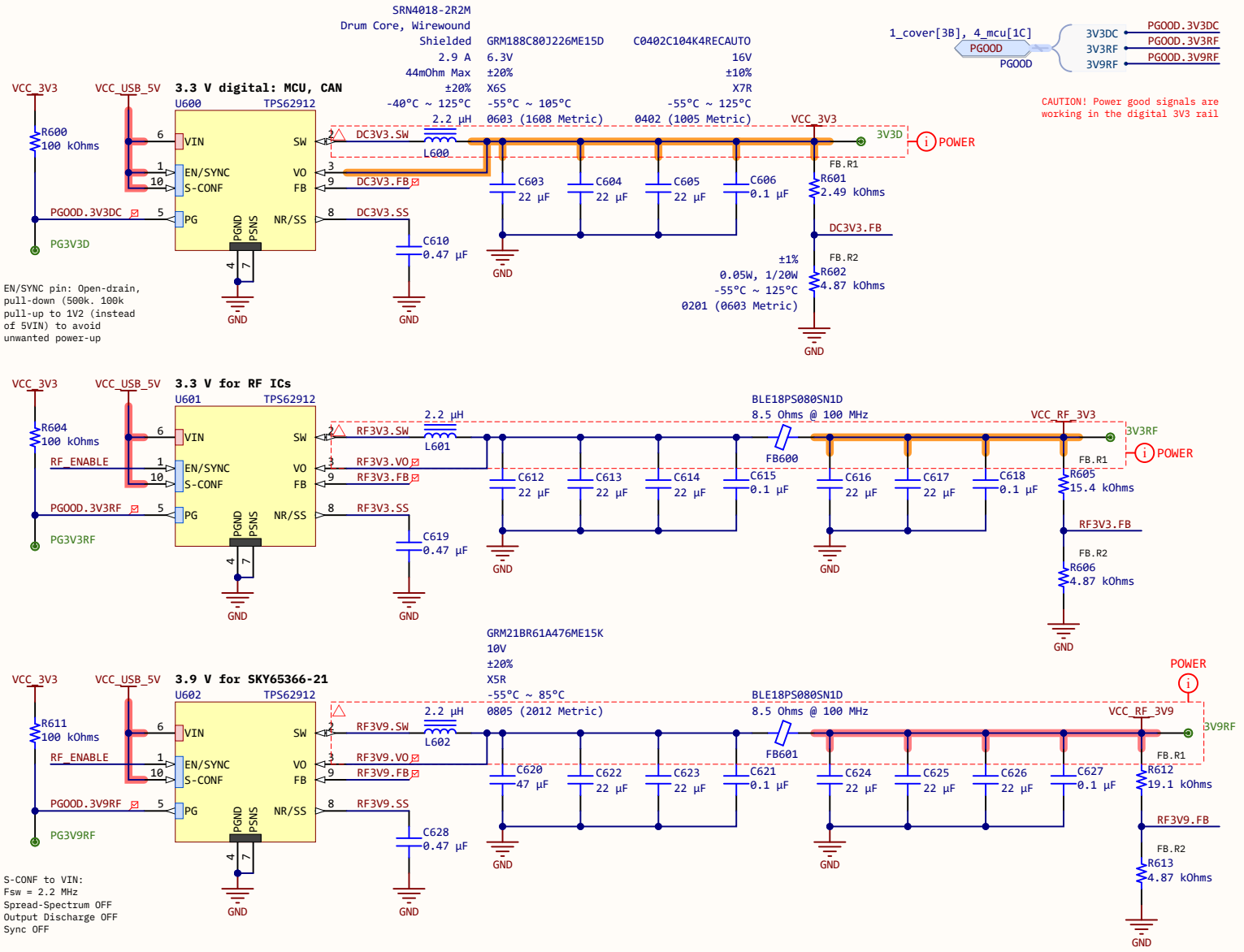
Power LED indicators



The TPS62912 PG pin is in high Z when V(FB) >= 95%, and driven low when V(FB) <= 90% . The open-drain pin requires a pullup. The PG signal is used for sequencing of multiple rails by connecting to the EN pin of other converters [1].

To ensure control of all digital IOs during the power-up/down of the SX1302 and avoid an inrush current, the 1.2 V rail shall be enabled before 3.3 V at start-up [2].

Low noise DC/DC converters



Notes:

Power supply based on low-noise DC/DC converters.
[1] Texas Instruments Inc. TPS62912/3 datasheet, SLVSFP4B, 03-2021
[2] Semtech Inc. Errata Note Corecell PCB #e539v01e Reference Design, Rev 1.0, 03-2020

Title: *Power management*		**Author:** Juan Del Pino Mena	
Prj: Estigia Comms Payload - EGSE		**Approved:** *	
		Prj. revision: 0.4	
		Variant: [No Variations]	
Date: 03/09/2024 19:56:45	**Last modified:** 31/08/2024	**Altium version:** 24.3.1.35	
Size: A4	Sheet 11 of 12	**License:** --	
File: 6_power_dcdc.SchDoc		**Git Hash:**	

Pluton UPV
Universitat Politècnica de València (UPV)
Camí de Vera, València
Spain

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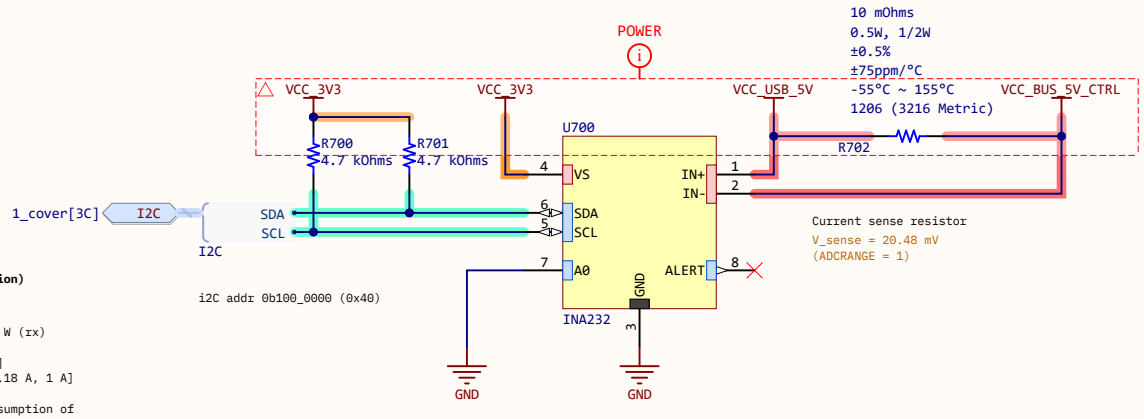
Voltage, current and power monitor

Power measurement excludes EGSE's own consumption. It only monitors the payload's.



R_SHUNT selection (early power budget estimation)

Carrier power consumption: 0.33 W (max)
LoRa SoM power consumption: 4.62 W (tx); 0.58 W (rx)

Expected total power consumption: [0.9 W, 5 W]
Thus, at V_cc = 5 V : current consumption: [0.18 A, 1 A]

Account for an instantaneous peak current consumption of double the maximum: I_peak = 2 A

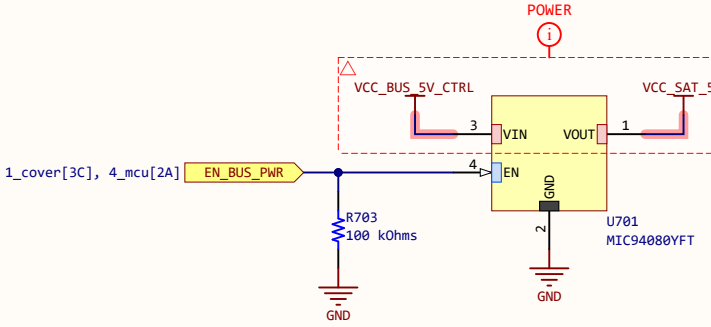
For minimum voltage drop, V_sense = 20.48 mV (INA232 cfg)

R_shunt < V_sense / I_peak = 10.24 mOhm

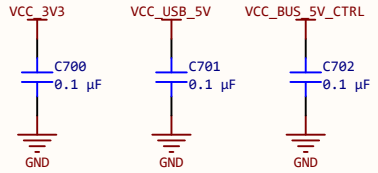
Power dissipated on R_shunt: 42 mW

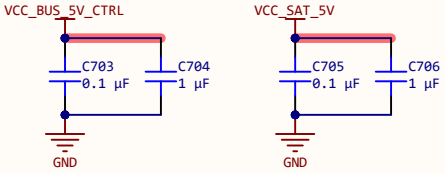
R_shunt = 10 mOhm, tolerance <=0.5 %, power >= 0.1 W

Load power switch



Decoupling capacitors





Notes:

[1] Texas Instruments Inc. INA232 datasheet, SBOSAA2, 12-2022
[2] Semtech Inc. Errata Note Corecell PCB #e539v01e Reference Design, Rev 1.0, 03-2020
[3] Microchip Inc. MIC94080/1/2/3/4/5 datasheet, DS20006118A, 2019

Title: *Bus power control & monitoring*		**Author:**	Juan Del Pino Mena
		Approved:	*
Prj: Estigia Comms Payload - EGSE		**Prj. revision:**	0.4
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Date: 03/09/2024 19:56:46	**Last modified:** 11/08/2024	**Altium version:**	24.3.1.35
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File: 7_power_prot_mon.SchDoc		**Git Hash:**	

Pluton UPV
Universitat Politècnica de València (UPV)
Camí de Vera, València
Spain

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