PROJECT:

LoRa Comms Payload: System-on-Module

PART OF THE MASTER'S THESIS:

"Development of a LoRa-based communications payload for CubeSat"

MASTER'S DEGREE IN ELECTRONIC SYSTEMS ENGINEERING
POLYTECHNIC UNIVERSITY OF VALENCIA
ACADEMIC COURSE 2023/2024

AUTHOR:

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DEPARTMENT OF ELECTRONIC ENGINEERING

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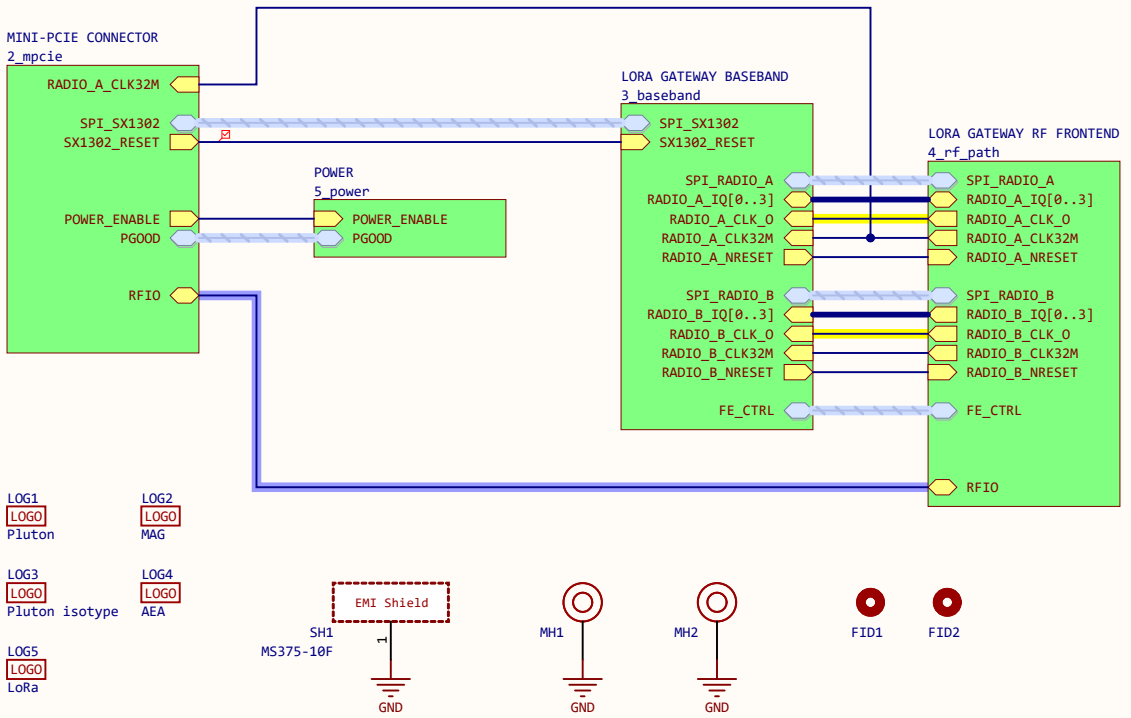
DEPARTMENT OF COMMUNICATIONS



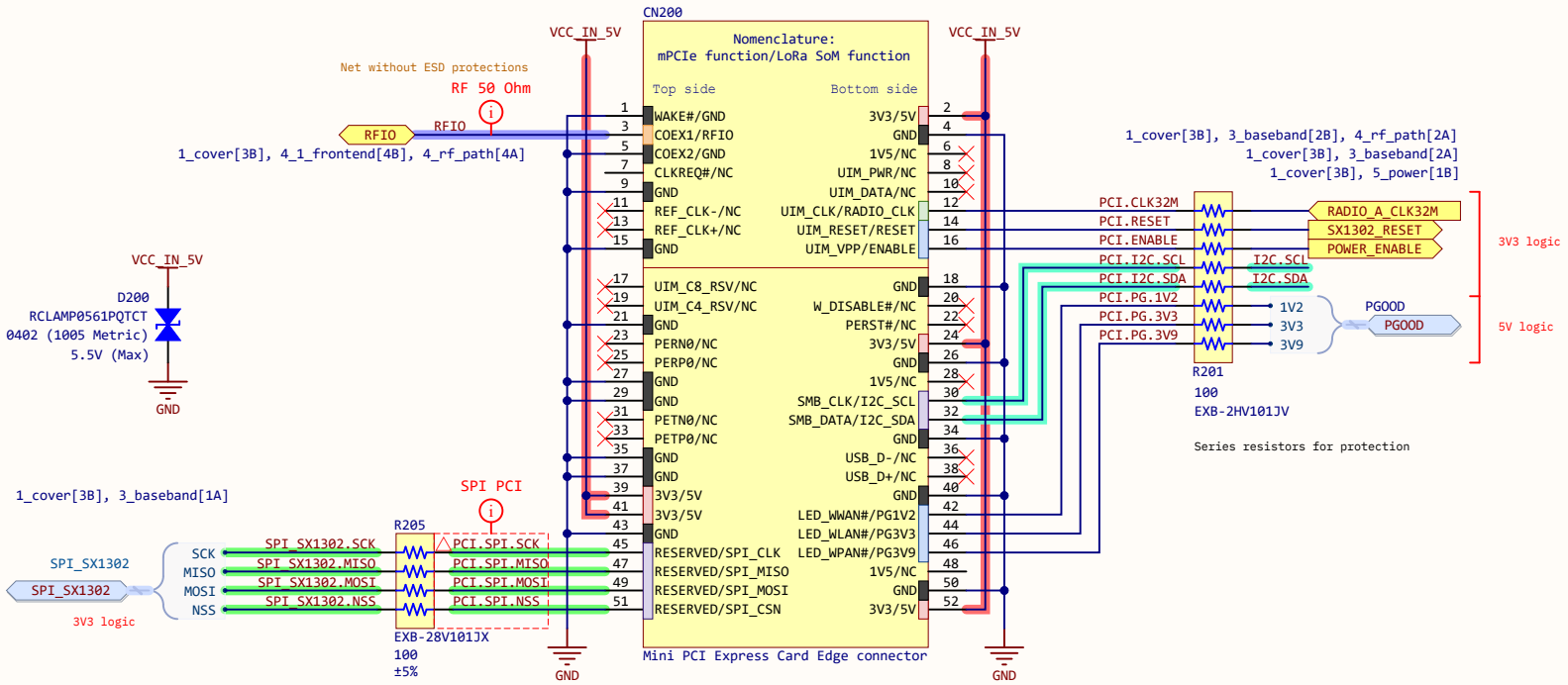
DEVELOPED IN PROUD COLLABORATION WITH:

Notes:

System-on-Module device with mPCIe form factor containing a LoRa gateway and RF frontend, with output via MMCX connector.

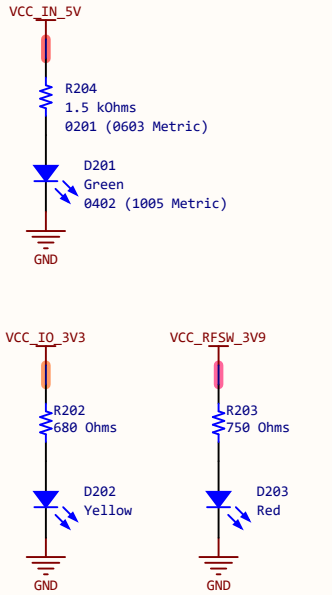
Title: *Cover and Block Diagram*		**Author:** Juan Del Pino Mena	**Pluton UPV**
Prj: Estigia comms payload - LoRa Gateway SoM		**Approved:** --	*Universitat Politècnica de València (UPV)*
		Prj. revision: 0.4	*Camí de Vera, València*
Date: 2024-08-11 13:32:40	**Last modified:** 2024-08-11	**Variant:** [No Variations]	*Spain*
Size: A4	Sheet 1 of 6	**Altium version:** 24.3.1.35	
File: 1_cover.SchDoc		**License:** --	
		Git Hash: 33fbb30496290060a8401dcbf550be183a479c3 [Locally Modified]	

Mini-PCI-express card edge connector

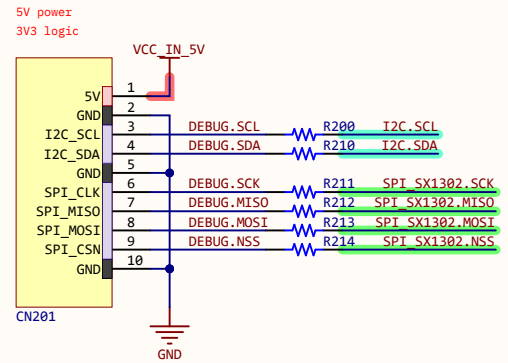


Power LED indicators

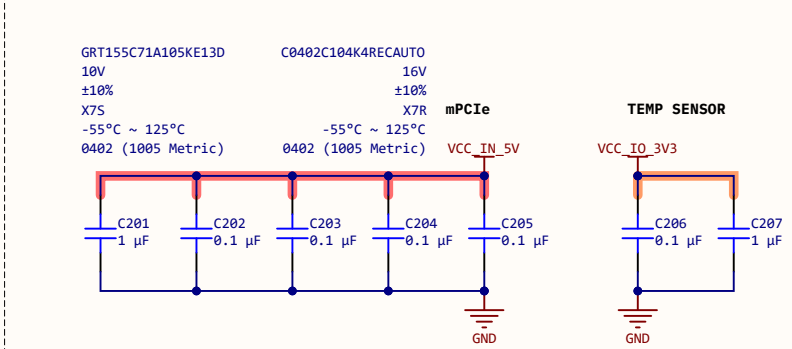
1V2 does not have an indicator since is too low voltage to lit a LED



Debug ports

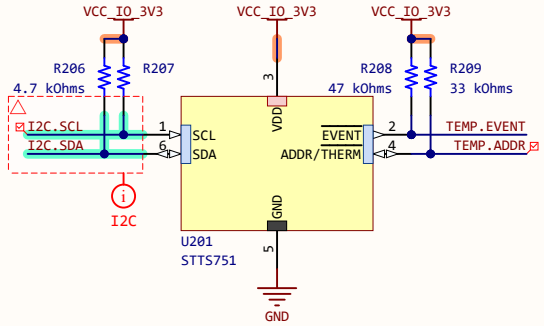


Decopling capacitors



One 100 nF cap per pin, a larger 1uF to stabilize supply. Place near the mPCIe pins.

Temperature sensor



i2c addr 0b011_1001 (0x39)

Notes:

The mPCIe connector is used in a non-standard configuration, neither the signals, nor the supply voltages. DO NOT CONNECT TO A REGULAR MPCIE SOCKET.

[1] Texas Instruments Inc. TXB0104 datasheet, SCES650J, 10-2020
[2] STMicroelectronics Inc. STTS751 datasheet, DocID 16483, Rev 7, 05-2019

Title: *Mini-PCIe and thermal sensor*		**Author:**	Juan Del Pino Mena
Prj: Estigia comms payload - LoRa Gateway SoM		**Approved:**	--
		Prj. revision:	0.4
		Variant:	[No Variations]
Date: 2024-08-11 13:32:41	**Last modified:** 2024-08-11	**Altium version:**	24.3.1.35
Size: A4	Sheet 2 of 6	**License:**	--
File: 2_mpcie.SchDoc		**Git Hash:**	41b6ea28c7eaa4a034106408df395347186357a6 [Locally Modified]

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Spain

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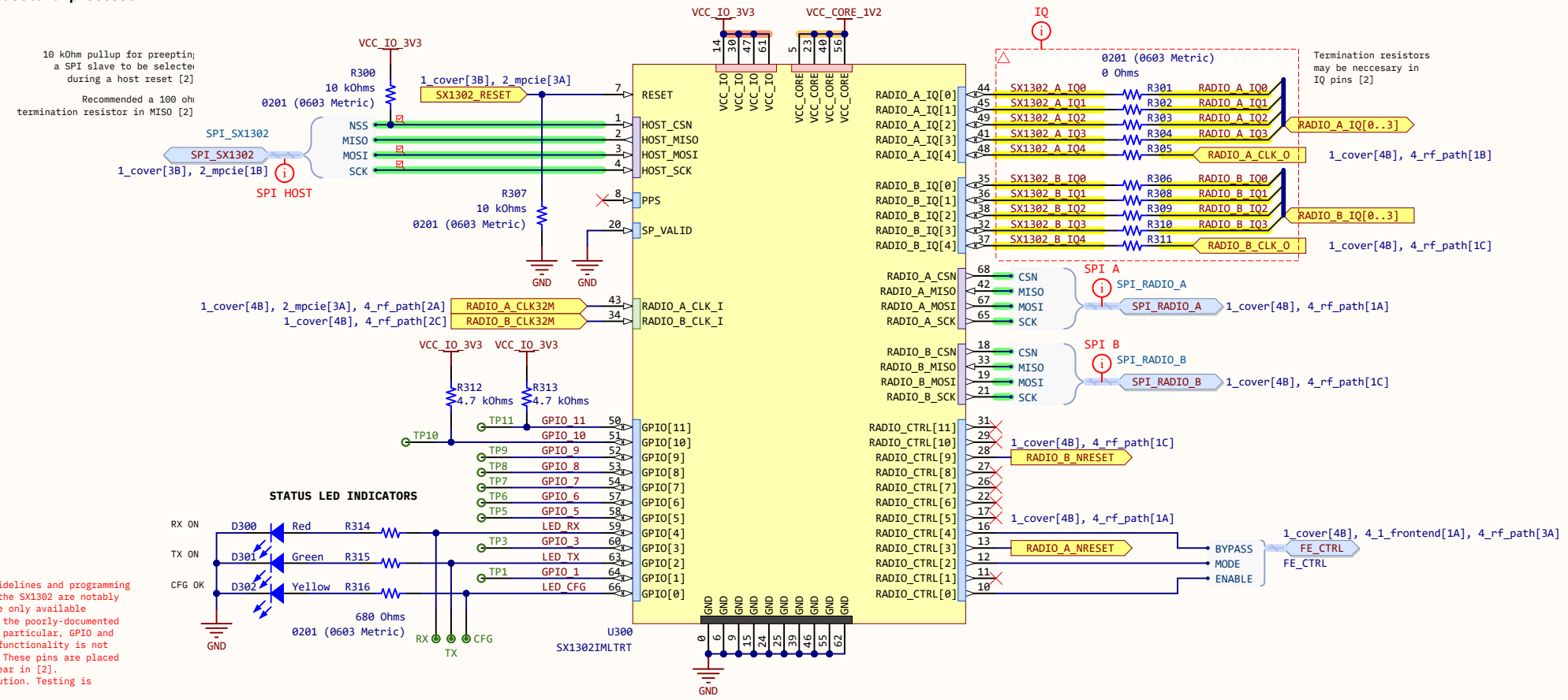
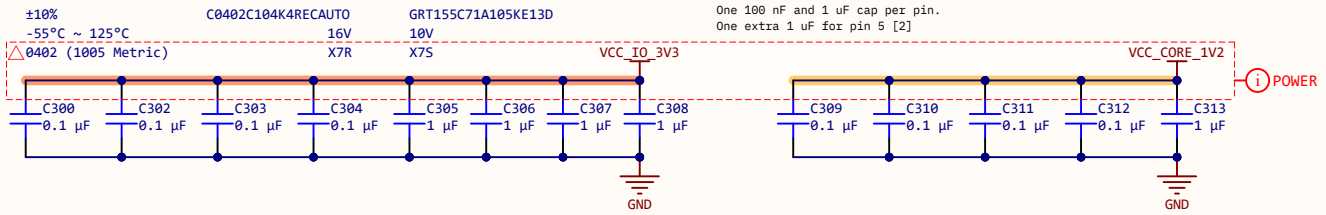
SX1302 baseband processor



Decoupling capacitors



Notes:

[1] Semtech Inc. SX1302 LoRa Gateway Baseband Processor Datasheet, DS.SX1302.W.APP, v1.2, 10-2020
[2] Semtech Inc. SX1302 Corecell Reference Design with SX1250 RF Front-Ends, PCB_E539V01A, 01-2020
[3] Semtech Inc. SX1302 Hardware Abstraction Layer repo, https://github.com/Lora-net/sx1302_hal

Title: *LoRa Baseband processor*		**Author:** Juan Del Pino Mena	
Prj: Estigia comms payload - LoRa Gateway SoM		**Approved:** --	
		Prj. revision: 0.4	
		Variant: [No Variations]	
Date: 2024-08-11 13:32:41	**Last modified:** 2024-08-11	**Altium version:** 24.3.1.35	
Size: A4	Sheet 3 of 6	**License:** --	
File: 3_baseband.SchDoc		**Git Hash:** 41b6ea28c7eaa4a03410640 8df395347186357a6 [Locally Modified]	

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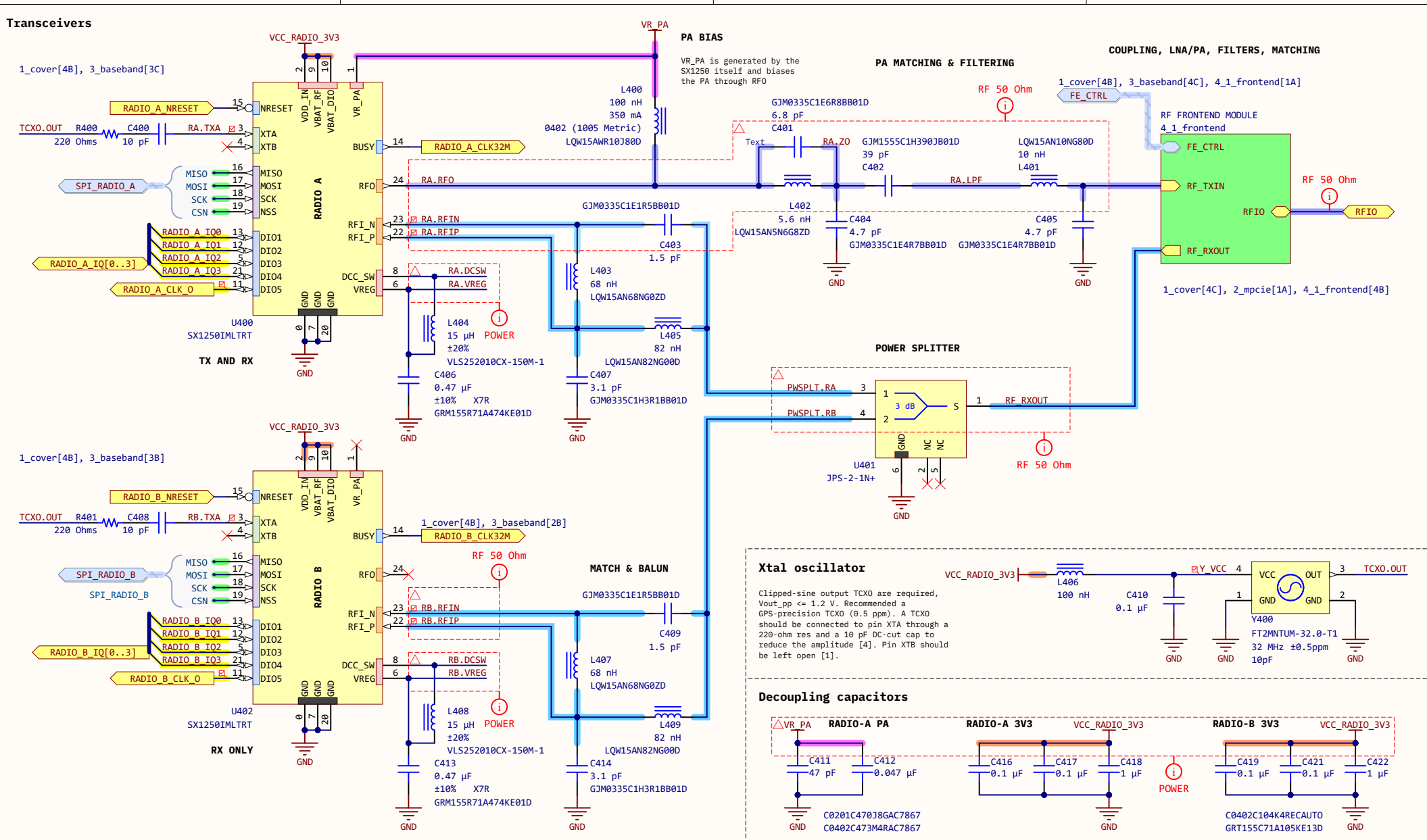

Notes:

[1] Semtech Inc. SX1302 LoRa Gateway Baseband Processor Datasheet, DS.SX1302.W.APP, v1.2, 10-2020
[2] Semtech Inc. SX1302 Corecell Reference Design with SX1250 RF Front-Ends, PCB_E539V01A, 01-2020
[3] Semtech Inc. SX1250 Multi-band Sub-GHz RF Front End Datasheet, DS.SX1250.W.APP, v1.2, 09-2019
[4] Semtech Inc. PCB Design Guidelines, AN1200.66, v1.1, 09-2022
[5] Semtech Inc. SX1261/2 Reference Design Explanation, AN1200.40, v1.1, 05-2018
[6] Silicon Labs Inc. Si446x/Si4362 RX LNA Matching, AN643, v0.4, 2014

Title: *LoRa Transceivers*		**Author:**	Juan Del Pino Mena
Prj: Estigia comms payload - LoRa Gateway SoM		**Approved:**	--
		Prj. revision:	0.4
		Variant:	[No Variations]
Date: 2024-08-11 13:32:42	**Last modified:** 2024-08-11	**Altium version:**	24.3.1.35
Size: A4	Sheet 4 of 6	**License:**	--
File: 4_rf_path.SchDoc		**Git Hash:**	41b6ea28c7eaa4a034106408df395347186357a6 [Locally Modified]

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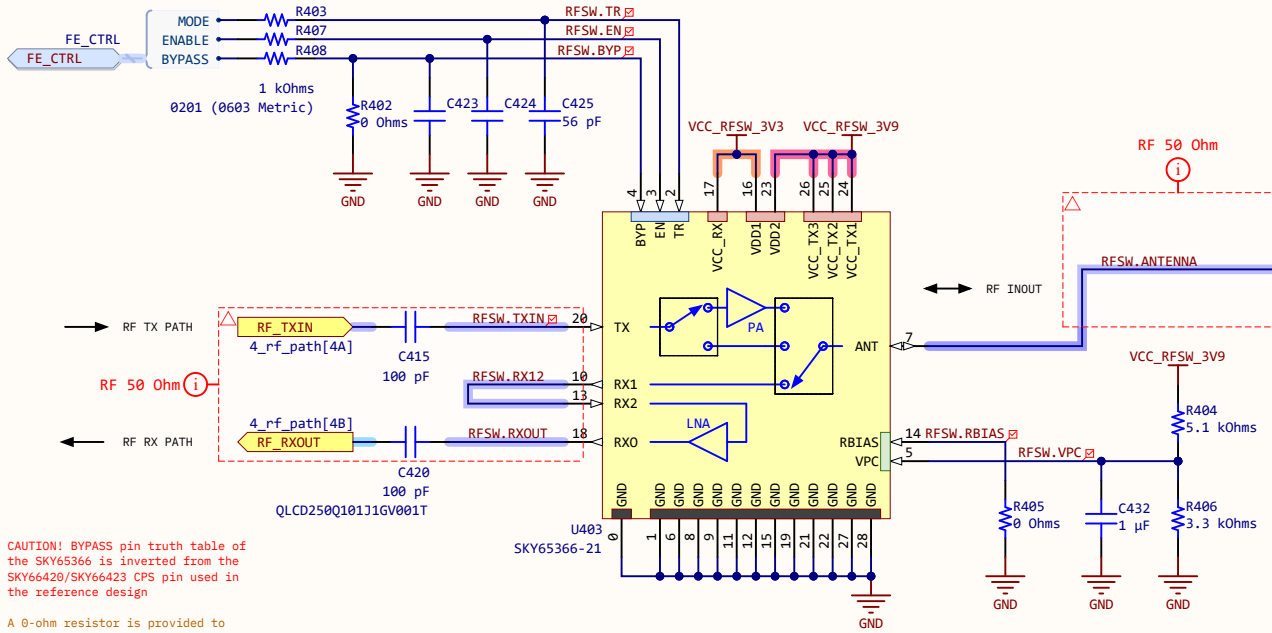
RF Frontend module

4_rf_path[4A], 3_baseband[4C], 4_rf_path[3A]



CAUTION! BYPASS pin truth table of the SKY65366 is inverted from the SKY66420/SKY66423 CPS pin used in the reference design

A 0-ohm resistor is provided to short BYP to GND to disable BYPASS if necessary

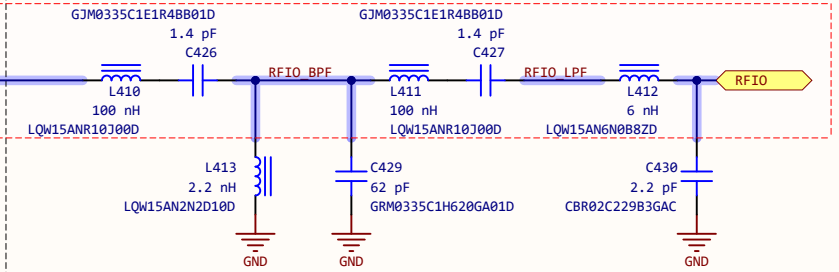
VPC = 2.25 V nomina
VPC Zin @ DC = 50kOhm [2]

Band Filtering, antenna matching and ESD protection

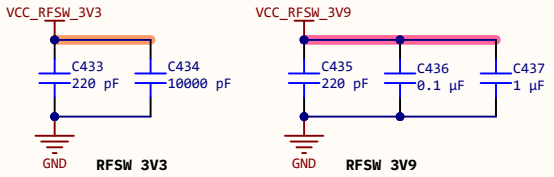
3rd order Chebyshev band-pass filter
Fc = 435 MHz, BW = 50 MHz, IL(Fc) = 1 dB,
RL(Fc) >= 20 dB, Za = Zb = 50 Ohm

LC lowpass filter & antenna matching
Fp = 435 MHz, Fc = 600 MHz, IL(Fp) = 0.1 dB,
RL(Fp) >= 50 dB, Zin = 50 Ohm, Zant = 55 Ohm

4_rf_path[4A], 2_mpcie[1A], 4_rf_path[4A]



Decoupling capacitors

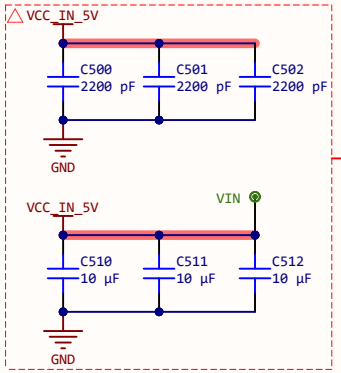


Notes:

[1] Semtech Inc. SX1302 Corecell Reference Design with SX1250 RF Front-Ends, PCB_E539V01A, 01-2020
[2] Skyworks Inc. SKY65366-21 400 MHz Tx/Rx Front-End Module, 203146E, 10-2020

Title: *RF FrontEnd module*		**Author:** Juan Del Pino Mena	**Pluton UPV** *Universitat Politècnica de València (UPV) Camí de Vera, València Spain*
Prj: Estigia comms payload - LoRa Gateway SoM		**Approved:** --	
		Prj. revision: 0.4	
		Variant: [No Variations]	
Date: 2024-08-11 13:32:42	**Last modified:** 2024-08-11	**Altium version:** 24.3.1.35	
Size: A4	Sheet 5 of 6	**License:** --	
File: 4_1_frontend.SchDoc		**Git Hash:** 41b6ea28c7eaa4a03410640 8df395347186357a6 [Locally Modified]	

Decoupling capacitors

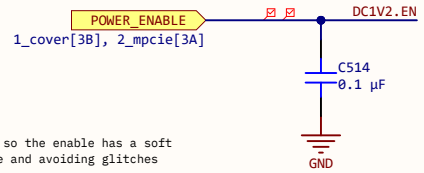


CC0201KRX7R8BB222
0201 (0603 Metric)
-55°C ~ 125°C
X7R ±10% 25V

GMC10X7R106K10NT
0603 (1608 Metric)
-55°C ~ 125°C
X7R ±10% 10V

One 2.2 nF plus one 10 uF per converter

Enable input

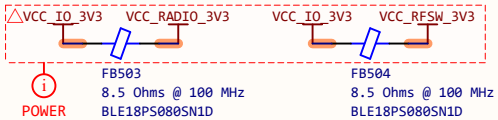


LPF so the enable has a soft rise and avoiding glitches

Power Good output

CAUTION! Power good signals are working in the 1V2 logic voltage.

Filtering the 3V3 rail



The TPS62912 PG pin is in high Z when V(FB) >= 95%, and driven low when V(FB) <= 90% . The open-drain pin requires a pullup. The PG signal is used for sequencing of multiple rails by connecting to the EN pin of other converters [1].

To ensure control of all digital IOs during the power-up/down of the SX1302 and avoid an inrush current, the 1.2 V rail shall be enabled before 3.3 V at start-up [2].

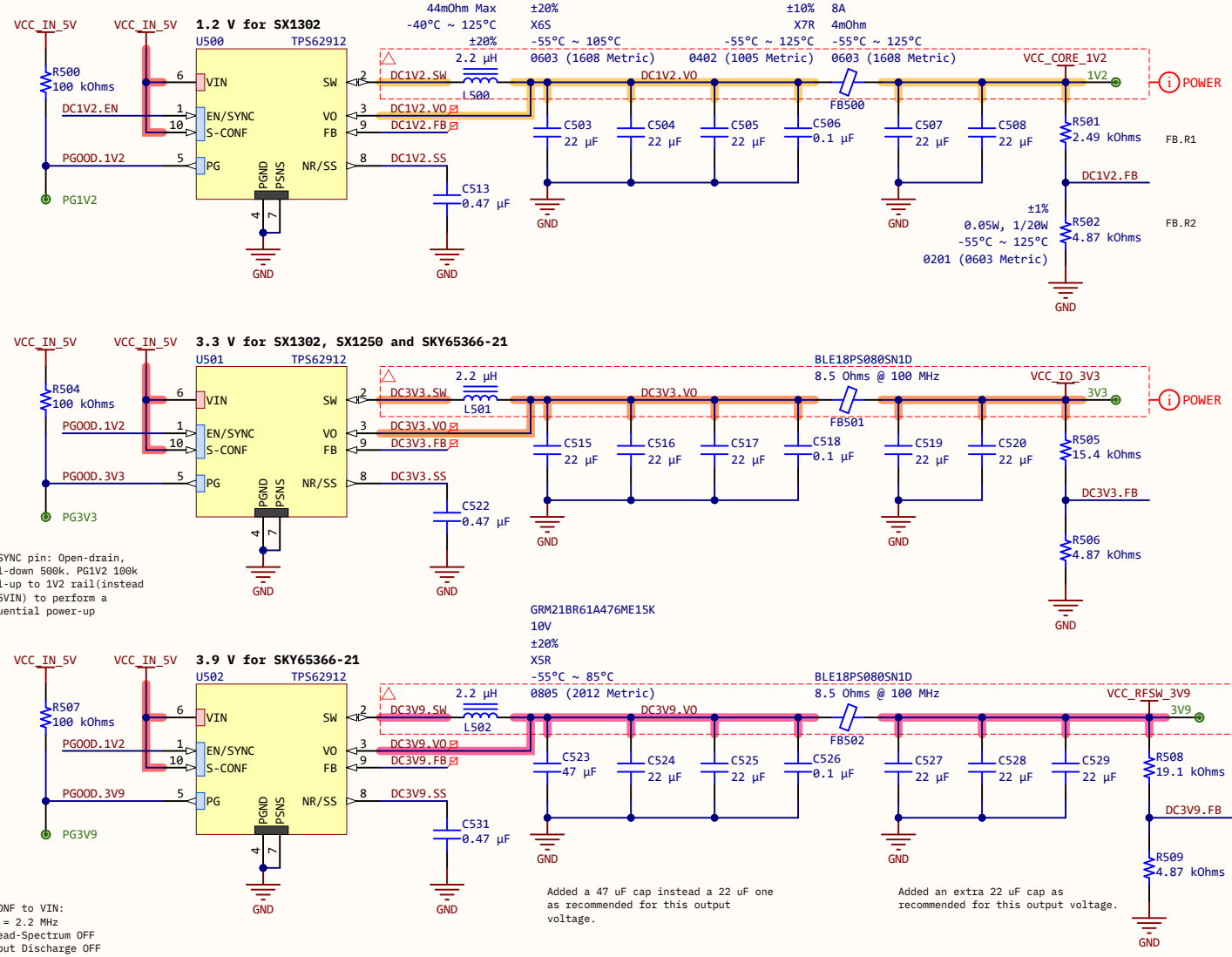
Low noise DC/DC converters

SRN4018-2R2M
Drum Core, Wirewound
Shielded
2.9 A
44mOhm Max
-40°C ~ 125°C
±20%

GRM188C80J226ME15D
6.3V
±20%
X6S
-55°C ~ 105°C
0603 (1608 Metric)

C0402C104K4RECAUTO
16V
±10%
X7R
-55°C ~ 125°C
0402 (1005 Metric)

BLE18PS080SN1D
8.5 Ohms @ 100 MHz
8A
4mOhm
-55°C ~ 125°C
-55°C ~ 125°C
0603 (1608 Metric)



GRM21BR61A476ME15K
10V
±20%
X5R
-55°C ~ 85°C
0805 (2012 Metric)

EN/SYNC pin: Open-drain, pull-down 500k. PG1V2 100k pull-up to 1V2 rail(instead of 5VIN) to perform a sequential power-up

S-CONF to VIN:
Fsw = 2.2 MHz
Spread-Spectrum OFF
Output Discharge OFF
Sync OFF

Added a 47 uF cap instead a 22 uF one as recommended for this output voltage.

Added an extra 22 uF cap as recommended for this output voltage.

Notes:

Power supply based on low-noise DC/DC converters with sequential power-up.
[1] Texas Instruments Inc. TPS62912/3 datasheet, SLVSFP4B, 03-2021
[2] Semtech Inc. Errata Note Corecell PCB #e539v01e Reference Design, Rev 1.0, 03-2020

Title:	***Power supply***
Prj:	Estigia comms payload - LoRa Gateway SoM
Date:	2024-08-11 13:32:42
Last modified:	2024-08-11
Size:	A4
Sheet	6 of 6
File:	5_power.SchDoc
Author:	Juan Del Pino Mena
Approved:	--
Prj. revision:	0.4
Variant:	[No Variations]
Altium version:	24.3.1.35
License:	--

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Git Hash: 41b6ea28c7eaa4a034106408df395347186357a6 [Locally Modified]