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POLITÈCNICA
DE VALÈNCIA

— **TELECOM**
UPV VLC

**MASTER'S DEGREE IN
TELECOMMUNICATIONS ENGINEERING**

Master's Thesis

“Alcázar: a free and open-source template for academic works, for nerd grown-up kids who do boring stuff such as theses with endless titles”

ACADEMIC COURSE: 2076/2077

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Department of Electronic Engineering



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KEYWORDS:

Keyword 1, Keyword 2, Keyword 3, Keyword 4, Keyword 4, Keyword 5, Keyword 6, Keyword 7, Keyword 8, Keyword 9, Keyword 10, Keyword N

ABSTRACT:

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Publications

The Master's Degree candidate, Name of the author of the thesis, has co-authored the following publications with Prof. Name of the supervisor of the thesis et al. The articles come as a result of the research activities carried out during the Master's Thesis. The candidate is the corresponding author in two of the three publications listed below:

- [1] M. Vega and J. Ramirez, "Neural augmentation and techno-spirituality," *Journal of Cybernetic Studies*, vol. 14, no. 3, pp. 187–212, 2053.
- [2] A. Jensen and A. Navarre, "On transhumanism and global power struggles: A post augmentation incident analysis," *National Augmentation*, vol. 32, no. 2, pp. 75–98, 2052.
- [3] S. Spiegel and J. Black, "The art of bounty hunting to the rhythm of jazz," in *Space Bounty Hunter Conference*, Bounty Hunter Guild, Convention Center, Mars City: Valentine Publications, Jun. 2071, pp. 45–50.

Note: [3] is not yet published.

ACKNOWLEDGEMENTS

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AGRADECIMIENTOS

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*“Y así, mi señor, es como sabemos que
la Tierra tiene forma de plátano”*

Sir Bedevere el Sabio

Interpretado por TERRY JONES

En *Monty Python y los caballeros
de la mesa cuadrada*, 1975

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Glossary

[A](#) | [C](#) | [D](#) | [F](#) | [G](#) | [I](#) | [J](#) | [N](#) | [P](#) | [R](#) | [S](#)

A

Adiabatic process A kind of thermodynamic process in which the thermodynamic system does not exchange heat or mass with its surrounding environment [1](#), [9](#)

C

Coupling capacitor A capacitor used to couple an AC signal from one circuit phase to another, blocking the DC component. Functionally opposite to a [Decoupling capacitor](#) [2](#)

D

Decoupling capacitor A decoupling capacitor removes unwanted AC components ([Noise](#) and [Ripple](#)) from a DC signal. Usually located on the power input pins of an active device, it's a common and effective technique for noise filtering on power traces. It provides a charge reserve physically near to the component, which supplies energy to it in case of an irregular or pulsed power consumption, thus preventing the supply voltage from decaying [xxi](#), [5](#)

F

Fiducial marks On a [PCB](#), fiducial marks are pads which act as reference points for [Stencil](#) alignment, computer vision automated component placement by [Pick and Place machine](#) machines and optical inspections systems. To achieve the best precision, three should be placed as far apart as possible [17](#)

G

GNU (GNU's Not Unix!) [xxi](#), [15](#)

I

IPython (Interactive Python) is a command shell for originally developed for [Python](#) (but nowadays it supports many other programming languages). It offers an interactive shells, debugging, media support, a browser-based notebook interface and parallel computing. [xxi](#)

J

Jupyter Lab A web-based interactive development environment for notebooks, code, and data. It is an open, flexible environment with support for extensions. Jupyter supports multiple programming languages, but the main one is [Python](#), which uses [IPython](#) as an interpreter and kernel [1](#), [9](#)

N

Noise Unwanted and unpredictable disturbance in a signal [xxi](#)

P

PCB (Printed Circuit Board) A rugged, non-conductive boards built on a dielectric substrate structure used to provide electrical connection between the components of a electronic circuit, as well as mechanical support for those components [xxi](#)

Pick and Place machine A machine with a robot arm and computer vision for picking components from a feeder and inserting them into a specific site on the [PCB](#) [xxi](#)

Python A high-level, cross-platform, interpreted, dynamically-typed, garbage-collected, general-purpose programming language. Has strong emphasis in code readability and includes a comprehensive standard library. It supports structured, object-oriented and functional programming paradigms [xxi](#)

R

Re-flow soldering The process consists on joining components to substrates by placing the parts into [Solder paste](#) and then warming the paste up to its melting point for a short period of time, in order to achieve re-flow and the interconnection between a component terminal and a [PCB](#) pad [xxii](#)

Ripple A residual, periodic variation of a DC voltage due to incomplete suppression of the AC signal after rectification [xxi](#)

S

Solder mask The insulating polymer coating used to mask or protect the [PCB](#)'s copper tracks

from corrosion and oxidation, dirt, dust, and fingerprints. It also prevents masked areas of being poured by solder during [Re-flow soldering](#) and other processes such as etching or plating. This way, no shorts are created between tracks. Solder mask give PCBs a distinct colour, usually green [xxii](#)

Solder paste A sticky mixture of powdered solder (the fusible metal alloy which bonds pads and

components) and flux (a viscous chemical cleaning agent) [xxi](#), [xxii](#)

Stencil A sheet of material (usually plastic or stainless steel) with openings according to the [Solder mask](#). The apertures are the same shape and size as the SMD component pads, and are placed in their corresponding position. With the stencil it is easy to deposit the right amount of [Solder paste](#) accurately and repeatably [xxi](#)

Introduction

1.1 Alcázar

This is an example of how this template may be used. As we can see in [Figure 1.1](#), the [Jupyter Lab](#) is lorem ipsum dolor sit amet [1], consectetur adipiscing elit. Integer tempus quis elit id sagittis. Cras tincidunt nisi at tellus luctus, et congue dolor posuere. Aliquam suscipit felis sit amet lacus ultrices aliquet.

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Figure 1.1 – Fachada del Palacio del rey don Pedro, en el Real Alcázar de Sevilla. [Alberto Bravo](#).

1.2.1.1 Nullam quis lacus

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Listing 1.1 – Some example large code

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3 %      , '
4 %      ^7MM      _ .09
5 %      MM
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7 % 8)   MM     MM 6M' 00 8)   MM   ' AMV 8)   MM     MM ' "
8 % , pm9MM   MM 8M     , pm9MM   AMV     , pm9MM   MM
9 % 8M   MM     MM YM.     , 8M   MM   AMV     , 8M   MM     MM
9 % `Moo9^Yo..JJML.YMbmd` `Moo9^Yo.AMMmmM `Moo9^Yo..JJML.

10 %
11 %
12 % Free and Open-Source template for academic works
13 % https://github.com/dpmj/alcazar
14
15
16
17 % Title page
18 \input{opening/titlepage.tex}
19
20 % License
21 \input{opening/license}
22
23 % About the document
24 % Collaborators, repositories, social networks, links, etc.
25 % Feel free to edit this doc:
26 \input{opening/about}
27
28 % Abstract
29 \input{opening/abstract}
30
31 % Publications
32 \input{opening/publications} % Optional: comment this line if you don't need it
33
34 % Acknowledgements
35 \input{opening/acknowledgements}
36

```

```

37 % Dedication
38 % To whom do you dedicate the thesis? Or maybe include a quote, poem, etc. Free space
39 → for yourself.
40 % Delete if you are too manly for these things
41 \input{opening/dedication}
42
43 % TABLES OF CONTENTS
44
45 \begingroup
46
47 % Greatly compress space used by TOC with less spacing, smaller font size and less
48 \renewcommand{\baselinestretch}{0.7}\small
49
50
51 % List of Contents
52 {
53
54     \newpage
55
56     \clearpage
57     \cleardoublepage
58     \phantomsection
59
60     \tableofcontents
61
62     \addcontentsline{toc}{chapter}{Table of contents}
63 }
64
65 % List of Figures
66 {
67     \listoffigures
68     \addcontentsline{toc}{chapter}{List of figures}
69 }
70
71 % List of Tables
72 {
73     \listoftables
74     \addcontentsline{toc}{chapter}{List of tables}
75 }
76
77 % List of Listings
78 % Seems that it does not work with multitoc
79 {
80     % \listoflistings
81     % \addcontentsline{toc}{chapter}{List of listings}
82
83     % \listof{lstlisting}{Code listings} % old code
84 }
85
86 \endgroup
87
88 % END OPENING

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1.2.1.3 Nulla elementum orci

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(a) Palacio de Villavicencio, Alcázar, Jerez de la Frontera. [Diego Delso](#).



(b) Mezquita, Alcázar, Jerez de la Frontera, España [Diego Delso](#).

Figure 1.2 – Alcázar de Jerez de la Frontera.

dolor. Nunc tristique eu lacus quis ullamcorper. Sed volutpat rutrum vehicula. Donec nunc nisl, suscipit in faucibus vitae, tristique eu risus. Nulla facilisis augue eget interdum rutrum. Aliquam sem nunc, fermentum sed urna ac, faucibus interdum nisi.

Proin a condimentum nibh. Praesent vulputate tellus vel metus rutrum, non luctus mi sollicitudin. Nam ac tellus ut eros sollicitudin luctus at ac mi. Vestibulum mollis nec nisi a laoreet. Proin neque tortor, placerat nec suscipit sit amet, ullamcorper in sem. Fusce faucibus ultrices cursus. Maecenas scelerisque mauris diam, at volutpat nisi porta vitae. Sed at ipsum et leo cursus varius eu eu lectus. Class aptent taciti sociosqu ad litora torquent per conubia nostra, per inceptos himenaeos. Ut felis ipsum, imperdiet rhoncus orci ac, consectetur luctus nisl. Cras aliquet elementum tellus ullamcorper malesuada. Integer purus est, pharetra eu ullamcorper quis, imperdiet non turpis.

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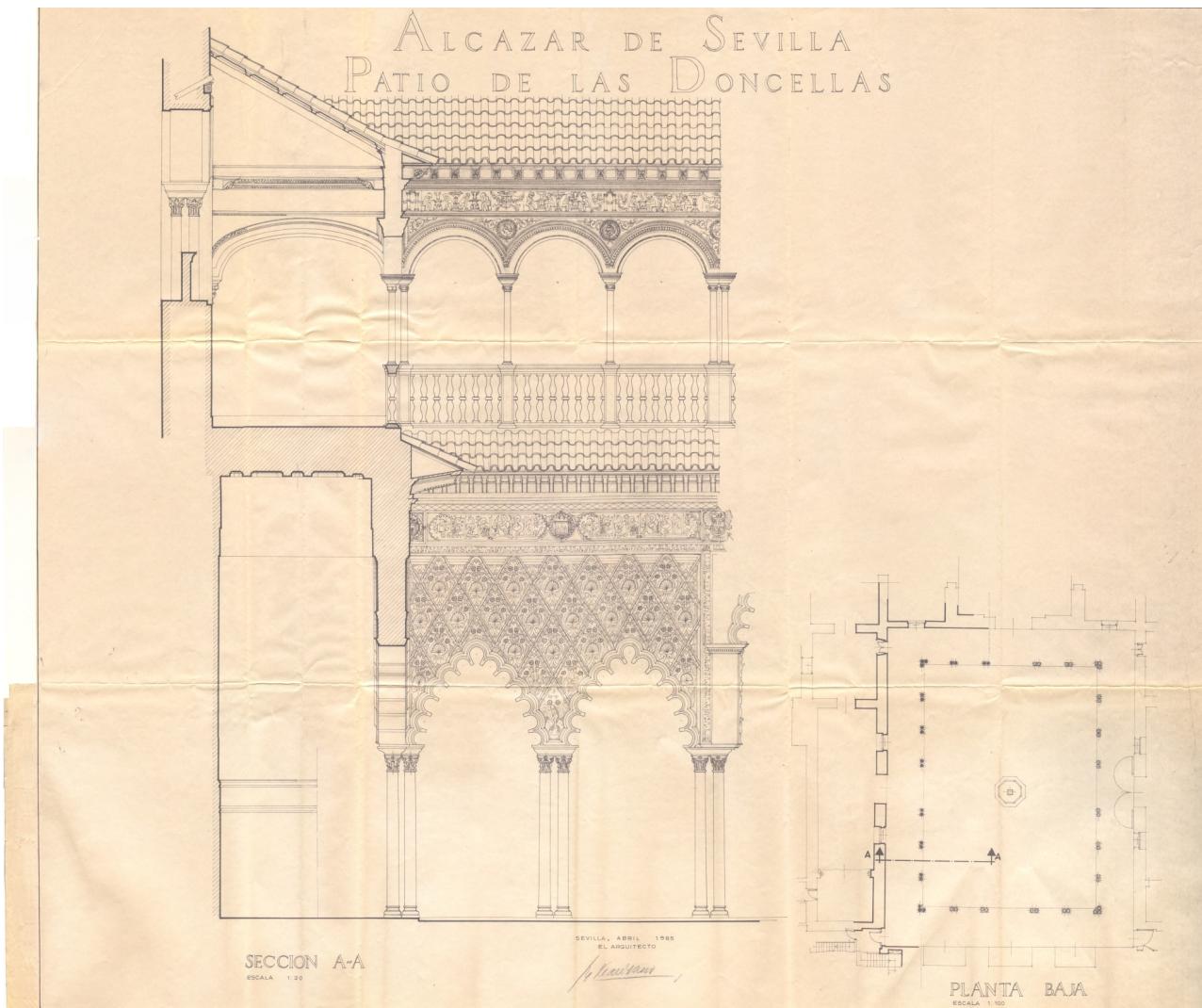


Figure 1.3 – Plano. Sección A-A y Planta Baja del Patio de las Doncellas. [Instituto Andaluz del Patrimonio Histórico.](#)

1

1
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Specifications

2.1 Aljibe

This is an example of how this template may be used. As we can see in [Figure 1.1](#), the [Jupyter Lab](#) is lorem ipsum dolor sit amet [1], consectetur adipiscing elit. Integer tempus quis elit id sagittis. Cras tincidunt nisi at tellus luctus, et congue dolor posuere. Aliquam suscipit felis sit amet lacus ultrices aliquet.

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2.1.1.1 Nullam quis lacus

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Voltage of internal LDO (VDD_SDIO)					
Pin	Default	VDD_SDIO = 3.3 V	VDD_SDIO = 1.8 V		
GPIO12/MTDI	Pull-down	0	1		
Booting mode					
Pin	Default	SPI boot	Download boot (programming)		
GPIO0	Pull-up	1	0		
GPIO2	Pull-down	Don't care	0		
Enabling/Disabling debugging log print over UOTXD (UART TXD) during boot					
Pin	Default	U0TXD Active	U0TXD Silent		
GPIO15/MTDO	Pull-up	1	0		
Timing of SDIO slave					
Pin	Default	FE Sampling FE Output	FE Sampling RE Output	RE Sampling FE Output	RE Sampling RE Output
GPIO15/MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1

Table 2.1 – Strapping pin configuration during boot on the ESP32. Extracted from ESP32's data sheet [1] (Table 5, page 21). FE: Falling Edge, RE: Rising Edge.

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APPENDIX A

Something you put a lot of effort into but which was vaguely related to the main content

A.1 Praesent vulputate tellus vel metus rutrum

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A.1.1 Faucibus interdum nisi

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A.1.2 Praesent vulputate tellus vel metus rutrum

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Figure A.1 – Alcázar de los reyes cristianos, Córdoba. [Ahura klik.](#)

ligula sodales, euismod est sed, semper libero [Fiducial marks](#).

In **blandit**, nulla et elementum pharetra, mi nunc sagittis tellus, sit amet scelerisque magna elit ac sapien. Curabitur ipsum dui, pretium a maximus id, varius gravida nisl. Sed vitae mattis elit, vitae hendrerit lorem [10].

A.1.2.1 **Lorem ipsum dolor sit amet, consectetur adipiscing elit**

Integer tempus quis elit id sagittis. Cras tincidunt nisi at tellus luctus, et congue dolor posuere. Aliquam suscipit felis sit amet lacus ultrices aliquet. Sed sagittis ultrices nisi, vel elementum elit dignissim non.

A.1.2.2 **Fusce faucibus ex at massa ultrices elementum**

Nullam ullamcorper lorem sit amet facilisis cursus. Suspendisse non erat non justo porta placerat. Morbi porttitor dictum molestie. Sed vitae iaculis libero. Suspendisse in gravida lacus, tempor ultrices nibh. Nam consequat scelerisque porttitor.

A.2 Nulla elementum orci in dolor dapibus

Nulla elementum orci in dolor dapibus, ac facilisis sem ultrices. Nullam eleifend id eros sed luctus. Maecenas arcu ipsum, scelerisque id lorem in, placerat posuere tellus. Etiam gravida velit sed arcu viverra dapibus. Mauris vitae augue dapibus, molestie justo eget, condimentum ipsum. Nulla tristique mi eget semper luctus. Etiam commodo vestibulum vulputate. Etiam quis sapien dolor. Nunc tristique eu lacus quis ullamcorper. Sed volutpat rutrum vehicula. Donec nunc nisl, suscipit in faucibus vitae, tristique eu risus. Nulla facilisis augue eget interdum rutrum. Aliquam sem nunc, fermentum sed urna ac, faucibus interdum nisi.

A.2.1 **Non luctus mi sollicitudin**

Nam ac tellus ut eros sollicitudin luctus at ac mi. Vestibulum mollis nec nisi a laoreet. Proin neque tortor, placerat nec suscipit sit amet, ullamcorper in sem. Fusce faucibus ultrices cursus. Maecenas scelerisque mauris diam, at volutpat nisi porta vitae. Sed at ipsum et leo cursus varius eu eu lectus. Class aptent taciti sociosqu ad litora torquent per conubia nostra, per inceptos himenaeos. Ut felis ipsum, imperdiet rhoncus orci ac, consectetur luctus nisl. Cras aliquet elementum tellus ullamcorper malesuada. Integer purus est, pharetra eu ullamcorper quis, imperdiet non turpis.

In vestibulum faucibus ligula eget blandit. Donec eget cursus risus, quis suscipit justo. Curabitur efficitur, dolor nec pulvinar pellentesque, lectus eros hendrerit nisi, in aliquet erat nunc non ipsum. Curabitur felis nunc, viverra nec quam ultrices, suscipit condimentum nibh. Nam faucibus felis hendrerit imperdiet maximus. Curabitur tincidunt porttitor lectus quis feugiat. Sed imperdiet bibendum mi.

A.2.1.1 Nullam quis lacus vel ante feugiat

Nullam quis lacus vel ante feugiat efficitur id ut quam. Pellentesque commodo elit nec urna gravida maximus. Suspendisse ut risus eu ipsum porta porta ac et orci. Donec dictum ligula sodales, euismod est sed, semper libero. In blandit, nulla et elementum pharetra, mi nunc sagittis tellus, sit amet scelerisque magna elit ac sapien. Curabitur ipsum dui, pretium a maximus id, varius gravida nisl. Sed vitae mattis elit, vitae hendrerit lorem.

Listing A.1 – Some example large code

```

1  """
2  Some interesting python code
3  Blah Blah Blah
4  """
5
6  import numpy as np
7  from matplotlib import pyplot as plt
8  from numpy.polynomial import Polynomial as Poly
9
10 plt.rcParams["font.family"] = "Libertinus Serif"
11 plt.rcParams['font.size'] = 14
12 plt.rcParams['mathtext.fontset'] = 'custom'
13 plt.rcParams['mathtext.rm'] = 'Libertinus Serif'
14 plt.rcParams['mathtext.it'] = 'Libertinus Serif:italic'
15 plt.rcParams['mathtext.bf'] = 'Libertinus Serif:bold'
16
17 R510 = 508.3 # Ohms
18 V5 = 5.018 # Volts
19
20 # Open files
21
22 nmos_vgs, nmos_vr = np.loadtxt('nmos_ids_vgs.csv', delimiter='\t', unpack=True,
23                                skiprows=1)
23 nmos_sim_vgs, nmos_sim_ids = np.loadtxt('CIC_P0_NMOS_ids_vgs_5.txt', delimiter='\t',
24                                unpack=True, skiprows=1)
25
25 # Do thingies
26
27 nmos_ids = nmos_vr / R510 # Current in resistor
28 p = Poly.fit(nmos_vgs, nmos_ids, 1) # Tendency line
29 print(f"f(x) = {p:unicode}")
30
31 # Plot stuff
32
33 fig0, ax0 = plt.subplots(figsize=[12, 6])
34 x = np.linspace(0, 6, 100)
35
36 plt.plot(nmos_vgs, nmos_ids, linestyle='none', marker=".", label='Experimental')
37 plt.plot(nmos_sim_vgs, nmos_sim_ids, linestyle='dashdot', label='Simulation')
38 plt.plot(x, p(x), linestyle='dashed', label='Tendency')
39
40 ax0.grid(True, which='major', color="#AAAAAA", linestyle='-', linewidth=0.6)
41 ax0.grid(True, which='minor', color="#AAAAAA", linestyle=':', linewidth=0.6)
42 ax0.minorticks_on()
43
44 ax0.legend()
45
46 plt.title(r'NMOS, curve $I_{DS} / V_{GS}$')
47 plt.xlabel(r'$V_{GS}$ (V)')
48 plt.ylabel(r'$I_{DS}$ (A)')
49
50 plt.xlim([0, 6])
51
52 # Dont forget to save

```

```
53  
54 plt.savefig("nmos_vgs_ids.pdf")
```

A

APPENDIX B

A long table of things

 Lorem ipsum dolor sit amet, consectetur adipiscing elit. Integer tempus quis elit id sagittis. Cras tincidunt nisi at tellus luctus, et congue dolor posuere. Aliquam suscipit felis sit amet lacus ultrices aliquet. Sed sagittis ultrices nisi, vel elementum elit dignissim non. Fusce faucibus ex at massa ultrices elementum. Nullam ullamcorper lorem sit amet facilisis cursus. Suspendisse non erat non justo porta placerat. Morbi porttitor dictum molestie. Sed vitae iaculis libero. Suspendisse in gravida lacus, tempor ultrices nibh. Nam consequat scelerisque porttitor¹.

 Nulla elementum orci in dolor dapibus, ac facilisis sem ultrices. Nullam eleifend id eros sed luctus. Maecenas arcu ipsum, scelerisque id lorem in, placerat posuere tellus.

 Etiam gravida velit sed arcu viverra dapibus. Mauris vitae augue dapibus, molestie justo eget, condimentum ipsum. Nulla tristique mi eget semper luctus [Table B.1](#).

¹And if you can believe it, It's a Friday once again!

Table B.1 – Example of a long landscape table.

Nº	EDT	Nombre de tarea	Trabajo	Duración	Predecesoras	Comienzo	Fin	Recursos
1	1	Dirección del proyecto	4 días	4 días		lun 03/07/23	jue 06/07/23	
2	1.1	Reunión inicial de planificación con el cliente	3 días	3 días		lun 03/07/23	mié 05/07/23	Ana Torres;Carla Aguilar;Diego Ortiz;Lucía Castro;Martina Martínez;Pablo Gómez;Rodrigo García
3	1.2	Reparto de tareas a los trabajadores	1 día	1 día	1.1	jue 06/07/23	jue 06/07/23	Ana Torres
4	2	Estudio de la viabilidad del despliegue	27 días	9,67 días		vie 07/07/23	jue 20/07/23	
5	2.1	Estudio de la orografía	5 días	1,67 días	1.2	vie 07/07/23	lun 10/07/23	Rodrigo García;Paloma Cuesta;Ramón García
6	2.2	Estudio del emplazamiento de las antenas del radioenlace y balance de potencias	4 días	1,33 días	2.1	mié 12/07/23	jue 13/07/23	Rodrigo García;Paloma Cuesta;Ramón García
7	2.3	Estudio del emplazamiento de las estaciones base y radio de cobertura	4 días	1,33 días	2.1	jue 13/07/23	vie 14/07/23	Rodrigo García;Paloma Cuesta;Ramón García
8	2.4	Estudio de la magnitud del tráfico	3 días	1 día	1.2	lun 10/07/23	mar 11/07/23	Rodrigo García;Paloma Cuesta;Ramón García
9	2.5	Revisión de la normativa	2 días	0,67 días	1.2	mar 11/07/23	mié 12/07/23	Rodrigo García;Paloma Cuesta;Ramón García
10	2.6	Establecimiento de los requisitos técnicos	5 días	1,67 días	2.1;2.2;2.3;2.4;2.5	lun 17/07/23	mar 18/07/23	Rodrigo García;Paloma Cuesta;Ramón García
11	2.7	Establecimiento de un presupuesto temprano	4 días	2 días	2.6	mar 18/07/23	jue 20/07/23	Ana Torres;Rodrigo García
12	3	Diseño del despliegue	41 días	14 días		jue 20/07/23	mié 09/08/23	
13	3.1	Diseño de la red	29 días	9,67 días		jue 20/07/23	jue 03/08/23	
14	3.1.1	Diseño de las estaciones base de telefonía	7 días	9,67 días		jue 20/07/23	jue 03/08/23	
15	3.1.1.1	Elección del emplazamiento físico	5 días	1,67 días	2	jue 20/07/23	lun 24/07/23	Rodrigo García;Paloma Cuesta;Ramón García
16	3.1.1.2	Diseño de la sectorización y el apuntado	2 días	0,67 días	3.1.1.1	mié 02/08/23	jue 03/08/23	Rodrigo García;Paloma Cuesta;Ramón García
17	3.1.2	Diseño de las estaciones base del radioenlace	7 días	2,33 días		lun 24/07/23	mié 26/07/23	
18	3.1.2.1	Elección del emplazamiento físico	5 días	1,67 días	2	lun 24/07/23	mar 25/07/23	Rodrigo García;Paloma Cuesta;Ramón García
19	3.1.2.2	Diseño del apuntado	2 días	0,67 días	3.1.2.1	mié 26/07/23	mié 26/07/23	Rodrigo García;Paloma Cuesta;Ramón García
20	3.1.3	Diseño de la topología de red	10 días	3,33 días	2	mié 26/07/23	lun 31/07/23	Rodrigo García;Paloma Cuesta;Ramón García
21	3.1.4	Diseño de la gestión y separación del tráfico	5 días	1,67 días	2	mar 01/08/23	mié 02/08/23	Rodrigo García;Paloma Cuesta;Ramón García
22	3.2	Elección de equipos y componentes	10 días	3,33 días		jue 03/08/23	mar 08/08/23	
23	3.2.1	Elección de los equipos de RF	5 días	1,67 días	3.1	jue 03/08/23	vie 04/08/23	Rodrigo García;Paloma Cuesta;Ramón García
24	3.2.2	Elección de los equipos de red	5 días	1,67 días	3.1	lun 07/08/23	mar 08/08/23	Rodrigo García;Paloma Cuesta;Ramón García
25	3.3	Elaboración del presupuesto base	2 días	1 día	3.1;3.2	mar 08/08/23	mié 09/08/23	Rodrigo García;Ana Torres
26	4	Despliegue físico	38 días	15,83 días		mié 09/08/23	jue 31/08/23	
27	4.1	Reunión de materiales	4 días	2 días	3	mié 09/08/23	vie 11/08/23	Diego Ortiz;Martina Martínez
28	4.2	Construcción	15 días	7,5 días		vie 11/08/23	mié 23/08/23	
29	4.2.1	Estaciones de telefonía	5 días	2,5 días	4.1	vie 11/08/23	mié 16/08/23	Diego Ortiz;Martina Martínez

Thank you for reading this Master's Thesis.