Quartus II Introduction using VHDL Design

Simone Zezza

A. A. 2010 / 2011

This tutorial presents an introduction to the Quartus II CAD system. It gives a general overview of a typical CAD flow for designing circuits that are implemented by using FPGA devices, and shows how this flow is realized in the Quartus II software. The design process is illustrated by giving step-by-step instructions for using the Quartus II software to implement a very simple circuit in an Altera FPGA device.

Computer Aided Design (CAD) software makes it easy to implement a desired logic circuit by using a programmable logic device, such as a field-programmable gate array (FPGA) chip. A typical FPGA CAD flow is illustrated in Figure 1. The CAD flow involves the following steps:

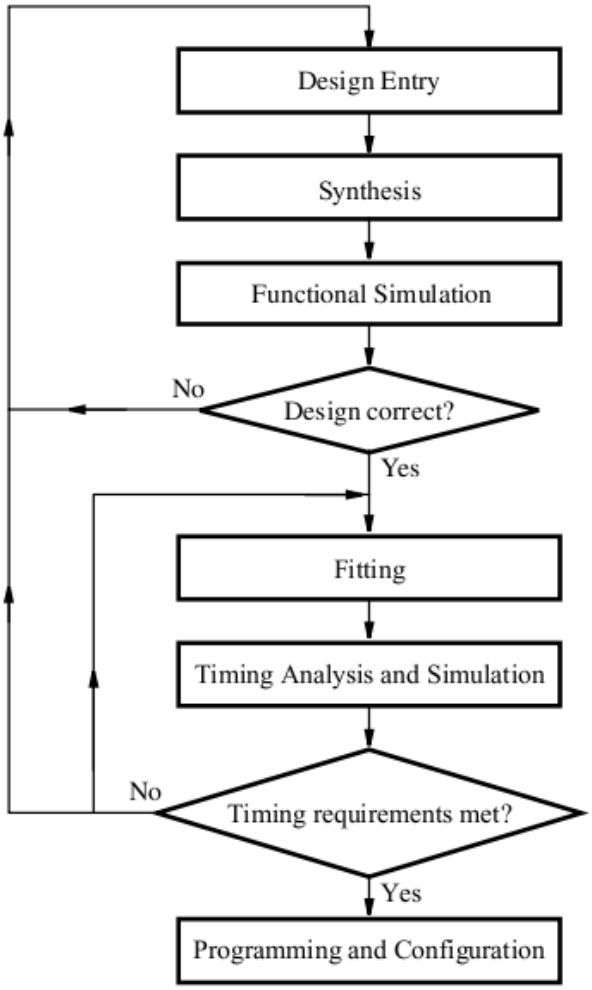

Figure 1: Typical design flow

- **Design Entry**: the desired circuit is specified either by means of a schematic diagram, or by using a hardware description language, such as Verilog or VHDL.
- **Synthesis**: the entered design is synthesized into a circuit that consists of the logic elements (LEs) provided in the FPGA chip.
- **Functional Simulation**: the synthesized circuit is tested to verify its functional correctness; this simulation does not take into account any timing issues.
- **Fitting**: the CAD Fitter tool determines the placement of the LEs defined in the netlist into the LEs in an actual FPGA chip; it also chooses routing wires in the chip to make the required connections between specific LEs.
- **Timing Analysis**: propagation delays along the various paths in the fitted circuit are analyzed to provide an indication of the expected performance of the circuit.
- **Timing Simulation**:the fitted circuit is tested to verify both its functional correctness and timing.
- **Programming and Configuration**: the designed circuit is implemented in a physical FPGA chip by pro- gramming the configuration switches that configure the LEs and establish the required wiring connections.

This tutorial introduces the basic features of the Quartus II software. It shows how the software can be used to design and implement a circuit specified by using the VHDL hardware description language. It makes use of the graphical user interface to invoke the Quartus II commands. Doing this tutorial, the reader will learn about:

- Creating a project
- Adding Design VHDL files to a project
- Compiling the Designed Circuit
- Timing simulation

0.1 Creating a project

To start working on a new design we first have to define a new design project. Quartus II software makes the the task of the designer easy by providing support in the form of a wizard. Create a new project as follows:

1. Open the develop environment **Quartus II 9.0sp2 Web Edition**.
2. Select File > New Project Wizard to reach the window in Figure 2, which asks for the name and directory of the project.

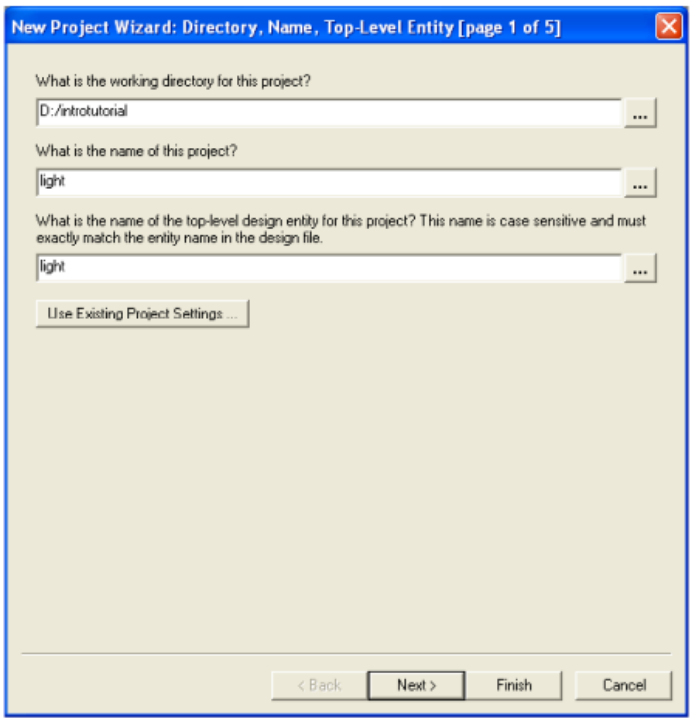

Figure 2: Creation of a new project

3. Set the working directory to be **mysynth**; of course, you can use some other directory name of your choice if you prefer. The project must have a name, which is usually **the same as the top-level design entity** that will be included in the project. **Press Next**.

4. The wizard reported in Figure 3 makes it easy to specify which existing files (if any) should be included in the project. Press the button ... and add the vhdl files to your design and **Press Next**.

5. In the Wizard reported in Figure 4, we have to specify the type of device in which the designed circuit will be implemented. Choose **Cyclone II** as the target device family. We can let Quartus II software select a specific device in the family, or we can choose the device explicitly. We will take the latter approach. From the list of available devices, choose the device called **EP2C35F672C6** which is the FPGA used on Altera DE2 board.

6. Press **Next** to skip the next wizard.

7. A summary of the chosen settings appears in the screen shown in Figure 5. **Press Finish**.

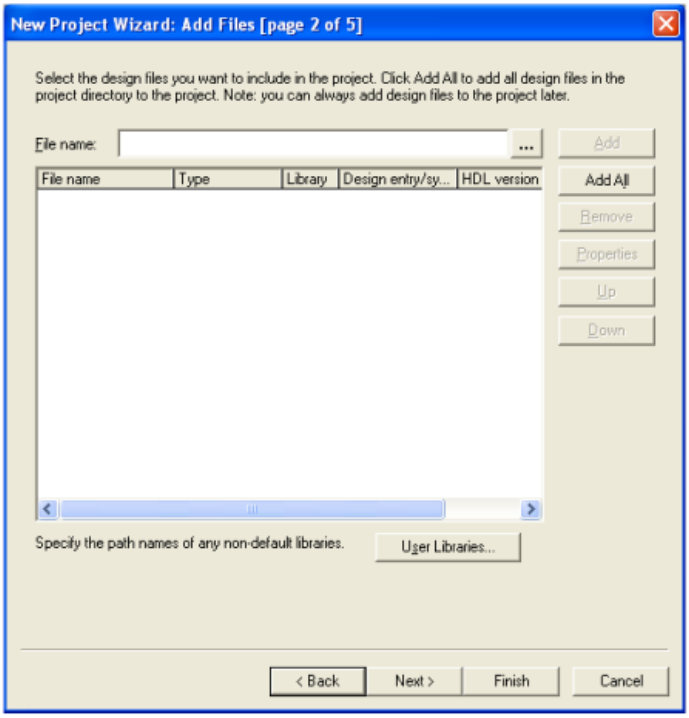

Figure 3: The wizard can include user specified design files.

0.2 Adding Design VHDL files to a project

As we indicated when discussing Figure 3, you can tell Quartus II software which design files it should use as part of the current project. To see the list of files already included in the light project, select **Assignments** > **Settings** and click on the item Files. An alternative way of making this selection is to choose **Project** > *Add/Remove* **Files** in Project.

0.3 Compiling the Designed Circuit

The VHDL code is processed by several Quartus II tools that analyze the code, synthesize the circuit, and generate an implementation of it for the target chip. These tools are controlled by the application program called the Compiler. Run the Compiler by selecting **Processing** > **Start Compilation**, or by clicking on the toolbar icon looks like a purple triangle. As the compilation moves through various stages, its progress is reported in a window on the left side of the Quartus II display. Successful (or unsuccessful) compilation is indicated in a pop-up box. Acknowledge it by clicking **OK**, which leads to the Quartus II

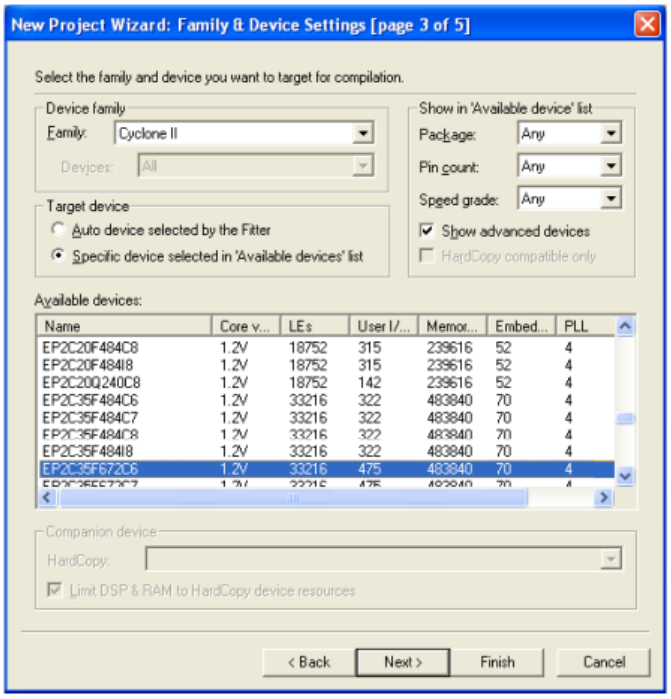

Figure 4: Choose the device family and a specific device.

display in Figure 6. In the message window, at the bottom of the figure, various messages are displayed. In case of errors, there will be appropriate messages given.

When the compilation is finished, a compilation report is produced. A window showing this report is opened automatically, as seen in Figure 6. The window can be resized, maximized, or closed in the normal way, and it

0.4 Timing simulation

ModelSim post synthesis simulation guide ....

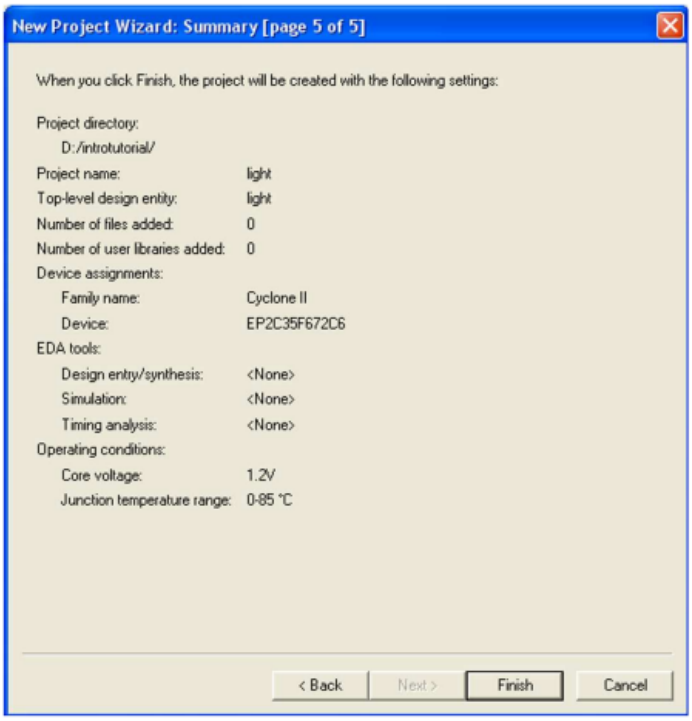

Figure 5: Summary of the project settings.

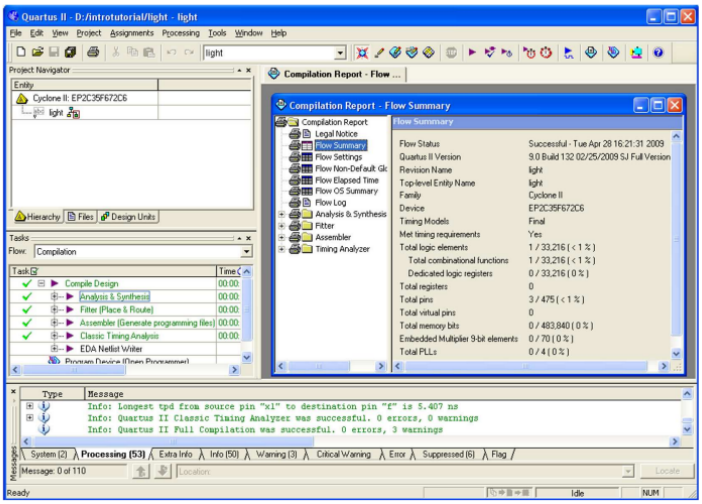

Figure 6: Display after a successful compilation.