1 Purpose

The purpose of this procedure is to facilitate the transfer of design information from the customer to imec. Preferably it`s provided for each design delivery, but it`s not a must if only the design name changes.

2 General delivery details

Some items may only be applicable for MPW e.g. sub dicing

Tape-out flavor incl. voltages: *TSMC 0.18 UM CMOS MIXED SIGNAL RF GENERAL PURPOSE II 1P6M+AL SALICIDE 1.8/3.3V PDK*		
Foundry/EP reference:	Target tape-out date: *4-Dec-20*	Tape-out type: *Mini@sic*
Project name: *PLL-USP2020*	File name: *PLL_USP2020.gds*	Topcell name: *PLL_USP202_3.gds*
File md5sum:	If based on past project, Foundry/EO ref.:	
PDK name: *TSMC 0.18 CMOS Logic or Mixed-Signal/RF, General Purpose*	Metal scheme: *1P6M_4X1U with UTM (20kA) topmetal*	
Multi chip tape-out: ☒ Yes ☐ No	Operation frequency: *1.28 GHz*	
Automotive project: ☐ Yes ☒ No	Extra sub dicing required? (only MPW) ☐ Yes ☒ No	
Dummy fill at imec required? (Only EP) ☒ Yes ☐No	Split condition (skew) wafers required? ☐ Yes ☐ No	
Number of dies (only MPW):	Number of wafers (only for dedicated mask sets):	
Technical contact email: *bruno.csanches@usp.br*	Administration contact: *wilhelmus.noije@usp.br*	
Post processing services via imec at 3rd party? ☐ Yes ☒ No → if No, specify backlapping thickness for bare die: Bumping or WLCSP ☐ Yes ☐ No Thinning and/or dicing ☐ Yes ☐ No Assembly/package design ☒ Yes ☐ No		

3 IP information

***Include all IP** that requires a replacement by imec or foundry and all OTP/MTP/ARM IP used in the design inside below table!*

Layout replacement required by imec e.g. SRAM, TSMC IO, std cell libraries? ☒ Yes ☐ No

If phantom/abstract/LEF views are used, imec needs to replace them. We need the full path name to identify the correct IP.

Full library path or memory name + delivery date:

1.	*TSMCHOME\digital\Back_End\lef\tpa018nv_270a\mt\6lm\lef\tpa018nv_6lm.lef*	Version: *270a*
2.	*TSMCHOME\digital\Back_End\lef\tpb018v_180a\wb\6lm\lef\tpb018v_6lm.lef*	Version: *180a*
3.		Version:
4.		Version:
5.		Version:
6.		Version:

*LVS-ERC **by imec** is a paid service and early notification is required.*

IP name (OTP/MTP/eFlash): Version:

IP merge required by foundry* (required for eFlash, eMemory)? ☐ Yes ☒ No

** A pre-merge **Calibre** LVS-ERC setup is required to perform pre- and post-merge checks at TSMC.*

4 Technology specific data

	6/7/12/16nm	22/28nm	40nm	55/65nm	90/130nm	0.18um	0.25/0.35um
Max MoM voltage		*Select*	*Select*	*Select*			
MiM value				*Select*	*Select*	*2fF/um2*	*Select*
AP thickness	*Select*	*Select*	*Select*	*Select*	*Select*		
Bump type (12inch only)	*Select*	*Select*	*Select*	*Select*	*Select*		
Substrate (bumping only)	*N/A*	*N/A*	*N/A*	*N/A*	*N/A*		
Number of bumps	*N/A*	*N/A*	*N/A*	*N/A*	*N/A*		
Polyimide*	*Select*	*Select*	*Select*	*Select*	*Select*	*Select*	*Select*
SRAM cell version	*N/A*	*N/A*	*N/A*	*N/A*	*N/A*		
SRAM total size (KB)	*N/A*	*N/A*	*N/A*	*N/A*	*N/A*	*N/A*	
ULL SRAM		*Select*					
Top metal thickness					*Select*	*20KA UTM*	*Select*
Complies to TSMCIDDQ	*Select*	*Select*	*Select*				

** Polyimide is a must for large chips and in case of lead free or Cu bumping.*

5 Mask, reticle field and wafer information

This section is not applicable for MPW.
Any special mask and reticle field requirements should be communicated to us before the first dry run tape-out!

Specific MLM layer on mask combination? ☐ Yes ☐ No
Specific requirements for the reticle field layout or scribe size? ☐ Yes ☐ No
Lot expediting? ☐ Yes ☐ No
Hold wafers required? ☐ Yes, *<insert requirements>* ☐ No
Further wafer processing via imec e.g. thinning, dicing? ☐ Yes ☐ No

6 Shipment information

By default we *follow the shipment information as specified on the purchase order. Any remarks or requirements can be added in this section and be communicated through email.*

7 Comments or special requests

This die has Analog sensitive circuits, therefore layers DMEXCL were added to avoid metal dummy fill in the circuit areas.

The die will be wire bonded to a QFN40(5x5) package.

8 Design upload

1. Add a visible **logo** or pin1 mark in top metal/AP. Add **version number** or date in design name.	2. Use our GPG key to **encrypt** the design. *gpg --import eptsmc_2018.asc* *gpg -r eptsmc@imec.be -e <file you want to encrypt>*
3. **Upload** it to eptsmc FTP: ftp.imec.be *Username = eptsmc Password = DvM623* *Upload location = Design_Drop_Folder* *FTP server should be in passive and binary mode!* *Commands: `pass ` & `bin`*	4. Update file name to *Design_delivery_<date>_<Europractice run>* or *Design_delivery_<date>_<TM-number>* and send to eptsmc@imec.be as **pdf**.