Computers Fundamentals

1st Year of Bachelor in Computer Science Engineering

Introduction to the laboratory practices

Academic year 2020 / 2021

- Available material to carry out the practices.
  - Integrated circuits.
  - Technical manuals of integrated circuits.
  - Simulation software.
  - Practice board.
  - Development board.
- Procedure to carry out the practices.
- Practices assessment.

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Outline

- To carry out the laboratory practices the student may use of the material that follows:
  - Integrated circuits.
  - Technical manuals of integrated circuits .
  - Simulation software:
    - Digital Works.
    - Xilinx ISE WebPack.
  - Practice board.
  - Development card.

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Outline

- Available material.
  - Integrated circuits.
  - Technical manuals.
  - Simulation software.
  - Practice board.
  - Development card.
- Procedure.
- Assessment.

- **Integrated circuit or chip:** It contains a series of both active and passive electronic devices as well as some interconnections between them in such a way that they perform the same functions as a complex electronic circuit.

  The integrated circuits can be divided into **analogic**, **digital** or **mixed** ones.

- Taxonomy of the digital integrated circuits depending on the number of contained internal devices:
  - **SSI** (Small Scale of Integration): 1 – 10 gates.
  - **MSI** (Medium Scale of Integration): 10 – 100 gates.
  - **LSI** (Large Scale of Integration): 100 – 1,000 gates.
  - **VLSI** (Very Large Scale of Integration): 1,000 – 10,000 gates.
  - **ULSI** (Ultra Large Scala of Integration): 10,000 – 100,000 gates.
  - **GLSI** (Giga Large Scale of Integration): More than 100,000 gates.

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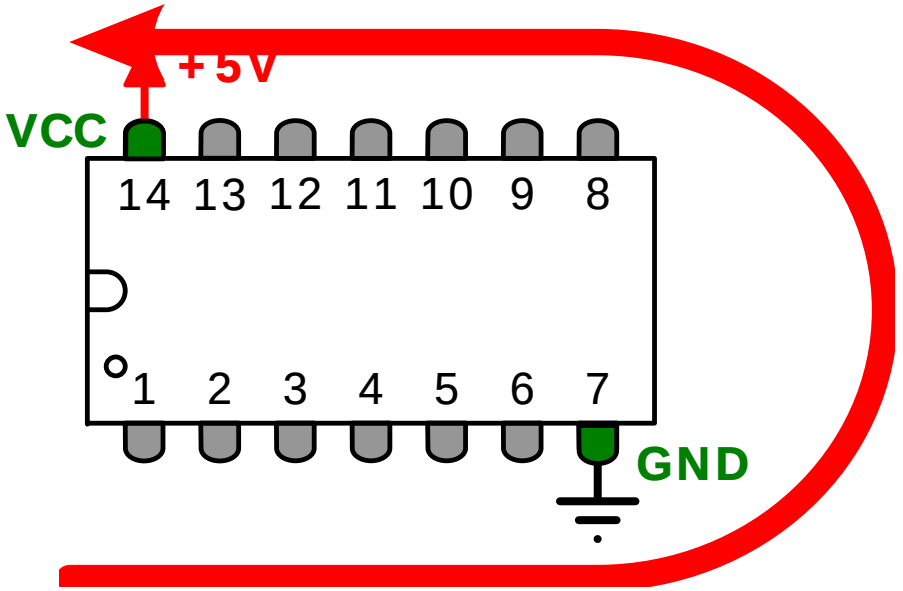
Outline

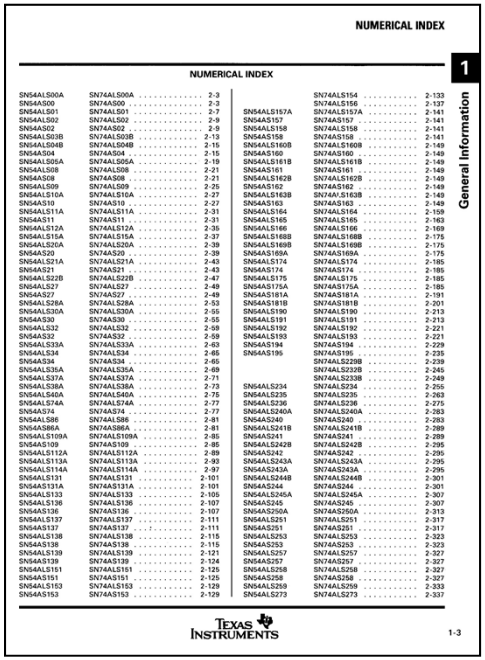
- **Available material.**
  - **Integrated circuits.**
  - **Technical manuals.**
  - **Simulation software.**
  - **Practice board.**
  - **Development card.**
- **Procedure.**
- **Assessment.**

- Taxonomy of the digital integrated circuits attending to its building tecnhology:
  - **Bipolar families** (built from bipolar transistors):
    - TTL family.
    - ECL family.
  - **MOS families** (built from MOS transistors):
    - NMOS family.
    - CMOS family.

- **Terminology:**

SN 74 LS 00 J


+5V
VCC
14 13 12 11 10 9 8
1 2 3 4 5 6 7
GND



NUMERICAL INDEX

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General Information

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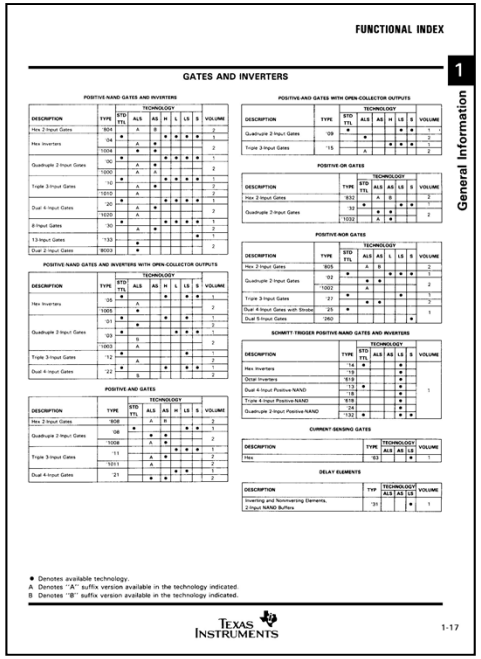
TEXAS INSTRUMENTS



FUNCTIONAL INDEX

1

General Information

GATES AND INVERTERS

POSITIVE NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	H	L	LS	S	VOLUME
Hex 2-Input Gates	804		A	B					2
Hex Inverters	04	•			•	•	•	•	1
			A	•					2
	1004		•	•					2
Quadruple 2-Input Gates	00	•			•	•	•	•	1
			A	•					2
	1000		•	A					2
Triple 3-Input Gates	10	•			•	•	•	•	1
			A	•					2
	1010		•	A					2
Dual 4-Input Gates	20	•			•	•	•	•	1
			A	•					2
	1020		•	A					2
8-Input Gates	30	•			•	•	•	•	1
			A	•					2
13-Input Gates	133		•				•		1
Dual 2-Input Gates	9003		•						2

POSITIVE NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	H	L	LS	S	VOLUME
Hex Inverters	06	•			•		•	•	1
	1005		•						2
	01	•				•			1
Quadruple 2-Input Gates		•							3
	03	•				•	•	•	1
			B						2
	1003		A						2
Triple 3-Input Gates	12	•				•			1
			A						2
Dual 4-Input Gates	22	•			•		•	•	1
			B						2

POSITIVE AND GATES

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	H	L	LS	S	VOLUME
Hex 2-Input Gates	808		A	B					2
Quadruple 2-Input Gates	08	•					•	•	1
			A	•					2
	1008		•	•					2
Triple 3-Input Gates	11			A	•				1
	1011			A					2
Dual 4-Input Gates	21			•	•				1
				•	•				2

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	H	L	LS	S	VOLUME
Quadruple 2-Input Gates	'09	•					•	•	1
			•						2
Triple 3-Input Gates	'15		A				•	•	1
									2

POSITIVE-OR GATES

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	LS	S	VOLUME
Hex 2-Input Gates	832		A	B			1
		•			•	•	2
Quadruple 2-Input Gates	32	•					1
			•	•			2
	1032		•	•			2

POSITIVE-NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	L	LS	S	VOLUME
Hex 2-Input Gates	805		A	B				1
		•			•	•	•	2
Quadruple 2-Input Gates	02		•	•				1
	1002			A				2
Triple 3-Input Gates	27	•				•		1
			•	•				2
Dual 4-Input Gates with Strobe	25	•						1
Dual 5-Input Gates	260						•	

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	LS	S	VOLUME
Hex Inverters	'14	•					1
	'19				•		
Octal Inverters	'619				•		
Dual 4-Input Positive-NAND	'13	•			•		1
Triple 4-Input Positive-NAND	'18				•		
Quadruple 2-Input Positive-NAND	'619				•		
	'24				•		
	'132	•			•		

CURRENT-SENSING GATES

DESCRIPTION	TYPE	TECHNOLOGY ALS	AS	LS	VOLUME
Hex	'83			•	1

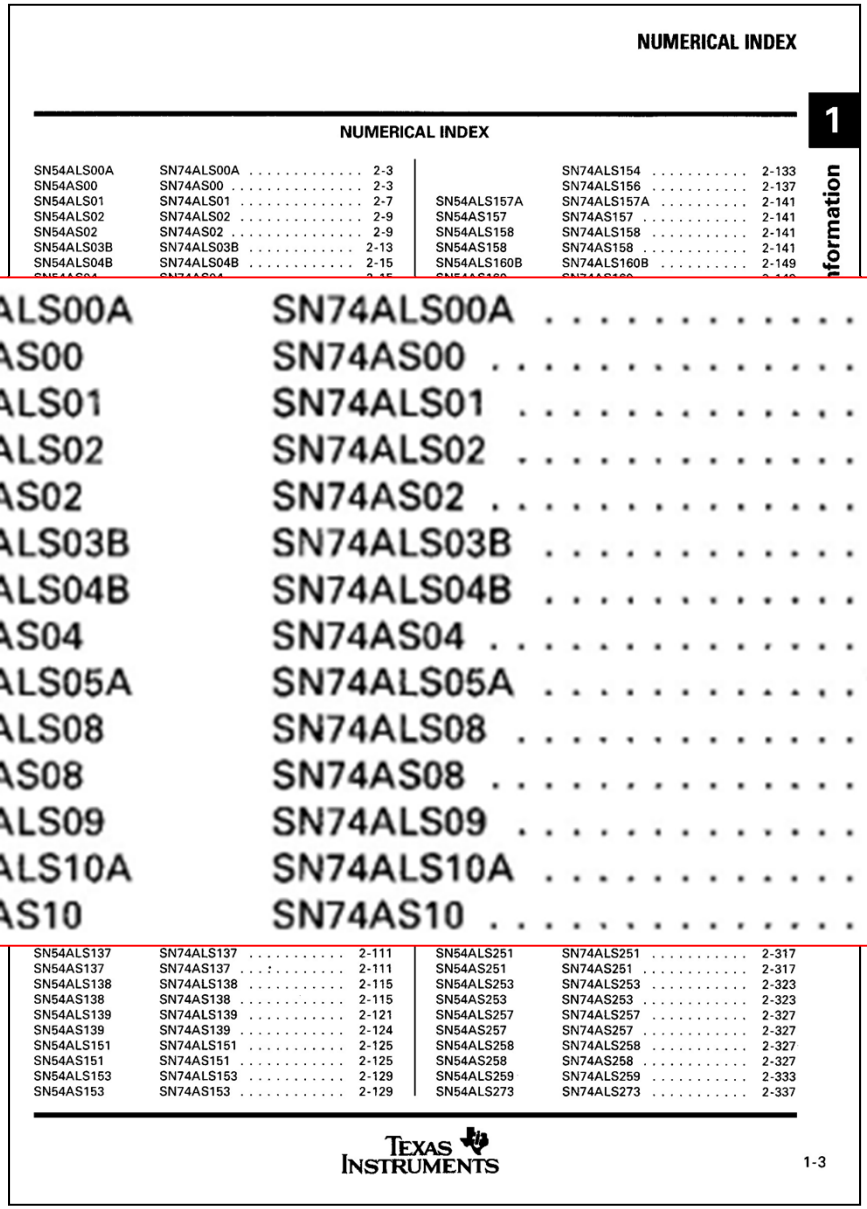
DELAY ELEMENTS

DESCRIPTION	TYP	TECHNOLOGY ALS	AS	LS	VOLUME
Inverting and Noninverting Elements, 2-Input NAND Buffers	'81			•	1

• Denotes available technology.
A Denotes "A" suffix version available in the technology indicated.
B Denotes "B" suffix version available in the technology indicated.

TEXAS INSTRUMENTS

NUMERICAL INDEX



NUMERICAL INDEX

1

Information

NUMERICAL INDEX

TEXAS INSTRUMENTS

1-3

GATES AND INVERTERS

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	H	L	LS	S	VOLUME
Hex 2-Input Gates	'804		A	B					2
Hex Inverters	'04	●			●	●	●	●	1
	'1004		A	●					2
			●	●					
Quadruple 2-Input Gates	'00	●			●	●	●	●	1
	'1000		A	●					2
			A	A					
Triple 3-Input Gates	'10	●			●	●	●	●	1
	'1010		A	●					2
			A						2
Dual 4-Input Gates	'20	●			●	●	●	●	1
	'1020		A	●					2
			A						
8-Input Gates	'30	●			●	●	●	●	1
			A	●					2
13-Input Gates	'133							●	1
Dual 2-Input Gates	'8003		●						2

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	H	L	LS	S	VOLUME
Hex Inverters	'05	●			●		●	●	1
	'1005		A						2
			●						
Quadruple 2-Input Gates	'01	●			●		●		1
			●						2
	'03	●				●	●	●	1
			B						2
	'1003		A						
Triple 3-Input Gates	'12	●					●		1
			A						2
Dual 4-Input Gates	'22	●			●		●	●	1
			B						2

POSITIVE-AND GATES

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	H	LS	S	VOLUME
Hex 2-Input Gates	'808		A	B				2
Quadruple 2-Input Gates	'08	●				●	●	1
			●	●				2
	'1008		A	●				
Triple 3-Input Gates	'11				●	●	●	1
			A	●				2
	'1011		A					2
Dual 4-Input Gates	'21				●	●		1
			●	●				2

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	H	LS	S	VOLUME
Quadruple 2-Input Gates	'09	●				●	●	1
			●					2
Triple 3-Input Gates	'15				●	●	●	1
			A					2

POSITIVE-OR GATES

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	LS	S	VOLUME
Hex 2-Input Gates	'832		A	B			2
Quadruple 2-Input Gates	'32	●			●	●	1
	'1032		●	●			2
			A	●			

POSITIVE-NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	L	LS	S	VOLUME
Hex 2-Input Gates	'805		A	B				2
Quadruple 2-Input Gates	'02	●			●	●	●	1
			●	●				2
	'1002		A					
Triple 3-Input Gates	'27	●				●		1
			●	●				2
Dual 4-Input Gates with Strobe	'25	●						1
Dual 5-Input Gates	'260						●	

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	LS	S	VOLUME
Hex Inverters	'14	●			●		1
	'19				●		
Octal Inverters	'619				●		
Dual 4-Input Positive-NAND	'13	●			●		
	'18				●		
Triple 4-Input Positive-NAND	'618				●		
Quadruple 2-Input Positive-NAND	'24				●		
	'132	●			●	●	

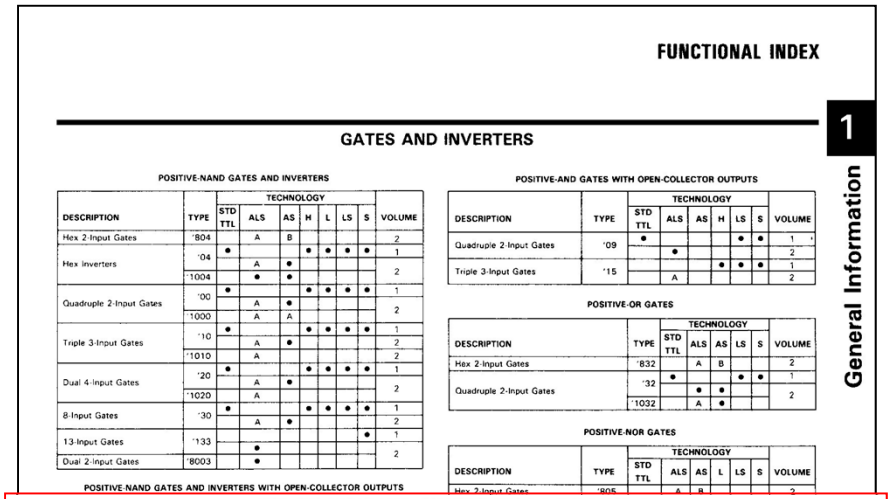
CURRENT-SENSING GATES

DESCRIPTION	TYPE	TECHNOLOGY ALS	AS	LS	VOLUME
Hex	'63			●	1

DELAY ELEMENTS

DESCRIPTION	TYP	TECHNOLOGY ALS	AS	LS	VOLUME
Inverting and Noninverting Elements, 2-Input NAND Buffers	'31			●	1

● Denotes available technology.
A Denotes "A" suffix version available in the technology indicated.
B Denotes "B" suffix version available in the technology indicated.



FUNCTIONAL INDEX

1 General Information

GATES AND INVERTERS

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Hex 2-Input Gates	'804		A	B					2
Hex Inverters	'04	●			●	●	●	●	1
			A	●					2
	'1004		●	●					
Quadruple 2-Input Gates	'00	●			●	●	●	●	1
			A	●					2
	'1000		A	A					
Triple 3-Input Gates	'10	●			●	●	●	●	1
			A	●					2
	'1010		A						
Dual 4-Input Gates	'20	●			●	●	●	●	1
			A	●					2
	'1020		A						
8-Input Gates	'30	●			●	●	●	●	1
			A	●					2
13-Input Gates	'133							●	1
Dual 2-Input Gates	'8003		●						2

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
Quadruple 2-Input Gates	'09	●				●	●	1
			●					2
Triple 3-Input Gates	'15				●	●	●	1
			A					2

POSITIVE-OR GATES

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Hex 2-Input Gates	'832		A	B			2
Quadruple 2-Input Gates	'32	●			●	●	1
			●	●			2
	'1032		A	●			

POSITIVE-NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	L	LS	S	
Hex 2-Input Gates	'805		A	B				2

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Hex 2-Input Gates	'804		A	B					2
Hex Inverters	'04	●			●	●	●	●	1
			A	●					2
	'1004		●	●					
Quadruple 2-Input Gates	'00	●			●	●	●	●	1
			A	●					2
	'1000		A	A					
Triple 3-Input Gates	'10	●			●	●	●	●	1
			A	●					2
	'1010		A						
Dual 4-Input Gates	'20	●			●	●	●	●	1
			A	●					2
	'1020		A						
8-Input Gates	'30	●			●	●	●	●	1
			A	●					2
13-Input Gates	'133							●	1
			●						2
Dual 2-Input Gates	'8003		●						

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SN54ALS00A, SN54AS00, SN74ALS00A, SN74AS00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

D2661, APRIL 1982 - REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

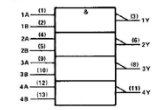
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS00A and SN54AS00 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS00A and SN74AS00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

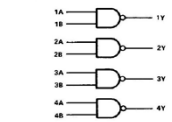
INPUTS A	INPUTS B	OUTPUT Y
H	H	L
L	X	H
X	L	H

logic symbol†

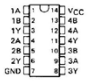


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

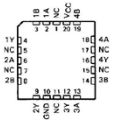
logic diagram (positive logic)



SN54ALS00A, SN54AS00 . . . J PACKAGE
SN74ALS00A, SN74AS00 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS00A, SN54AS00 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

TEXAS INSTRUMENTS

SN54ALS00A, SN74ALS00A
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

2 ALS and AS Circuits

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . 7 V
Input voltage . . . 7 V
Operating free-air temperature range: SN54ALS00A . . . −55°C to 125°C
SN74ALS00A . . . 0°C to 70°C
Storage temperature range . . . −65°C to 150°C

recommended operating conditions

		SN54ALS00A MIN	NOM	MAX	SN74ALS00A MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS00A MIN	TYP†	MAX	SN74ALS00A MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.5	0.85		0.5	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.5	3		1.5	3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C ALS00A TYP	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX SN54ALS00A MIN	SN54ALS00A MAX	SN74ALS00A MIN	SN74ALS00A MAX	UNIT
t_{PLH}	A or B	Y	7	3	16	3	11	ns
t_{PHL}	A or B	Y	5	2	13	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS

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SN54ALS00A, SN54AS00, SN74ALS00A, SN74AS00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

D2661, APRIL 1982 – REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

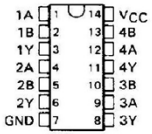
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS00A and SN54AS00 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS00A and SN74AS00 are characterized for operation from 0°C to 70°C.

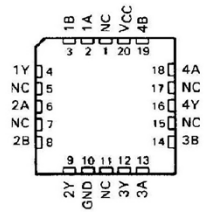
FUNCTION TABLE (each gate)

INPUTS A	INPUTS B	OUTPUT Y
H	H	L
L	X	H
X	L	H

SN54ALS00A, SN54AS00 . . . J PACKAGE
SN74ALS00A, SN74AS00 . . . D OR N PACKAGE
(TOP VIEW)

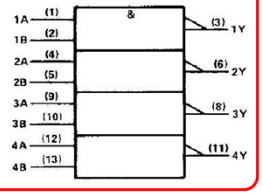


SN54ALS00A, SN54AS00 . . . FK PACKAGE
(TOP VIEW)



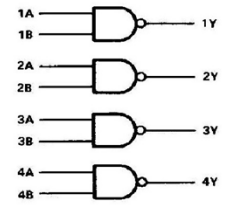
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS INSTRUMENTS

SN54ALS00A, SN74ALS00A
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS00A . . . . . −55°C to 125°C
SN74ALS00A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS00A			SN74ALS00A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS00A			SN74ALS00A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.5	0.85		0.5	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.5	3		1.5	3	mA

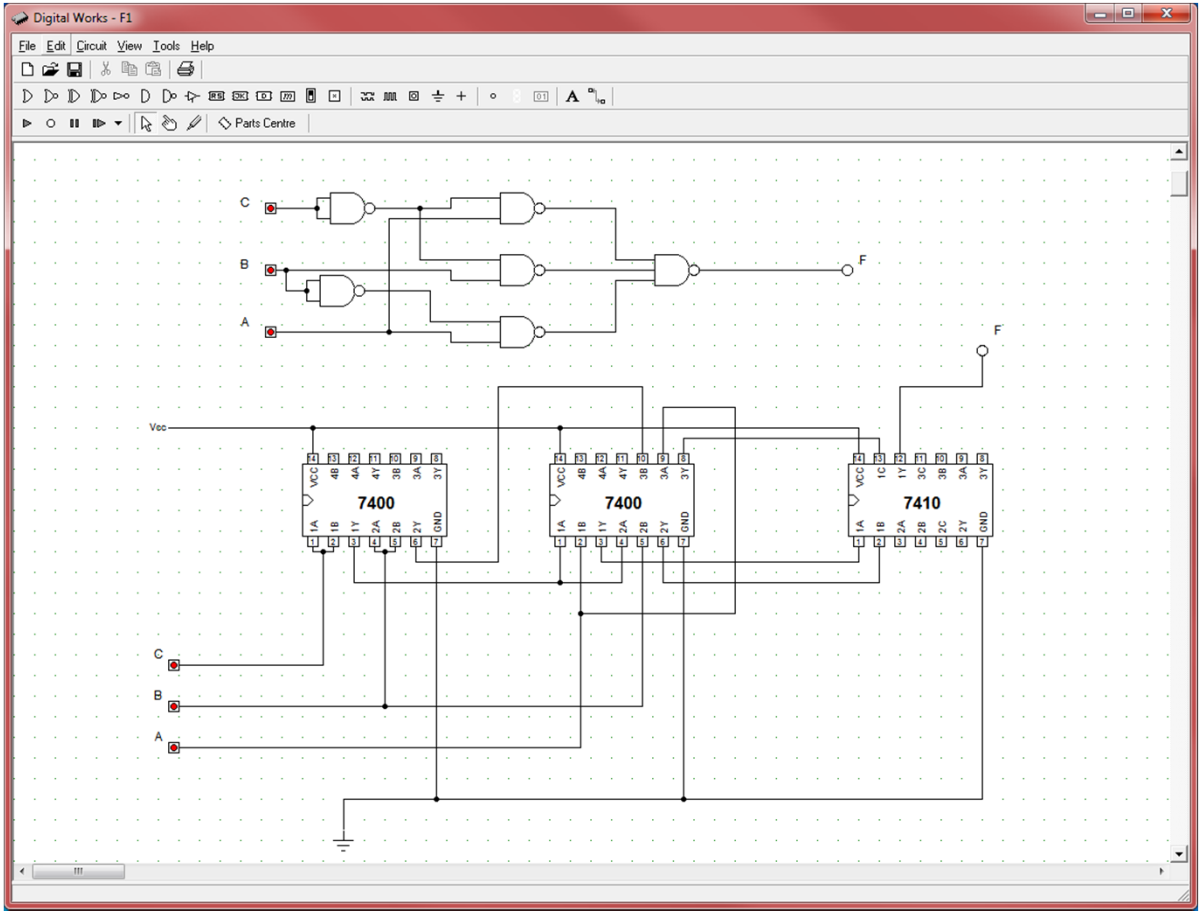
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

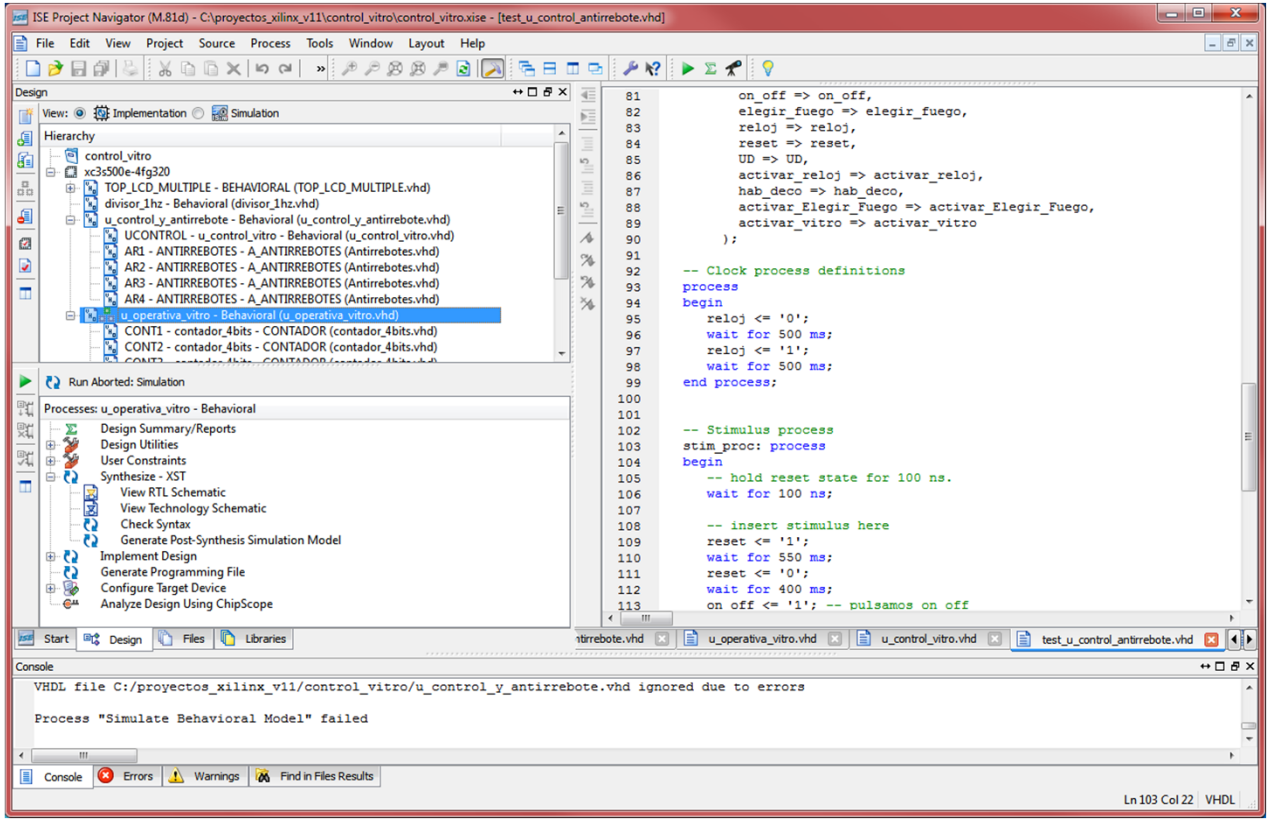
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX			UNIT
			'ALS00A	SN54ALS00A		SN74ALS00A	
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	7	3	16	3	11	ns
t_{PHL}	A or B	Y	5	2	13	2	8	

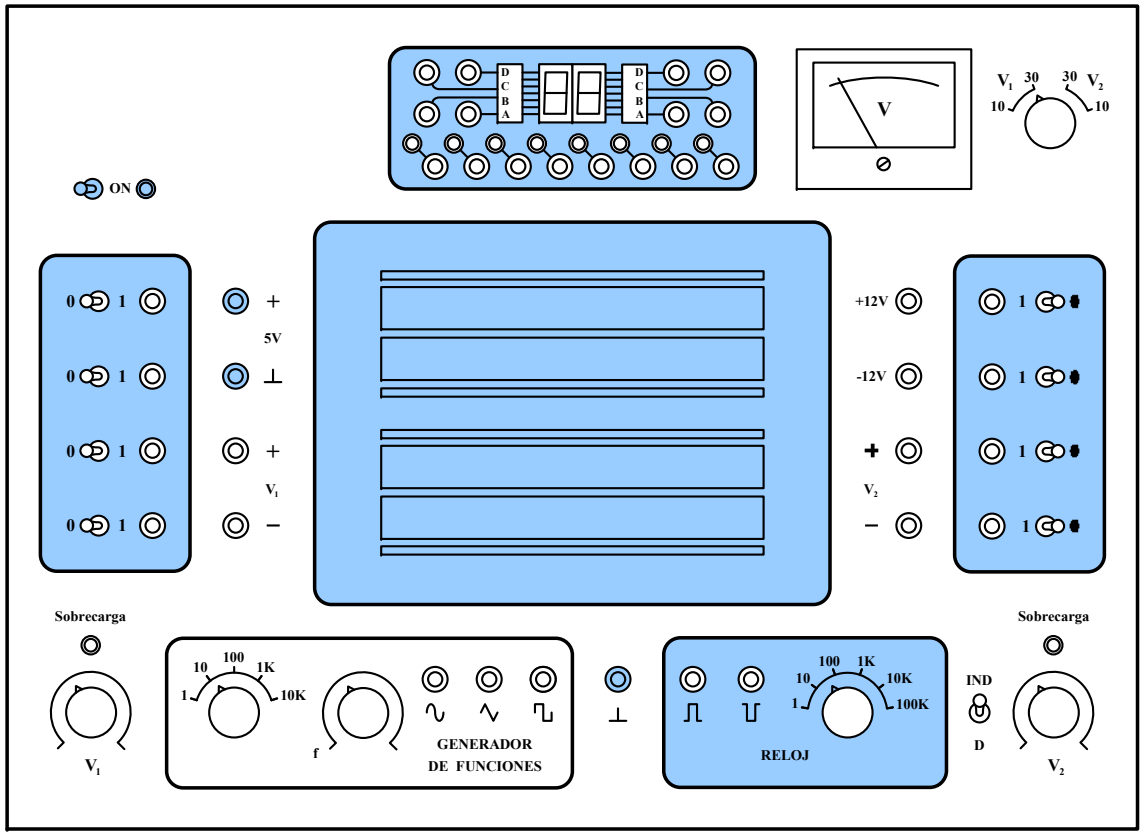
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- Digital Works.



- Xilinx WebPack.




D C B A
D C B A
V
V1 30 30 V2
10 10
ON
0 1
0 1
0 1
0 1
+
5V
⊥
+
V1
−
+12V
-12V
+
V2
−
1
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1
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Sobrecarga
10 100 1K
1 10K
f
GENERADOR
DE FUNCIONES
⊥
100 1K
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V1
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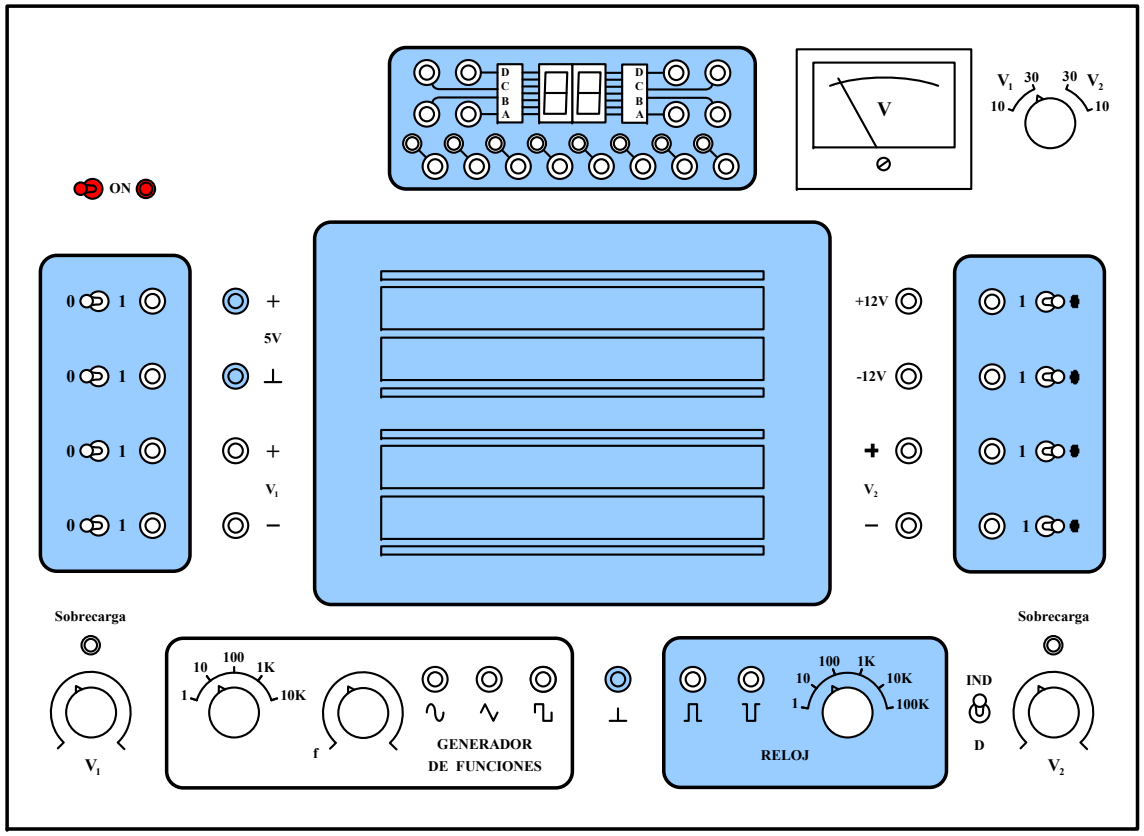
D C B A
D C B A
V
V1 30 30 V2
10 10
ON
0 1
0 1
0 1
0 1
+
5V
⊥
+
V1
−
+12V
-12V
+
V2
−
1
1
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Sobrecarga
10 100 1K
1 10K
f
GENERADOR
DE FUNCIONES
⊥
100 1K
10 10K
1 100K
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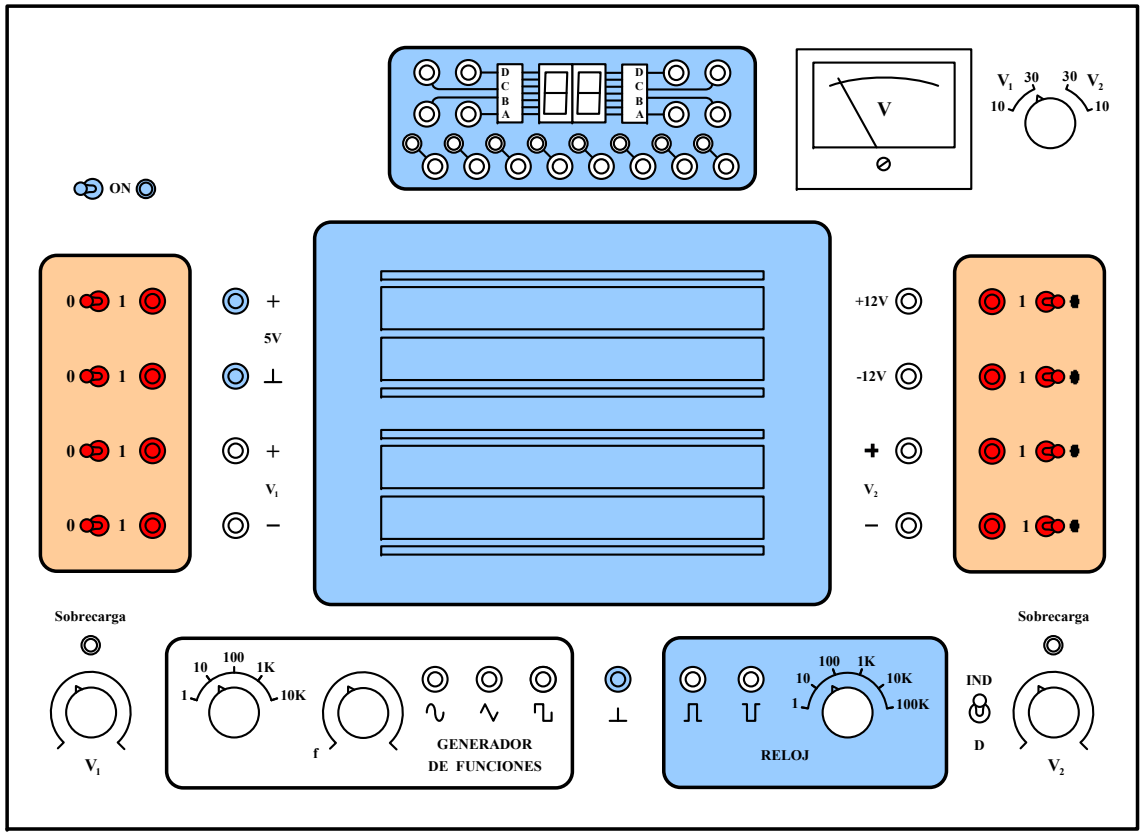
Sobrecarga
V1
V2


D C B A
D C B A
V
V1 30 30 V2
10 10
ON
0 1
0 1
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GENERADOR
DE FUNCIONES
⊥
100 1K
10 10K
1 100K
RELOJ
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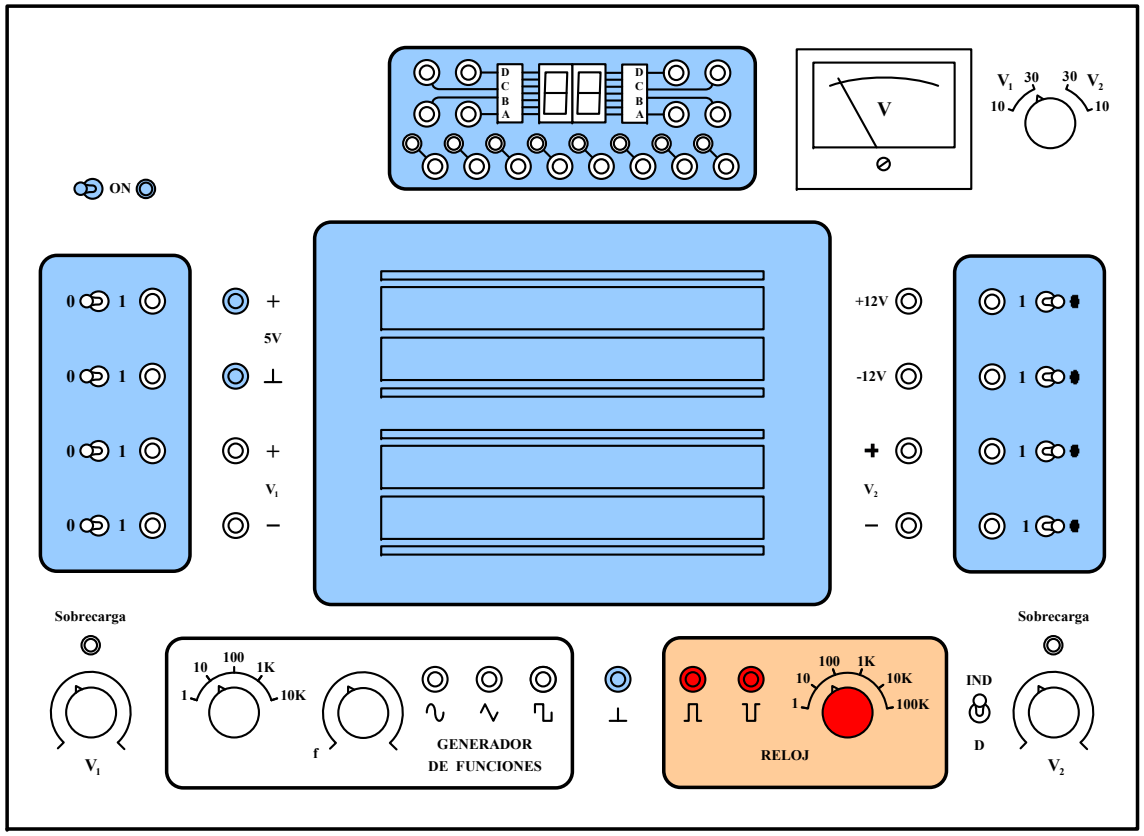
Sobrecarga
V1
V2


D C B A
D C B A
V
V1 30 30 V2
10 10
ON
0 1
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+
5V
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V1
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V2
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Sobrecarga
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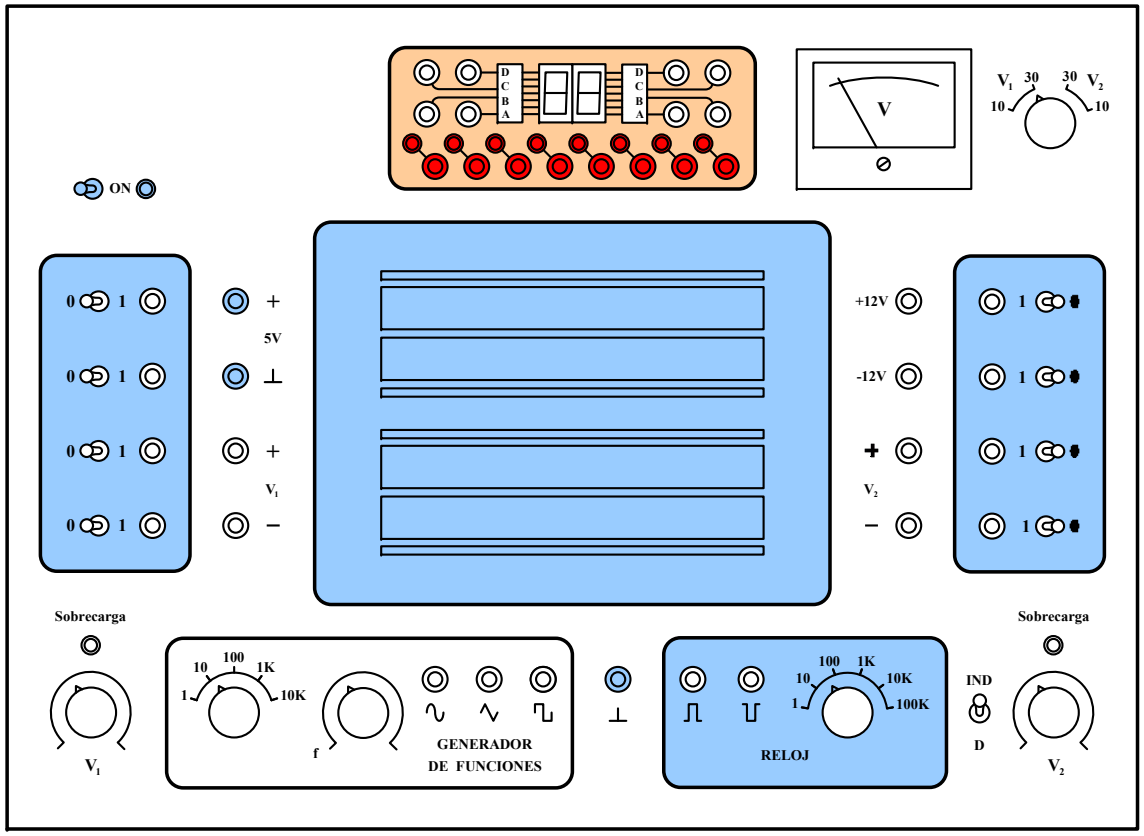
GENERADOR
DE FUNCIONES
⊥
100 1K
10 10K
1 100K
RELOJ
IND
D
Sobrecarga
V1
V2


D C B A
D C B A
V
V1 30 30 V2
10 10
ON
0 1
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0 1
0 1
+
5V
⊥
+
V1
−
+12V
-12V
+
V2
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Sobrecarga
10 100 1K
1 10K
f
GENERADOR
DE FUNCIONES
⊥
100 1K
10 10K
1 100K
RELOJ
IND
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Sobrecarga
V1
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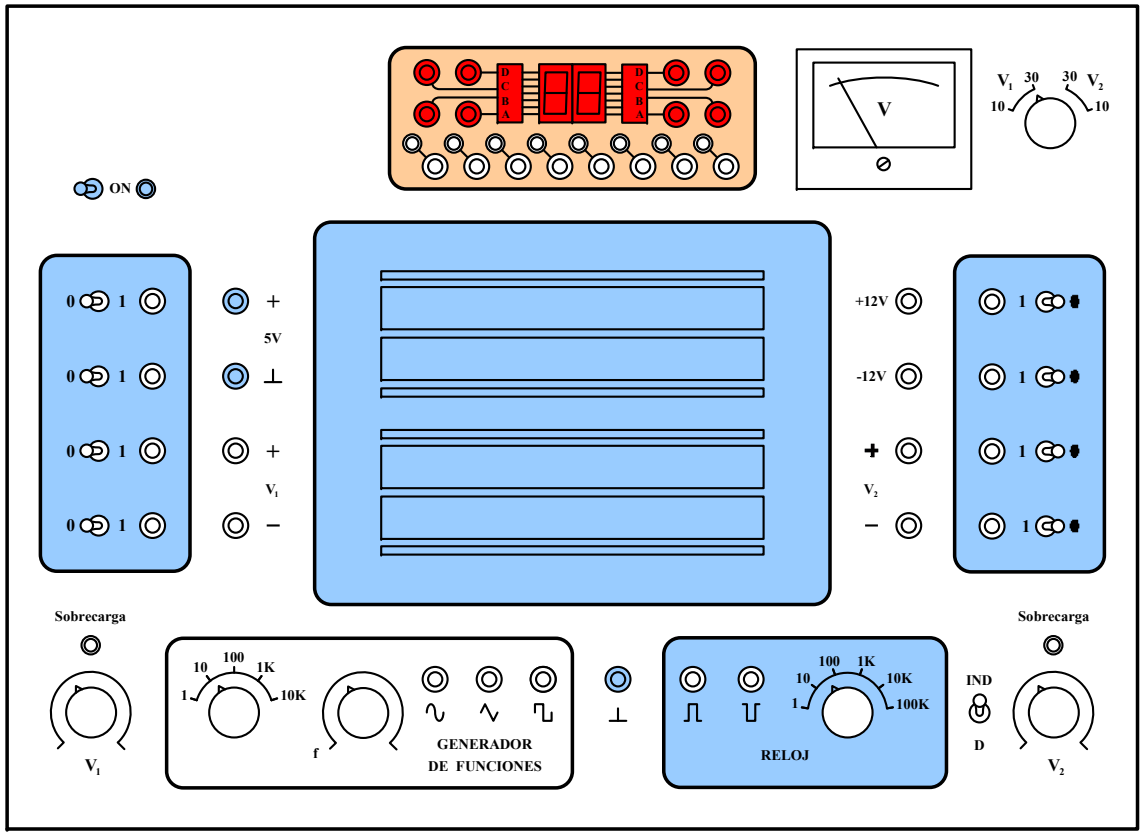
ON
D C B A
D C B A
V
V1 30 30 V2
10 10
0 1
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+
5V
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+
V1
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+12V
-12V
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V2
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Sobrecarga
10 100 1K
1 10K
f
GENERADOR
DE FUNCIONES
⊥
100 1K
10 10K
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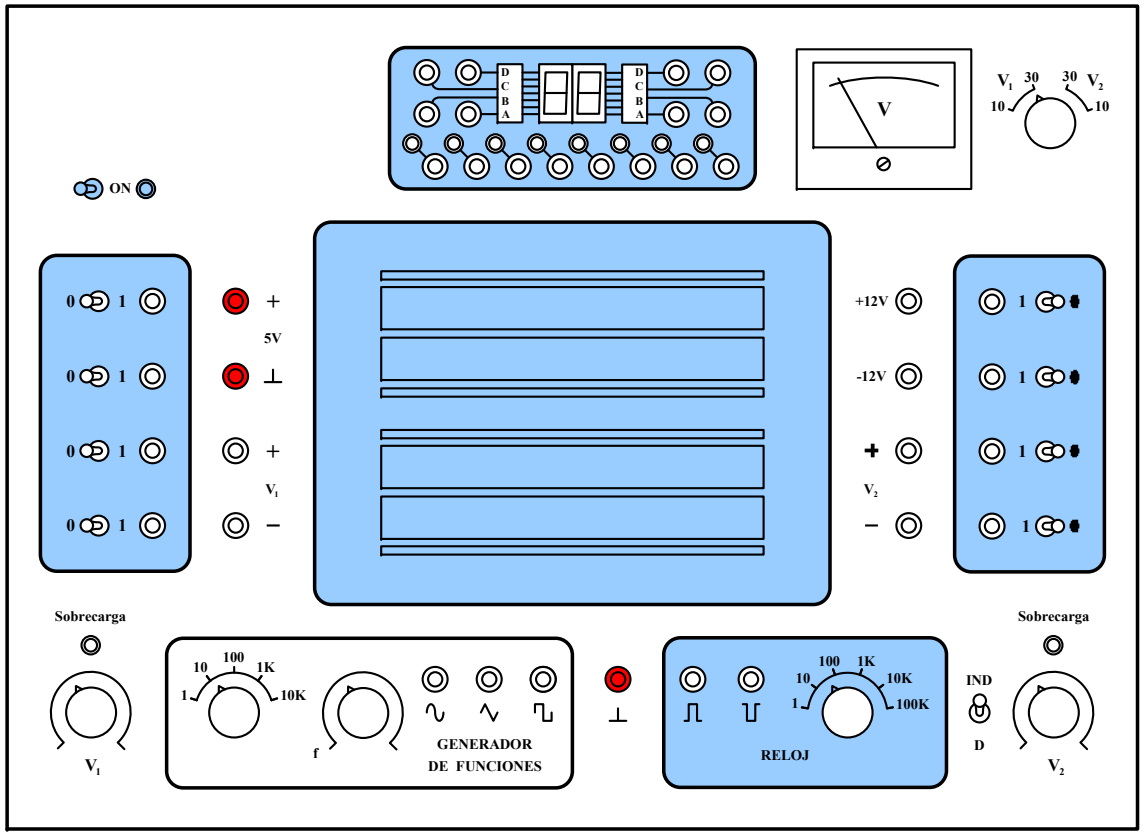
D
Sobrecarga
V1
V2


D C B A
D C B A
V
V1 30 30 V2
10 10
ON
0 1
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+
5V
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V1
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+12V
-12V
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Sobrecarga
10 100 1K
1 10K
f
GENERADOR
DE FUNCIONES
⊥
100 1K
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D
Sobrecarga
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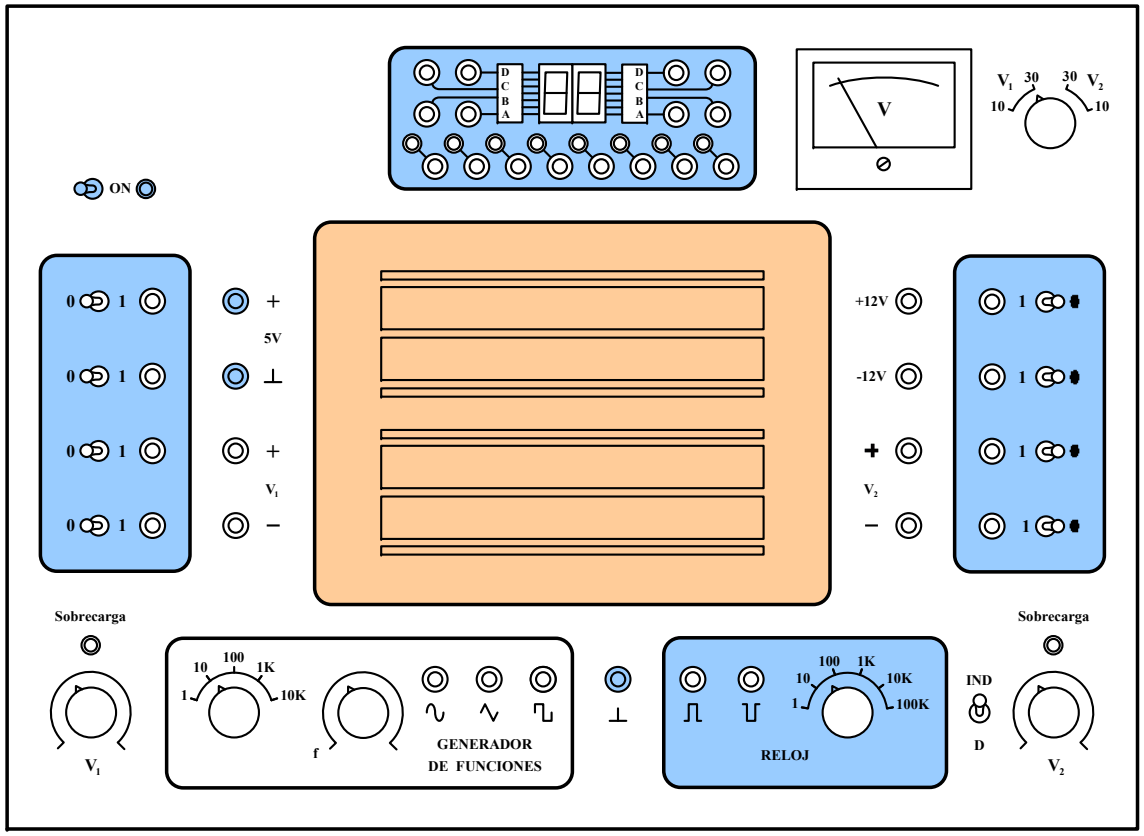
D C B A
D C B A
V
V1 30 30 V2
10 10
ON
0 1
0 1
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0 1
+
5V
⊥
+
V1
−
+12V
-12V
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V2
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Sobrecarga
10 100 1K
1 10K
f
GENERADOR
DE FUNCIONES
⊥
100 1K
10 10K
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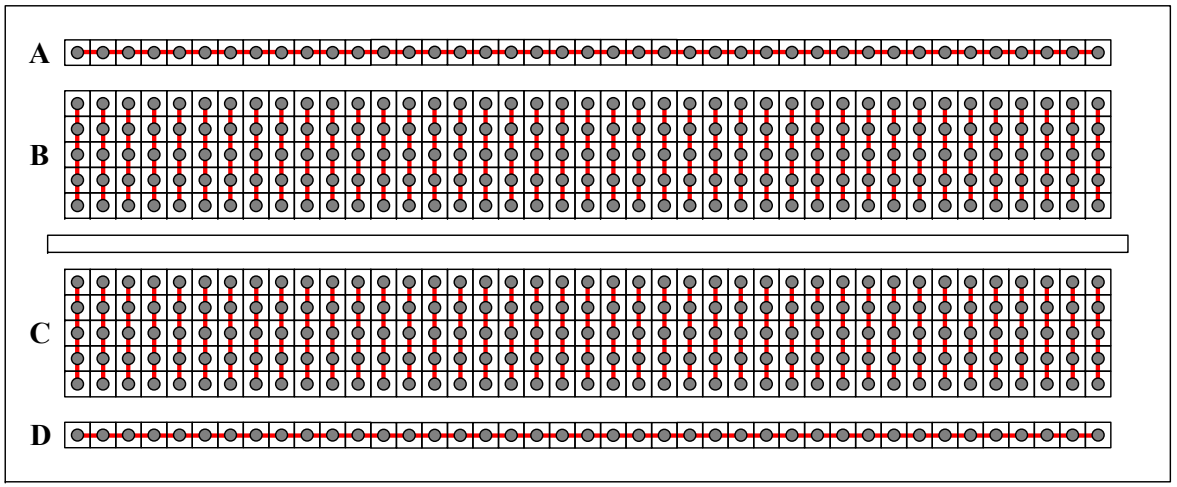
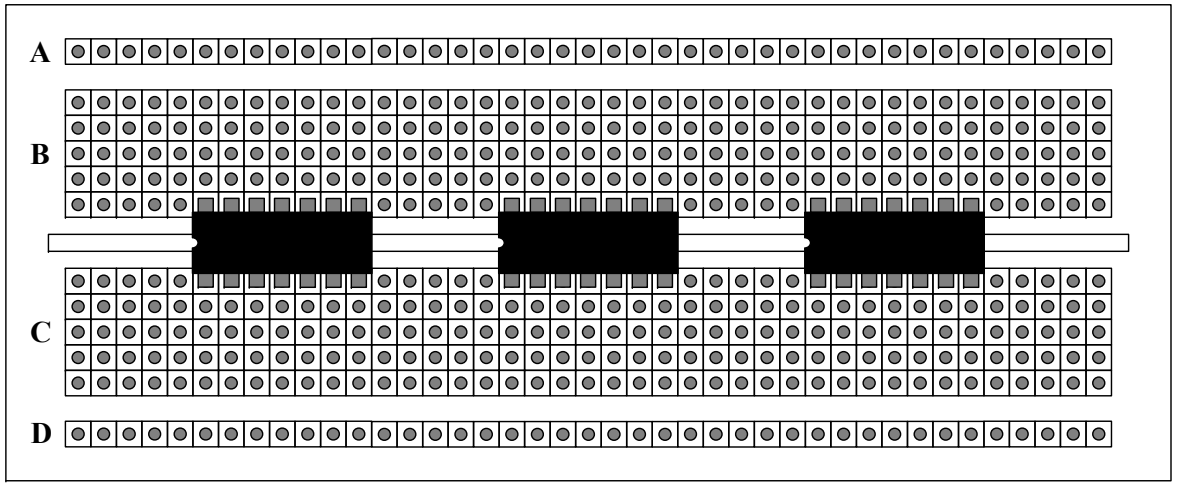
IND
D
Sobrecarga
V1
V2


A
B
C
D


A
B
C
D

Development card