Computer Fundamentals

1st Year of Bachelor in Computer Science Engineering

Practice 2 B

Realization of logic functions with SSI devices (II)

Simplification through the Karnaugh method

Simulation in Digital Works

Academic year 2020/2021

Goals

- Simplification of logic functions.
- Transformation of functions through algebraic manipulation.
- Implementation of functions by means of a single kind of logic gates.
- Introduction to the simulation software Digital Works.
- Initiation in the implementation of functions via logic gates.

Available material

- PC equipped with the software package Digital Works 3.0.5.0.
- 2-input NAND gates (I.C. 7400).
- 2-input NOR gates (I.C. 7402).

Specifications

Given the function:

$$F1\ (D, C, B, A) = \sum_4 (5, 8, 9, 12, 13, 14) + \sum_\phi (0, 4, 6)$$

Operating process

1. Represent the truth table of the function F1.

2. Obtain the simplified expression in form of sum of products (SOP) of the function F_1 following the Karnaugh method.

3. Transform the expression of function F1 obtained in the exercise 2 in such a way that it can be implemented by means of only NOR gates.

4. Draw in Digital Works the **logic diagram** of the expression obtained in the exercise 3.

5. Draw in Digital Works the **hardware diagram** of the F1 expression got in the exercise 4 and check its right operation.

6. Obtain the simplified expression in form of product of sums (POS) of the function F1 through the Karnaugh method.

7. Transform the expression of function F1 got in the exercise 6 in order it can be implemented using exclusively NAND gates.

8. Draw in Digital Works the **logic diagram** of the expression got in the exercise 7.

9. Draw in Digital Works the **hardware diagram** of the F1 expression achieved in the exercise 8 and check its right operation.

10. (Opt) Write the structural description as well as the data flow description concerning the exercise 4 in VDHL. To do this, you must create two source code files. If possible, check the syntax with any programming editor or with the Xilin ISE WebPack framework.

11. (Opt) Do now for the exercise 8, the same task described in exercise 10.