Computer Fundamentals

1st Year of Bachelor in Computer Science Engineering

Practice 3

Realization of logic functions with MSI devices (I)

Simulation in Digital Works

Academic year 2020/2021

Goals

- Understanding of the operation mode of a few combinational MSI functional blocks.
- Realization of logic functions through multiplexers.
- Realization of logic functions by means of decoders and logic gates.
- Visualization of numbers via 7-segment displays.

Available material

- PC equipped with the software package Digital Works 3.0.5.0.
- 2-input NAND gates (I.C. 7400).
- 4-input NAND gates (I.C. 7420).
- 8-input NAND gates (I.C. 7430).
- 8-channel multiplexers (I.C. 74151).
- 4-to-16 lines decoders (I.C. 74154).

Specifications

A digital system can receive the 16 possible combinations of 4-bit numbers through its input-line set: $D_3D_2D_1D_0$.

First part: Using a multiplexer, design a circuit whose output E will adopt a high level when the combination in the inputs belongs to excess-3 BCD code.

Second part: Using decoders and logic gates, design a circuit which will represent in a 7-segment display (that is governed through a 7-segment BCD converter) the following information:

- If the present combination in the input matches a decimal digit greater than 0 which is expressed in excess-3 BCD code, in the display will be visualized the value of the aforementioned digit decremented in a unit.
- If the current combination in the input matches the digit 0 which is expressed in excess-3 BCD code, in the display will be shown the value 9.
- If the input combination does not belong to the excess-3 BCD code, in the display will be depicted the value 0.

Operating process

1. Represent the truth table of the first circuit and obtain the numerical disjunctive canonical expression of the function E.
2. Obtain the logic diagram of the first circuit using a multiplexer.
3. Draw in Digital Works the **logic diagram** obtained in the exercise 2 and simulate it to check its right operation.
4. Draw in Digital Works the **hardware diagram** of the logic diagram in the exercise 3, completing the simulation as well as the check to detect that is working properly.
5. Symbolise the truth table of the second circuit and get the numerical disjunctive canonical expression of the different output functions.

6. Get the logic diagram of the second circuit using decoders and logic gates.

7. Draw in Digital Works the **logic diagram** achieved in the exercise 6 and complete the simulation as well as the check, in order to detect that is working properly.

8. Draw in Digital Works the **hardware diagram** of the logic diagram obtain in the exercise 7, performing the simulation and its check to test whether is operating rightly.

9. Represent the truth table of the system indicated by the lecturer during the laboratory session and obtain the numerical disjunctive canonical expressions of the different output functions.

10. Obtain the logic diagram concerning the truth table of the circuit in the exercise 9 using the components indicated by the lecturer.

11. Draw in Digital Works the **logic diagram** obtained in the exercise 10, simulate it to check its right operation and contrast the results with the truth table of the exercise 9.

12. Draw in Digital Works the **hardware diagram** of the logic diagram in the exercise 11, completing the simulation as well as the check to detect that is working properly according to the truth table of the exercise 9.

Notes:

- The logic symbols of the BCD to 7-segment decoder and the 8-input NAND logic gates can be found in the folder Symbols within the Parts Centre.
- The logic symbol of the BCD to 7-segment decoder will be used for both the logic and the hardware diagrams.
- The simulations in Digital Works concerning the exercises 3, 4, 7 and 8 should be done as previous work before attending the laboratory session, be sent by email to the lecturer (one email for two-people group) and be shown to the lecturer at the beginning of the laboratory session.
- The exercises from the 9^{th} to the 12^{th} will be done during the laboratory session.
- Through the Sequence Generator, the traversing of truth table must be defined in an ordered way from the first combination to the last one.