BOOLEAN_FUNCTION_MINIMIZATION

/ README.md in main

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```
1   # BOOLEAN_FUNCTION_MINIMIZATION
2
3   **AIM:**
4
5   To implement the given logic function verify its operation in Quartus using Verilog
    programming.
6
7   F1= A’B’C’D’+AC’D’+B’CD’+A’BCD+BC’D
8
9   F2=xy’z+x’y’z+w’xy+wx’y+wxy
10
11  **Equipment Required:**
12
13  Hardware – PCs, Cyclone II , USB flasher
14
15  **Software – Quartus prime**
16
17  **Theory**
18
19  **Logic Diagram**
20
21  **Procedure**
22
23  1.  Type the program in Quartus software.
24
25  2.  Compile and run the program.
26
27  3.  Generate the RTL schematic and save the logic diagram.
28
29  4.  Create nodes for inputs and outputs to generate the timing diagram.
```

Use Control + Shift + m to toggle the tab key moving focus. Alternatively, use esc then tab to move to the next interactive element on the page.

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```
34  **Program:**
35
36  /* Program to implement the given logic function and to verify its operations in quartus
    using Verilog programming.
```