

ATLAS ITk Pixel Detector Overview

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Abstract

For the High Luminosity upgrade of the Large Hadron Collider the current ATLAS Inner Detector will be replaced by an all-silicon Inner Tracker. The pixel detector will consist of five barrel layers and a number of rings, resulting in about 13 m² of instrumented area. Due to the huge non-ionising fluence (1·10¹⁶ neq/cm²) and ionising dose (5 MGy), the two innermost layers, instrumented with 3D pixel sensors and 100 µm thin planar sensors, will be replaced after about five years of operation. Each pixel layer comprises hybrid detector modules that will be read out by novel ASICs, implemented in 65 nm CMOS technology, with a bandwidth of up to 5 Gbit/s. Data will be transmitted optically to the off-detector readout system. To save material in the servicing cables, serial powering is employed for the supply voltage of the readout ASICs. Large scale prototyping programmes are being carried out by all subsystems.

This paper will give an overview of the layout and current status of the development of the ITk Pixel Detector.

I. INTRODUCTION

IN the High Luminosity (HL) era of the Large Hadron Collider (LHC), the average number of collisions per bunch crossing (BC) will increase from the current 30 to about 200, resulting in an increase of the peak luminosity from 1·10³⁴ cm⁻²s⁻¹ to 5–7·10³⁴ cm⁻²s⁻¹. The integrated luminosity of 350 fb⁻¹ at the end of Run 3 will accumulate more rapidly up to 4000 fb⁻¹ until the end of the HL programme. The requirement for the pixel detector of the ATLAS experiment [1] and its readout also becomes more demanding: the occupancy is kept below 1% by increasing the detector granularity with the frontend chip operating at 1 MHz trigger rate. The innermost pixel system has to withstand a harsher radiation environment up to 2·10¹⁶ neq/cm². This HL upgrade is planned to take place during the Long Shutdown (LS) 3 as indicated in Figure 1.

II. ATLAS INNER TRACKER UPGRADE

For the HL upgrade of the ATLAS detector, the current Inner Detector (ID), consisting of silicon

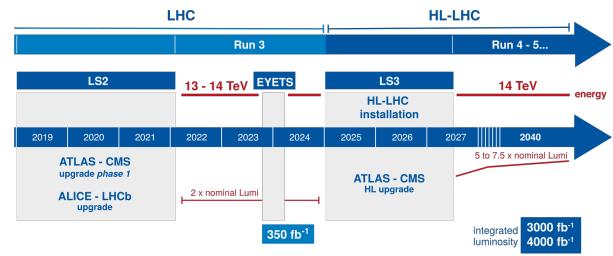


Figure 1: Timeline of the Large Hadron Collider in the coming years. The High Luminosity upgrade is planned for Long Shutdown (LS) 3 [2].

pixel, silicon strip detectors and Transition Radiation Tracker (TRT) is going to be replaced by an all-silicon Inner Tracker (ITk) [3, 4], which has 13 m² of pixel detectors with 5 billion readout channels and 160 m² of strip detectors with 50 million readout channels. The layout of active elements in the ITk Pixel detector in the r-z projection is shown in Figure 2. The five-layer design provides a higher tracking coverage of up to | η | = 4, while at the same time multiple scattering is minimised by greatly reducing the material budget compared to the current ID, as shown in Figure 3.

Sections i, ii and iii will introduce the sensors, readout chips and pixel modules as building blocks of the pixel detector, with which larger structures are built and described in sections iv to vii.

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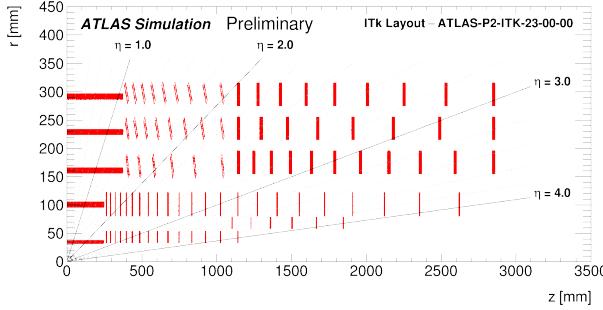


Figure 2: Layout schematic of active elements in the r - z projection of the ITk Pixel detector [5].

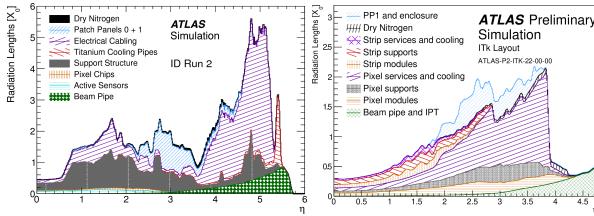


Figure 3: Comparison of the material budget in the detector between the current Inner Detector during Run 2 [3] and ITk [6].

i. Sensors

The pixel sensors are required to have an efficiency of $>98.5\%$ before, and $>97\%$ after an irradiation with a corresponding end-of-life fluence [3]. Two technologies are used for the ITk Pixel detector: 3D sensors in the innermost layer (L0) in triplet modules, consisting of three single frontend-sensor assemblies on a triplet flex, and planar sensors in quad modules in all other layers (L1–L4), consisting of four frontend chips on a quad sensor tile on a quad flex. Both technologies use n-implant in p-substrate with a generally thinner active thickness compared to the current pixel detector, thus charge and hit efficiencies are saturated at lower bias voltages which lead to a reduction of dissipated power. At the moment, a market survey is finished for both technologies and pre-production is ongoing.

i.1 3D Sensors

3D sensors with a pixel size of $50 \times 50 \mu\text{m}^2$ and $25 \times 100 \mu\text{m}^2$ with a single collection electrode in the centre and a good efficiency, as shown in Figure 4, are used in the endcap and barrel regions of L0, respectively. They consist of $150 \mu\text{m}$ active thickness plus $100 \mu\text{m}$ support wafer. 3D sensors are intrinsically more radiation tolerant and therefore

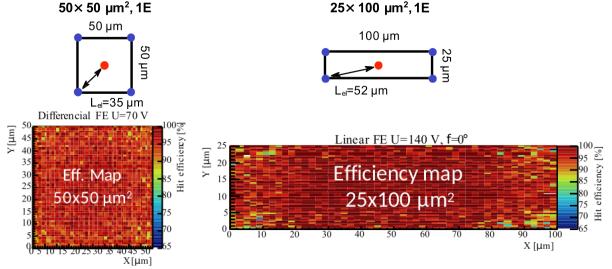


Figure 4: Top: pixel sizes used in 3D sensors with a single collection electrode (red) [7]. Bottom: Efficiency maps for different pixel sizes [7].

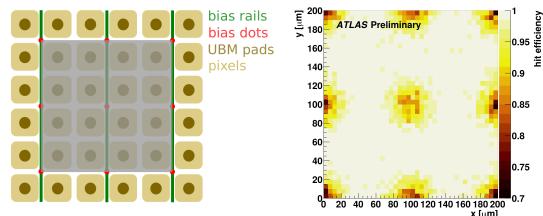


Figure 5: Pixel matrix design with punch-through bias structure (left) and efficiency map (right) of 4×4 pixels (grey area) of a planar sensor before irradiation [8].

used in the innermost layer which is only 34 mm from the beam. It will be replaced after 2000 fb^{-1} with an expected fluence of $1.3 \cdot 10^{16} \text{ neq/cm}^2$ as part of the Inner pixel system replacement [3].

i.2 Planar Sensors

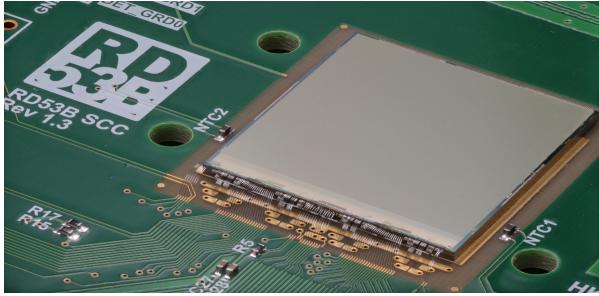
Planar sensors have a pixel size of $50 \times 50 \mu\text{m}^2$ in all regions. The thickness is $100 \mu\text{m}$ in L1 in the Inner System and $150 \mu\text{m}$ in the outer layers. There are designs with punch-through bias structure as shown in Figure 5 left and without (not shown). The efficiency of a 4×4 pixel region (grey area) before irradiation is shown in Figure 5 right, where a slightly lower efficiency is observed in regions with punch-through bias dots [8].

ii. RD53 Readout Chip

The frontend (FE) readout chip is developed by the RD53 collaboration [9], consisting of 24 institutes from Europe and the United States, as a common readout chip for ATLAS and CMS pixel detectors. It evolved from the RD53A prototype [10], consisting of three different frontend flavours, into ITkPix [11] for ATLAS with 400×384 pixels using differential frontend, and CROC for CMS with 432×336 pixels using linear frontend. ITkPixV1, shown in Figure

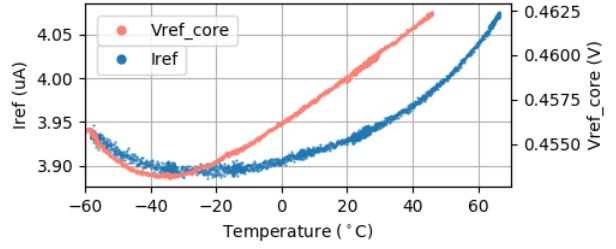
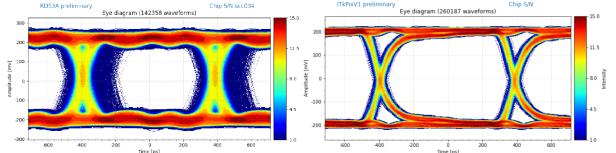
Table 1: Technical specifications of ITkPix [3, 11].

Chip size	$20 \times 21 \text{ mm}^2$
Pixel size	$50 \times 50 \mu\text{m}^2$
Hit rate	3 GHz/cm^2
Trigger rate	1 MHz
Latency	$12.8 \mu\text{s}$
Data rate	5.12 Gbit/s
Low threshold	600 e
Radiation tolerance	500 Mrad
Low power	$4 \mu\text{A}/\text{pixel}$

**Figure 6:** An ITkPixV1 chip on a single chip card [13].

6 on a single chip card (SCC), was submitted in March 2020 and is currently being verified. Submission of the final version, ITkPixV2, is foreseen for the end of 2021.

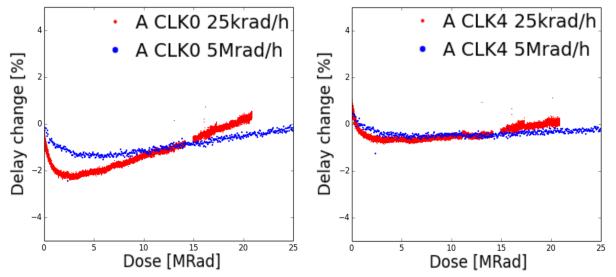
Apart from an issue with the time-over-threshold (ToT) latch which is fixed in version 1.1, Figures 7, 8 and 9 show a small selection of verifications tests. The chips main reference current and voltage are stable within 4% over a large temperature range of up to 120°C (Figure 7). The eye-diagramme of command data recovery (CDR) and PLL in Figure 8 shows an improved jitter from RD53A with 29.94 ps RMS to ITkPixV1 with 11.2 ps RMS [12]. X-ray irradiation campaigns are ongoing with ring oscillators as test structures. Figure 9 compares high dose rate of 5 Mrad/h (blue) with a low dose rate of 25 krad/h (red) on the CLK gates of lengths 0 and 4 [12]. While it is faster to accumulate ionising dose at end-of-life with a high rate, low rate of ionising radiation that reflects realistic irradiation conditions in the detector generates more degradation at the same accumulated dose, which can be seen from the steeper slope. Studying both rates could allow an estimate of scalability of the degradation.

**Figure 7:** Main reference current and voltage of the ITkPixV1 show only a change of less than 4% over 120°C temperature range [13].**Figure 8:** Eye diagrammes of command data recovery (CDR) and PLL from RD53A (left) to ITkPixV1 (right). The jitter improved from 29.94 ps RMS to 11.2 ps RMS, respectively [12].

iii. Pixel Module

There are linear and round triplet modules in the innermost layer L0 for the barrel and rings, and quad modules for layers 1–4 making the largest part of the detector. About 10000 modules are going to be assembled for the ITk Pixel detector by hand during the next four years. Bare, hybridised sensor-frontend assemblies are glued onto module flexes using custom built tools, where glue is distributed by means of a laser-cut stencil and the thickness of the glue layer is controlled via precision shims as shown in Figure 10.

Every assembled module has to pass a quality control procedure which involves visual inspection, metrology and electrical testing at different temper-

**Figure 9:** X-ray irradiations comparing high (blue) and low (red) dose rate on ring oscillators of lengths 0 (left) and 4 (right) on the ITkPixV1 [12].

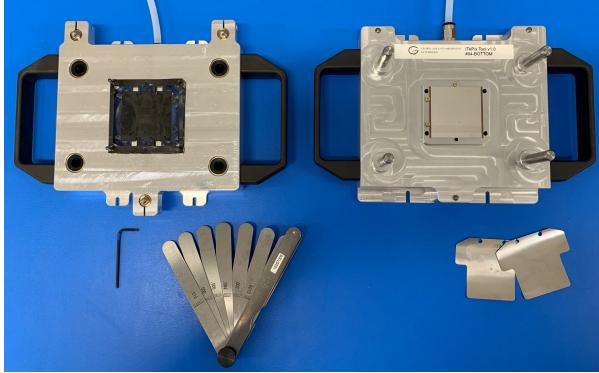


Figure 10: Custom tools for pixel quad module assembly.



Figure 11: One of the first ITkPixV1 digital quad module on a prototype flex PCB being tested.

atures. Currently, the RD53A module programme is ongoing for institutes to set up infrastructure and gain experience in assembly, quality control and system test. Also first ITkPixV1 digital quad modules using prototype flexes are being tested with custom readout and power adapter boards as shown in Figure 11. These first tests verified the flex design but also allow access to probe multi-chip features like command forwarding, data aggregation etc.

iv. Serial Powering

Readout chips on a triplet or quad module are powered in parallel using up to 8 W of power. By powering up to 14 [14] of those modules in series in a chain, the amount of required cables is reduced and thus material budget in the detector. This is made possible through shunt-LDO (SLDO) powering mode of the frontend chip by providing the chip with a constant and redundant power budget. Experience in operating serial powering chains was gained through demonstrators based on FEI4 modules [15]. Studies on the first serial powering chain with RD53A quad modules is ongoing as shown in

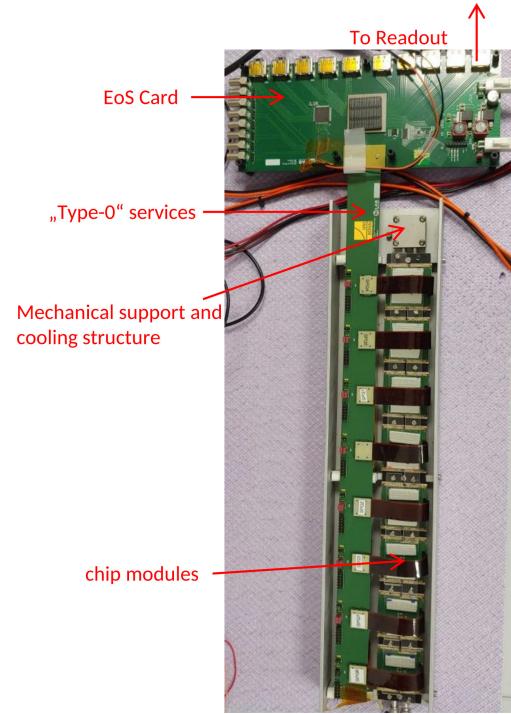


Figure 12: Serial powering test with RD53A quad modules connected to pseudo Type-0 services and end-of-stave (EoS) card [16].

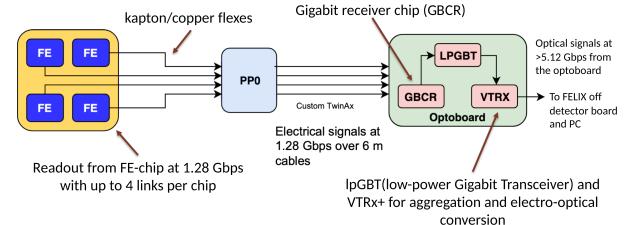


Figure 13: Schematic of the data path [7].

Figure 12 and chains with ITkPix modules are in preparation.

v. Data Transmission and Services

Each frontend chip is capable of transmitting data via 4 links with 1.28 Gbit/s, resulting in up to 16 links on a quad module. The activity of a frontend chip depends on the hit rate and thus the position of the module in the detector. When full data rate is not required, the number of physical outgoing links per module can be reduced by aggregating data within the module through the frontend chips. The number of required data links can vary from 9 lines per triplet module in the innermost layer down to 1 line per quad module in L3. These links

are shown in Figure 13 as kapton-copper flexes (Type-0 services) between module and patch panel 0 (PP0). From PP0 data is transmitted through custom Twinax cables to the optoboard [17], where electrical signal is recovered by the Gigabit Receiver Chip [18] and is aggregated and converted to optical signal through the low-power Gigabit Transceiver (IpGBT [19]) and VTRx [20] before being sent off detector to the readout.

vi. Mechanical Support

In the detector, modules are attached onto and supported by lightweight carbon fibre composite structures, as shown in Figure 14. The Inner System uses a quarter shell concept for the barrel and endcap regions with different designs for the endcap rings (a). For the Outer System, the Barrel region (b) consists of longerons for the flat region and inclined half rings towards higher $|\eta|$, and Outer Endcap consists of modules that are attached onto half rings embedded in half shells (c).

vii. System Test

System test with realistic module staves and infrastructure is ongoing for all subsystems of the pixel detector, using all components introduced above. Figure 15 shows an example of the system test infrastructure for Outer Barrel at CERN, consisting of a CO₂ cooling plant, a dry air unit, racks with power supplies, detector control system (DCS), an interlock matrix, and a light-tight and thermally insulated testbox with a source stage.

The demonstrator is a full-size, 1.6 m long prototype stave that is loaded with FEI4-based modules [23]. The module arrangement is indicated in Figure 16 top: with 14 flat quad modules in the centre, 7 on each A-side and C-side, and 13 and 16 inclined dual modules towards high $|z|$ on the A-side and C-side, respectively. The modules are connected in 6 serial powering chains. The middle plot shows a noise level of all modules, measured warm and cold with CO₂ cooling at 17°C and -25°C, respectively. As expected the noise level decreases with lower temperature. A source scan of the C-side quad modules performed at -25°C is shown in the bottom plot by running two ⁹⁰Sr sources on the stage over all modules. The quad modules on the C-side were fully functional on the module level. After integration onto the stave some frontend chips lost communication which is mostly due

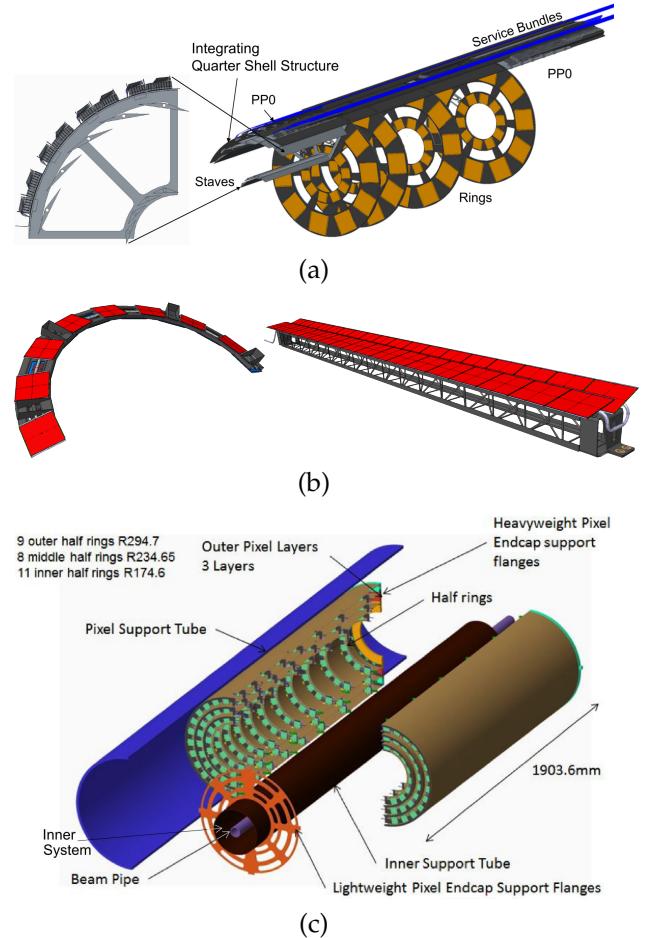


Figure 14: Lightweight local support carbon fibre structures with pixel modules for the Inner System (a), Outer Barrel (b) and Outer Endcap (c) [21, 22].

to issues related to cables, except for the chip on BM_03 which shows a perfect source scan when warm [23]. The path leading to the cold source scan of the demonstrator provided valuable experience and demonstrated a working constellation of system infrastructure.

III. SUMMARY

This paper has given a brief overview of the status of the pixel system of ATLAS Inner Tracker upgrade. Module components, sensor, frontend chip and module flex are being finalised. Module institutes are set up and being qualified for assembly and testing so the RD53A module programme can progress with full speed. With these modules, the gained experience with serial powering tests and fully functional FEI4 prototype systems preparing



Figure 15: System test infrastructure at CERN SR1. From left to right: CO₂ plant, dry air unit, racks with power supplies and interlock system, and light tight and thermally insulated testbox [24].

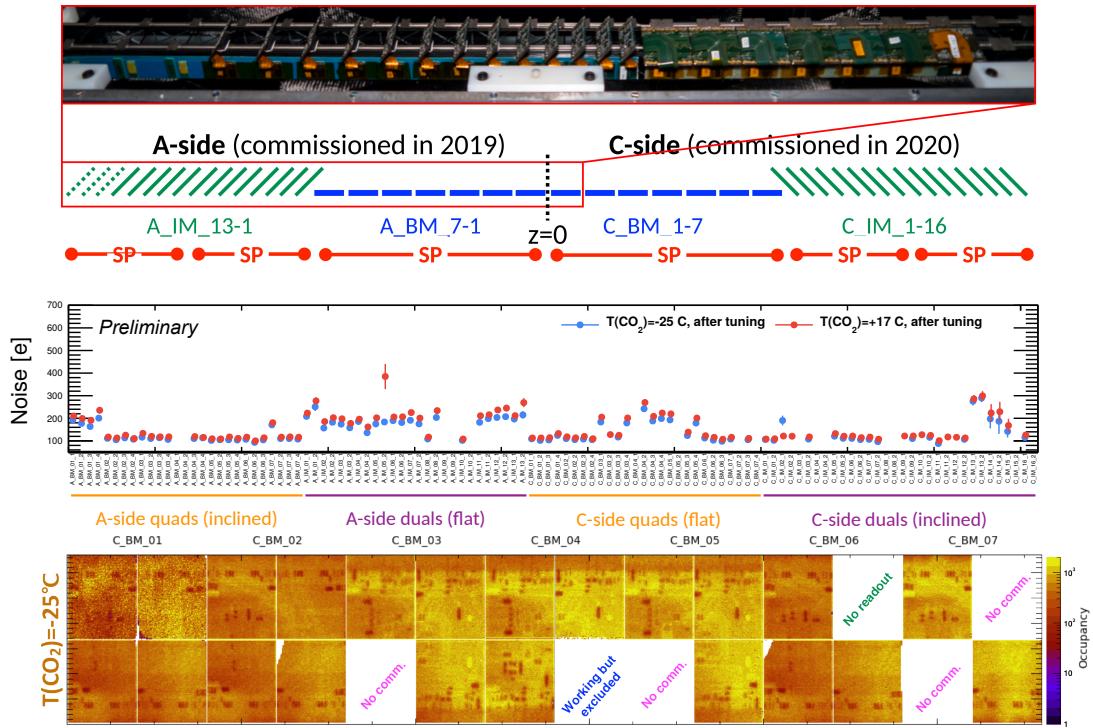


Figure 16: Results from the Outer Barrel demonstrator using prototype FEI4 modules. Top: layout of the modules. Middle: noise level of the modules measured warm and cold with CO₂ cooling at 17°C and -25°C , respectively. Bottom: source scan of the C-side quad modules at -25°C using ⁹⁰Sr sources [23].

for the next generation demonstrators with the first RD53A modules to validate every aspect of the ITk Pixel detector development.

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