



TIPP2023

TECHNOLOGY IN INSTRUMENTATION & PARTICLE PHYSICS CONFERENCE

4 - 8 SEPTEMBER 2023

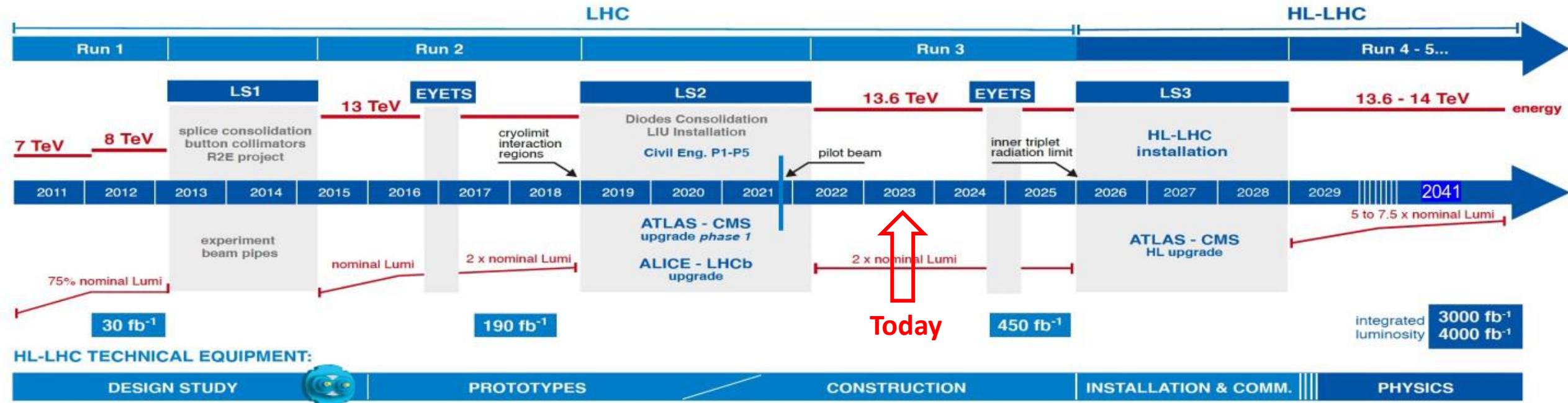


ATLAS ITk Pixel Overview



Koji Nakamura *On-behalf of ITk Pixel collaboration*

High Luminosity LHC



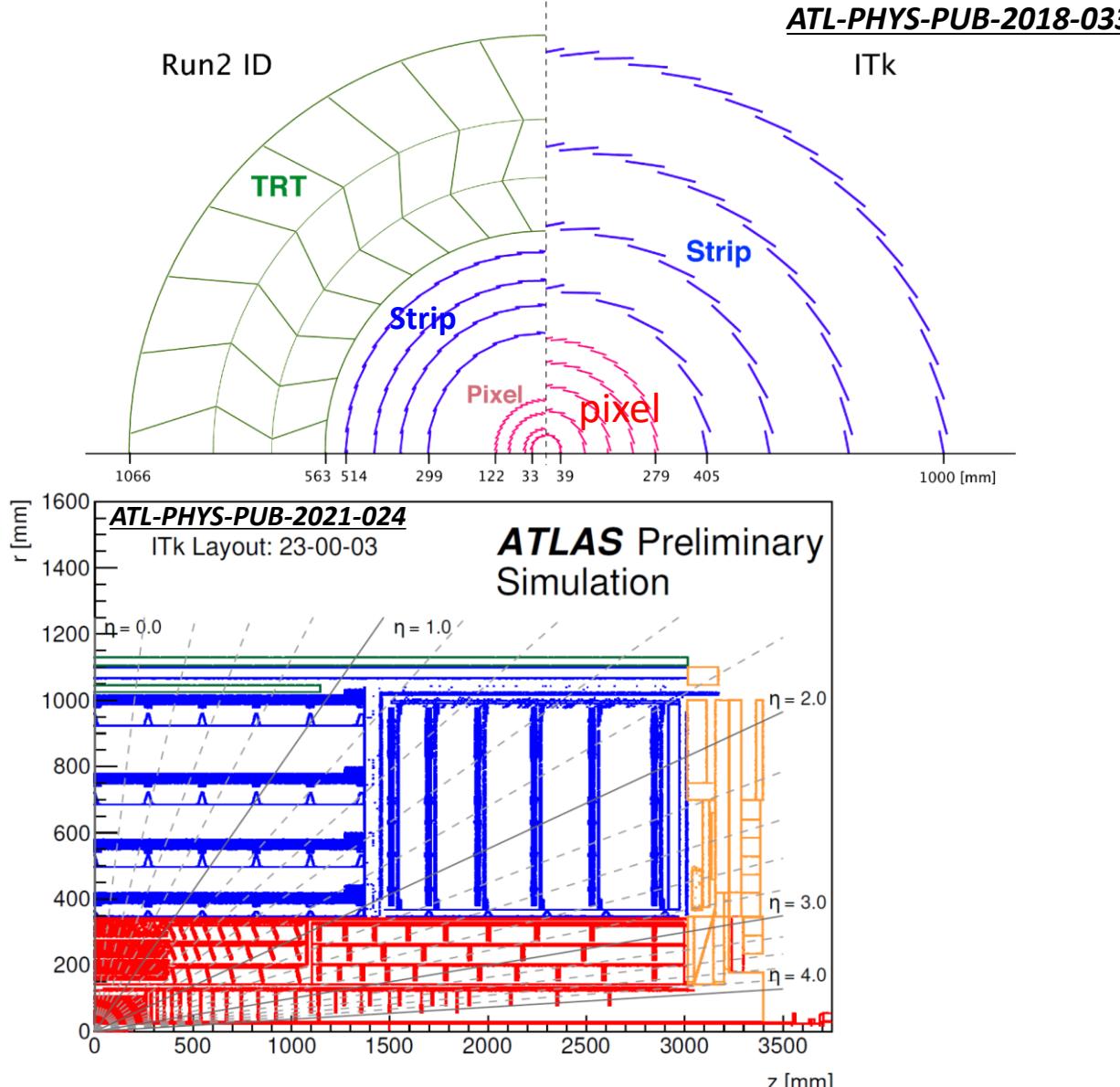
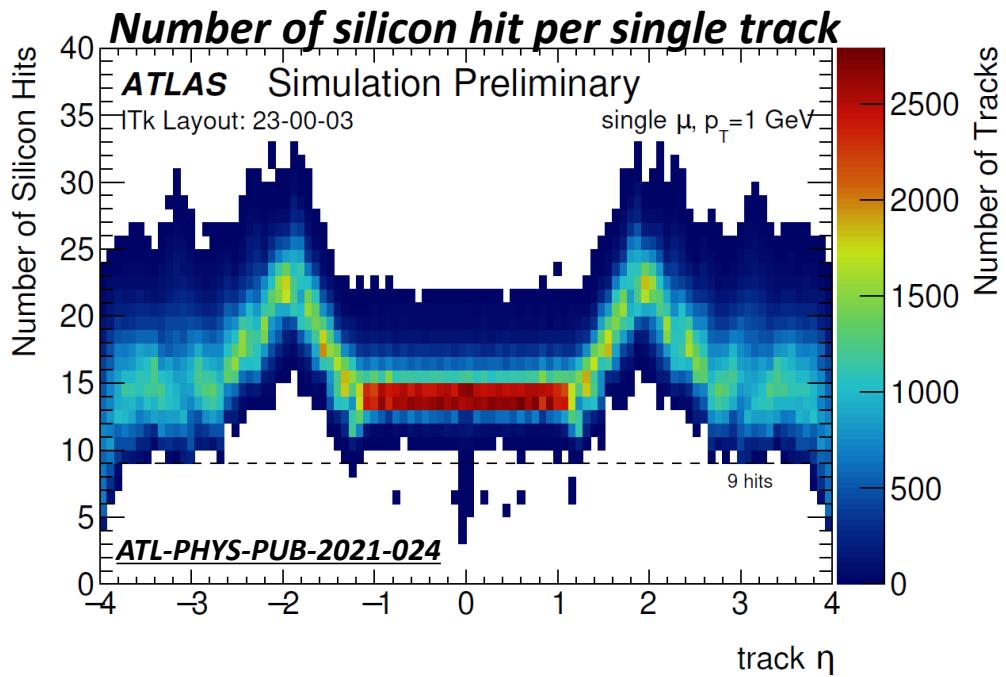
- LHC and its experiments are running well (Run 3) and produced many results.
- The “HL-LHC” period will start in ~2029 and will accumulate $\int L dt \sim 4000 \text{fb}^{-1}$.
- Need to upgrade Inner detector of ATLAS experiment to deal with more radiation damage, more “dense” events.

Inner Tracker (ITk) and Pixel detector

• Inner Tracker (ITk)

- Instantaneous Luminosity : $7 \times 10^{34} \text{ cm}^2/\text{s}$
 - x3.1 times** Run3 peak lumi
- Increased Pile-up
 - Up to **200 pile-up events** per bunch crossing.

→ Full Silicon based system



Inner Tracker (ITk) and Pixel detector

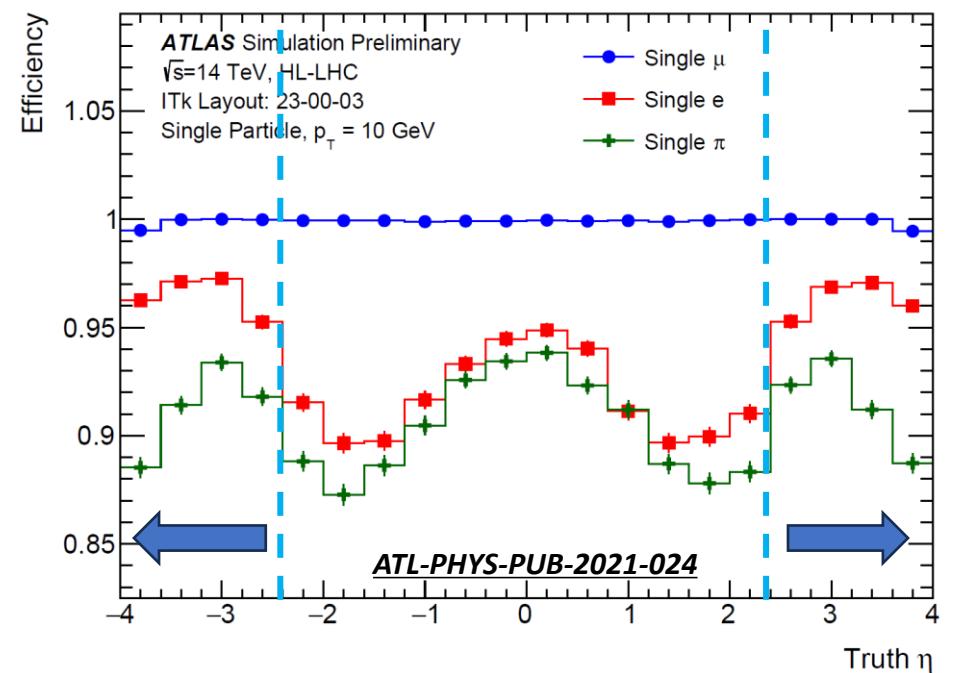
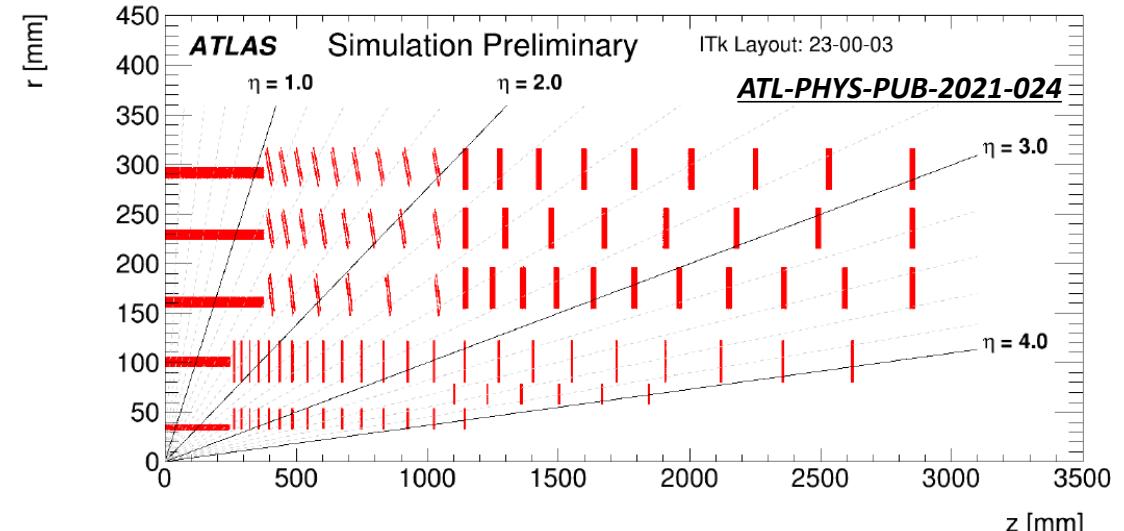
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• ITk Pixel system

- Larger coverage area
 - Pixel : current $1.9 \text{ m}^2 \rightarrow$ **upgrade 13.5 m^2**
- Higher Forward coverage
 - Current $\eta < 2.5 \rightarrow$ **upgrade $\eta < 4.0$**
 - **Better Pileup removal & background rejection**



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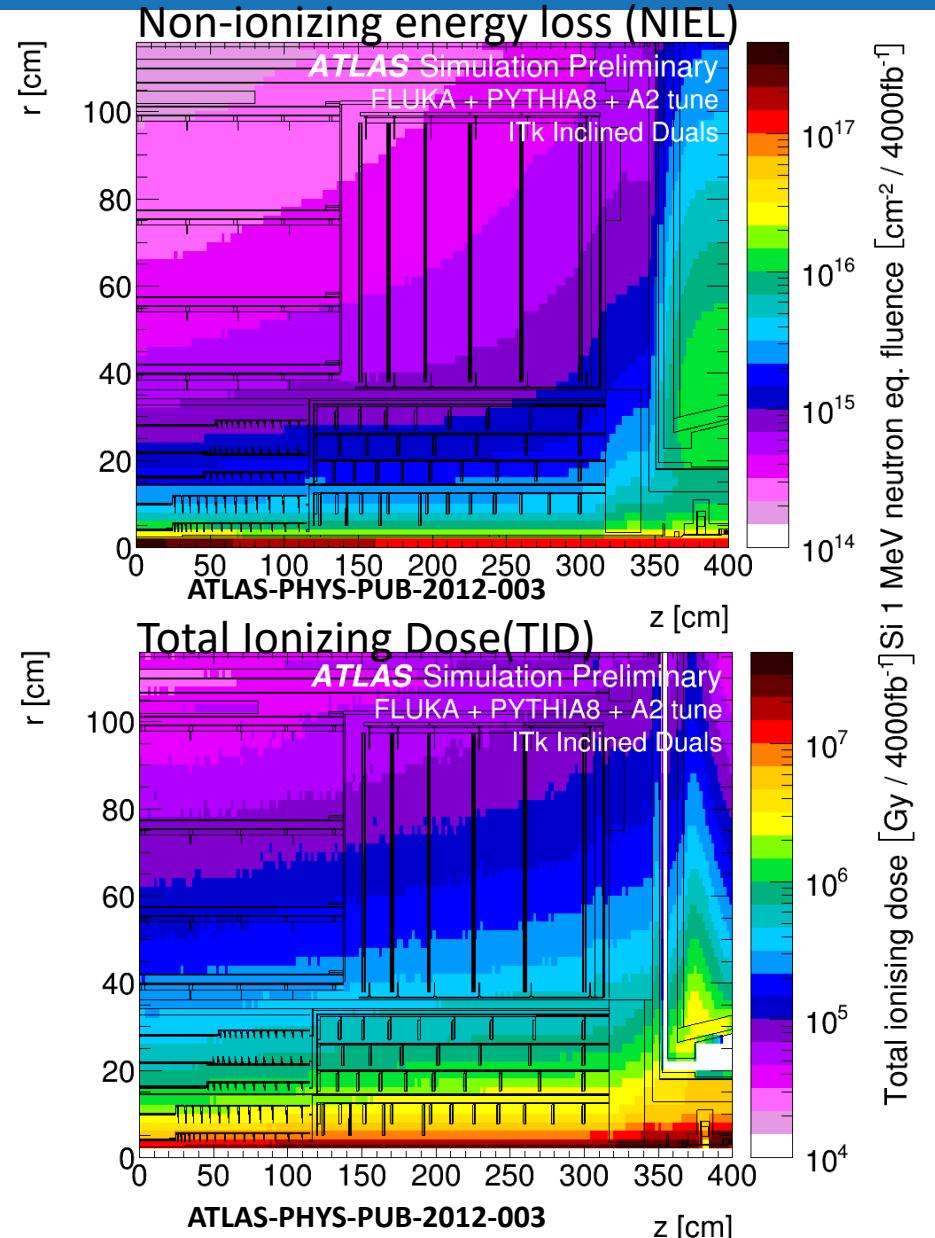
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• Required high radiation tolerance.

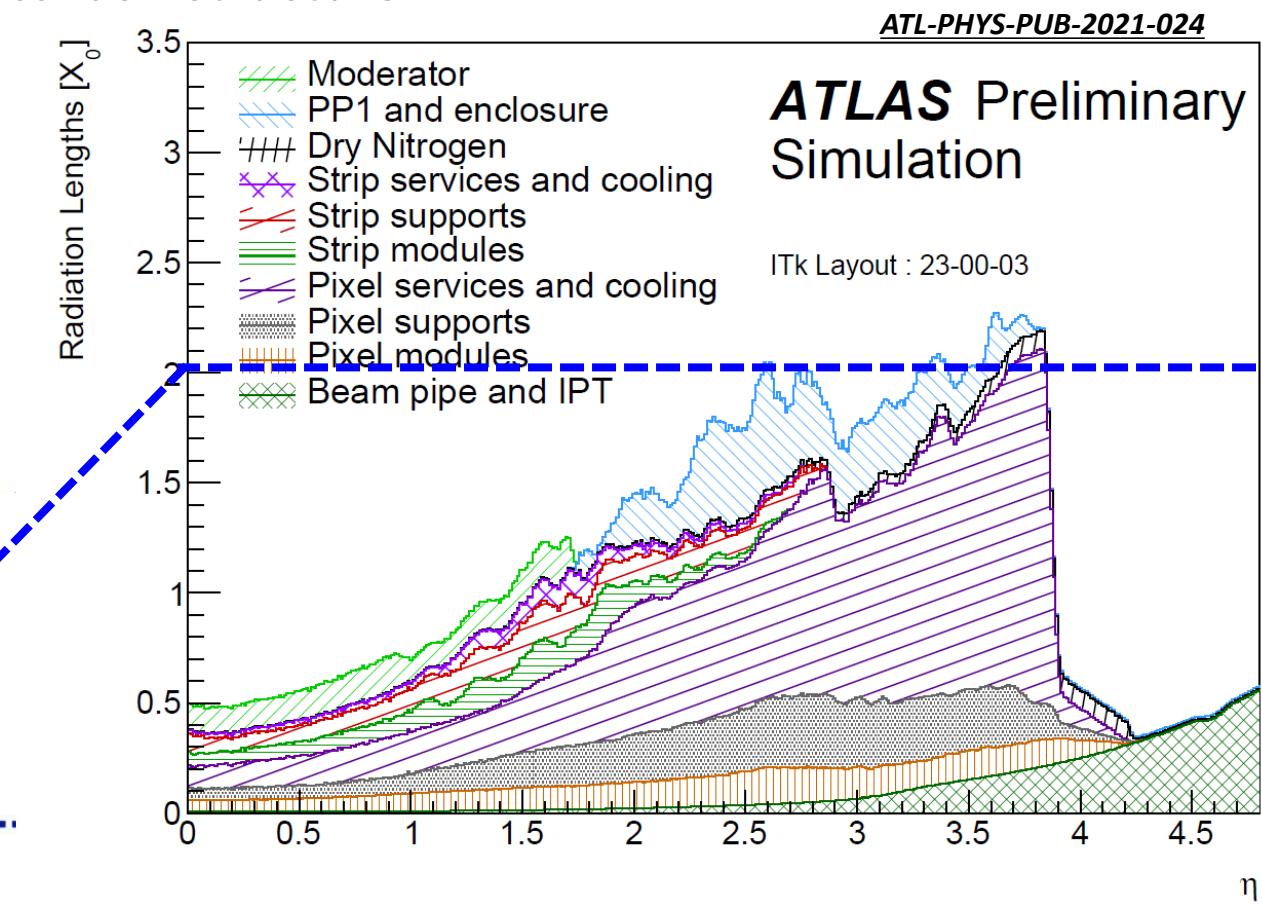
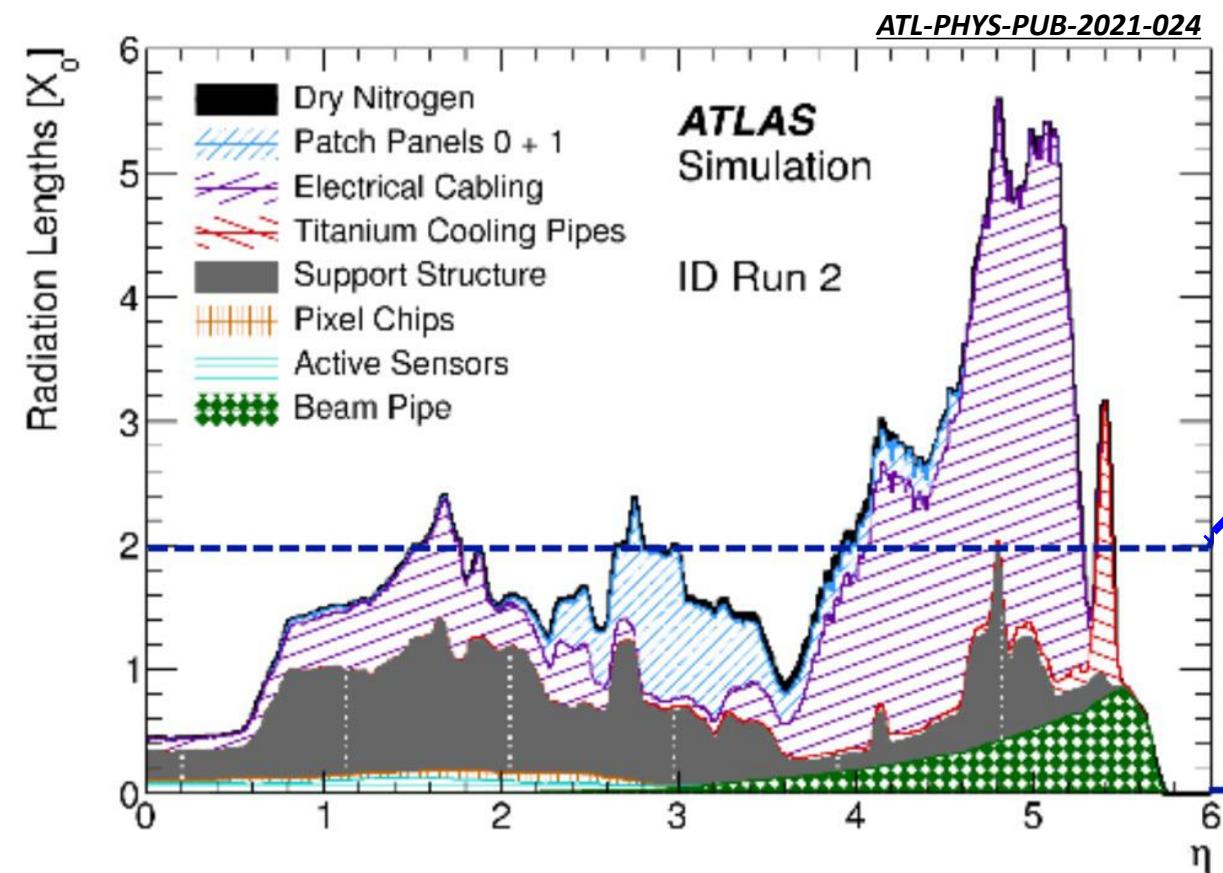
- x10 increase of Radiation damage:
 - Requirement (including safety factor)
 - **$17 \times 10^{15} \text{ neq/cm}^2$** at inner layers*
 - **$5 \times 10^{15} \text{ neq/cm}^2$** at outer layers

*Inner 2 layers will be replaced at half.

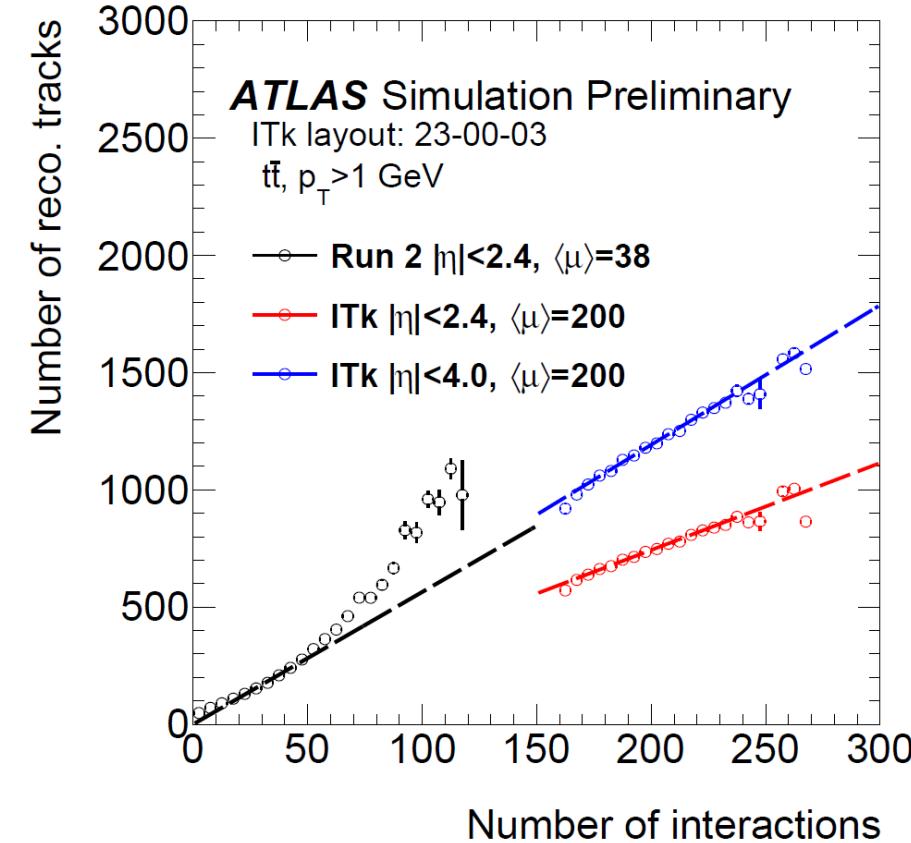


Material budget

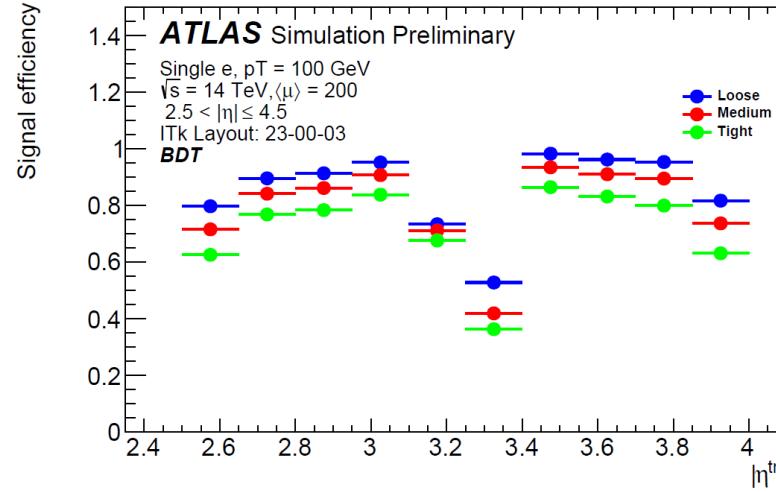
- Reduce material by
 - Advanced cabling: serial powering for pixels, data link sharing
 - Minimize material in modules using thin Sensor and FE-chip
 - CO₂ cooling with titanium pipes, Low-mass carbon structure



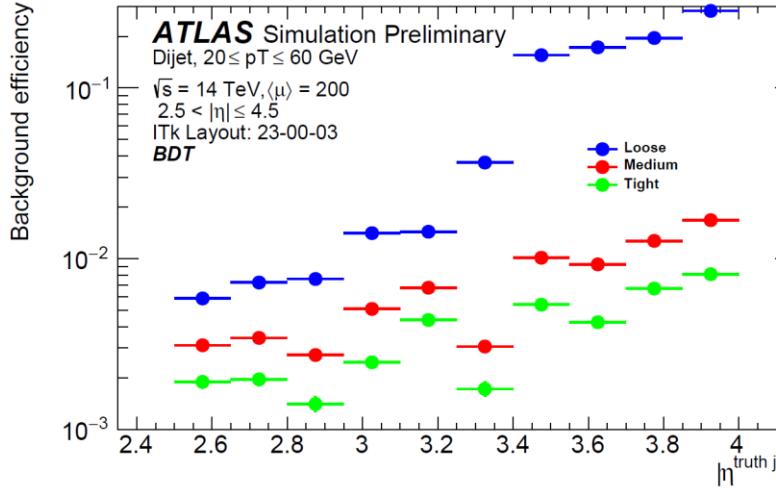
Number of tracks v.s. Pile-up



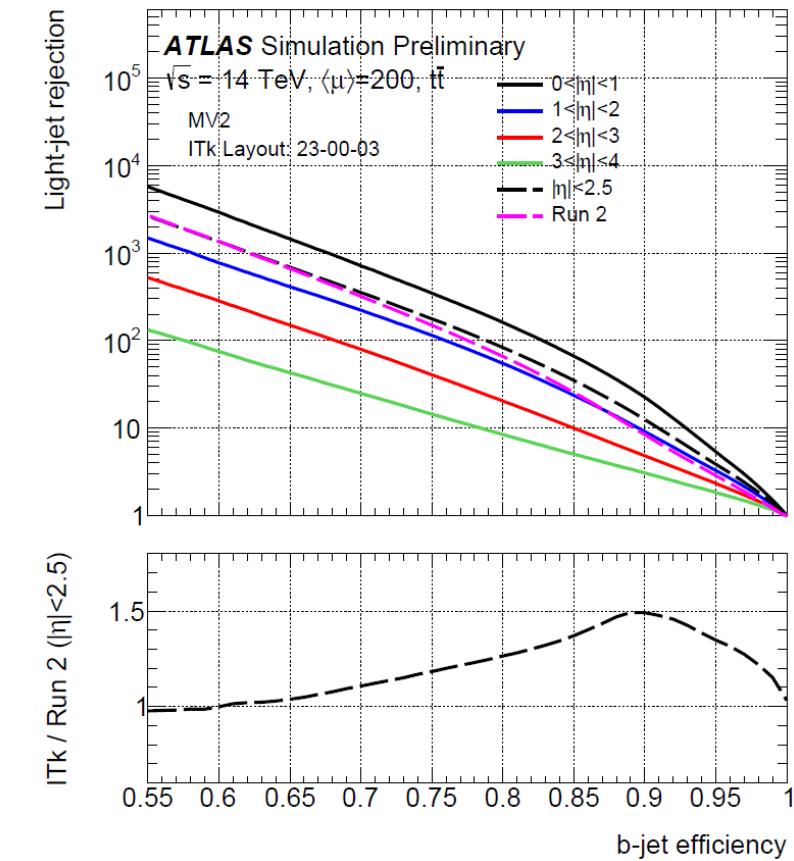
Forward Electron reconstruction efficiency



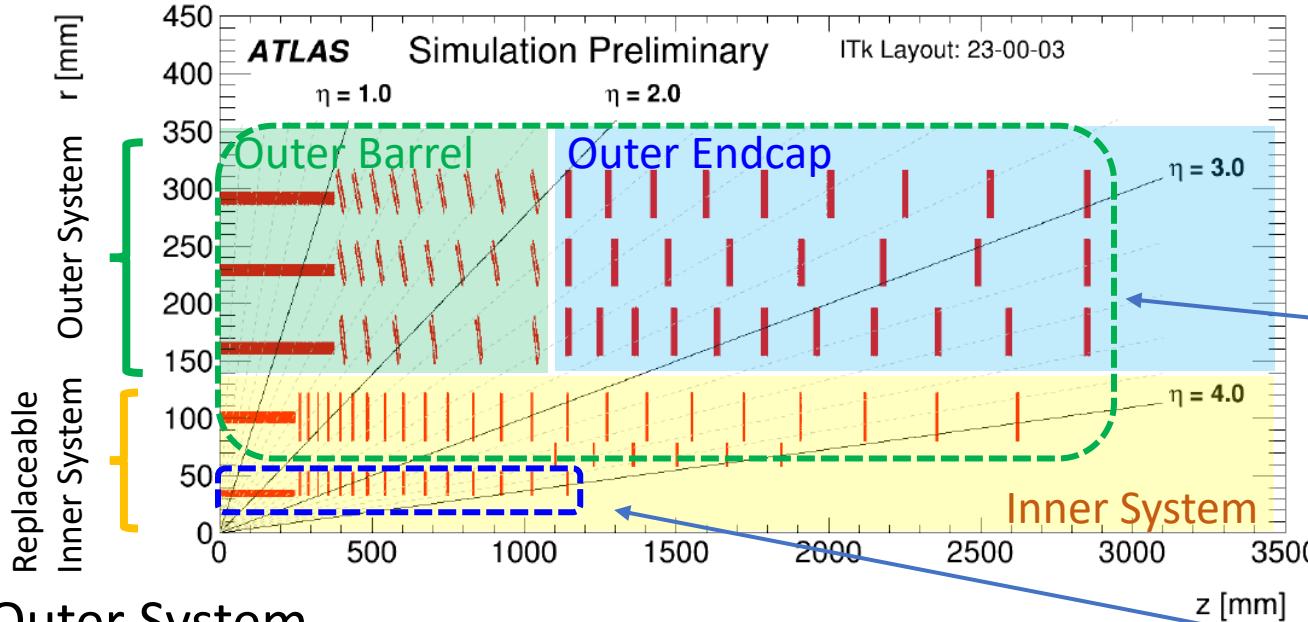
Forward Background efficiency



B-tagging Performance



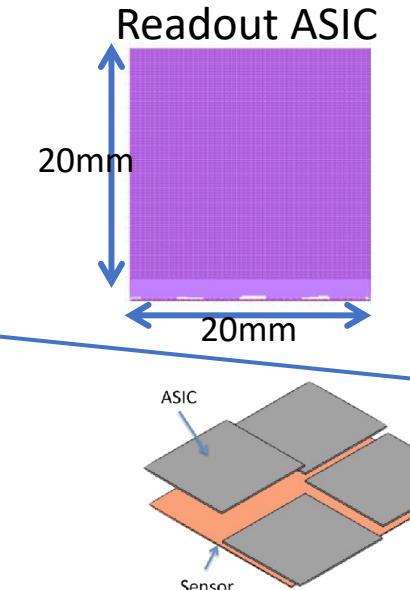
ITk Pixel detector Layout



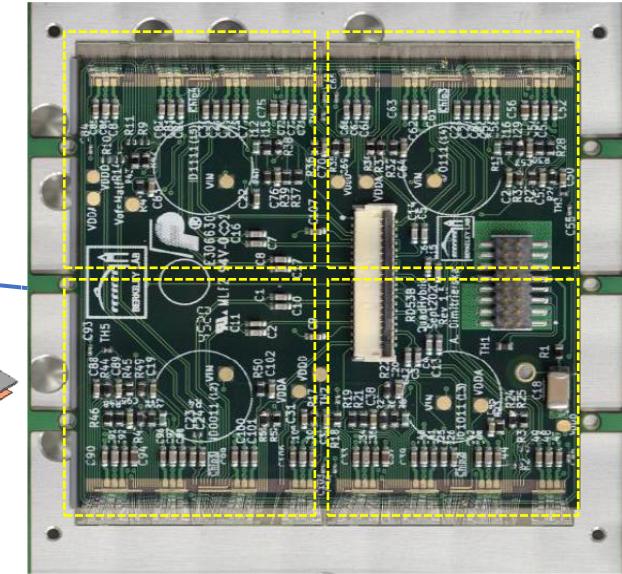
- **Outer System**
 - 3 layers of flat staves and inclined rings
 - **6816 planar quad modules** with 150um thick sensor + 150um thick ASIC (50x50 μm^2 pixel size)

Produce ~11,000 modules including yield
- **Inner System**
 - 2 layer of flat staves and rings
 - L0 : **1188 3D single modules** (25x100 μm^2 for flat and 50x50 μm^2 for endcap)
 - L1 : **1200 planar quad modules** with 100um thick sensor +150um thick ASIC (50x50 μm^2 pixel size)

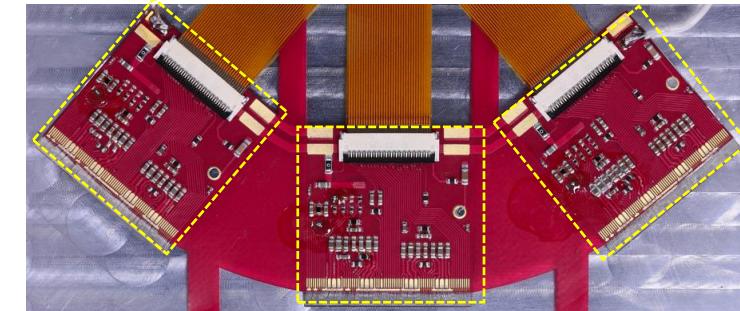
Produce ~2,000 modules for each type including yield



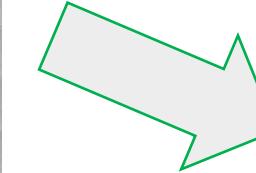
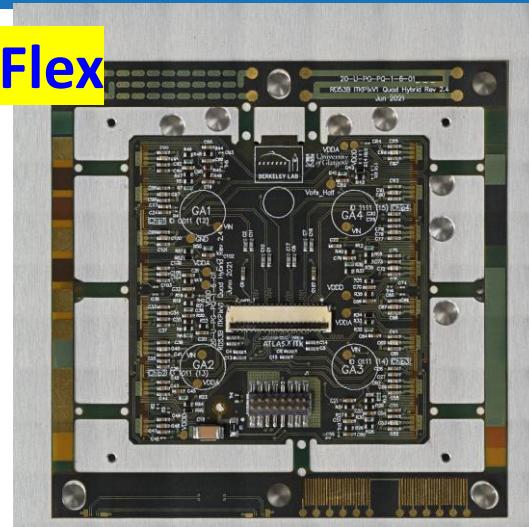
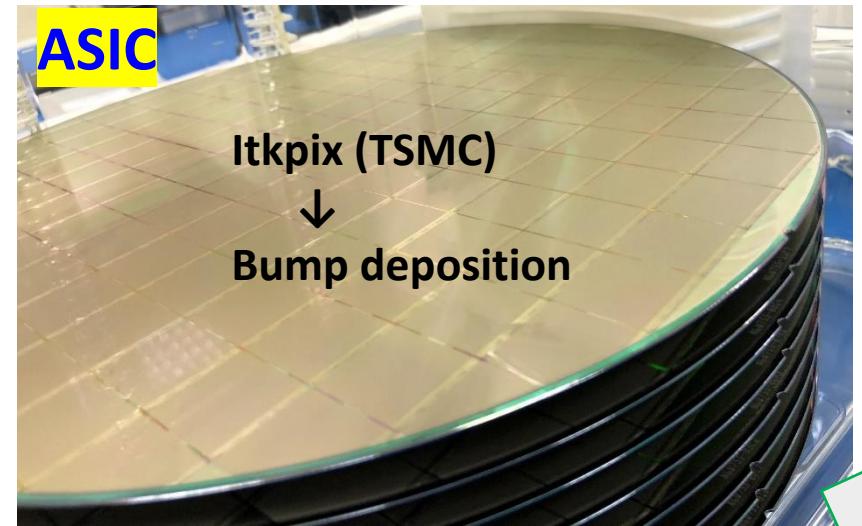
Layer 1-4
Planar : Quad module (single sensor)



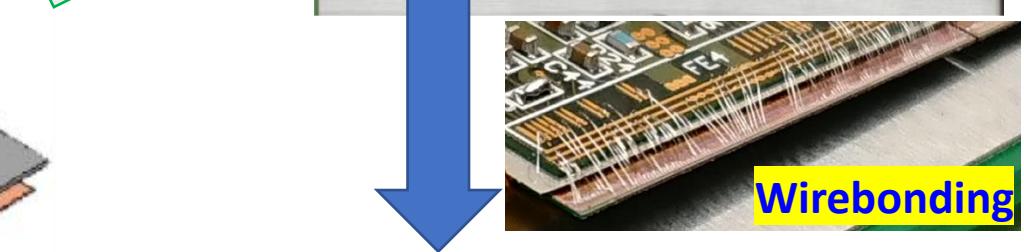
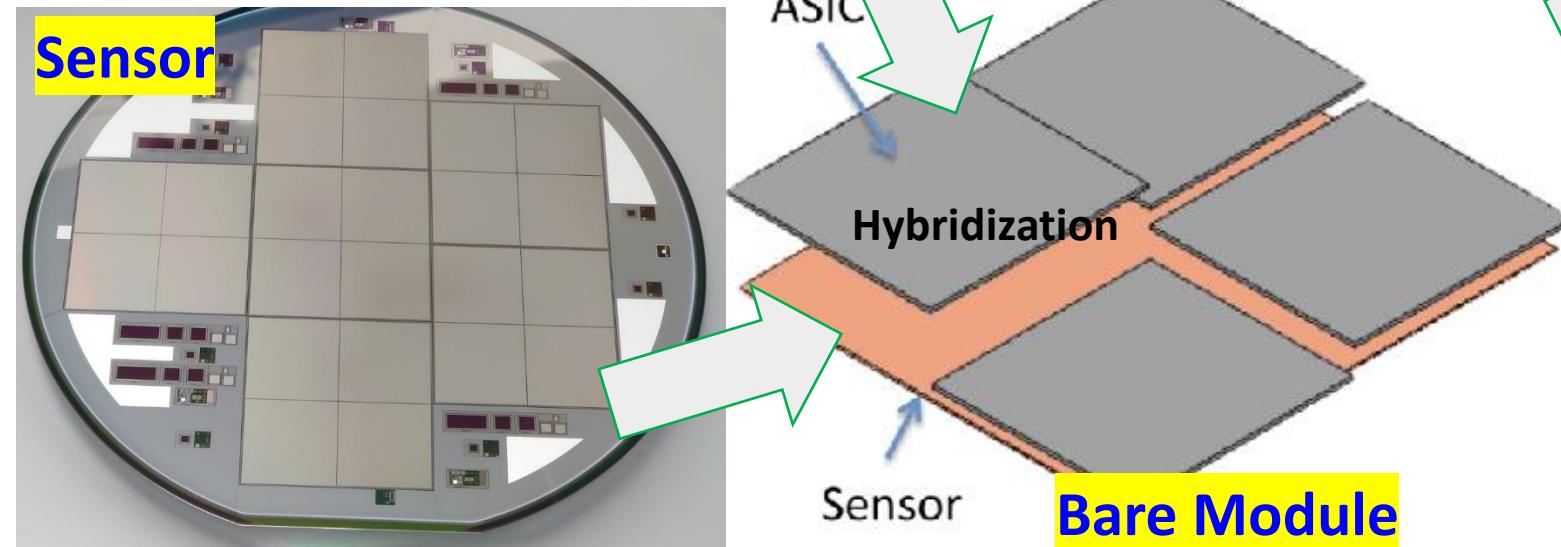
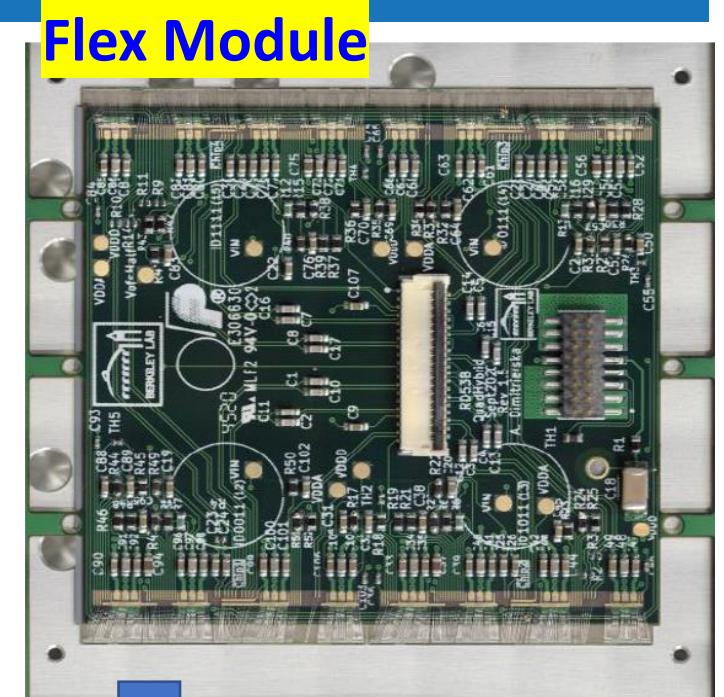
Layer 0
3D : Single module (Triplet with one PCB)



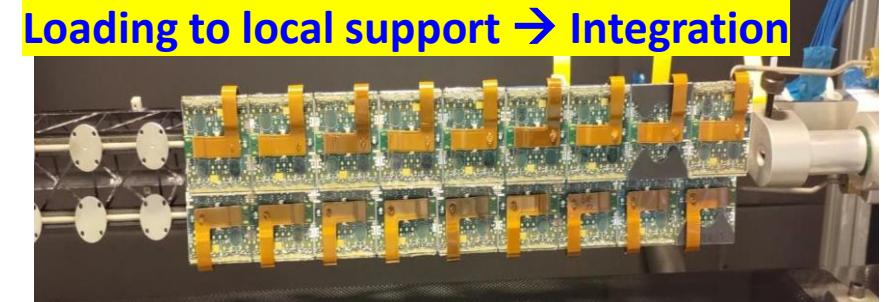
Production flow



Assembly



Loading to local support → Integration

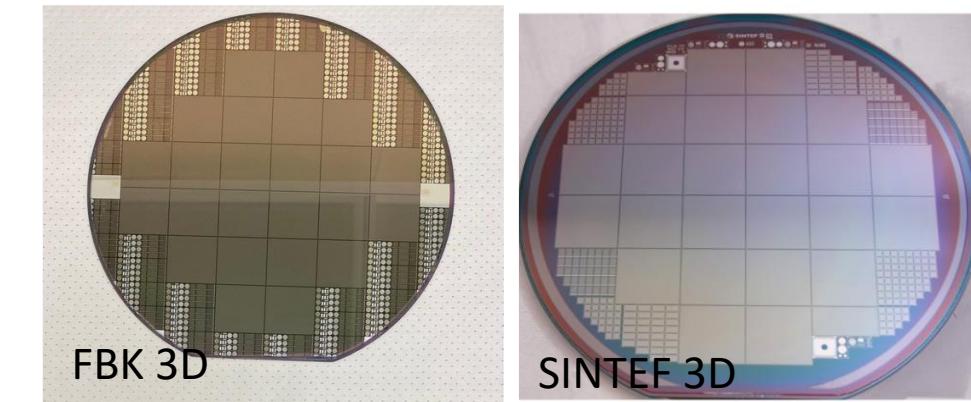
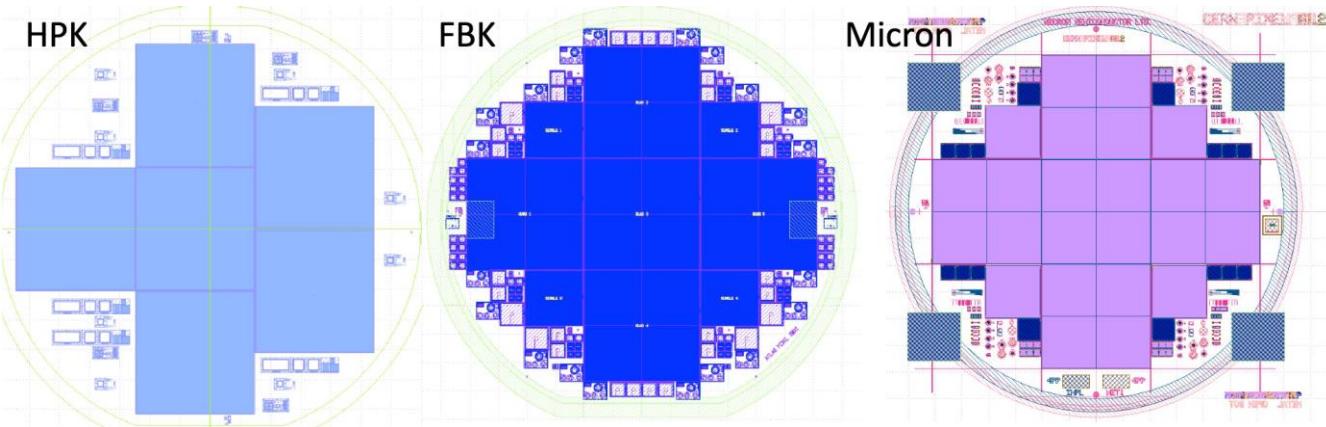
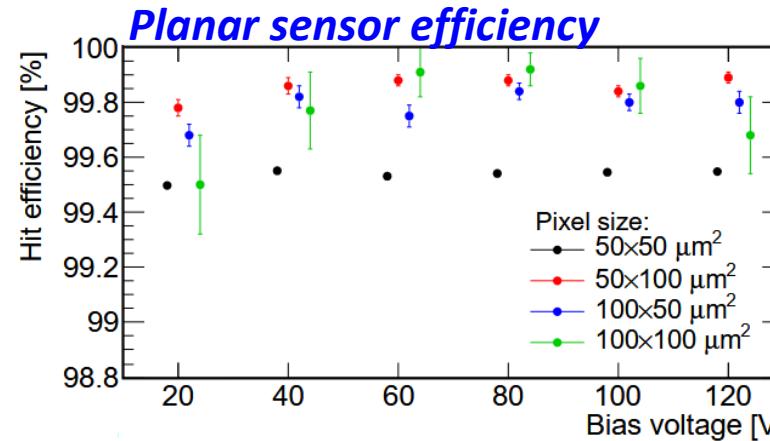
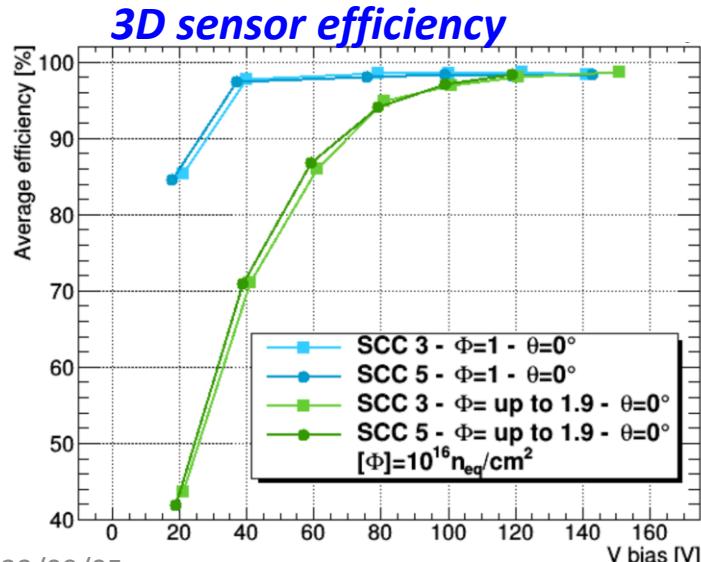


- **Pre-Production (10% of install amount) finished in 2022.**

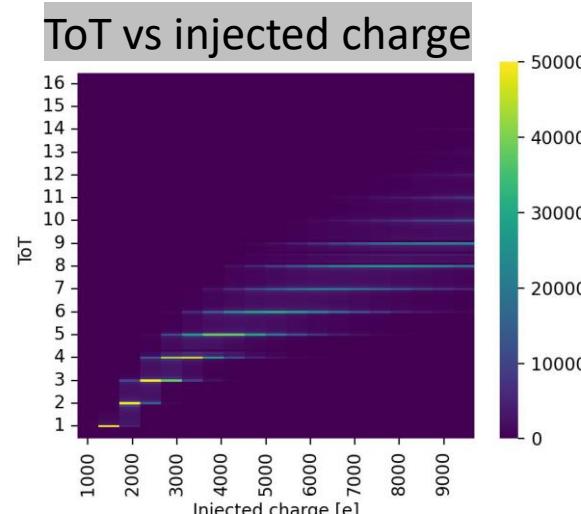
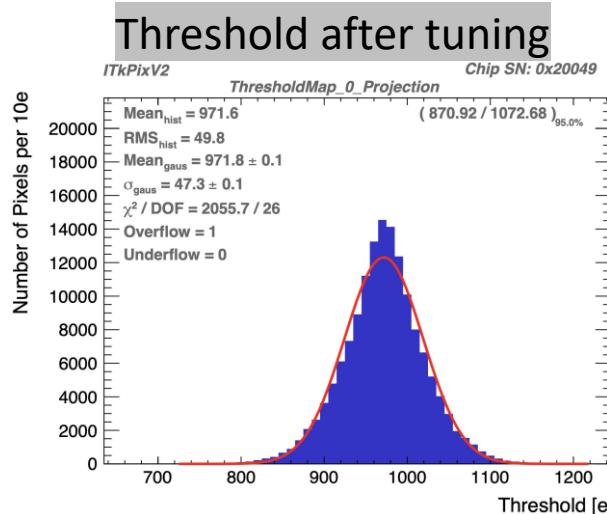
- Planar : 845 quad sensors from HPK(150um), FBK(100um) and Micron(150um+100um).
- 3D : 210 single sensors from FBK($50 \times 50 \mu\text{m}^2 + 25 \times 100 \mu\text{m}^2$) and SINTEF($50 \times 50 \mu\text{m}^2$) delivered

- **Evaluation of quality (QC/QA)**

- Basic performance measured.
- Several Hybridization module tested at the testbeam.
- Qualification for Production order almost completed. (some of Production order placed.)

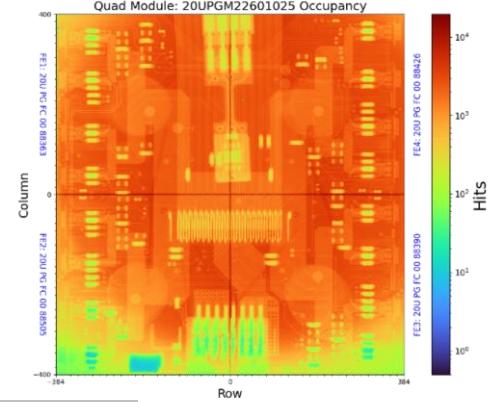


- Prototype chips RD53A and ITkpix-v1 were validated and used as prototype program
 - 65nm TSMC process, 4x1.28Gbps data link, differential comparator, ~50e ENC, 500Mrad TID tolerance
- ATLAS approved final FE-chip (ITkpix-v2) submission on 17th March 2023
 - First delivery of 20 wafers (engineering run) 26th June.
 - Production of 100 wafers released when engineering run delivered (with risk but to mitigate schedule)
- First verification of new chip and preparation for chip testing:
 - In the first verification, basic functions are working as expected. Detailed checks are ongoing.
 - Reduced time for wafer level probing from 48hrs->24hrs (5 wafer/week/site)

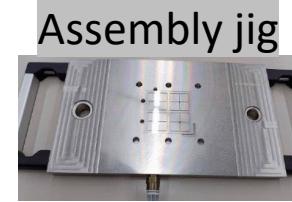
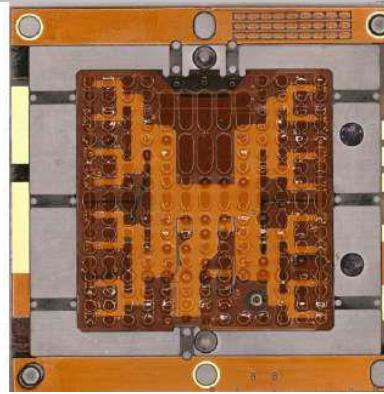


- Hybridization (Flip-chip)
 - Qualify bump-strength after thermal cycle
 - Design validated by prototype, follow-up during pre-production
 - Cross check with FEA and share stress measurement
- Flex PCB
 - Common design for Layer 1-4 (all Quad)
 - Triplet hybrid for Layer 0.
 - Optimized Copper thickness :
 - Low Cu required by thermal stress
 - High Cu required low power consumption
- Module assembly and readout test
 - Exercise production across module sites
 - Site-qualification
 - Extensive module QC
 - Electrical readout, metrology, bump-stress, operation at low temperature

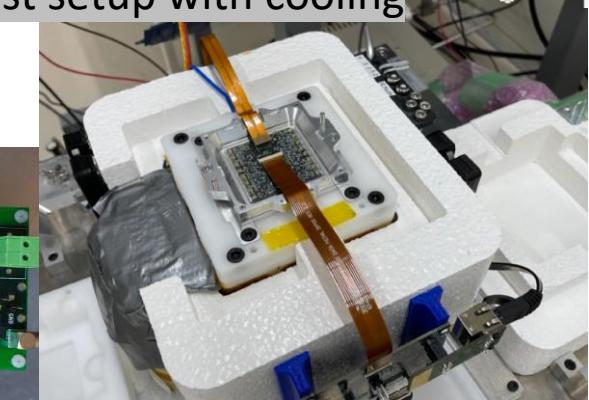
Xray source



Glue pattern for Flex



Test setup with cooling



Test setup

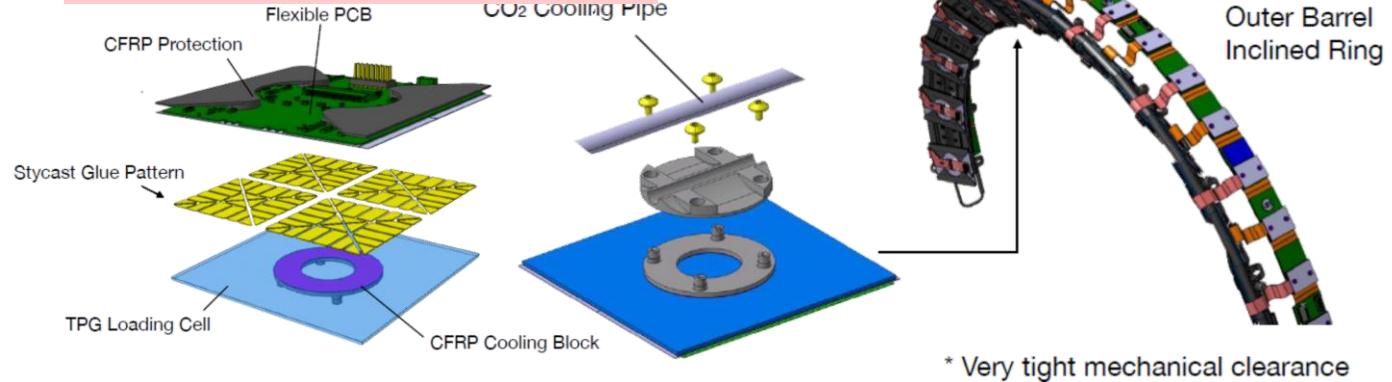


Local support & Mechanical prototype

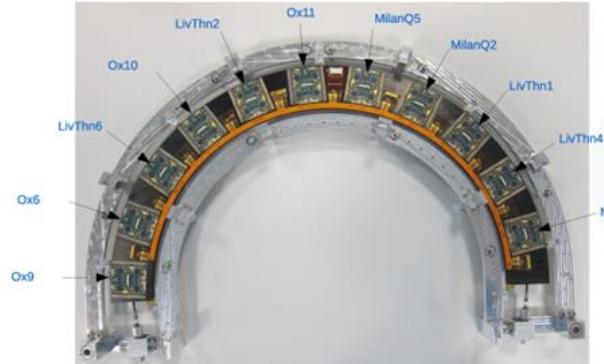
• Local support

- stable low-mass support
- Critical element is interface to cooling pipe

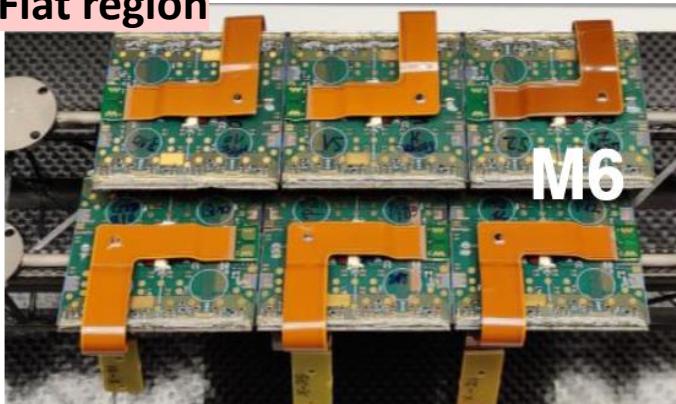
Outer Barrel Cooling interface



Inclined Ring



Flat region



• Mechanical prototypes

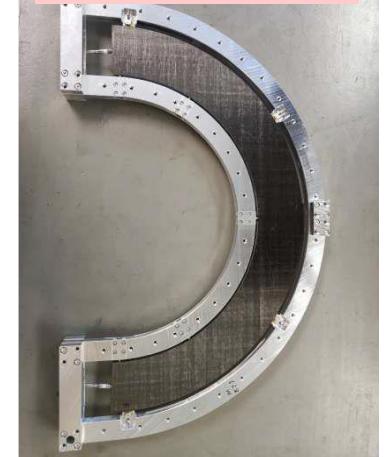
- Bare local support pre-production for outer barrel and outer endcap on-going
- Inner system pre-production about to start

Details in Gabriele's [talk](#)

Steven's [talk](#)



Endcap half-ring



Inner system coupled ring



Outer Barrel inclined half-ring

Conclusion

