

ITk readout with FELIX

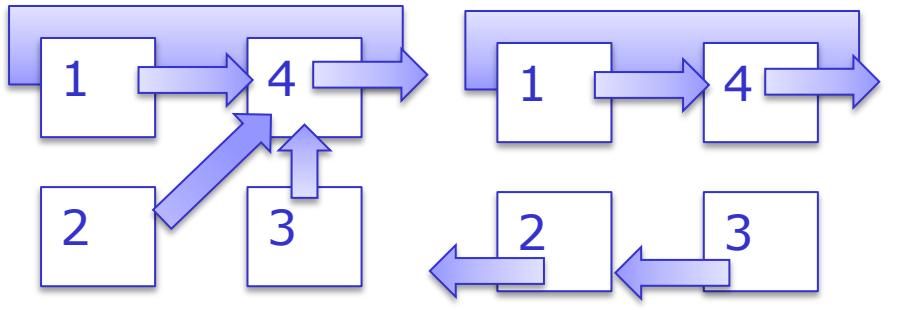
A. Paramonov
on behalf of many people

Outline

- Pixel readout with FELIX:
 - CERN SR1 & B161
 - V. Dao, L. Flores, H. Joos, S. Kuehn, B. Moser, I. Siral, C. Solans, B. Vormwald, V. Tsiskaridze
 - Bern
 - D. Dal Santo and others
 - Wuppertal
 - M. Wensing, W. Wagner
 - Göttingen
 - A. Skaf, M. Drescher, W. Alkakhi, J.G. Knetter, A. Quadt
 - LBNL
 - T. Heim, A. Rastogi, S. Pagan Griso
 - SLAC
 - B. Bullard, R. Hyneman, Su Dong , M. Wittgen
 - ANL
 - M. Trovato, R. Luz, A. Paramonov, J. Zhang
- Strip readout with FELIX
 - Combined effort
 - A. Toldaiev, E. Le Boulicaut, D. Trischuk, Z. Tao, B. Gallop, M. Warren

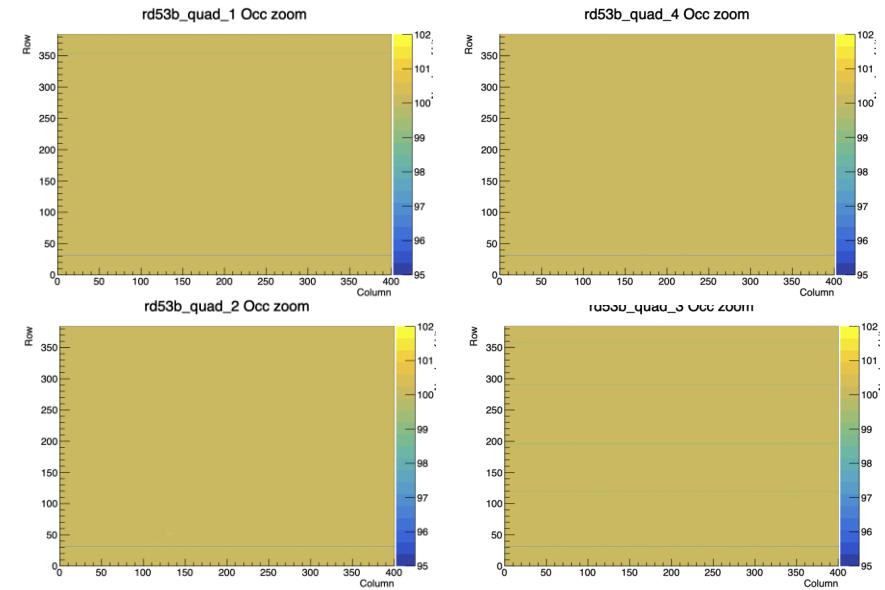
ITk Pixel: CERN B161

- Hardware
 - VLDB+
 - ITKPix v1 digital quad
 - FLX712
- FW: Felix Phase-II RM5 14-11-2022
- Software: ITK-FELIX-SW for ITKPix
- Status
 - Development before testing in SR1
 - Fully working digital, analog, CML, and threshold scans
 - **Data demultiplexing with software**

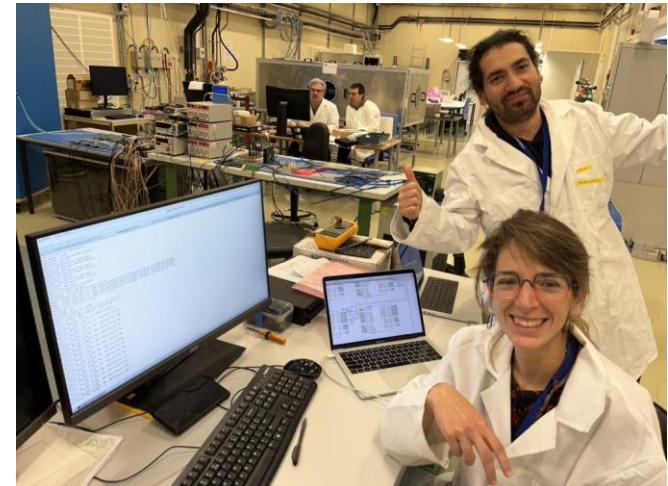


25% link occupancy
(1,2,3-to-4) configuration

50% link occupancy
(3-to-2, 1-to-4) configuration

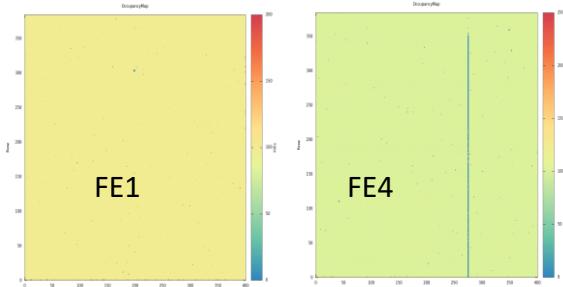


Link sharing works. Sensitive chip-to chip links. Chip-to-FELIX connections is OK.

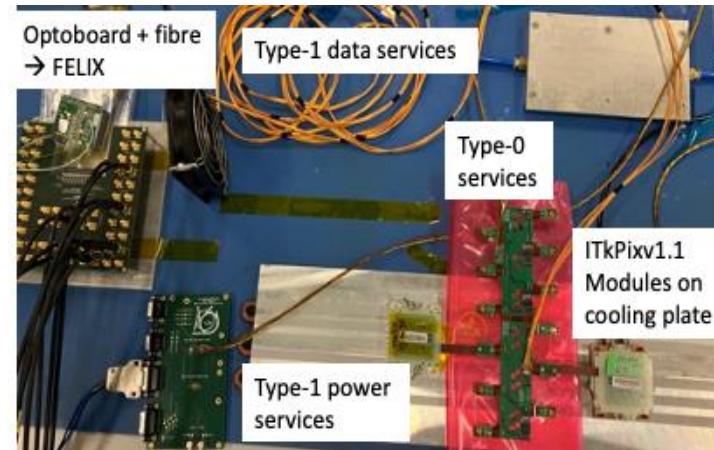
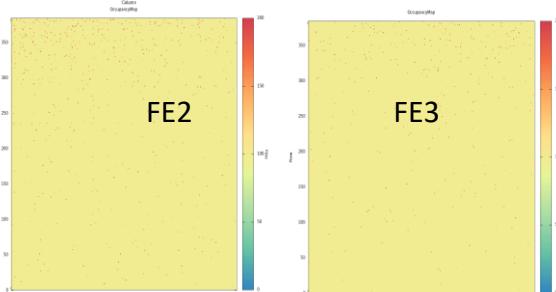
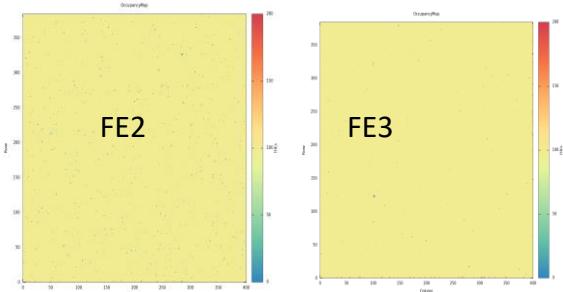


ITk Pixel: SR1

- Multi-module testing with ITkpixv1.1 quad modules in serial powering chains, including electrical (1.28 Gbps) and optical transmission
 - Qualification of services for data transmission
 - Qualification of data merging in serial-powering chain
- Complications with FELIX and ITkpixv1.1
 - No software available which can run all scans and works in data merging
 - Validation of detector prototype components delayed by non-availability of required FELIX readout.



Analog Scan result in data merging 4-to-1 using FELIX-client itk-daq-sw with software trigger for quad module with flex v.2.4



Setup with ITkPixv1.1 quad modules in Pixel Outer Barrel services chain in SR1

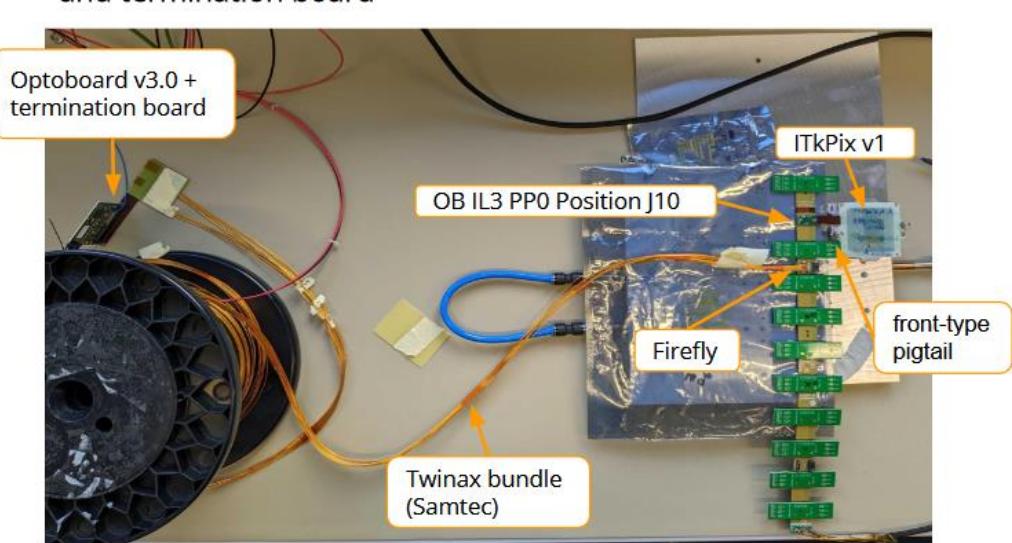
Analog Scan result in data merging 2-to-2 using Felixcore itk-daq-sw with software trigger, for digital quad module with flex v.2.4

Requirements for Loaded Local Supports and Integration

- ONE scan software that ...
 - ... implements **all scans** relevant for Loaded Local Support QC and Integration QC:
 - Analog readback, register read
 - Digital/analog scan
 - Threshold/noise scan
 - ToT measurement
 - Cross-talk measurements
 - Disconnected bump bond scan
 - Noise occupancy measurement
 - Selftrigger scan
 - ... is **compatible with FELIX**
 - ... runs **reasonably efficient multiple-modules** at the same time ($O(20)$ modules simultaneously). For integration $O(500)$ modules at the same time.
 - ... is **qualified** against single module tests, i.e. makes comparisons possible
 - ... has the **potential to scale** to system sizes of a real detector (also wrt. DAQ environment)
- Timescale:
 - Loaded Local Support **pre-production about to start** (LLS FDR just over)
 - Test setups being built and commissioned now (site qualification for pre-production)
 - Testing of first modules expected at 10 institutes **early summer 2023**
 - Readout for surface testing during **integration required from Q3/2024**

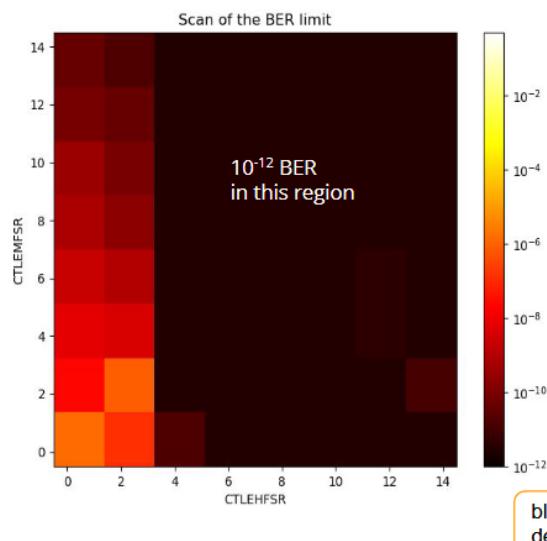
ITk Pixel: Bern

- Test of opto-boards and readout chains
- GBCR parameter scans

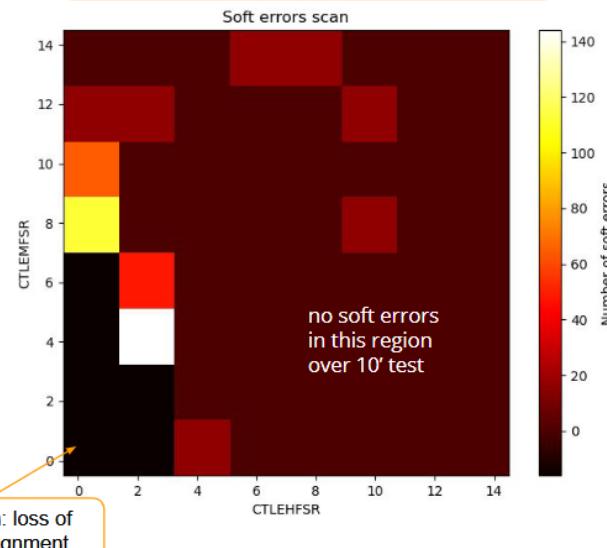


Molex twinax bundle was also validated with ITkPix v1.1

PRBS7 test



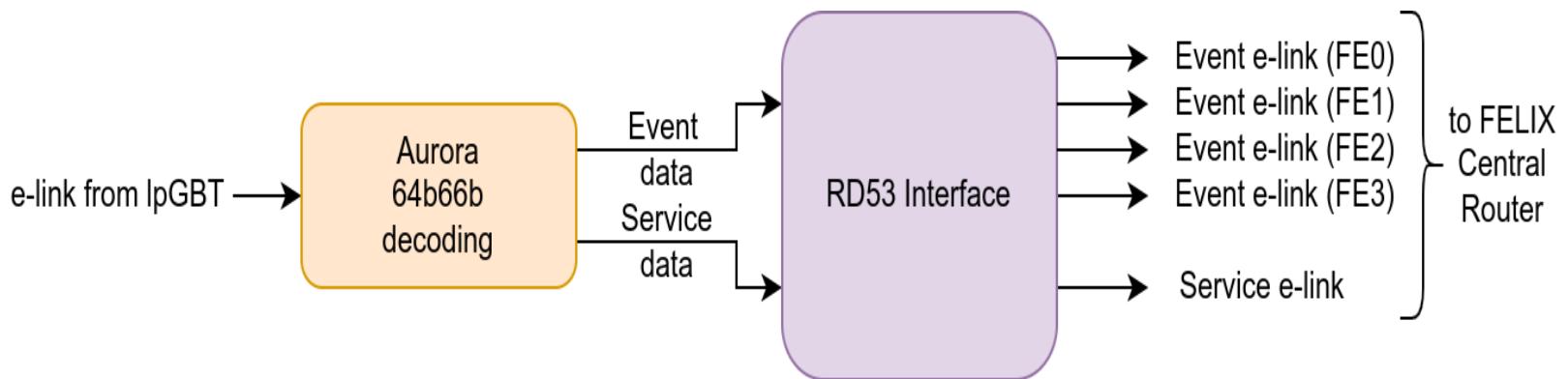
New FELIX feature: *soft error counter*
- count errors in control blocks of
64b/66b ITkPix signal



64b/66b test

ITk Pixel: Wuppertal

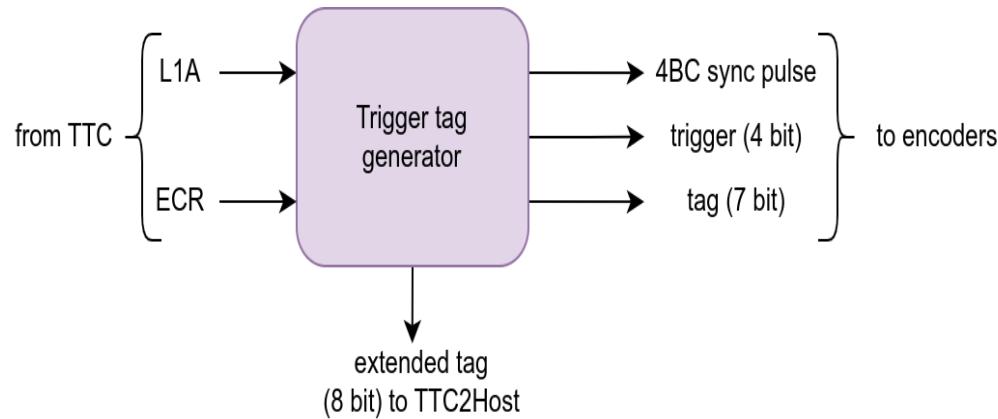
- Event from up to 4 front-end chips travel through one 64b/66b Aurora link and can be splitted inside FELIX based on the chip ID bits into independent data streams:
- Introduction of more “virtual” e-links:



- If link sharing is disabled data will always be routed to FE0. Service e-link is shared between all front-ends.
- First firmware (4 channel IpGBT) is available on [CERNBox](#).
- Untested, due to lack of hardware. At the moment working on a simulation test bench for verification.

ITk Pixel: Wuppertal

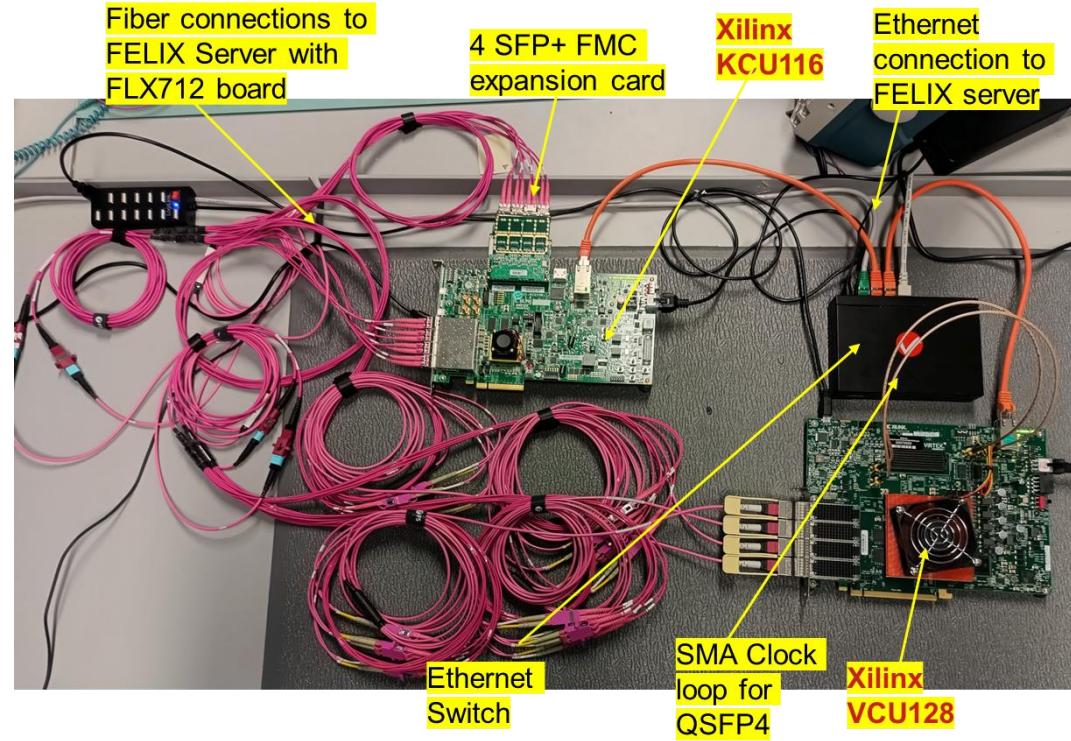
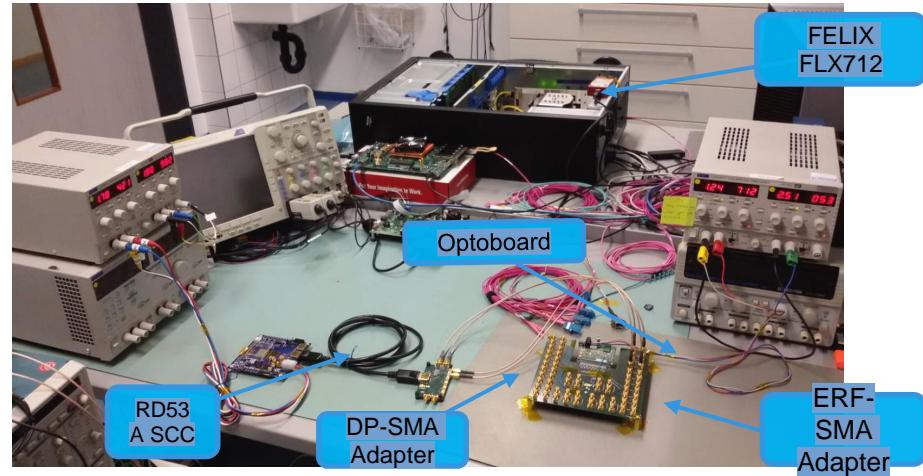
- Trigger tag generation in FELIX for pp data-taking:



- Tag generation for Pixel:
 - 32 (RD53A) or 53 (ITkPixV1) base tags, assigned round-robin with reusing tags for “orthogonal” triggers.
 - Extended tag for TTC2Host is generated by extending the base-tag with 2 bits for the triggered BC number (00: first BC, 01: second BC, 10: third BC, 11: fourth BC)
- Tag generation for Strips (to be discussed):
 - 128 base tags, with every triggered 4BC block gets new tag, no re-using of tags like in Pixel
 - TTC2Host publishes the base tag

ITk Pixel: Göttingen

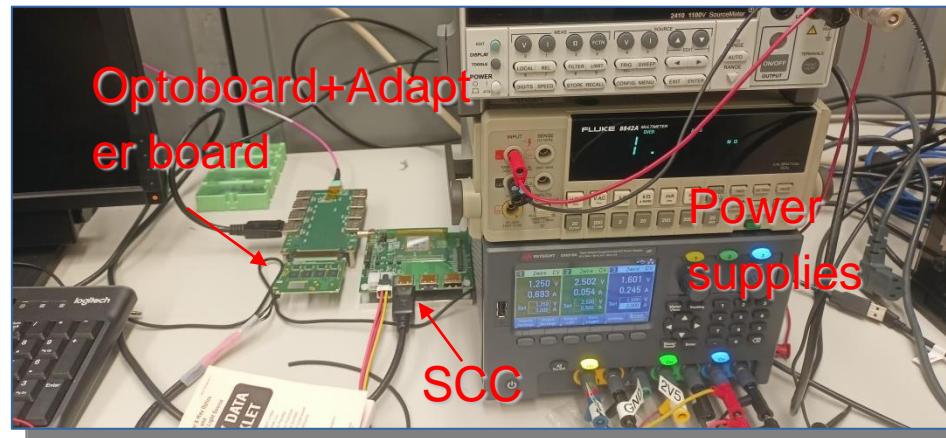
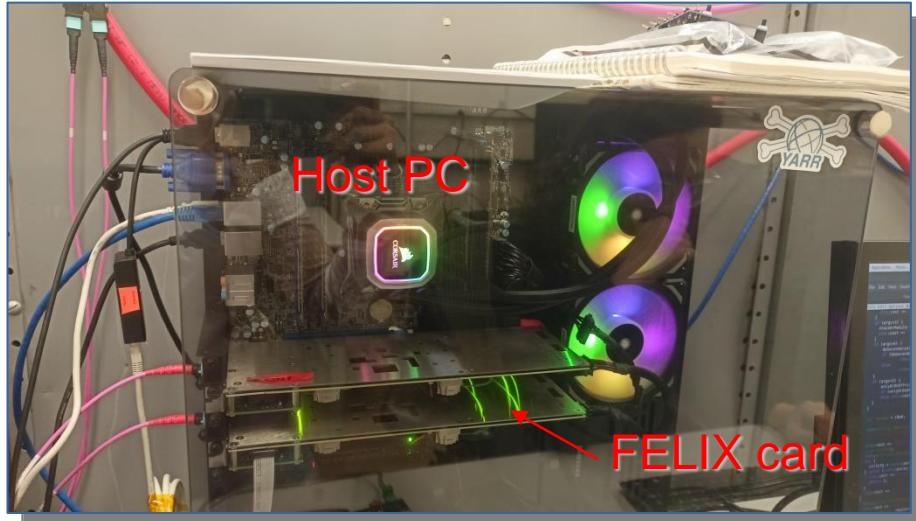
- Yarr-FELIX-optoboard Read-out chain
 - Netio
 - Netio-next



- Felix stress test with front-end emulation
- (24) IpGBT ASICs and (168/42) RD53A SCCs/QMs

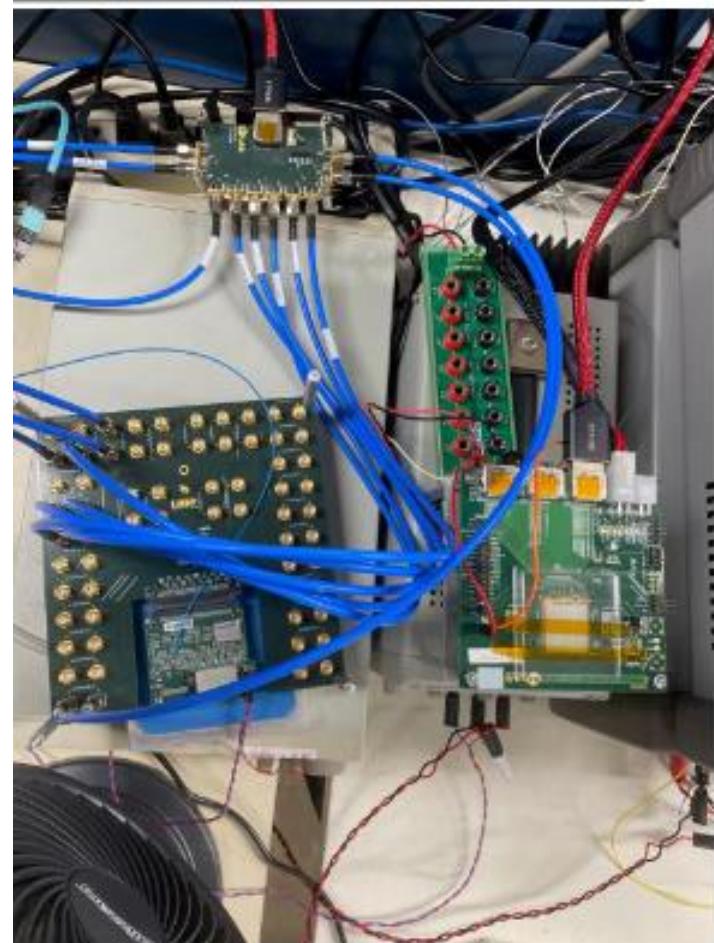
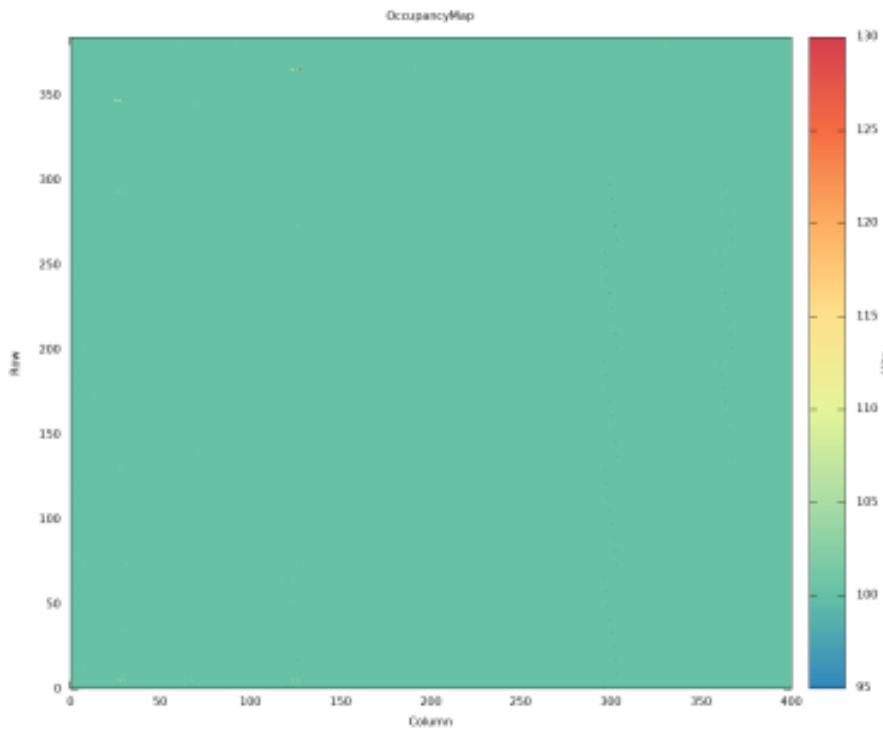
ITk Pixel: LBNL

- Observed issues in communications between YARR and felixcore:
 - around 5% of packets are lost. Also, last packet seen in felixcore ~4 seconds later after YARR finished sending all commands due to network buffering. Hence, many empty mask stages (StdDataLoop wait time ~ 1 sec).
 - Data received around 0.5 seconds later in every mask stage initially, but then becomes asynchronous due to the network latencies (especially towards last few mask stages).
- Solution: MR [YARR!615](#): Aggregate the command packets from YARR (NetioTxCore) to send longer messages.



ITk Pixel: SLAC

- Scans with an ITkPix SCC and an optoboard
- Debugging with a quad module is in progress



ITk Pixel: ANL

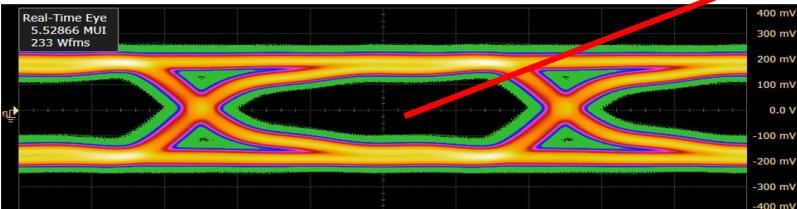
- September 2022 – digital scans of ITkPix SCC via VLDB+ work well.
- Late October 2022 – received optoboard 2.1 from SLAC.
- Early Nov 2022 – fixed a bug in IpGBT firmware. Later in November performed scans with optoboard and ITkPix quad module. See FLXUSERS-589
- Investigated bit errors in 64b/66b bitstream (ITkPix 1.28 Gb/s output)
 - The 1nF DC-blocking caps are a bit small to prevent baseline wander (see below)
- Added counters for 64b/66b errors

GBCR output for 64b/66b

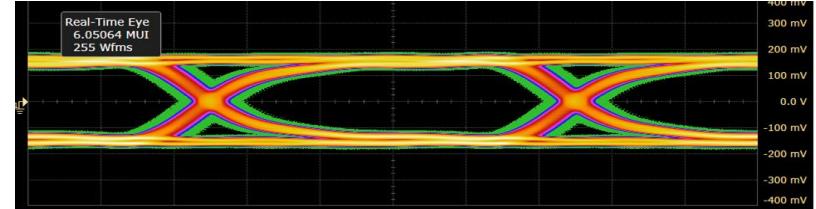


64b66b

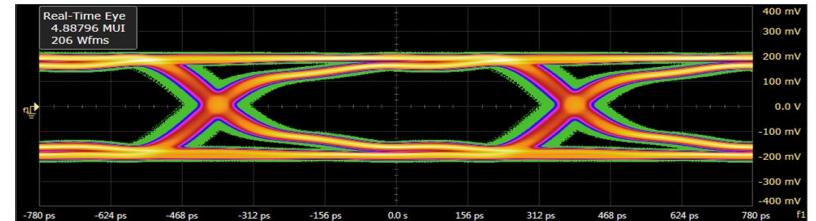
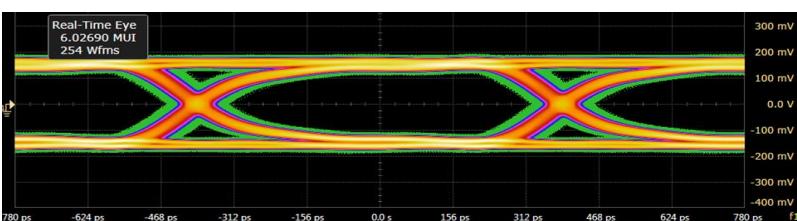
1 nF



PRBS7

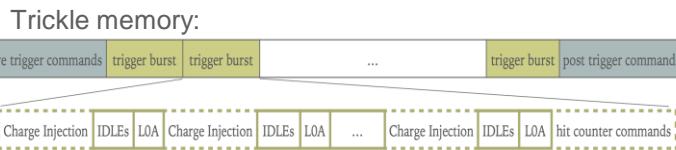
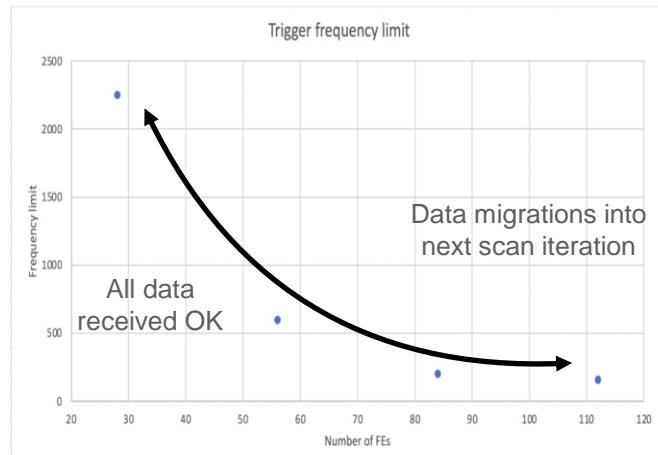
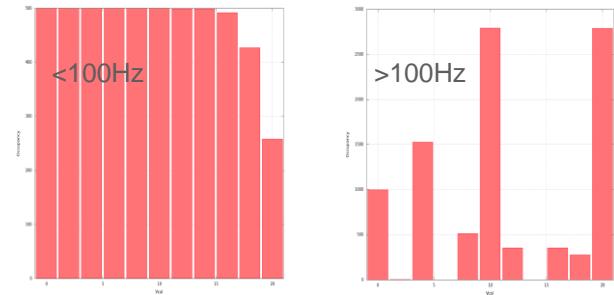
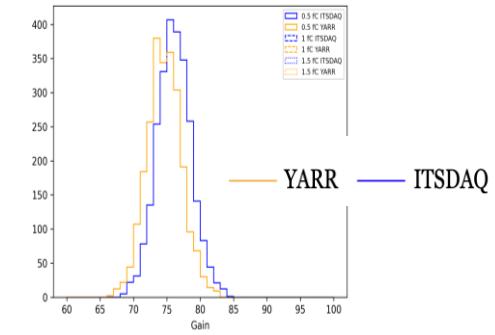


22 nF



ITk Strips SR1

- By now: [ITSDAQ calibration results](#) have been reproduced with YARR+FELIX including scans on two opposing stave sides
- The [SW trigger limit](#) and data migration in YARR scans on multiple staves at trigger frequency > **100 Hz** ("SW trigger" = 1 netio message with trigger command sequences for all FEs)
- Data migration in YARR scans — when large spikes of data are buffered — fixed in the [feedback-based readout](#)
- SW trigger limitation (work in progress):
 - ▶ Broadcast elink ([FLXUSERS-587](#)) → trigger frequency of 1 FE scans $\sim=$ **10-15 kHz**
 - ▶ Trickle memory triggers ([\[1\]](#) [\[2\]](#)) → bursts of **2 kHz-1MHz** triggers (\sim 1000 triggers per burst @ 1MHz)
 - ▶ Long-term solution: FW trigger emulator ([FLXUSERS-586](#))



ITk Strips

- Future plans:
 - Readout with trigger rates of 1 MHz to saturate the links
 - Migration to felix-star
 - Additional FW features as in <https://its.cern.ch/jira/browse/FLXUSERS-418>

Backup

ITK readout with FELIX



CERN EP-ADE-TK



Setup in b161

- Hardware

- VLDB+, FMC to SMA, SMA to DP, DP to pigtail, power to pigtail
- ITKpix v1 digital quad with 3 working front-ends
- FELIX Phase-1

- Firmware

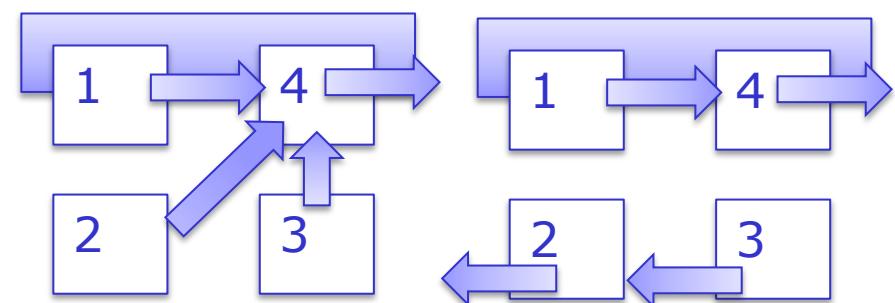
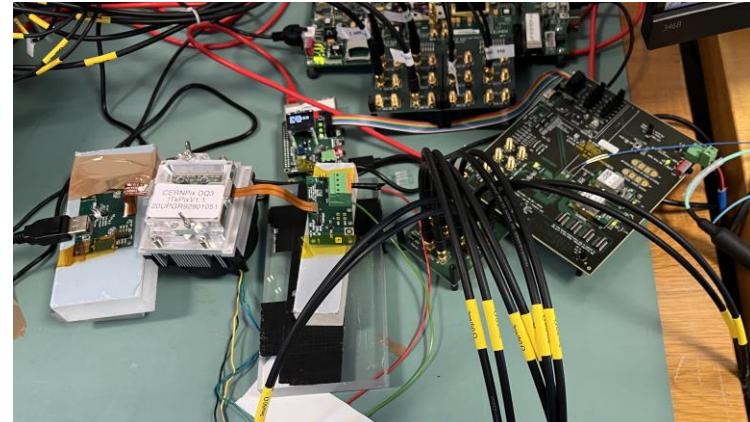
- Felix Phase-II RM5 14-11-2022

- Software

- ITK-FELIX-SW for ITKpix

- Status

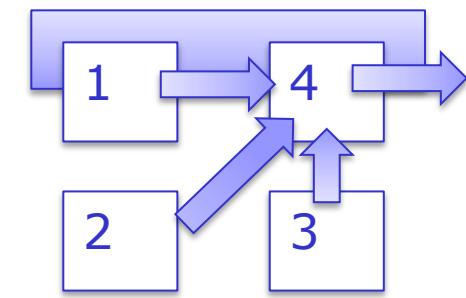
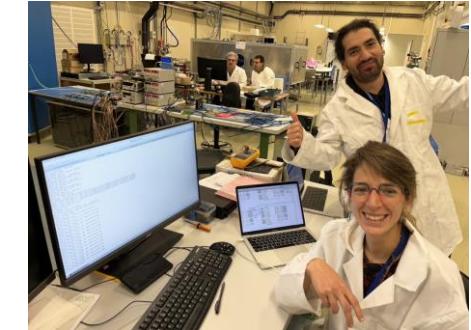
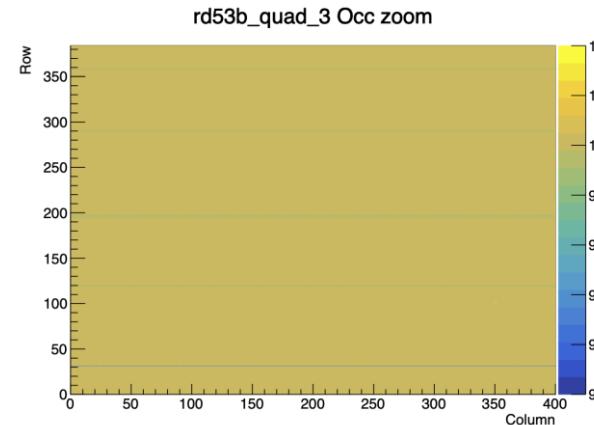
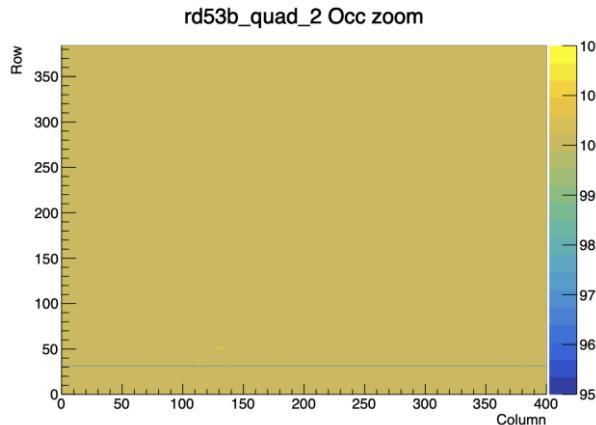
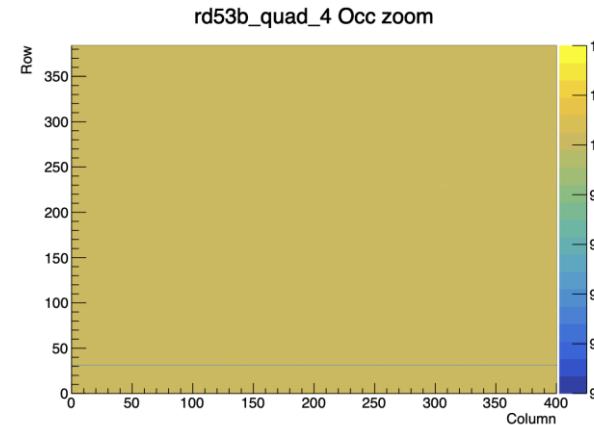
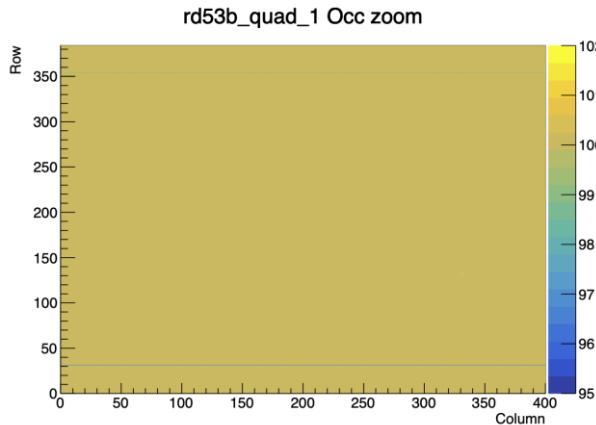
- Development before testing in SR1
- Fully working digital, analog, CML, and threshold scans
- Data demultiplexing at software level
- Developed tool to convert config files to merging
- Not using firmware trigger



25% link occupancy
(1,2,3-to-4) configuration

50% link occupancy
(3-to-2, 1-to-4) configuration

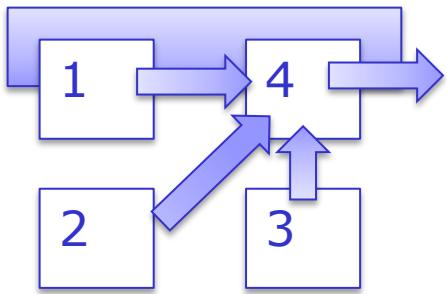
Data merging results in SR1



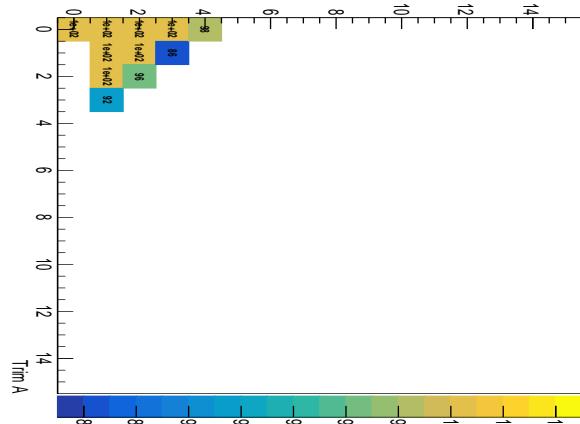
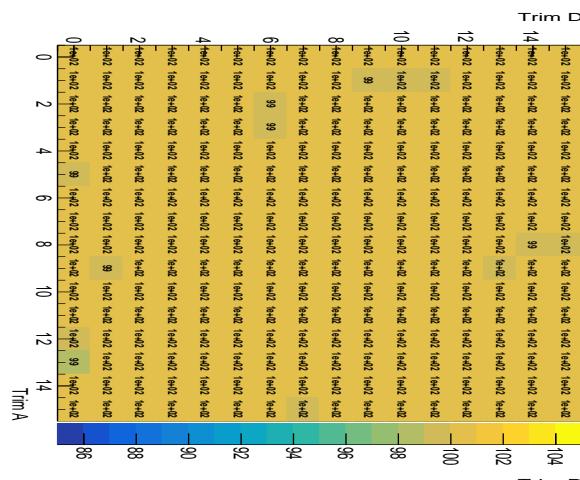
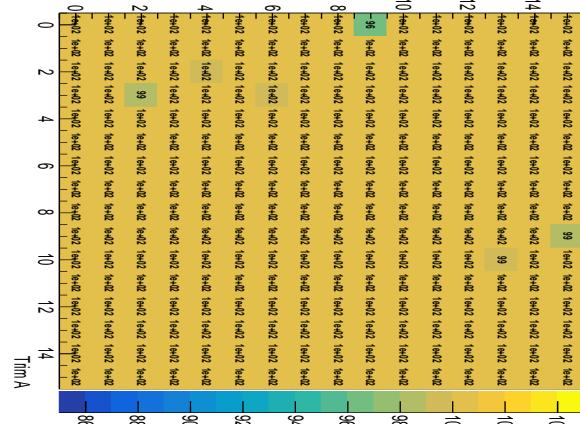
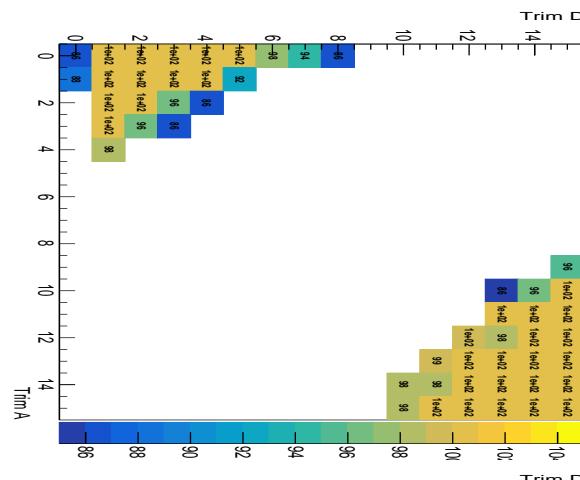
25% link occupancy
(4-to-1) configuration

- Evaluated different mask sequences and triggers per event
- Sweet spot seems to be masking (8x4) x 20 freq and 20 triggers
- Results fully reproducible in SR1

Analog and Digital trim values

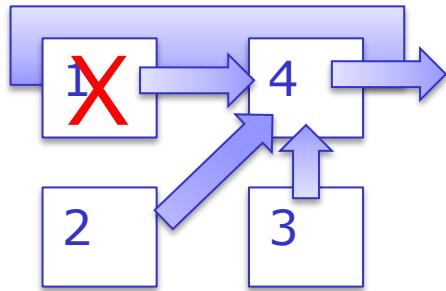


25% link occupancy
(1,2,3-to-4) configuration
Carried out in SR1

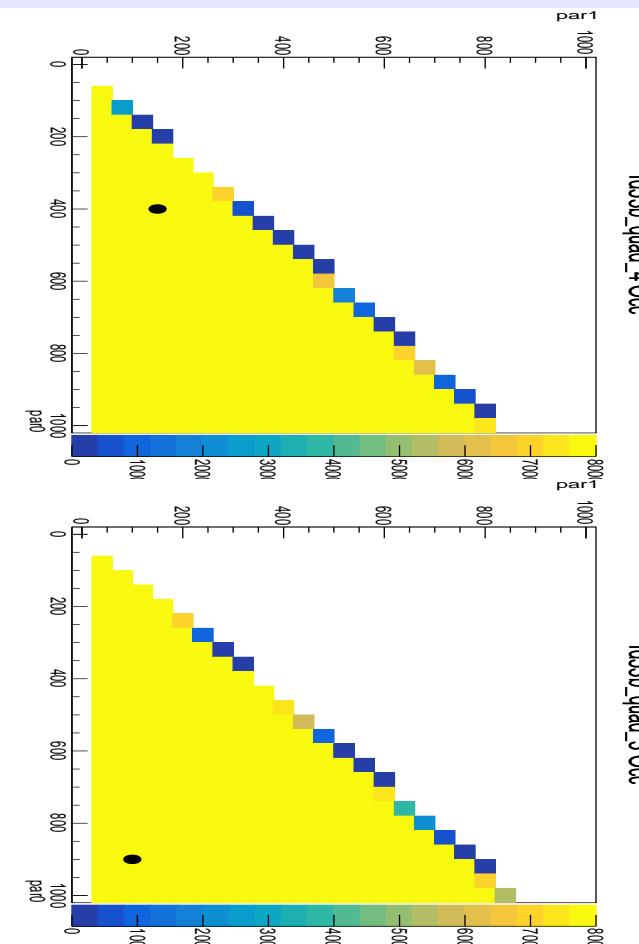
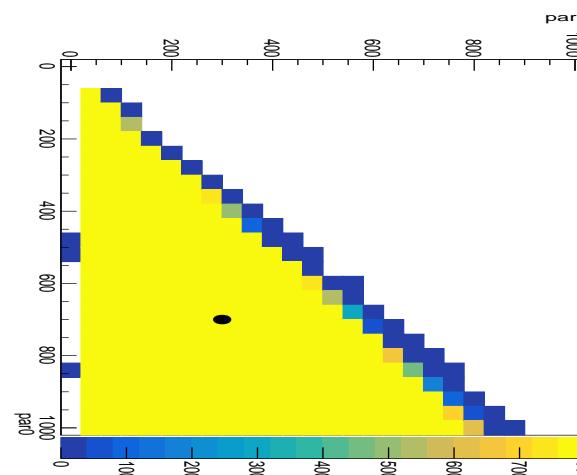


- Some values for TrimA/TrimD are not good for data transmission

CML bias scan



25% link occupancy
 (1,2,3-to-4) configuration
 Measured in b161
 One chip not wire-bonded

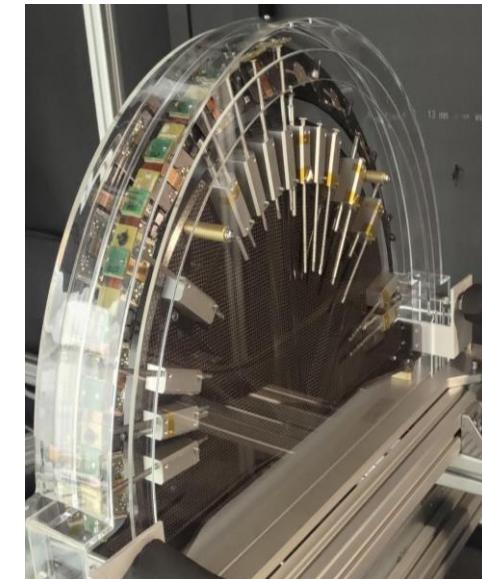
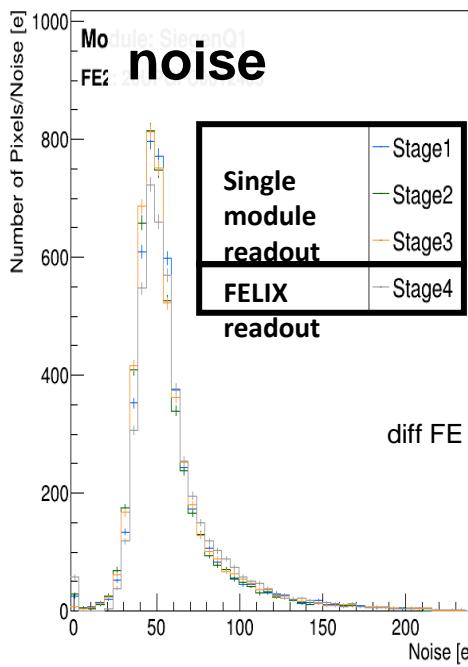
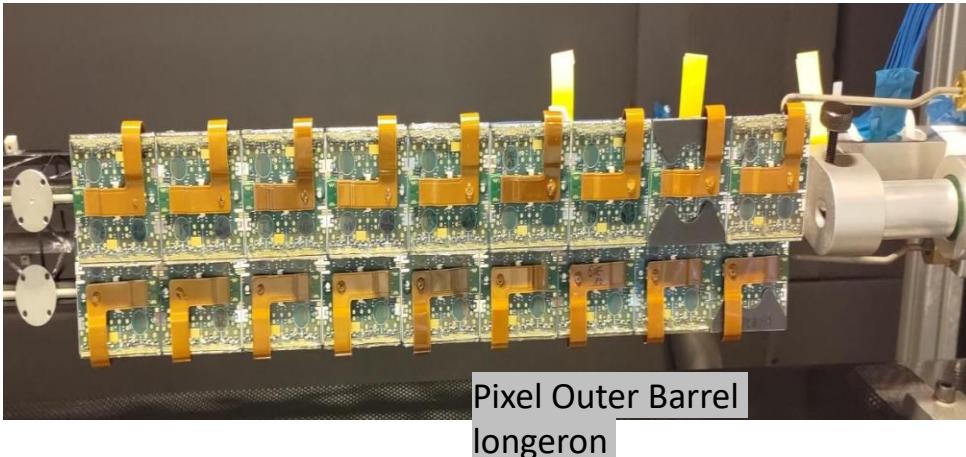


- Scan of CML_BIAS_2 (reg 96) vs CML_BIAS_1 (reg 5)
- Can identify settings outside of operational range

Status of RD53A Readout for the SR1 Demonstrators

- Multi-module testing in serial powering chains including electrical and optical transmission chain (IpGBT, GBCR)

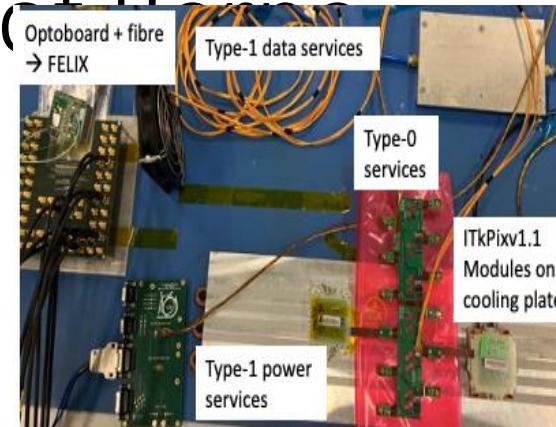
- Complications of RD53A:
 - Three analog frontend (lin/diff/sync)
 - Not all well supported
- Using ITk Pixel specific FELIX FW with felixcore at 1.28 Gbps
- Three scan softwares in use depending on the application (cherry picking of the software used for different scans/front-ends)
 - Standard scans for lin/diff
 - Source scans for lin/diff/sync
 - Disconnected bump-bond scan for sync
- Huge effort of a committed team to collect all relevant data for the Loaded Local Support FDR ([Results](#))



Pixel Outer Barrel inclined half-ring

Status of Tests with ITkPixV1.1 modules in SR1 and at University of Berne

- Multi-module testing with ITkpixv1.1 quad modules in serial powering chains, including electrical and optical transmission chain (IpGBT, GBCR) at 1.28 Gbps
 - Qualification of services for data transmission
 - Qualification of data merging in serial-powering chain
 - Investigation of features seen with RD53A demonstrators
- Complications with FELIX and ITkpixv1.1
 - No software available which can run all scans (see later page) and works in data merging
 - Validation of detector prototype components delayed by non-availability of required FELIX readout.



Setup with ITkPixv1.1 quad modules in Pixel Outer Barrel services chain in SR1

STATUS AND RESULTS:

1. Data transmission chain tests with BERT scans ([@Berne](#))
 - Verification of data transmission quality running prbs pattern scans and digital scans. Configuration of FEes with YARR branch from Marco (devel_itkpix_felixNetio) modified by V. Tsiskaridze to work with software triggering.
 - Using new feature of soft error counter to count errors in control blocks of 64b/66b ITkPix signal
2. Testing multiple modules in data merging ([@SR1](#))
 - Pixel Outer Barrel Layer 2 modules have 2 e-links per module, data of other two FEes merged (FE3->FE2, FE1->FE4 = 2-to-2), Layer 3/4 modules have one e-link (merging of 4FEes in one (FE1,2,3->FE4) = 4-to-1)
 - GBCR settings based on optimized values from Berne
 - Results in [system test meeting](#) and ITk Week services session in presentations by Daniele Dal Santo and Susanne Kuehn

Status of Tests with ITkPixV1.1 modules in SR1

3. Tests performed with the **ITK-FELIX-SW** software developed by C. Solans, V. Dao, I. Siral et al.

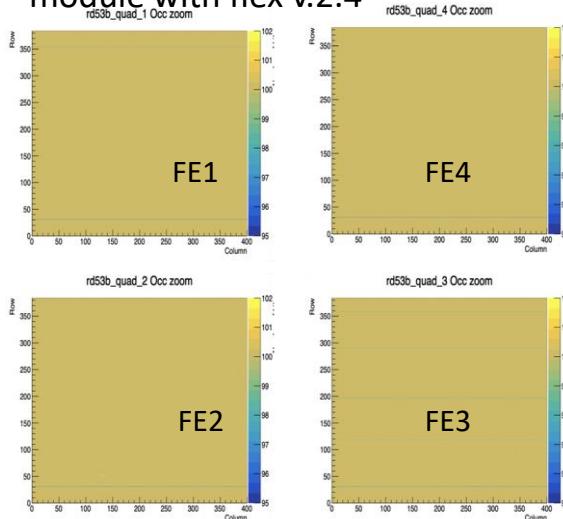
- It has digital, analog, cml and threshold scans implemented and runs on Felixcore
- Data multiplexing at software level
- **It doesn't use firmware trigger**

Results in OB services

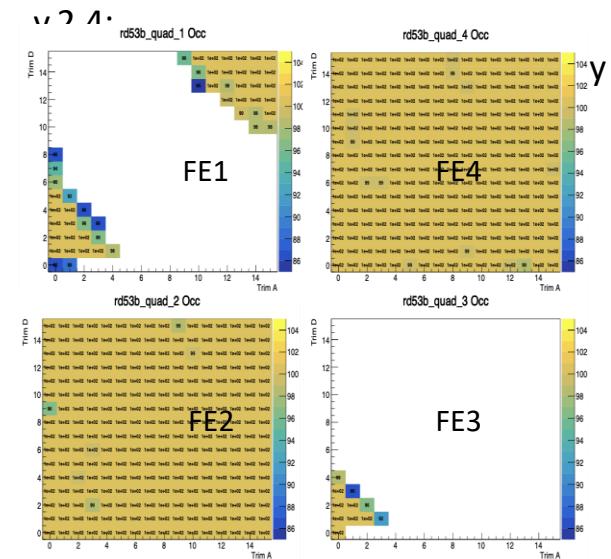
chain setup:

- Tuning of FE parameters required due to known phase issues in ITkpixv1.1 FE chip to get scans stably running.
- Testes dependency on masking stage, frequency and injections: better success with 50 triggers and smaller mask with high repetition [related to chip activity?]
- Digital scan is “almost”

Digital Scan result in data merging 4-to-1 using Felixcore ITK-FELIX-SW with software trigger for quad module with flex v.2.4



FE parameter optimization scan for FEs in data merging 2-to-2 using Felixcore ITK-FELIX-SW with software trigger for quad module with flex v.2.4.



Some values for TrimA/TrimD are not good for data transmission → under investigation

Status of Tests with ITkPixV1.1 modules in SR1

3. Tests performed with the software further developed by V. Tsiskaridze

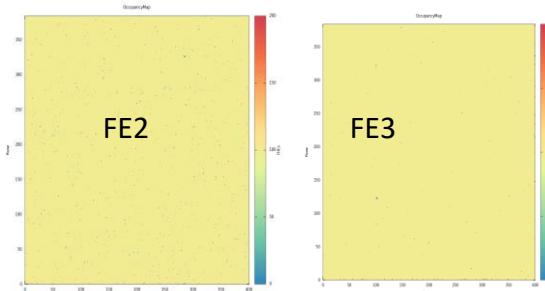
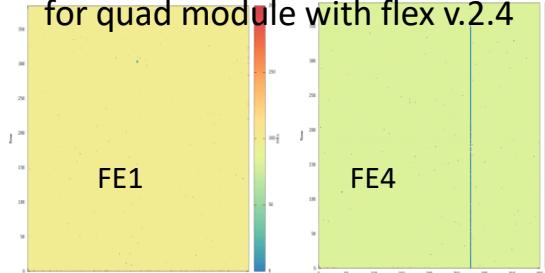
- It implements **feedback-less** readout approach using **trigger-tagging** with both **software** and **firmware** triggering.
- It supports both **felix-client** (felix-star) and **netio** (felixcore) controllers.
- The plotting and chip configuration engine is used from YARR.

Results in OB services chain

setup:

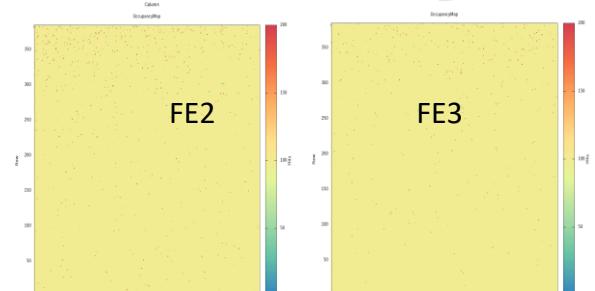
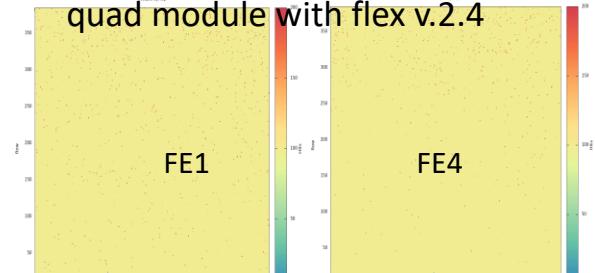
- Tuning of FE parameters required due to known phase issues in ITkpixv1.1 FE chip to get scans stably running.
- The number of mask stages and delay between triggers had to be increased to reduce communication errors in the readout chain and to increase quality of the scan.
- Tests performed with different readout

Analog Scan result in data merging 4-to-1 using FELIX-client itk-daq-sw with software trigger for quad module with flex v.2.4



consistent with single module

Analog Scan result in data merging 2-to-2 using Felixcore itk-daq-sw with software trigger, for digital quad module with flex v.2.4



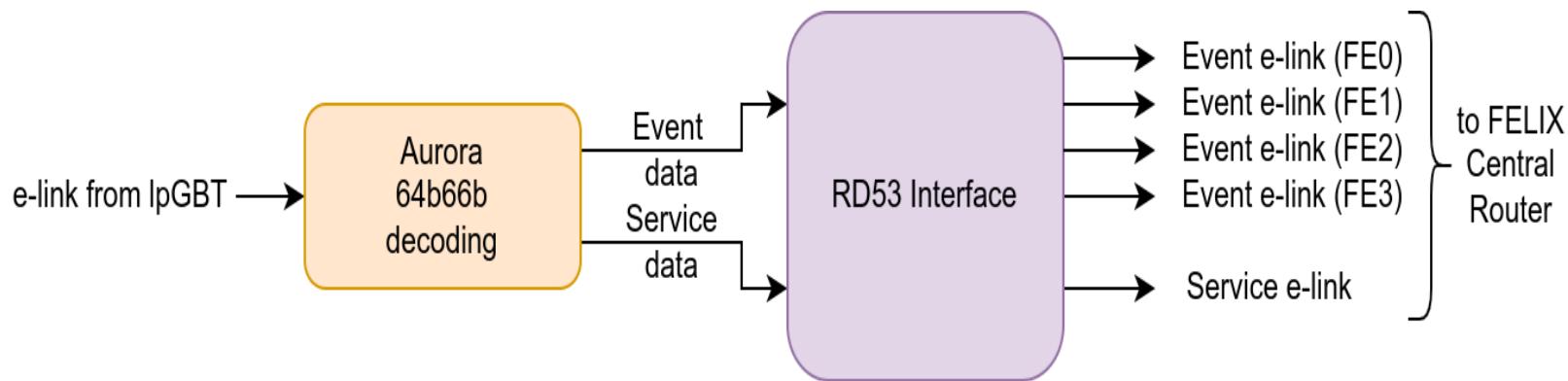
Requirements for Loaded Local Supports and Integration

- ONE scan software that ...

- ... implements **all scans** relevant for Loaded Local Support QC and Integration QC:
 - Analog readback, register read
 - Digital/analog scan
 - Threshold/noise scan
 - ToT measurement
 - Cross-talk measurements
 - Disconnected bump bond scan
 - Noise occupancy measurement
 - Selftrigger scan
 - ... is **compatible with FELIX**
 - ... runs **reasonably efficient multiple-modules** at the same time ($O(20)$ modules simultaneously). For integration $O(500)$ modules at the same time.
 - ... is **qualified** against single module tests, i.e. makes comparisons possible
 - ... has the **potential to scale** to system sizes of a real detector (also wrt. DAQ environment)
- **Timescale:**
 - Loaded Local Support **pre-production about to start** (LLS FDR just over)
 - Test setups being built and commissioned now (site qualification for pre-production)
 - Testing of first modules expected at 10 institutes **early summer 2023**
 - Readout for surface testing during **integration** required from **Q3/2024**

Implementation of link sharing in FELIX

- FELIX needs to support link sharing for ITkPixV1 readout.
- Event from up to 4 front-end chips travel through the same Aurora link and have to be splitted inside FELIX based on the chip ID bits in each Aurora frame.
- Introduction of more “virtual” e-links:



- If link sharing is disabled data will always be routed to FE0. Service e-link is shared between all front-ends.
- First firmware (4 channel IpGBT) is available on [CERNBox](#).
- Still completely untested, due to lack of hardware. At the moment working on a simulation test bench for verification.

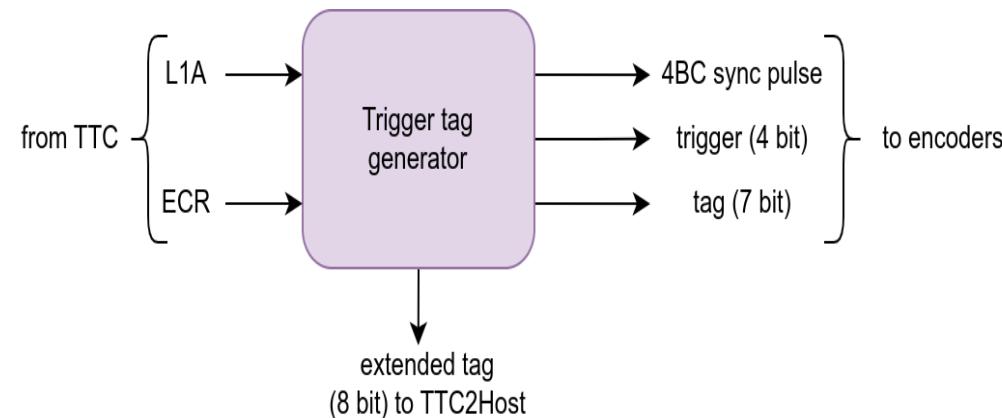
Trigger tag generation in FELIX

- ITk Pixel + Strips have trigger tag based readout.
- FELIX TTC interface generates tags with the following modes:
 - RD53A, ITkPixV1, Strips encoder
- Automatic synchronisation with 4BC window using bunch counter reset (BCR).
- Distribution of trigger tags towards encoders and also TTC2Host channel:

```
Opened FLX-device 0, firmw FLX712-PIXEL-2chan-2206151546-GIT:rm-4.11/1722,  
    trailer=32bit, buffer=64MB, DMA=0  
Using DMA #0 polling  
Display data from E-link : all  
Chunk types: BOTH=<<, FIRST=++, LAST==, MIDDLE==, TIMEOUT="] ] ", NULL=@@,  
OUTOFBAND="#" and "TEC" for chunk truncation/error/CRCerr.  
==> BLOCK 0 (E=600=24-0 seq=0): 1011 bytes payload (27 data)  
    3 1b d4 d 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 << (sz=27)  
=> TTC: Fmt=3 Len=27 BCID=DD4 L1ID=00000000 Orbit=00000000 TTType=0000 LOID=00000000  
    L1Acount=000000000000 (0) TAG=1  
]] (sz=984)  
==> BLOCK 1 (E=000=0-0 seq=0): 1012 bytes payload (8 data)  
    0 0 80 80 0 0 0 0 << (sz=8) (empty event with tag=1)
```

Trigger tag generation in FELIX (cont'd)

- Interfaces:



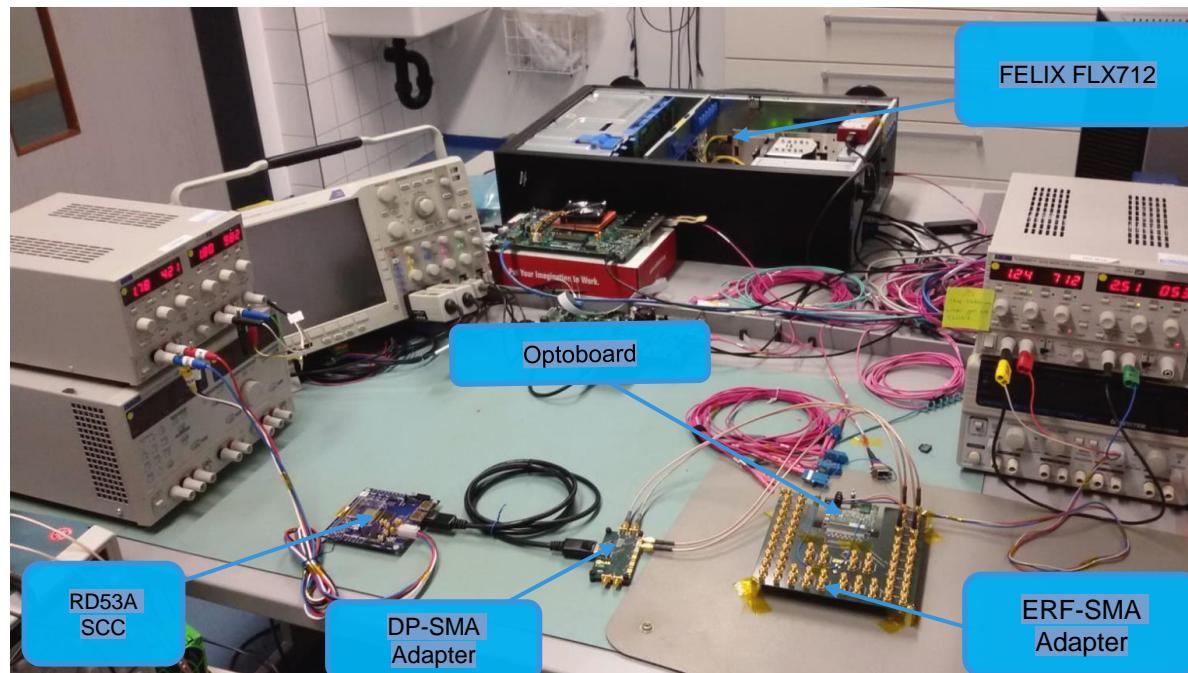
- Tag generation for Pixel:
 - 32 (RD53A) or 53 (ITkPixV1) base tags, assigned round-robin with reusing tags for “orthogonal” triggers.
 - Extended tag for TTC2Host is generated by extending the base-tag with 2 bits for the triggered BC number (00: first BC, 01: second BC, 10: third BC, 11: fourth BC)
- Tag generation for Strips (to be discussed):
 - 128 base tags, with every triggered 4BC block gets new tag, no re-using of tags like in Pixel
 - TTC2Host publishes the base tag
- Implementation into encoders must be performed by the encoder developers.

FELIX Read-out Chain Developments in Goettingen

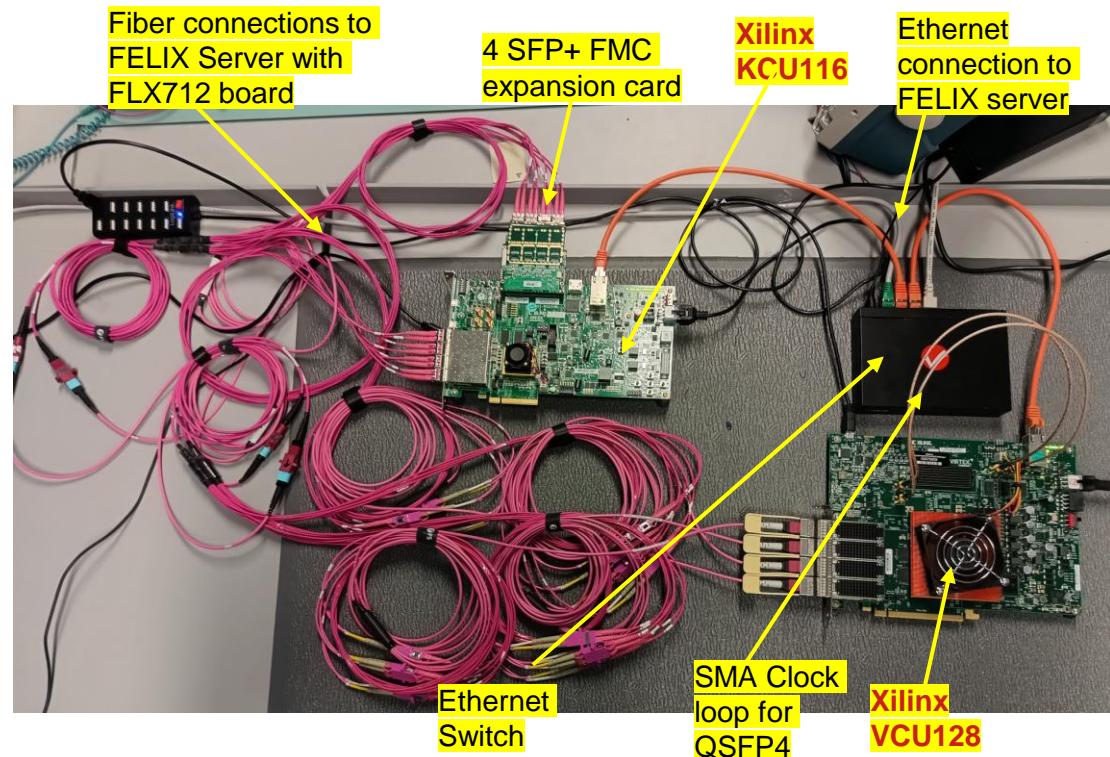
A. Skaf, M. Drescher, W. Alkakhi,
J.G. Knetter, A. Quadt

- ATLAS ITk-Pixel FELIX- based read-out development axes:
 - Yarr-FELIX-optoboard read-out chain:
 - RD53A SCC/QM (Felixcore/NetIO: OK; Felixstar/NetIO-Next: still debugging)
 - RD53B in the pipeline
 - Full FELIX stress test using only 2 FPGA boards connected to all 24 fibers of FLX712
 - Hardware: multi-instance IpGBT emulators each connected to 7 RD53A emulators, with dedicated hit-map memories
 - Firmware: for one Microblaze PS and dedicated peripherals per FPGA board
 - Software: Python applications and scripts to simplify the system configuration and control to perform the stress test
 - Setup validated (RD53/felixcore/NetIO), properly started stress test!
 - Next, extend to ItkPix and/or felixstar/NetIO-Next flavours..
 -
 - FELIX firmware Tx phase alignment implementation to enhance communication quality
 - based on CERN HPTD group work
 - Tests ongoing..

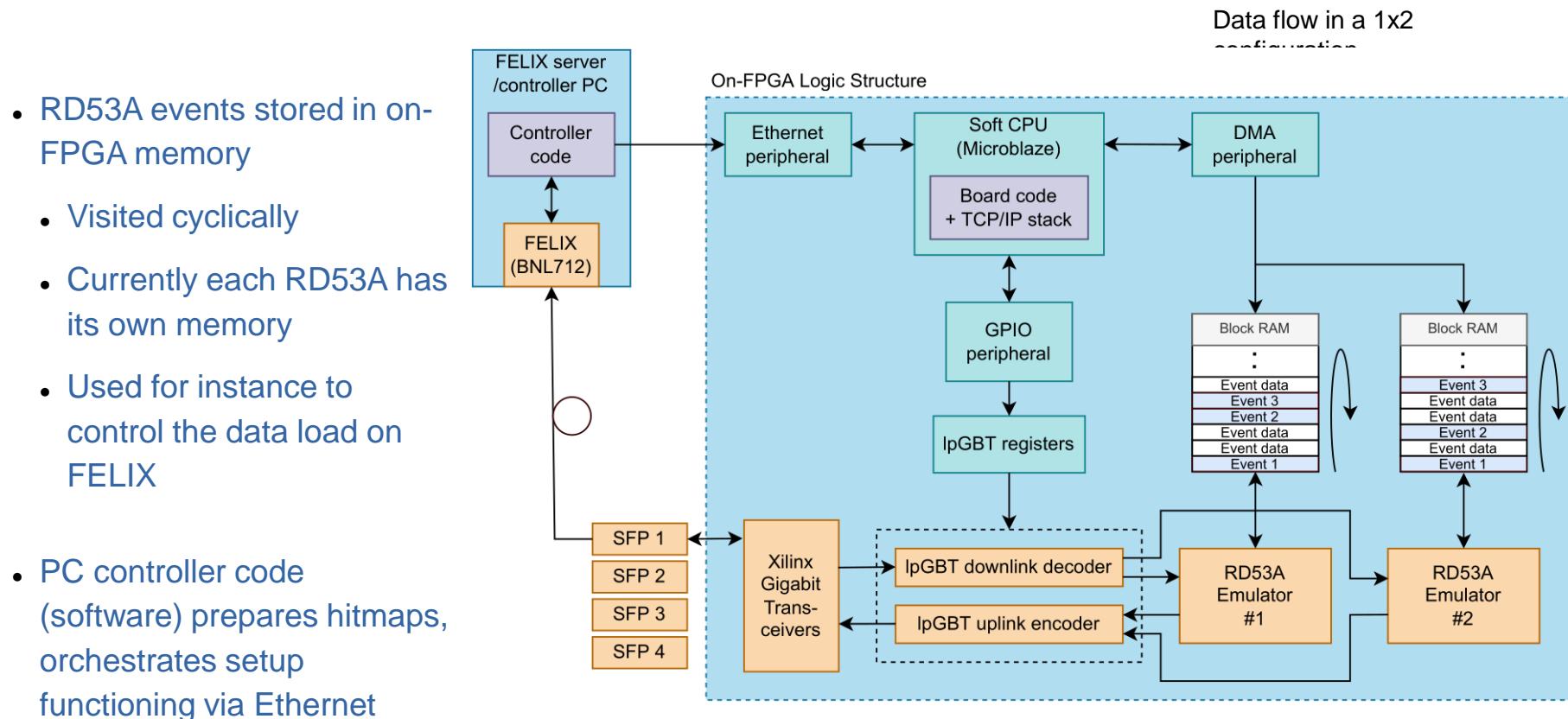
- Yarr-FELIX-optoboard Read-out chain
 - RD53A SCC/QM
 - Felixcore/NetIO: OK
 - Felixstar/NetIO-Next: still debugging
 - RD53B in the pipeline



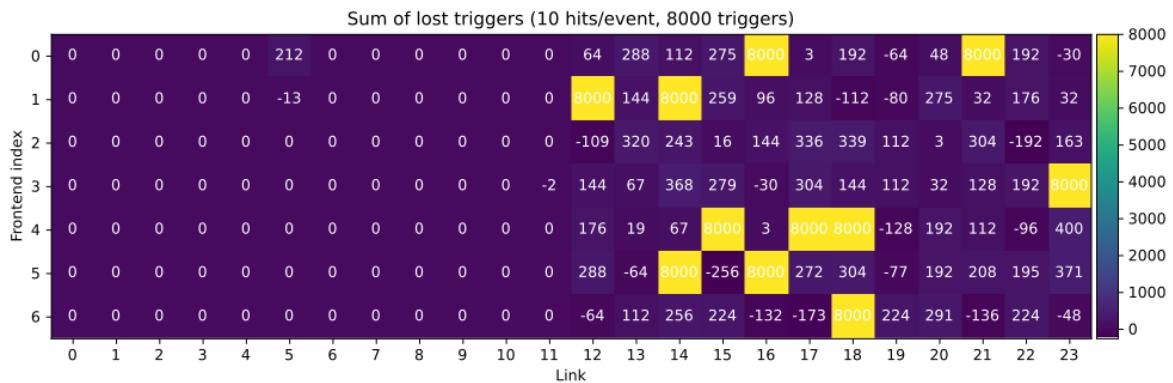
- Stress test is hard to achieve, in lab, with (24) IpGBT ASICs and (168/42) RD53A SCCs/QMs !
- Instead, all necessary hardware can be implemented on 2 FPGA boards:
 - VCU128 hosting 4 QSFP28 (16 fiber connections)
 - KCU116 with originally 4 SFP+, extended to 8 by adding an FPGA Mezzanine Card (FMC)
- *Extensive use of FPGA capabilities (CPU, Ethernet, Memory, Peripherals) besides IpGBT and RD53A emulators to provide:*
 - Configuration/control through a Gigabit Ethernet network
 - Uploading event hitmaps to the RD53A emulators



- FPGA board = System-on-Chip (SoC)
 - Hardware design contains CPU + custom logic, in addition to IpGBT/RD53A emulators
 - Bare metal code (firmware) controls this design



- Validated full chain implementation
 - flx-info shows working links (IpGBT) and E-Links (RD53A)
 - Flawless YARR digital scans of the RD53A emulator possible
- Promising preliminary test results: scanning one FE at a time
- Further investigation required
 - Missing triggers on some links, mostly on FELIX device 1
 - Swapping device 0 ↔ 1 yields same picture
 - →Most likely not a problem of the stress test components



Card type : FLX-712
Firmw type: PIXEL

Link alignment status

Channel	0	1	2	3	4	5	6	7	8	9	10	11
Aligned	YES											

Channel	12	13	14	15	16	17	18	19	20	21	22	23
Aligned	YES											

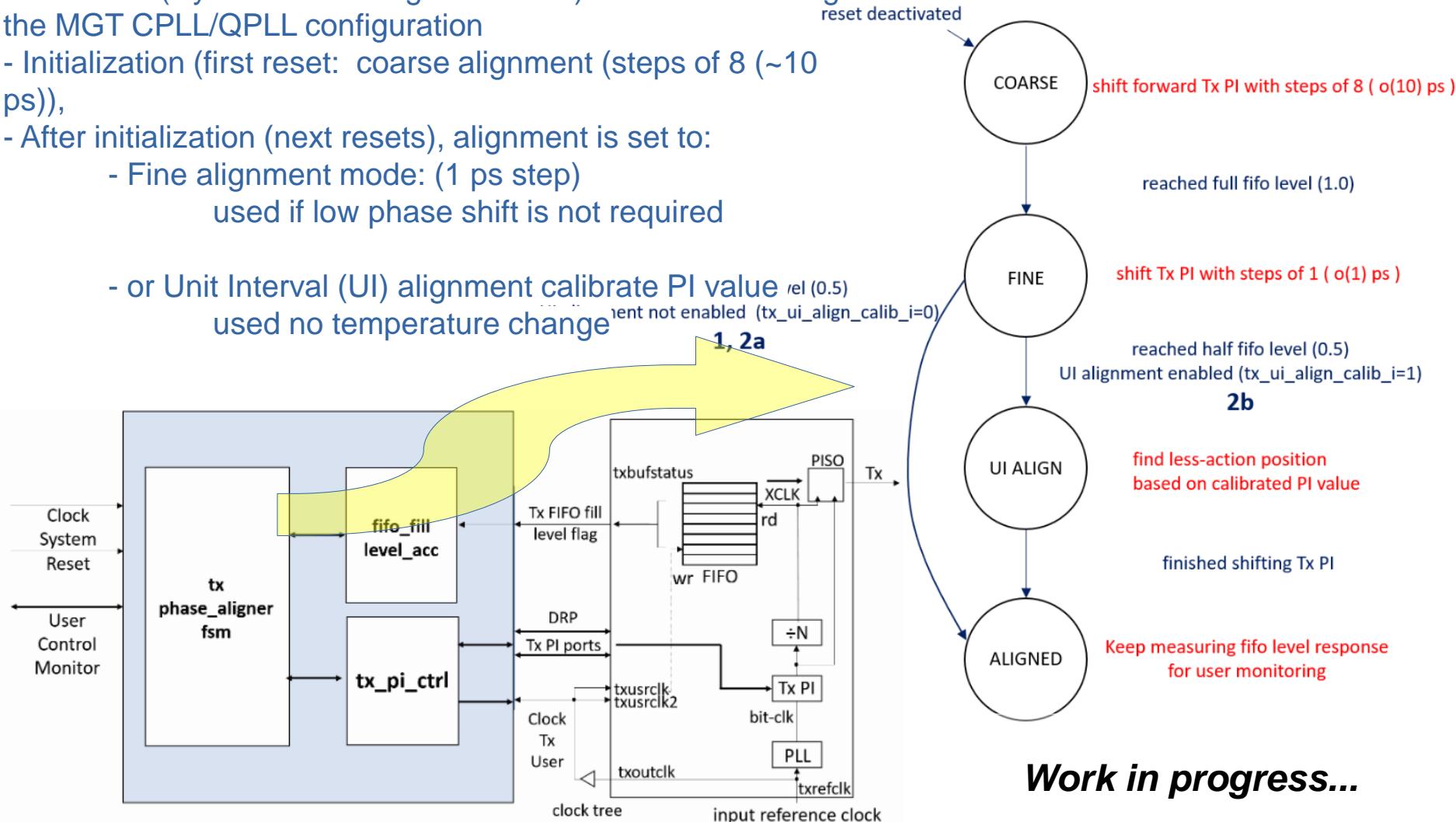
E-link alignment status

Endpoint 0 ('*'=aligned, '-'=not aligned)	LNK 0	8	16	24	32
0:	-----*	-----*	-----*	-----*	-----*
1:	-----*	-----*	-----*	-----*	-----*
2:	-----*	-----*	-----*	-----*	-----*
3:	-----*	-----*	-----*	-----*	-----*
4:	-----*	-----*	-----*	-----*	-----*
5:	-----*	-----*	-----*	-----*	-----*
6:	-----*	-----*	-----*	-----*	-----*
7:	-----*	-----*	-----*	-----*	-----*
8:	-----*	-----*	-----*	-----*	-----*
9:	-----*	-----*	-----*	-----*	-----*
10:	-----*	-----*	-----*	-----*	-----*
11:	-----*	-----*	-----*	-----*	-----*

Endpoint 1 ('*'=aligned, '-'=not aligned)	LNK 0	8	16	24	32
0:	-----*	-----*	-----*	-----*	-----*
1:	-----*	-----*	-----*	-----*	-----*
2:	-----*	-----*	-----*	-----*	-----*
3:	-----*	-----*	-----*	-----*	-----*
4:	-----*	-----*	-----*	-----*	-----*
5:	-----*	-----*	-----*	-----*	-----*
6:	-----*	-----*	-----*	-----*	-----*
7:	-----*	-----*	-----*	-----*	-----*
8:	-----*	-----*	-----*	-----*	-----*
9:	-----*	-----*	-----*	-----*	-----*
10:	-----*	-----*	-----*	-----*	-----*
11:	-----*	-----*	-----*	-----*	-----*

Tx Phase Aligner Blocks

- Use DRP (Dynamic Reconfigurable Port) interface to change the MGT CPLL/QPLL configuration
- Initialization (first reset: coarse alignment (steps of 8 (~10 ps)),
- After initialization (next resets), alignment is set to:
 - Fine alignment mode: (1 ps step)
used if low phase shift is not required
 - or Unit Interval (UI) alignment calibrate PI value
used no temperature change



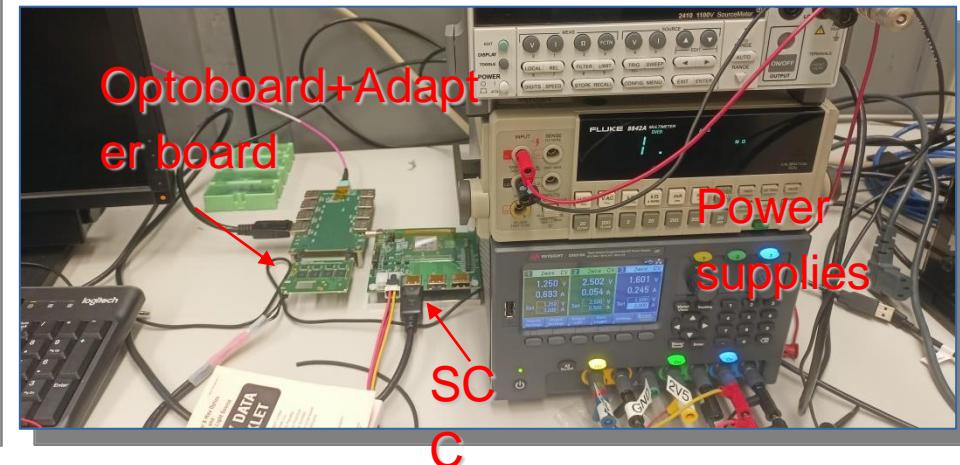
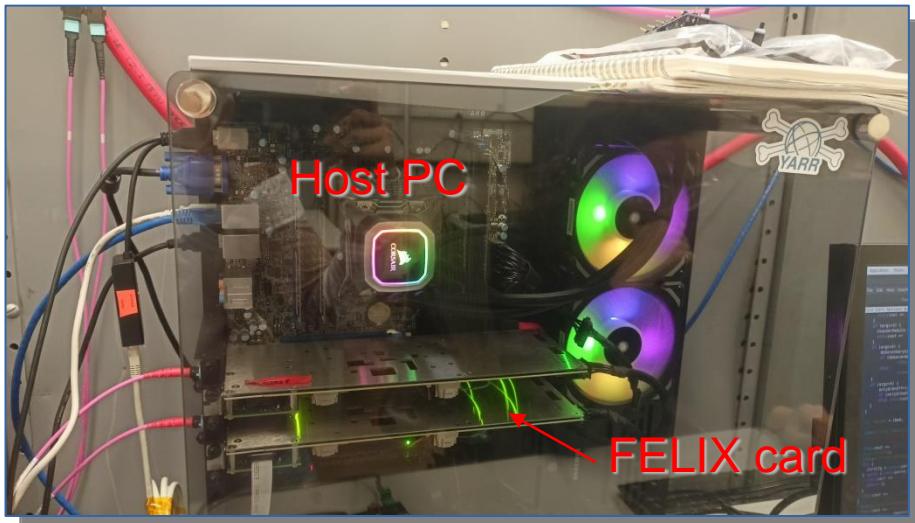
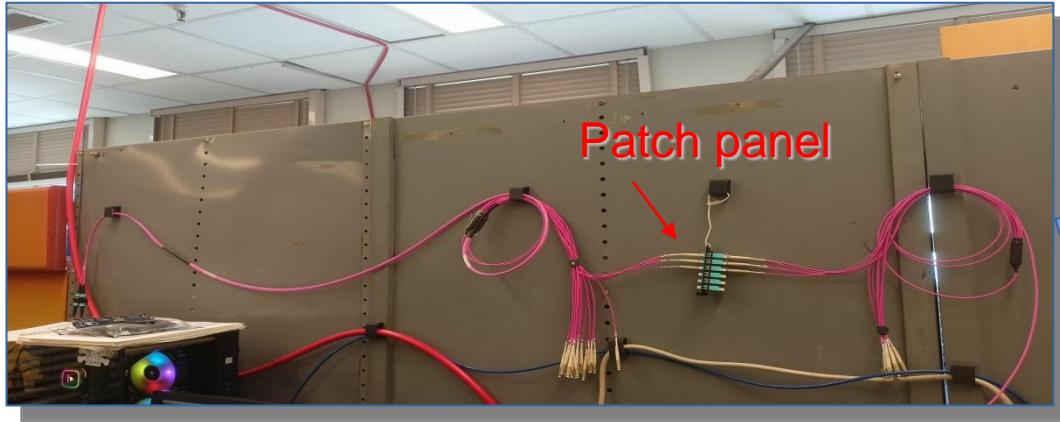
Work in progress...

- Tx Phase Alignment feature added to FELIX Phase 2
- Only few ps of Tx clock phase shift is achievable
- Expected better data communication quality (to be confirmed)
- Require specific MGT clocking configuration / connectivity (not straightforward in FLX712)
- Implementation maintained in FELIX firmware repository
- Validation is still ongoing
- TC link integration in FELIX is to follow..

Status of ITk Pixel DAQ at LBL

- Started with resources available on CDS, EDMS, JIRA ticket [FLX-2032](#).

- FELIX driver, ATLAS TDAQ software, Optoboard software & YARR present on the same host PC.
- Also, FELIX setup for strips hosted on the same PC on a separate FELIX card.
(Schematic & detailed description in backup [slide 5](#)).



Status of ITk Pixel DAQ at LBL

- Two options for trigger generation: software-based & firmware
 - Problems seen with both triggers in data readout.
 - Fig. 1: Digital scan output with firmware-based trigger (parameter details in backup [sl1](#))
 - Using the YARR log, TCP/IP dump and felixcore verbose for investigating the timing issues

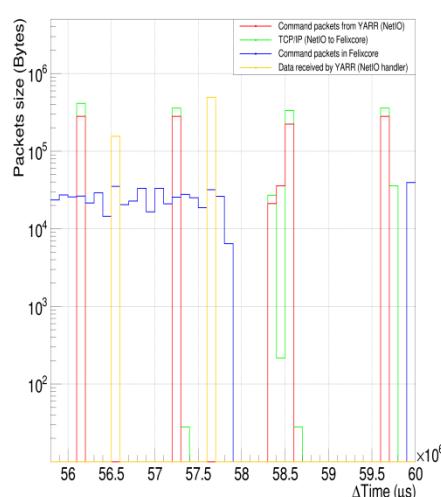
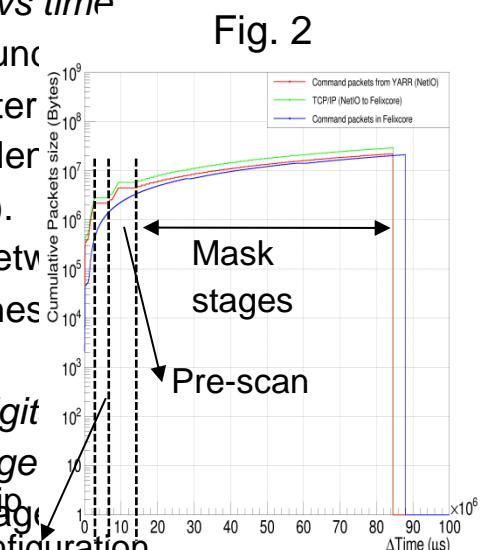
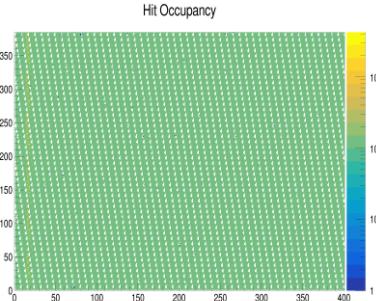
Observations

Fig. 2: Cumulative command packets size from YARR (red), in the network from TCP/IP dump (green) and in felixcore (blue) vs time

- All the packets from YARR are not seen by felixcore, around **lost**. Also, last packet seen in felixcore **~4 seconds later** after finished sending all commands due to network buffering. Here many empty mask stages (StdDataLoop wait time ~ 1 sec).
- Many smaller-sized TCP/IP packets are created by the network before sending to felixcore, hence downstream buffer flushes a slower rate.

Fig. 3: Example behavior of a few mask stages from the digit with data from chip seen in NetioHandler (yellow). Full range

- Data received around **0.5 seconds later** in every mask stage ^{Chip configuration} network latencies (especially towards last few mask stages).
- No command packets seen in felixcore occasionally due to network buffering, hence no readout data from chip [devel itkpix felixNetio](#)



Status of ITk Pixel DAQ at LBL

• Improvements

- MR [YARR!615](#): Aggregate the command packets from YARR (NetioTxCore) to send longer messages, flushing the NetIO FiFo regularly using IsCmdEmpty() call.
- Advantages: Commands reach the chip faster, and in its entirety. Less number of packets overall, hence less crowding of command packets in FELIX.

• Results

- Successful digital scan (backup [slide 13](#)).
- All the command packets from YARR reach felixcore almost instantly (Fig. 4). Also, less number of extra packets created network while in buffer.
- Scan time **faster by 10%**, due to aggregation of command packets.
- Data received within 0.2 to 0.3 seconds later in every mask which is roughly a **factor of 2 faster** than before (Fig. 5).

• Future development plans

- Include data processor feedback in the scans for pixels (more on backup [slide 14](#)).
- Enable parallelized sending of command packets from YARR (more on backup [slide 15](#)).
- Fix software-based trigger generation (more on backup [slide 15](#)).
- Enable FELIX firmware to read the chip configuration registers (right now its bypassed through the ServiceEnable=0).

Fig. 4

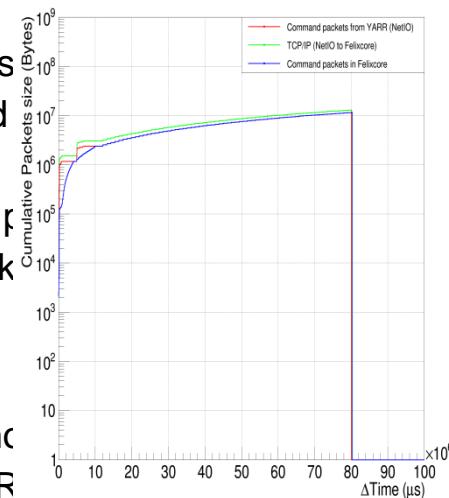
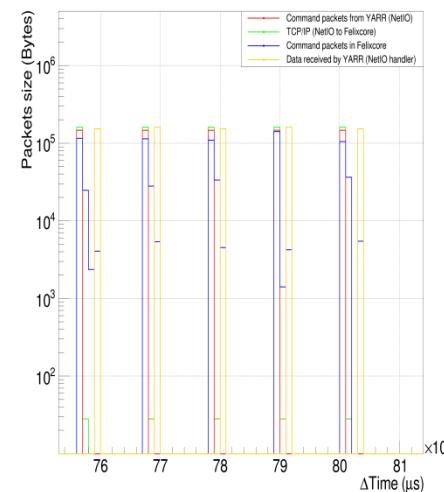
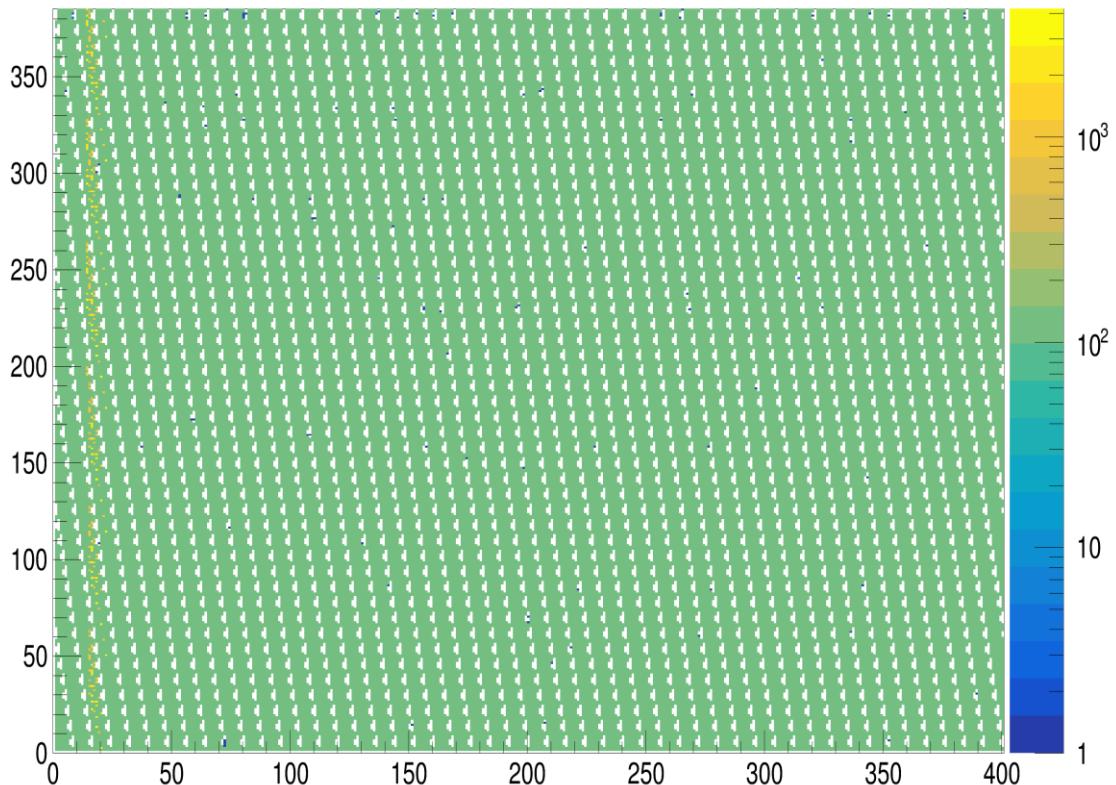


Fig. 5



Hit Occupancy

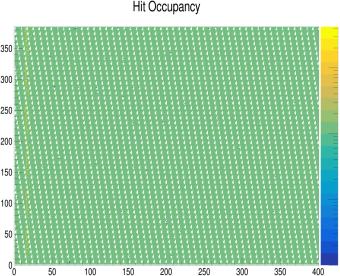


- Firmware-based trigger generation.
- `StdDataLoop()` wait time = 1 s.
- Trigger frequency = 5000 Hz.
- Trigger count (injections) = 100.
- Number of mask stages = 64.

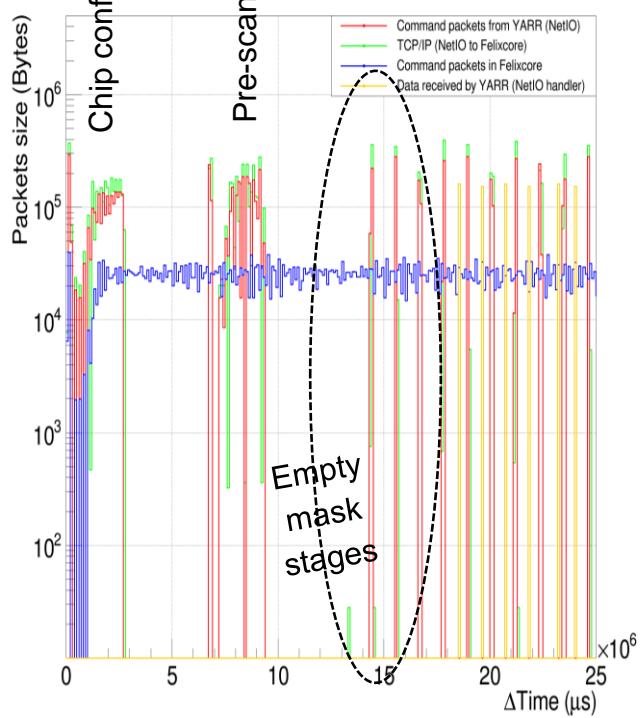
Missing chip readout data.
Incorrect digital scan results.

YARR branch -

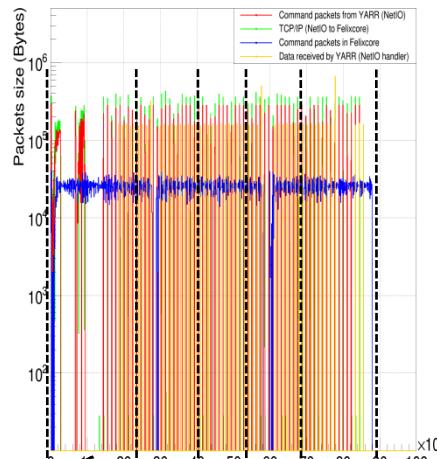
devel itkpix felixNetio



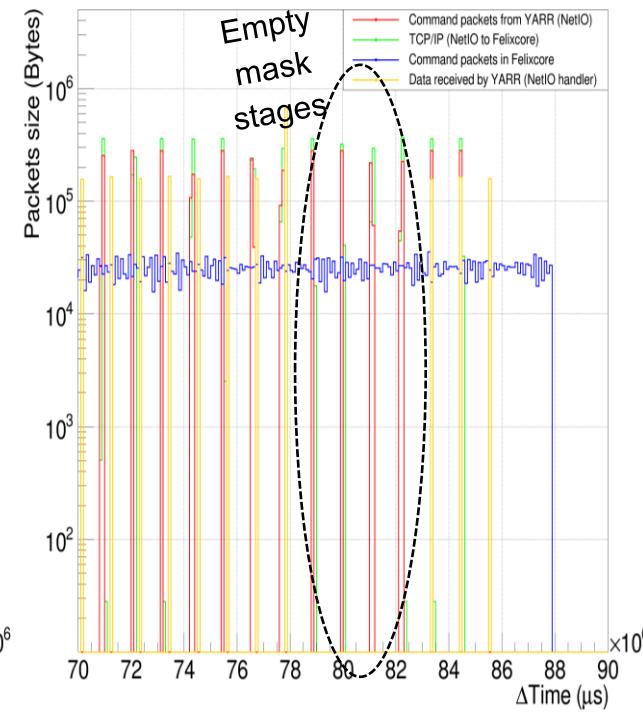
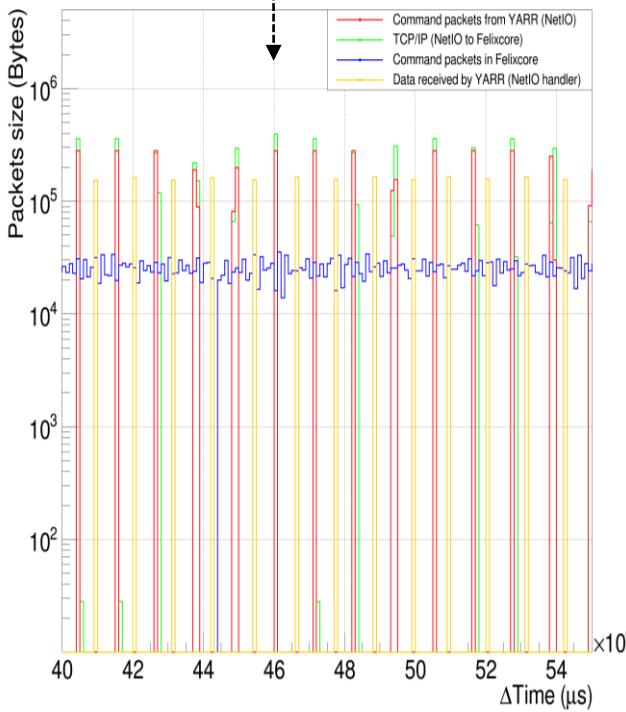
Chip configuration



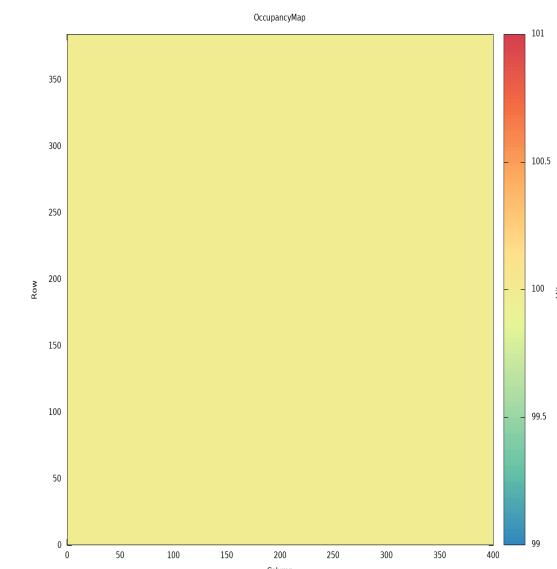
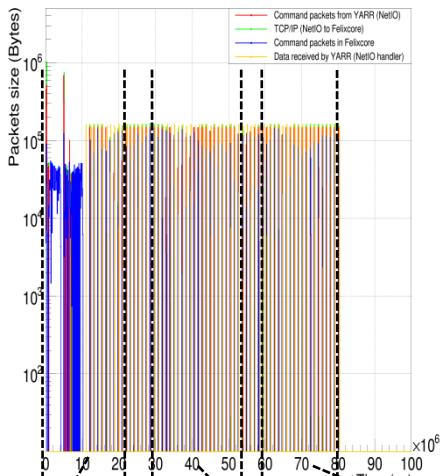
Size of the packets vs time



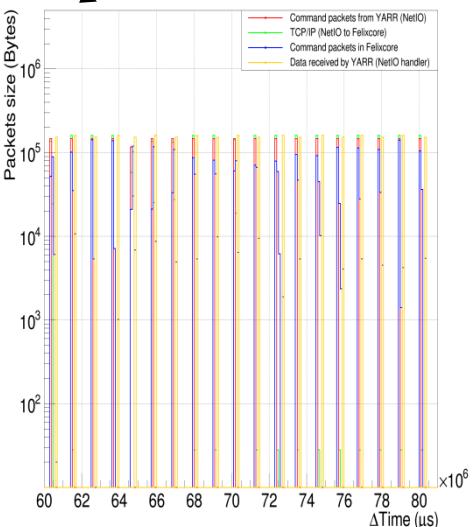
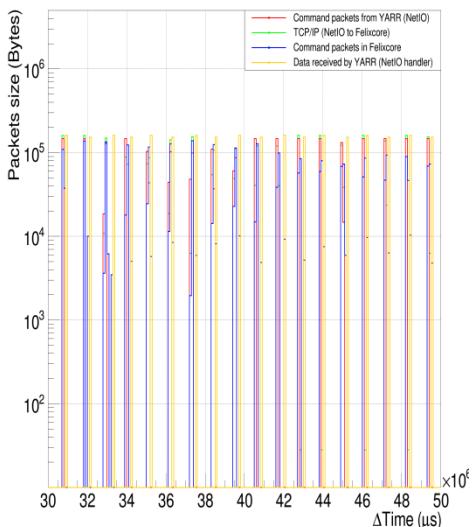
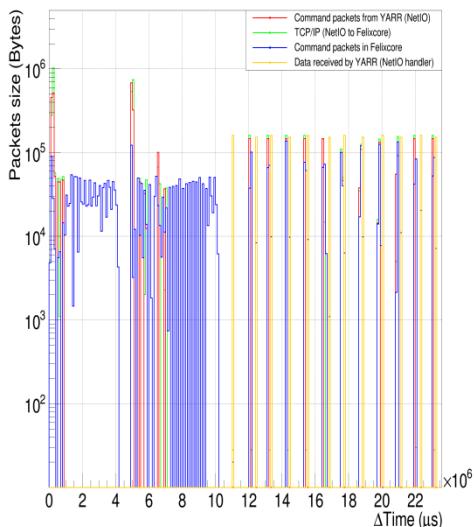
- Command takes a long time to reach the chip.
- Also, many small encoded packets per command are sent out to felixcore (and eventually the chip).
- As a result, felixcore buffer is flushed only after its full which takes a long time, and by then, the scan time for that mask stage runs out.
- Hence, no data or data chunks arriving later.



Size of the packets vs time



Digital scan ✓



YARR branch -
[devel_itkpix_felixNetio_fixFWtrigger](#)



Many software-related developments are yet to be done... Some of the high-priority ones are as follows:

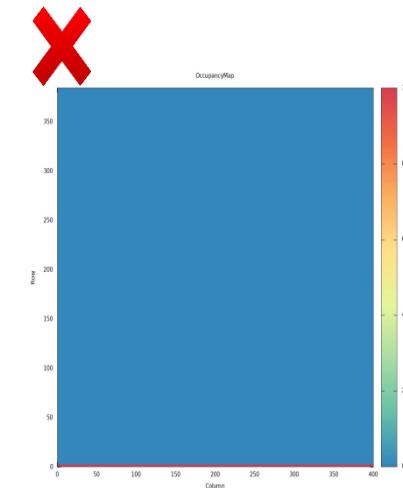
- **Data processor feedback:** Along with sending out larger commands, allow YARR to continue reading data in each stage, by looking at feedback from the DataProcessor, with an estimation for approximate size of incoming data.

MR - [otoldae/YARR:devel_DataFeedback](#) exists for strips, needs to be implemented for pixels.

- **Enable parallelizing commands from YARR:** New class “Rd53bParMaskLoop” exists in devel branch, which applies the current mask in parallel to the entire pixel matrix.

Right now, the SW doesn't support sending out multiple commands in parallel to FELIX (or commands are lost in FELIX?), as a result masking is not set properly.

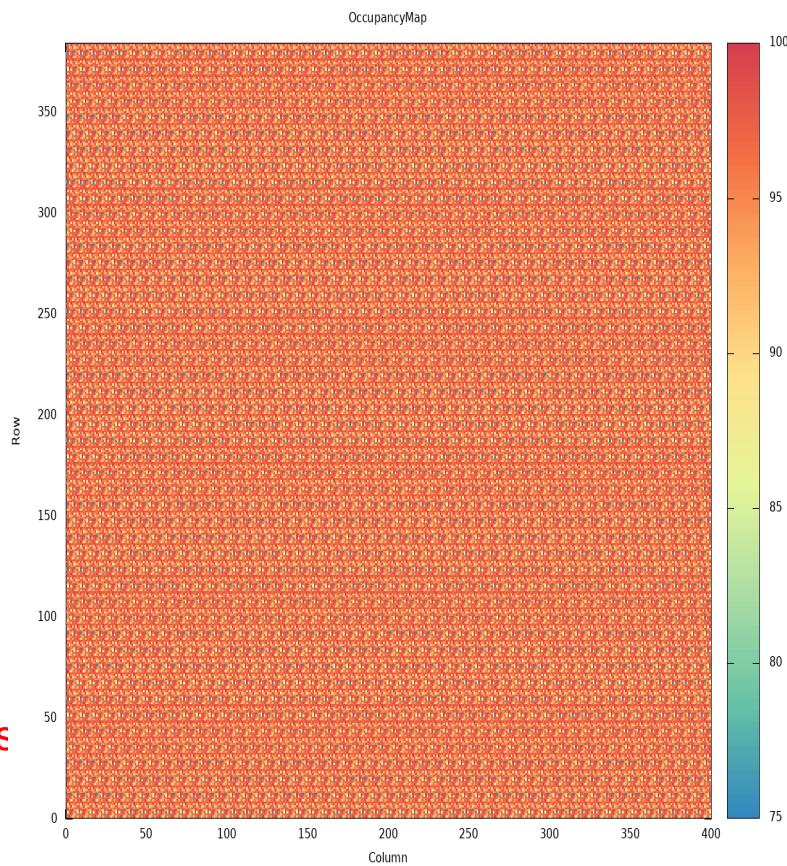
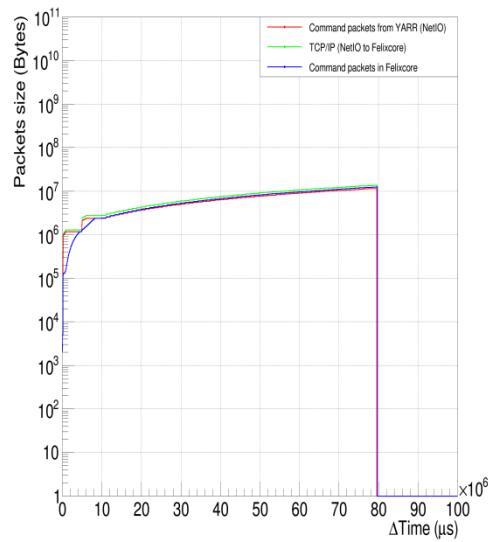
```
232 void Rd53b::configurePixelMaskParallel() {
233     logger->debug("Configure all pixel mask regs in parallel ...");
234     // Setup pixel programming
235     this->writeRegister(&Rd53b::PixAutoRow, 1);
236     this->writeRegister(&Rd53b::PixConfMode, 0);
237     this->writeRegister(&Rd53b::PixBroadcast, 1);
238     // Writing all core columns at the same time, loop over dc in core
239     for (unsigned dc=0; dc<4; dc++) {
240         this->writeRegister(&Rd53b::PixRegionCol, dc);
241         this->writeRegister(&Rd53b::PixRegionRow, 0);
242         std::array<uint16_t, _Row> maskBits;
243         for (unsigned row=0; row<_Row; row++) {
244             maskBits[row] = toTenBitMask(pixRegs[dc][row]);
245         }
246         this->sendPixRegBlock(m_chipId, maskBits);
247         while(!core->isCmdEmpty()){};
248     }
249 }
250 }
```



- **Fixing the software-based trigger generation:** SW triggers from the YARR (NetIO) are delivered unevenly to felixcore because of the network buffering – also seen within the strips community [here](#).

Unlike firmware triggers, full sequence of SW trigger command is packed together by NetIO and sent out for every trigger-generation. As a result, extra latency introduced in the network before reaching FELIX.

Cumulative size of the packets vs time



- Software-based trigger generation (in the new branch).
- StdDataLoop() wait time = 1 s. Varied it up to 5 seconds at which point every mask stage had non-zero occupancy, but then felixcore crashed in between the scan.
- Trigger frequency = 5000 Hz. Therefore, wait time in trigger() very small. Cannot run at 100 Hz as felixcore server crashes in between the digital scan.
- Trigger count (injections) = 100
- Number of mask stages = 64

Solution: NetIO-next + Felix-s