



ATLAS ITk Pixel Detector Overview

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On behalf of the Atlas Itk Pixel collaboration

 ICHEP 2022
BOLOGNA

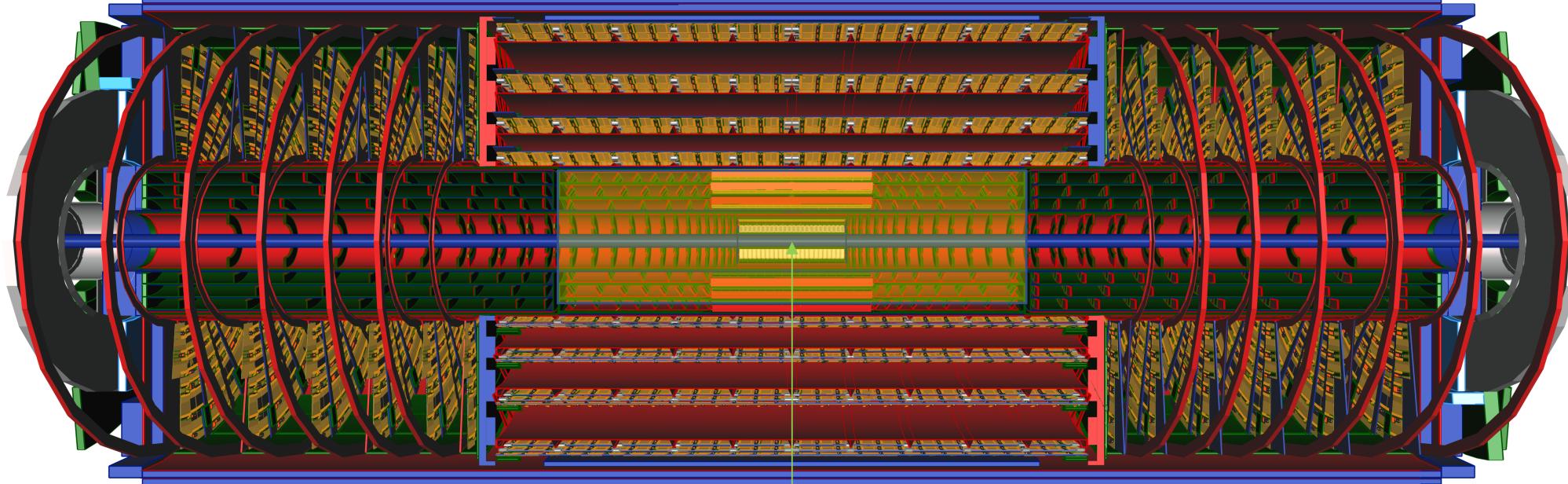


ICHEP 2022
XLI
International Conference
on High Energy Physics
Bologna (Italy)

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Talk and Detector Layout

Inner Tracker to replace the present Inner Detector (Pix + SCT + TRT)



[ATL-PHYS-PUB-2021-024](#)

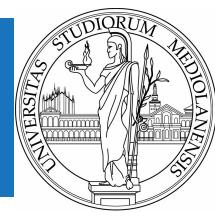
- Increased granularity
- All silicon solution
- Occupancy < 10%
- Trigger rate to 1MHz

3m
Interaction point

Talk layout

- Motivation
- Description of the ITk-pix
- Technical challenges
- Status and recent results
- Plans

Motivation



Present ATLAS inner detector will have reached the end of operating life after (extended) Run3

Tracking at high luminosity more challenging:

Resolve events with $\langle \mu \rangle > 200$ pileup events

Solution: all tracking with new Silicon detectors

Increased acceptance to $|\eta| < 4$

Increased transparency (1/2 in terms of X_0) $L < 2.4 X_0$

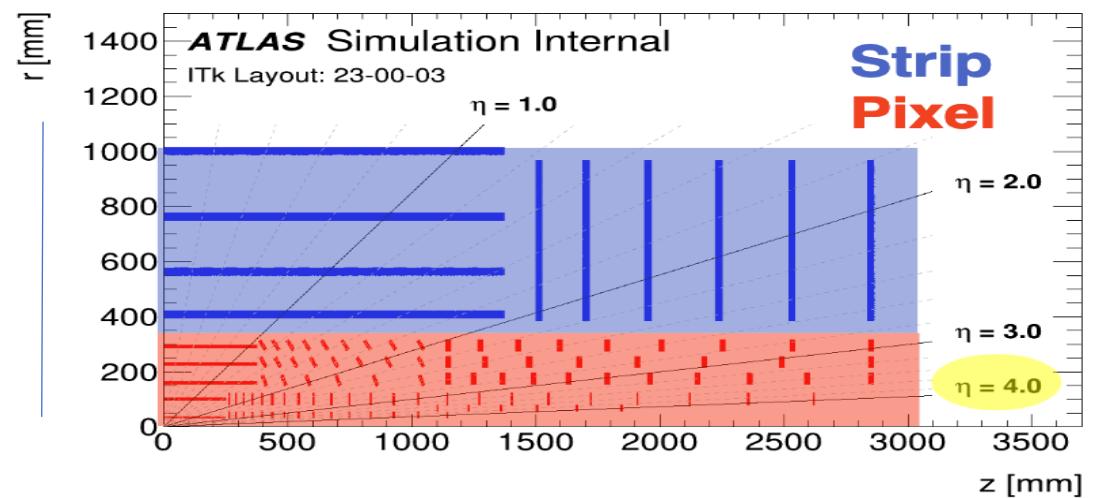
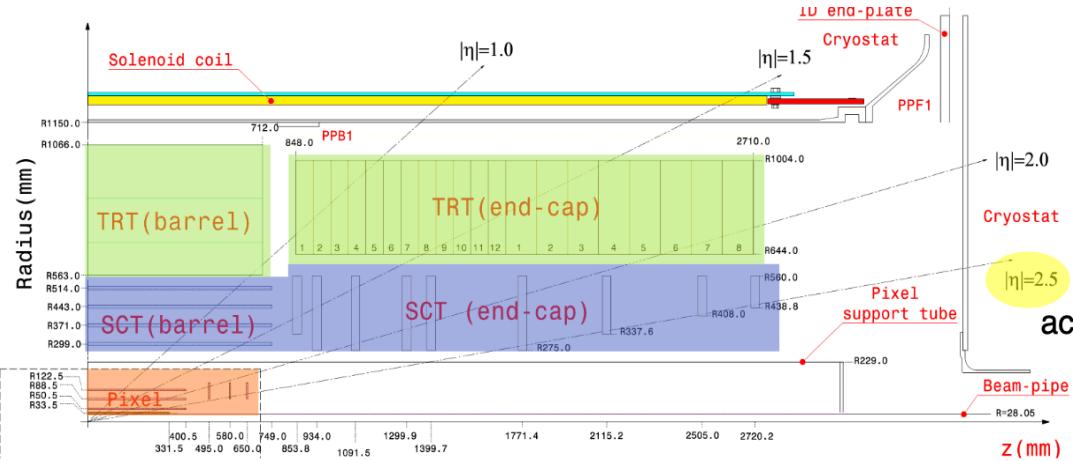
Details on [the expected tracking performance](#) in T. Strebler talk

Inner Tracker (ITk) use same space inside the solenoid coil

- outer layer: strips: 4 barrel layers, 2 x 6 disks
- inner layers: pixel

Pixel Numerology: 5×10^9 pixels

- 5 barrel layers, 23 inclined disks (outer barrel)
- 28 outer disks (outer end-cap)
- 21 inner disks, 23 L1 disks, (inner system)



The modules

The building blocks are the **modules**

Flip-chip assembly of Silicon sensor with ASIC

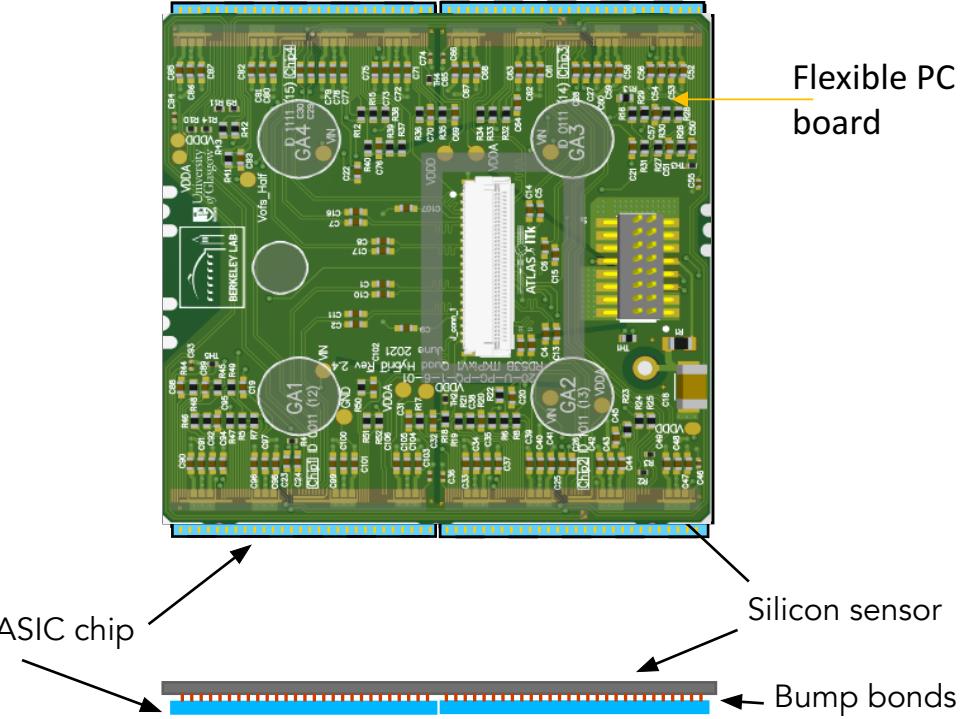
Printed board flexible circuit glued on sensor, wire bonded to ASICS

3 types of modules:

- “Quad” with 4 ASICS on one sensor
- “Triplet” with 3 single sensor-ASIC assembly
 - Both Ring (for disks) and Linear (for barrel) shaped
- All chips thinned to 150 μm
- All sensors 150 μm thick, apart from L1 which are 100 μm

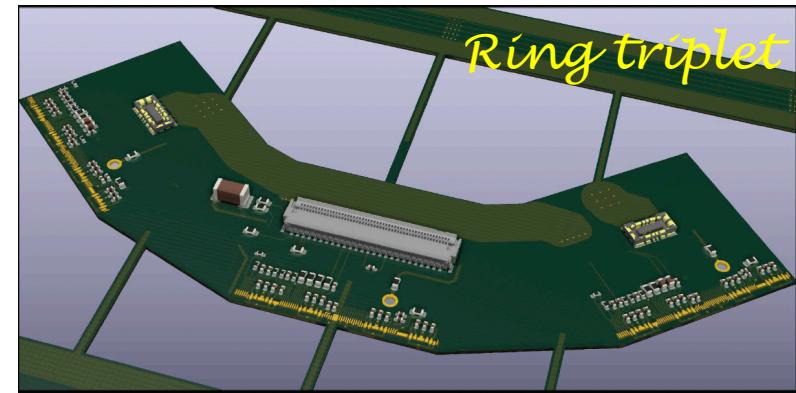
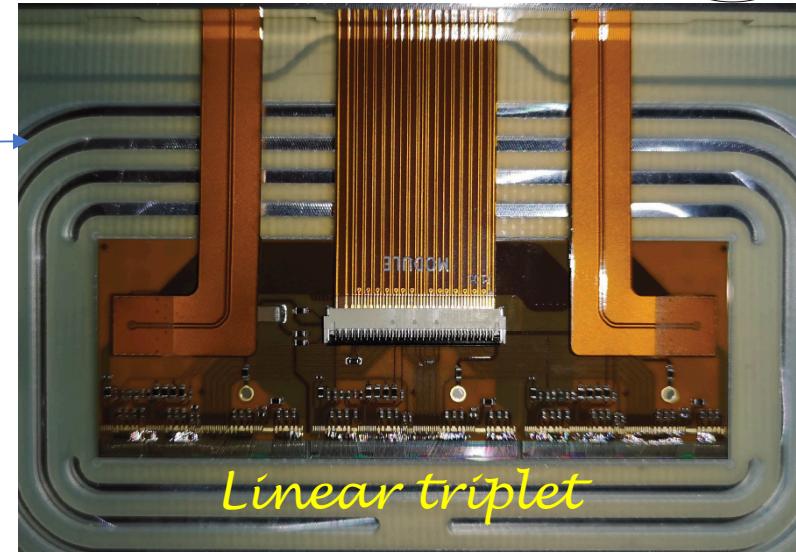
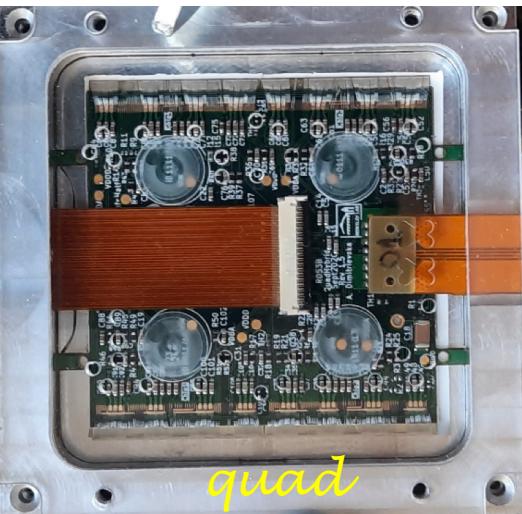
Two types of sensors:

- 3D for inner part of inner system
- Planar, all the rest



Module details

- Inner system:
 - L0 3D Silicon sensors 150 μm thick “triplets”
 - Barrel pixel size 25 x 100 μm
 - Endcap pixel size 50 x 50 μm
 - L1 planar 100 μm thick “quads”
 - Pixel size 50 x 50 μm
- Layer 2-4
 - 150 μm pixel size 50 x 50 μm “quads”



Summary of module numbers

Module type	Installed
L0 barrel triplet	96
L0 coupled ring	180
L0 endcap ring	120
L1 quads	1160
L2-L4 quads	6816

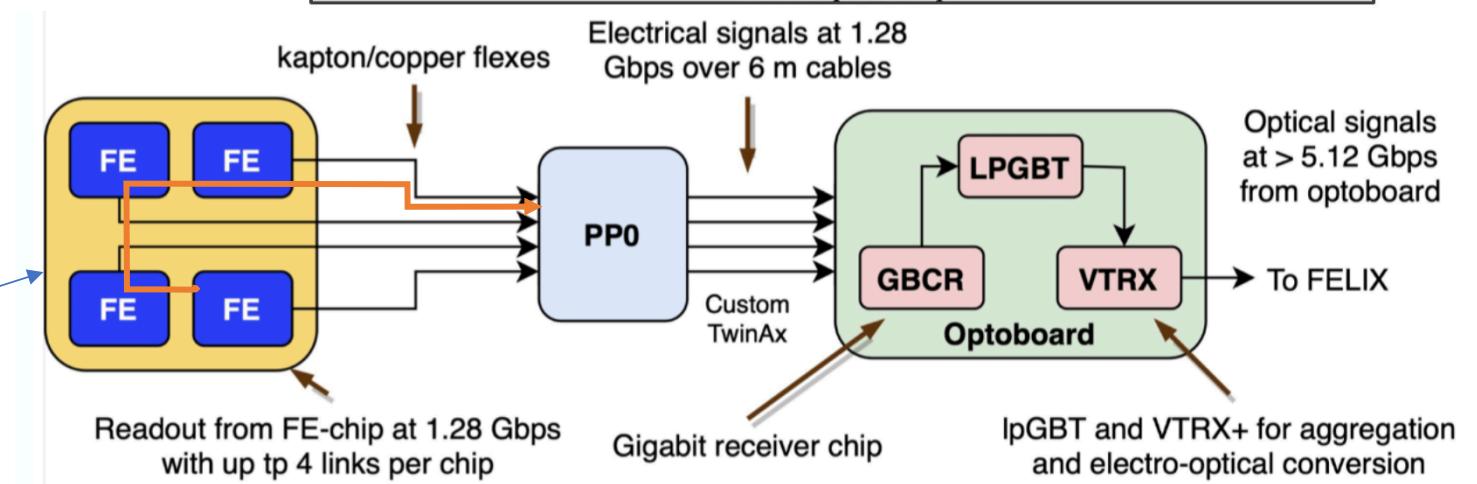
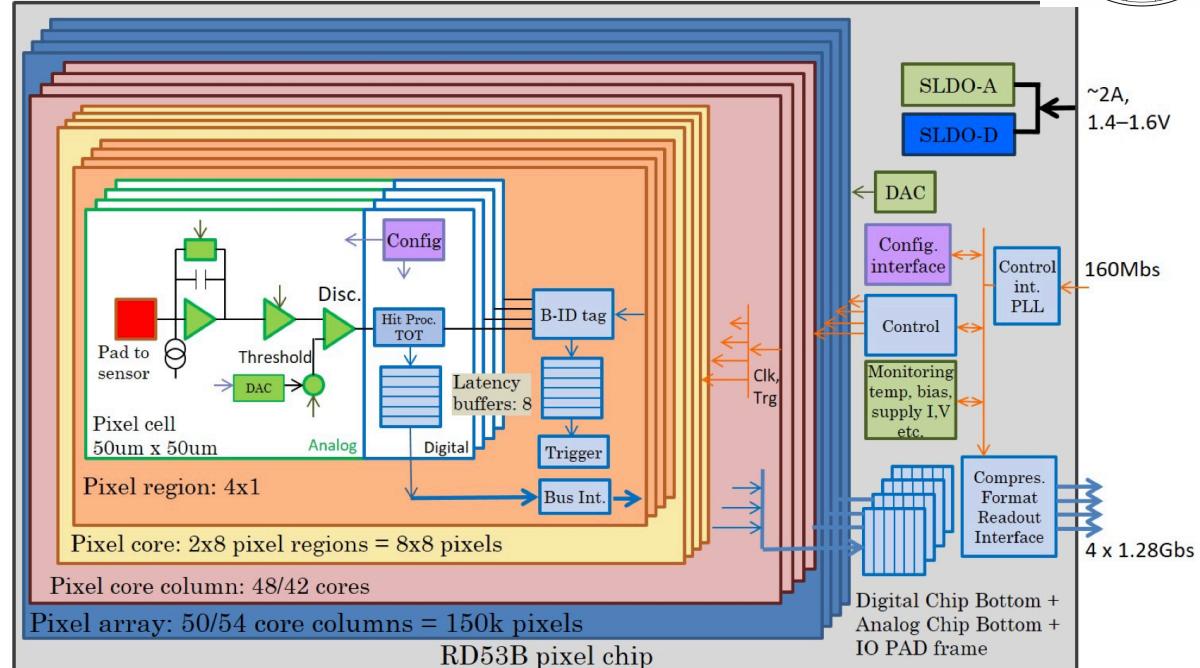
The readout chip

All pixels read out with same ASIC “ITkPix”

[Atlas flavour of [RD53](#) common ATLAS-CMS ASIC]

Main features:

- 152800 pixels per chip (384 rows per 400 columns)
- 65nm technology, $50 \times 50 \mu\text{m}^2$, total area $2 \times 2 \text{ cm}^2$
- 4 data links per chip at 1.28 Gb/s,
- “Differential” analog input
- Digital readout with Time over Threshold=
- Column readout, data encoding
- Shunt Low Drop Output regulators $I = \text{const}$
- 40 MHz clock with 780ps phase adj.
- Data merging: FE readout via another FE
 - Used in lower occupancy layers



The sensors

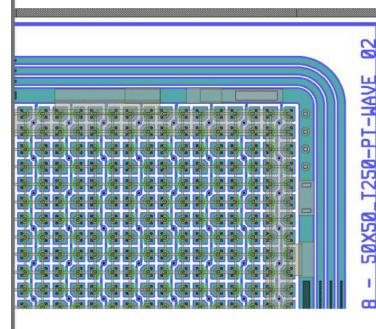
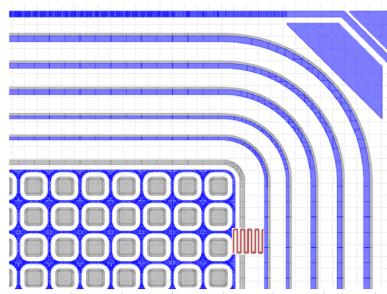
Two types of sensors:

Planar:

Various design detail left up to vendor :

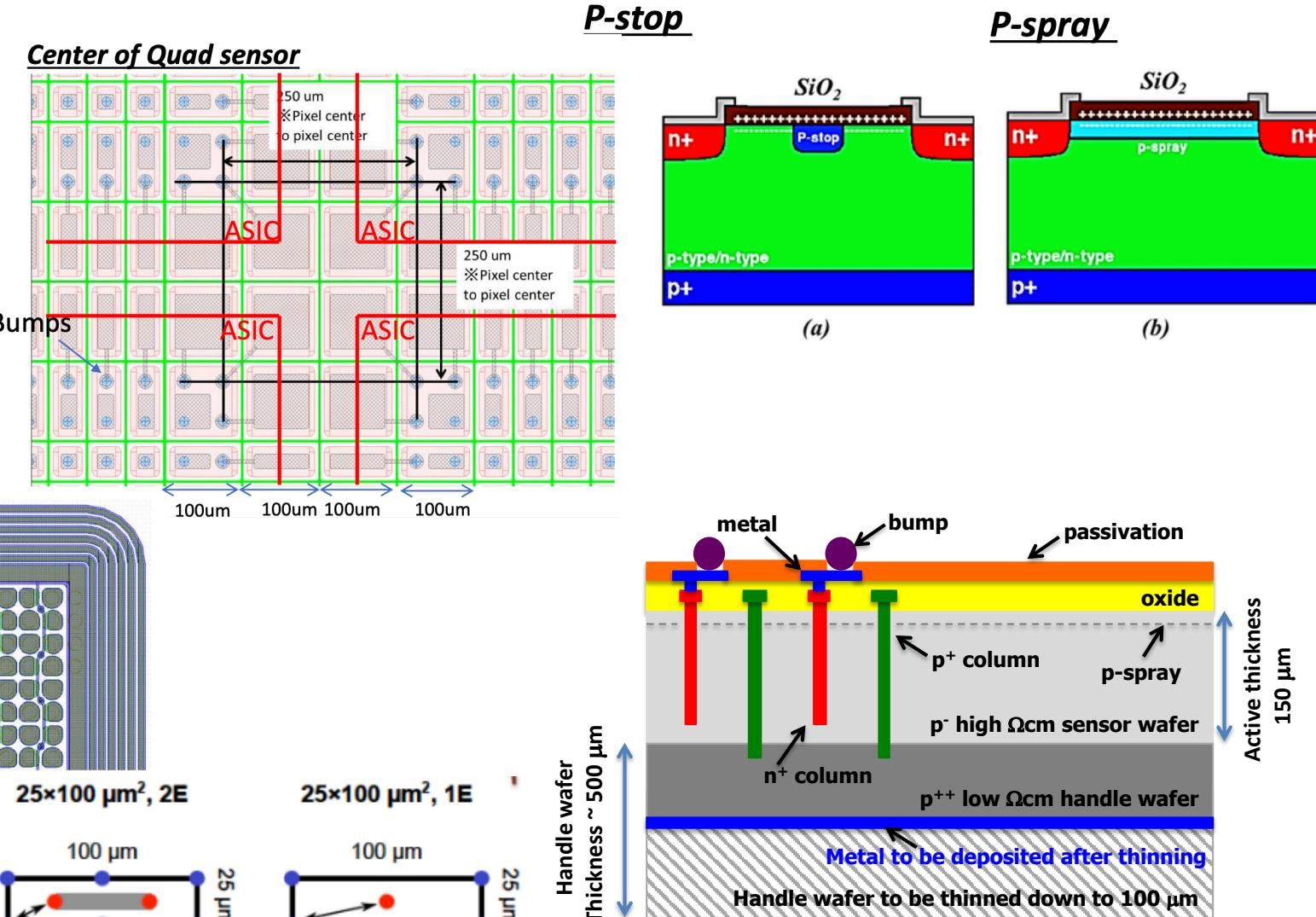
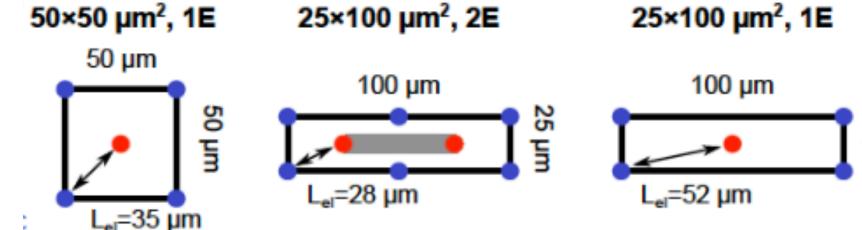
- p-stop vs. p-spray insulation
- Polysilicon bias or punch-through
- Guard-ring geometry

Requirements defined on performance



Inner system uses 3D sensors

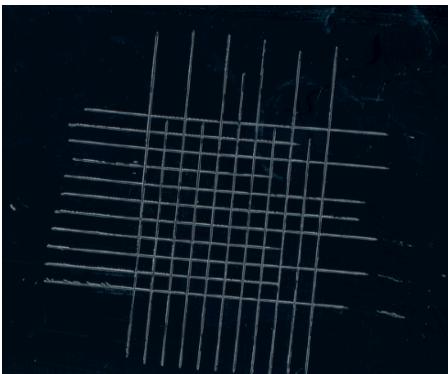
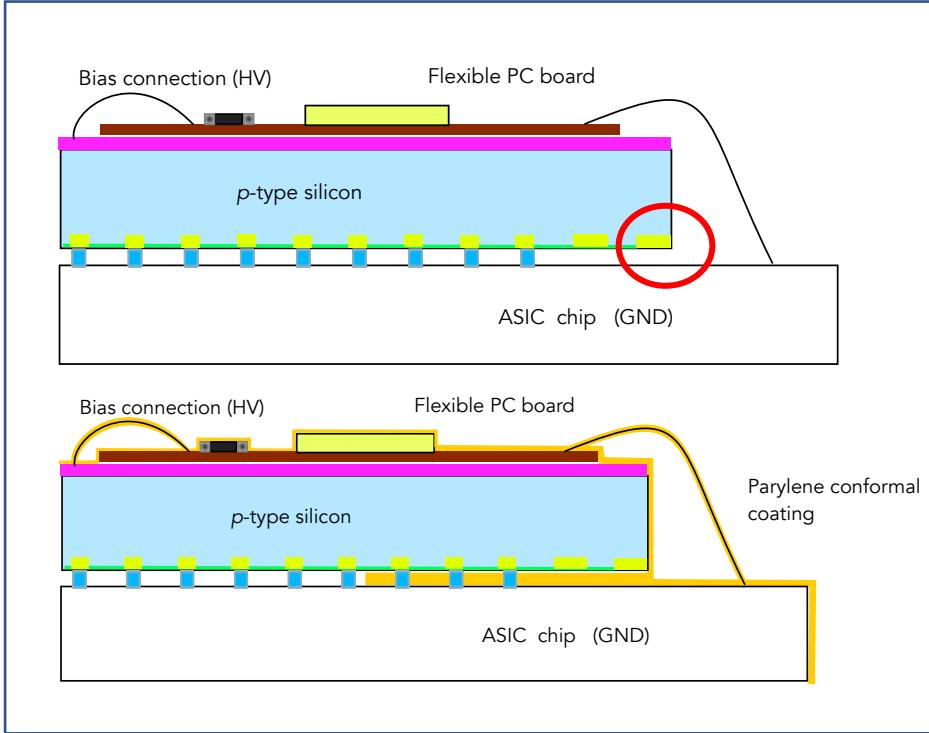
- High radiation tolerance
- Lower bias voltage



Technology challenges

Technology challenges

- Large area ASIC, $20 \times 20 \text{ mm}^2$, large area sensor $40 \times 40 \text{ mm}^2$
- High density, low pitch bump bonding $50 \mu\text{m} \times 50 \mu\text{m}$
- Radiation hardness
- Large temperature range: operating at [-25 to -10°C] to limit radiation damage effects, heat to +20°C during maintenance
 - Avoid delamination of bumps: thin metal flex circuit
- Low-mass services, to reduce X_0
- Serial powering (see [talk by F. Hinterkeuser](#), this session)
- Large Bias voltage across thin air gap ($10\mu\text{m}$) → conformal coating
 - 54 quad modules (RD53a) coated with parylene N
 - Excellent reproducibility and adhesion
 - Both commercial and in-house lab coating
 - Tested after irradiation and thermal cycles



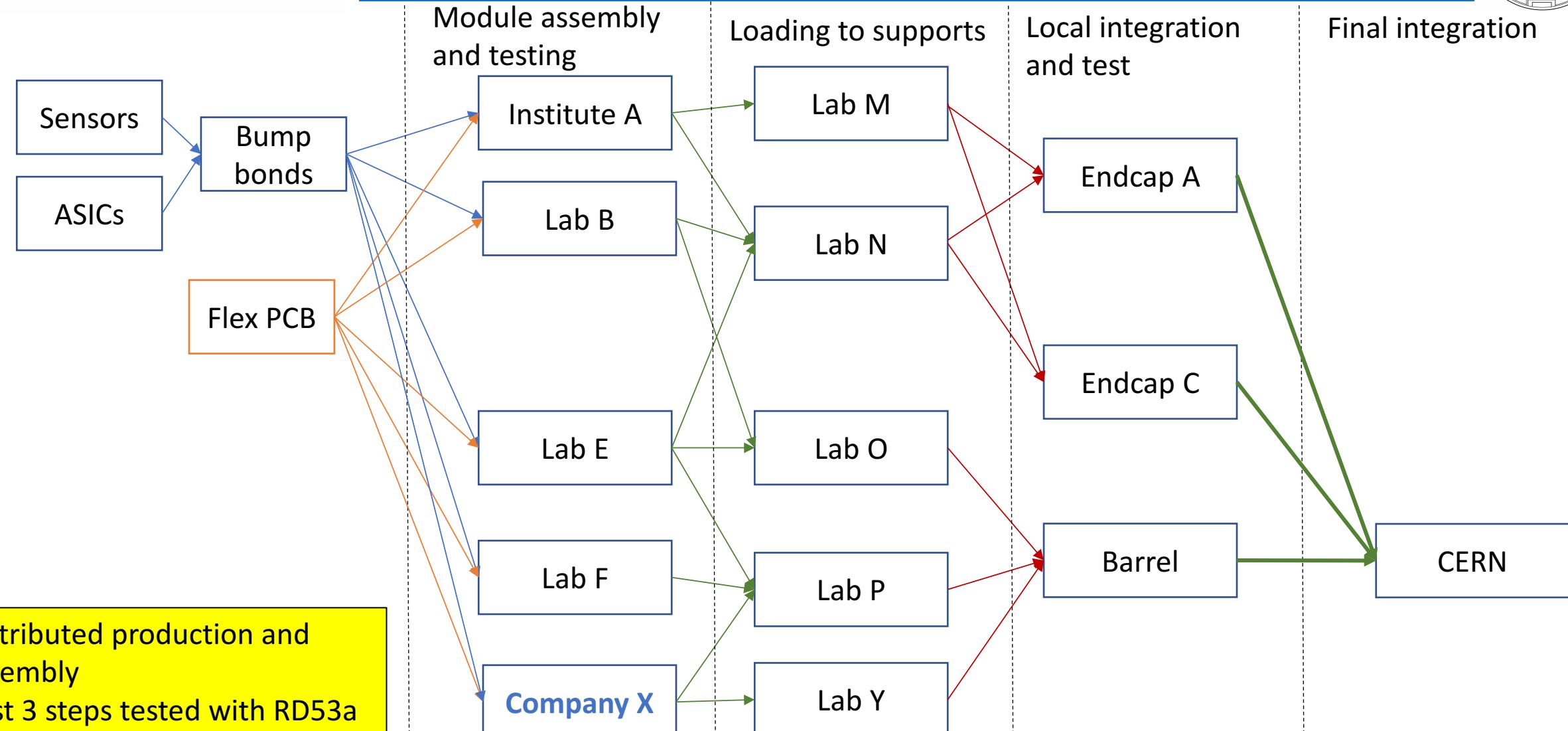
Adhesion tests on Silicon after $1 10^{16}$ neutron eq. cm^{-2} (reactor neutrons on Silicon)

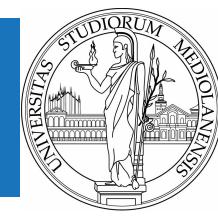
Status of the project



- Finished pre-prototyping using chip “RD53a”
 - half size w.r.t. ITkPix chip
 - 3 types of analog front-ends, for comparison
- Set up complete procedures for assembly, testing, loading on supports
- 158 quad modules built; distributed production among 15 sites
- 20 triplet modules built in four sites
- Procedures set up to ensure uniformity and quality control
- Model of **distributed production** and test finalized for all sites
- Most of flip chip bonding made in companies: SnAg and In bump bonds
- Part of assembly done in companies (Japan) part in labs, where all module testing occurs
- Loading onto support and cooling structure in 4 sites
- Endcaps and barrel will be integrated at CERN
- First version of pre-production modules “ITkPix” chip (RD53b, Atlas flavour) being assembled at present

General Production model





radiation hardness, assembly procedure, test procedure, production yield, loading to supports

RD53a quad

- Irradiated at CYRIC (5×10^{15} neq/cm 2), parylene coated,
- then thermal cycled 100x from -40°C to +25°C
- no new disconnected pixels (<0.07%), no delamination of parylene.

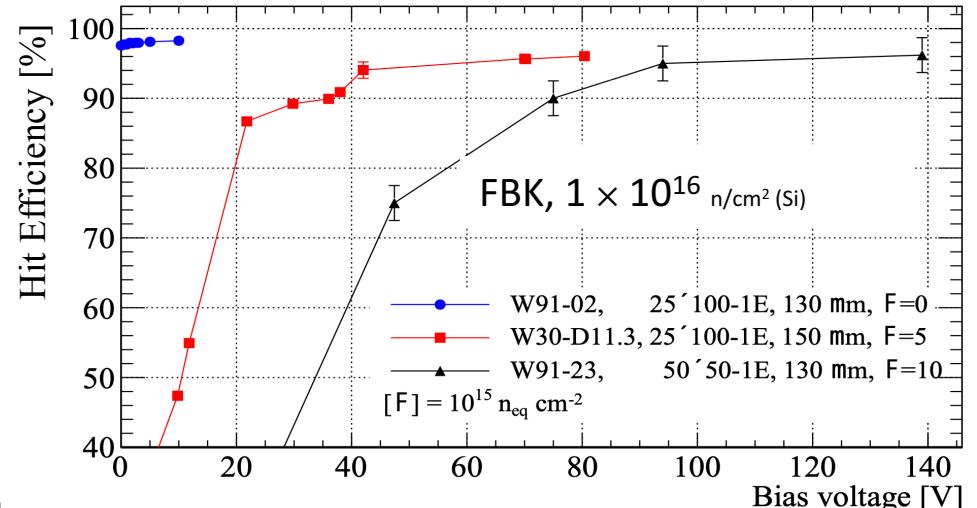
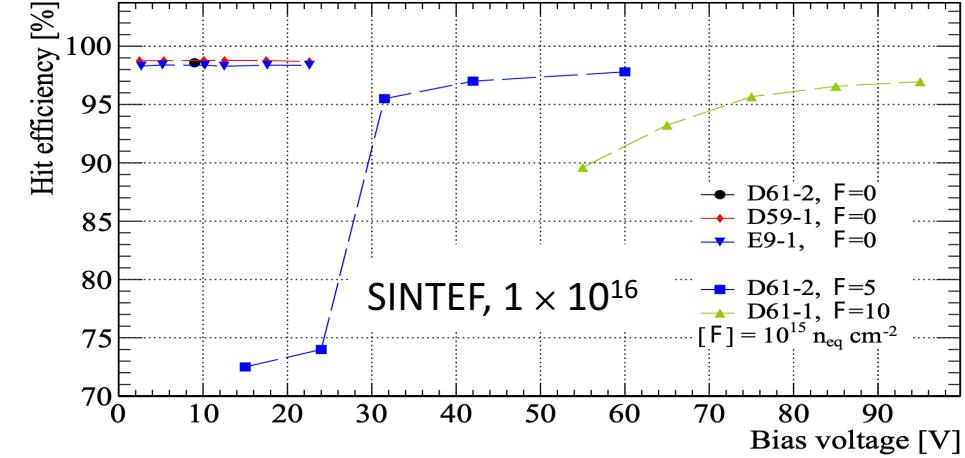
RD53a triplets 3D sensors

- Irradiated to 1.6×10^{16} n.eq/cm 2
- Fully efficient at $V_{bias} < 100$ V

ITkPixV1.0 quad (4 of)

- Parylene coated
- Irradiated to 6.3×10^{15} n.eq/cm 2
- Thermal cycled 100x [-55°C +60°C]
- No delamination, no disconnected bumps

3D sensors



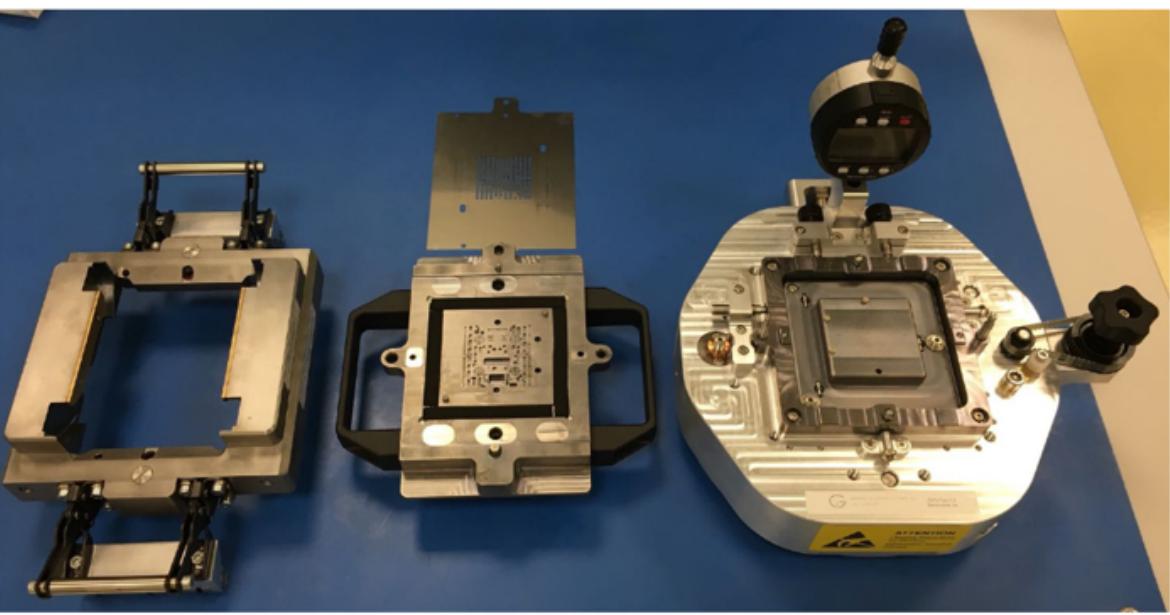
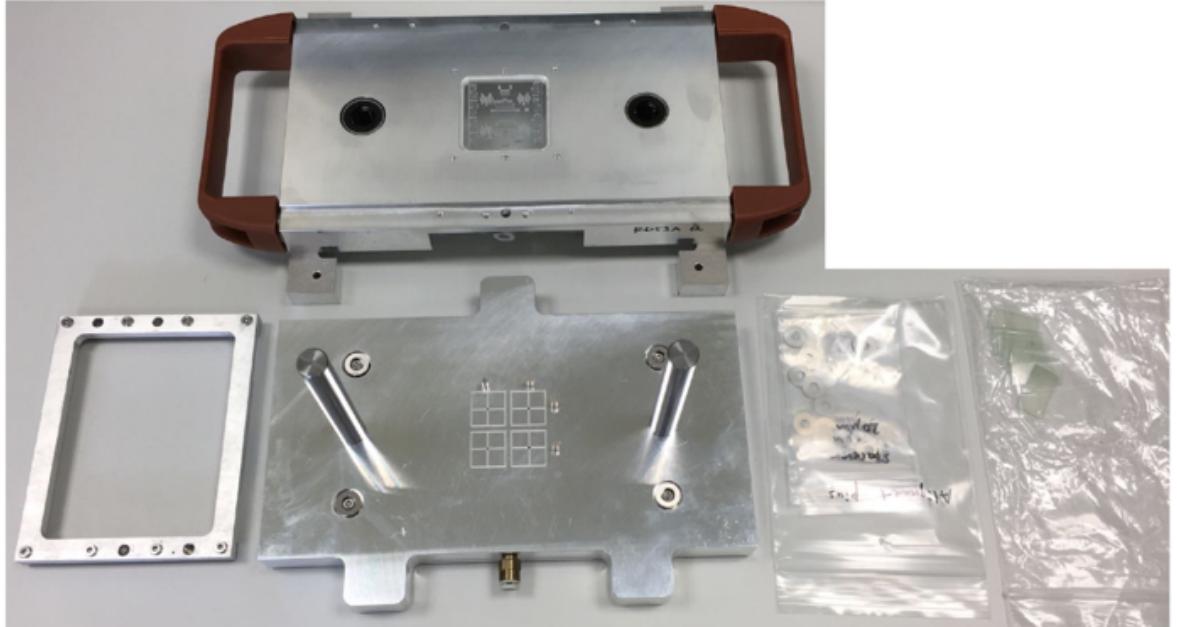
Highlights from RD53a prototyping



radiation hardness, **assembly procedure**, test procedure, production yield, loading to supports

Module assembly = gluing flex PC board + wire bonding + metrology

Using stencil + precision tools. Curing at room temperature

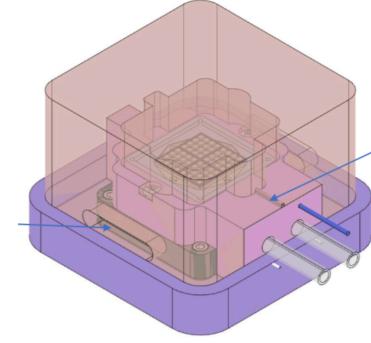


Gantry positioning also used at one assembly site.

Highlights from RD53a prototyping



radiation hardness, assembly procedure, **test procedure**, production yield, loading to supports



QC process for all modules to catch low quality modules put in place for prototyping

wafer probed chips, x-ray images of flip-chip assemblies,

Sensor I-V: on wafer, flip-chip, assembly, thermal cycles: look for assembly mishap, chipping

Electrical tests and disconnected bump: as assembled, after thermal cycles: weak bonding (wire & bump)

Cold test at operating temperature (-15°C): defects induced by thermal stress (delamination)

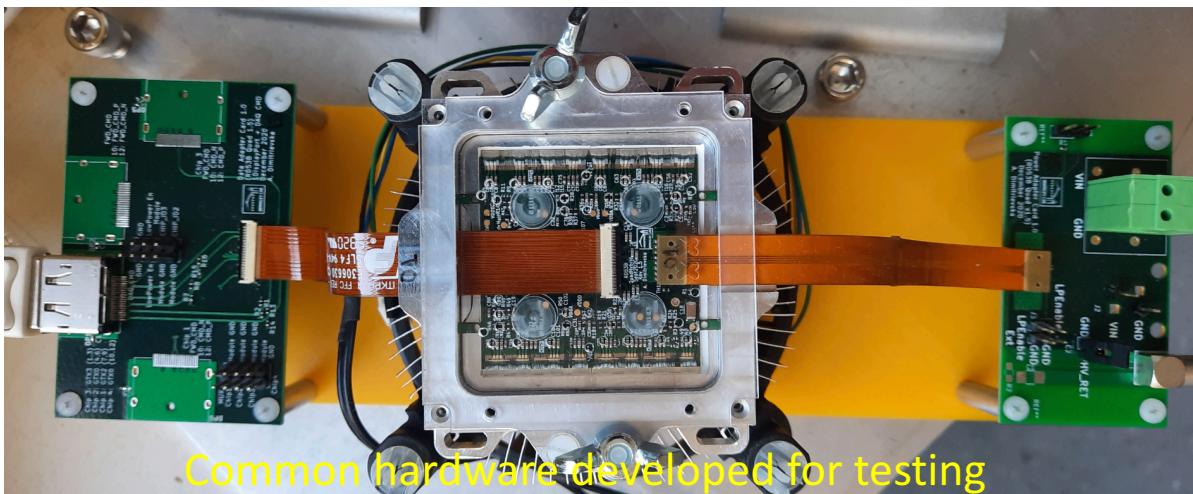
Burn-in at room temperature (30°C) on module: look for chip early failure

3 categories:

- test of module quality;
- check that module still functional after process,
- module characterization and final “working point setup”

Full use of database to store results

Use in ITkPix preproduction with extended site qualification



Highlights from RD53a prototyping



radiation hardness, assembly procedure, test procedure, **production yield**, loading to supports

Production yield difficult to quantify based on the RD53a.

Yield of a good quad module (4 chips communicating) **80% when production grade equipment was used.**

Quad: front-end chip and sensor mismatch in overall size (50% of pixels not connected)

Three different analog circuits on the same chip made electrical tests time consuming

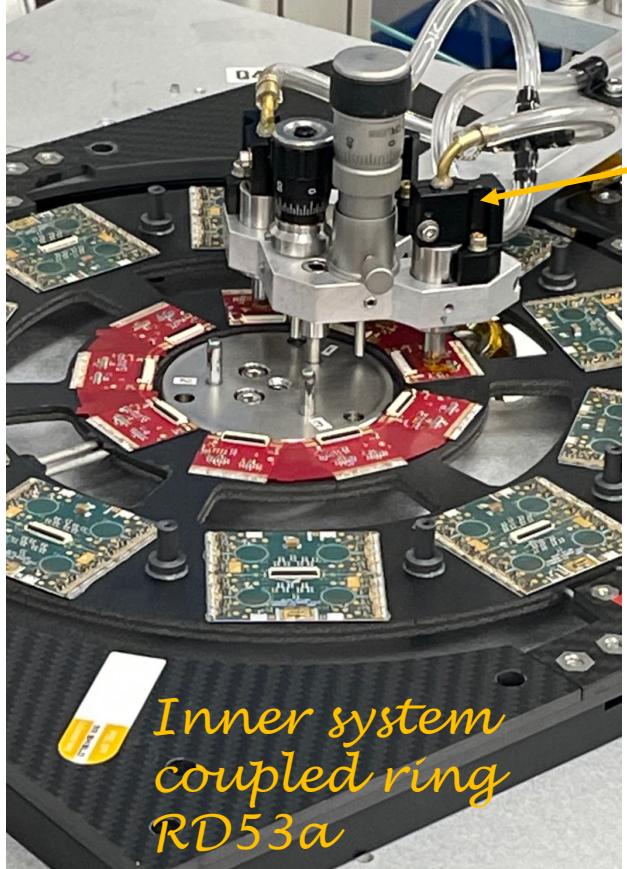
- No hint of early chip failure;
- Test procedures detected defective assemblies

Yield to be re-checked with ITkPixV1.x

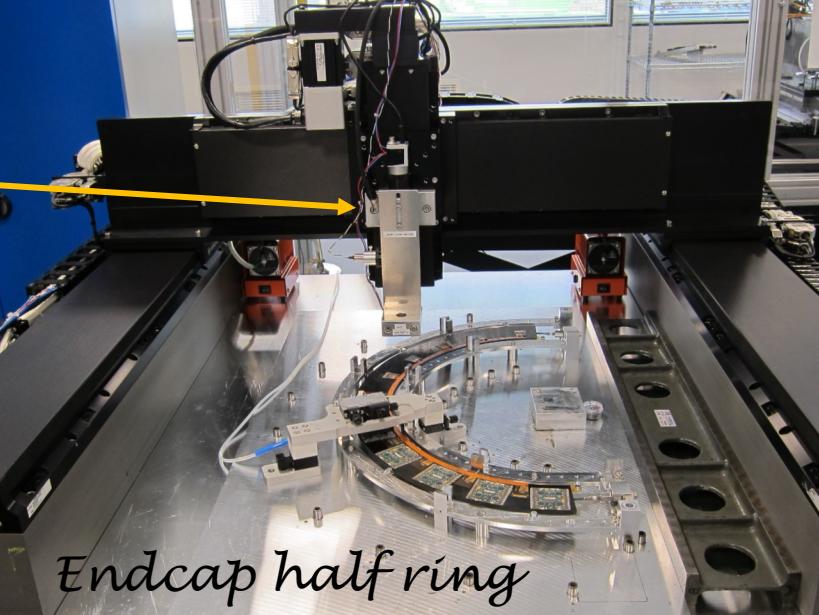
Triplets have low statistics, production approach will be more detail-oriented

Highlights from RD53a prototyping

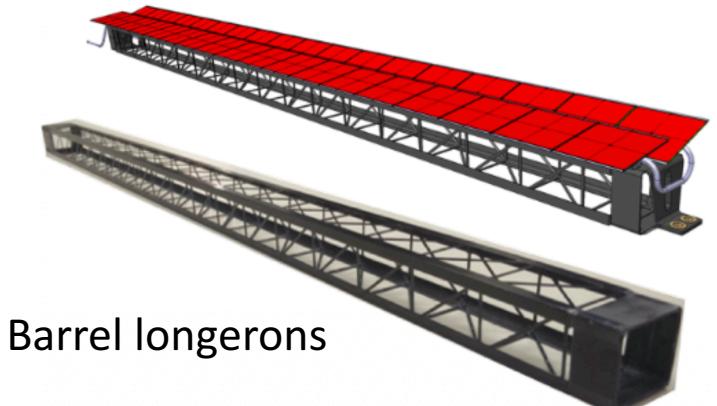
radiation hardness, assembly procedure, test procedure, production yield, **loading to supports**



Tools developed
for precision placing



Building up system test infrastructure for testing
loaded local supports (RD53a)
Preparing for thermal cycles of
bare and loaded support structures



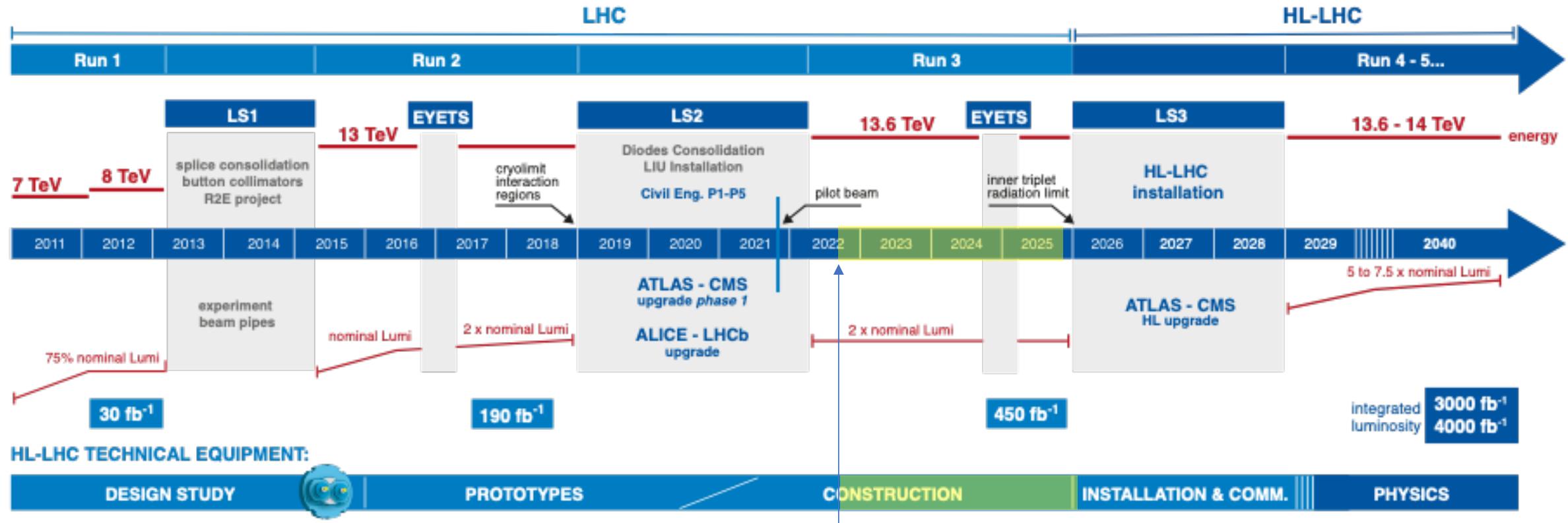
Timeline

ITkPixV1 pre-production for \leq one year

- Establish production rate and confirm yield and production model

Submission of RD53c final FE chip this summer

From 2023, two years to complete production (10^4 modules) before long shutdown-3 (Jan 2026)



Conclusions

The Itk Pix project is progressing:

RD53a prototyping exercise finished

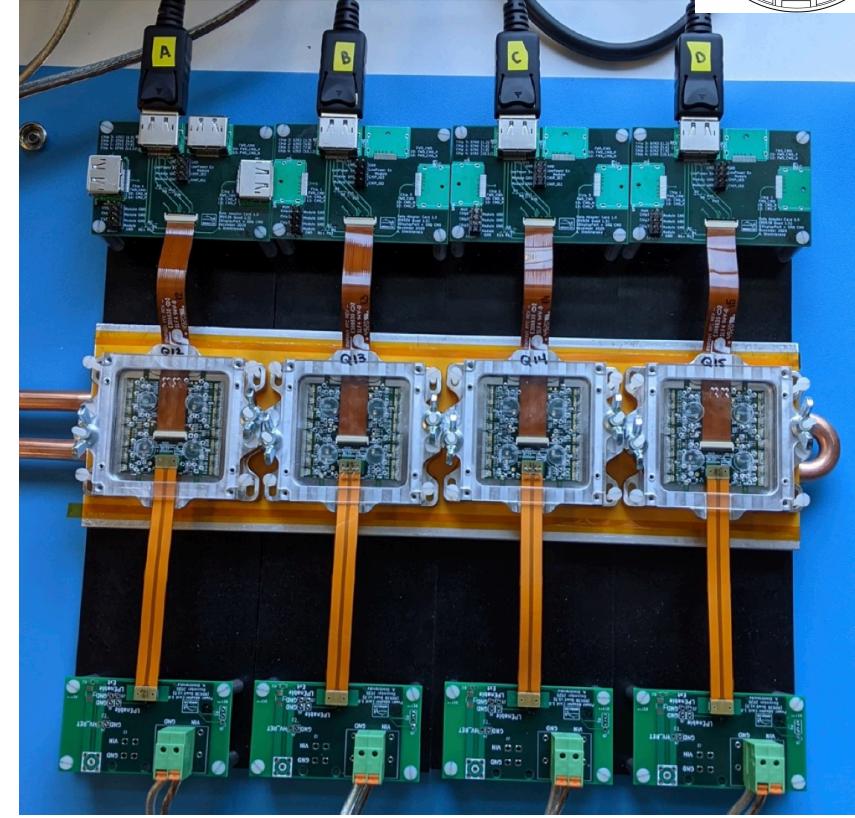
Was very important to establish procedures and qualifying labs

Production model being detailed on the RD53a experience

Next steps: gear up for scale expansion from few to 100's of modules

ITKpix V1 modules being built

- Finalize the electrical test procedure
- Qualify sites for production
- Have a reliable estimation of yield
- Set up and commission the system test at local support level
- Demonstrate to be able to produce on time all the required modules
- Demonstrate to be able to correctly place on local supports, connect and test
- Create a culture of consistent quality check in a distributed production model



*Thank you for
your time
and
for your questions*