



Initial ITkPixV2 Test Results and Qualification Status

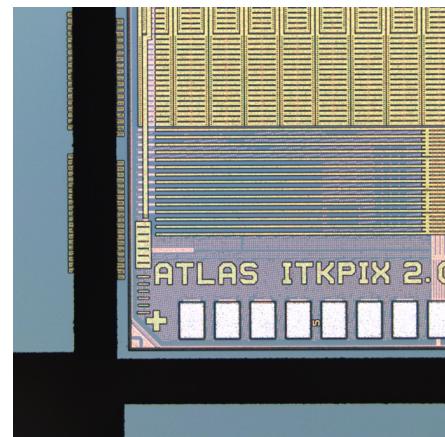
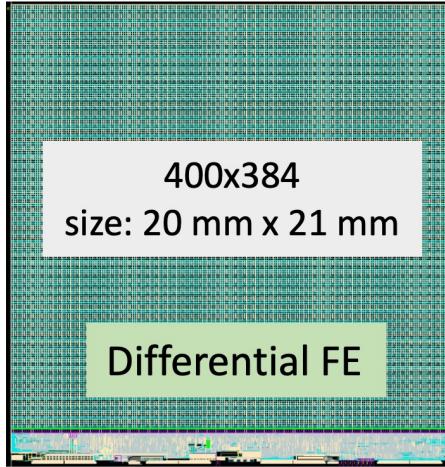


Maria Mironova on behalf of the ITkPixV2 testing team and RD53 collaboration

ITk Week
14 September 2023

Introduction

ITkPixV2



- Recap:

- ITkPixVI submitted in March 2020, mask change due to major issue in ToT memory submitted in October 2020 (ITkPixVI.I)

- CROCvI submitted in June 2021

- ITkPixV2 submitted in April 2023

- Major improvements in verification → found and fixed many hidden bugs

- Full SEU simulation → identified and improved many weak spots

- Late identification of major bug in data merging/link sharing in testing → simple fix but required rerunning full flow (~10 weeks)

- Many improvements implemented (full list in [backup](#))

- Proper fix to the ToT memory bug in ITkPixVI (already validated in CROCvI)

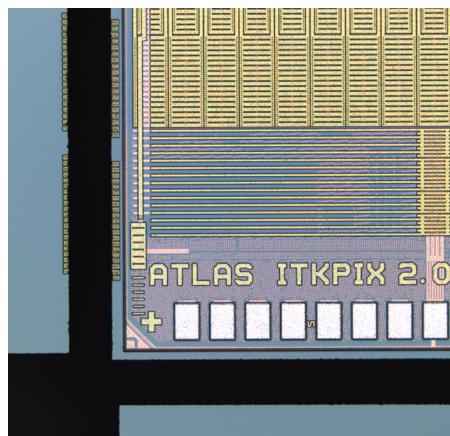
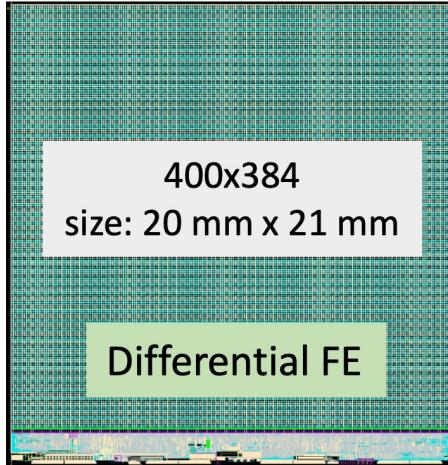
- Stability against single-event transients

- Startup and powering stability

- Improvements and additional monitoring sensors for temperature and radiation

Introduction

ITkPixV2

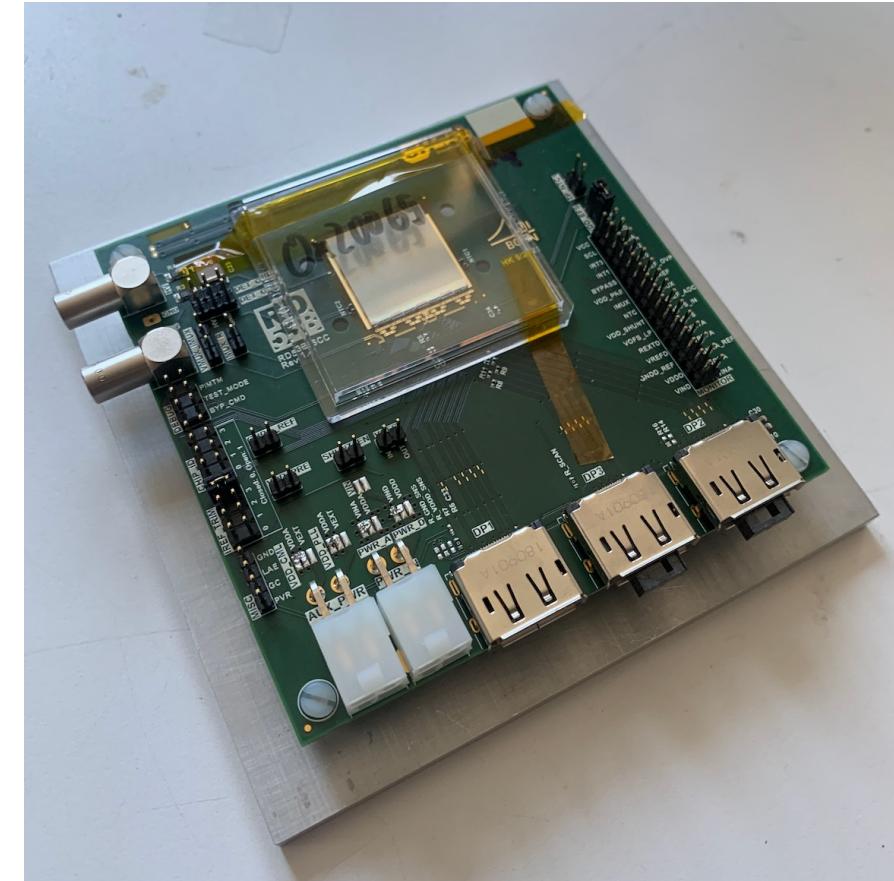
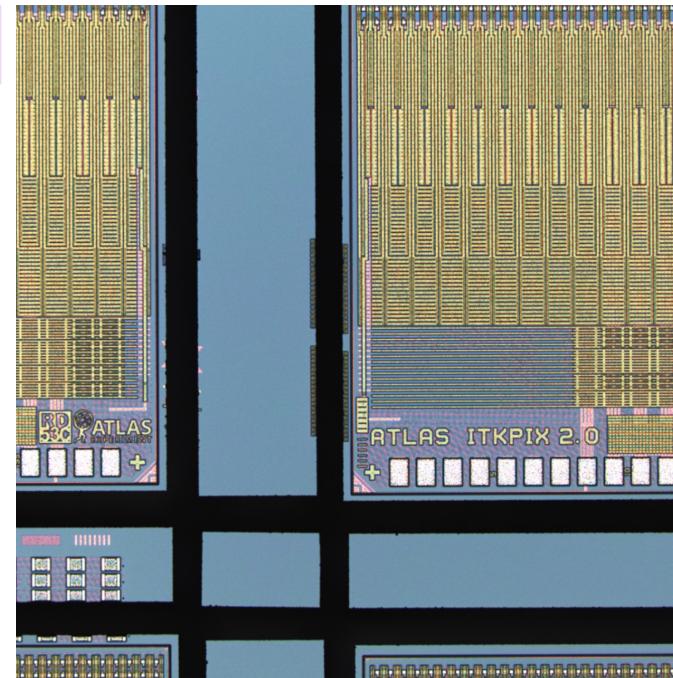
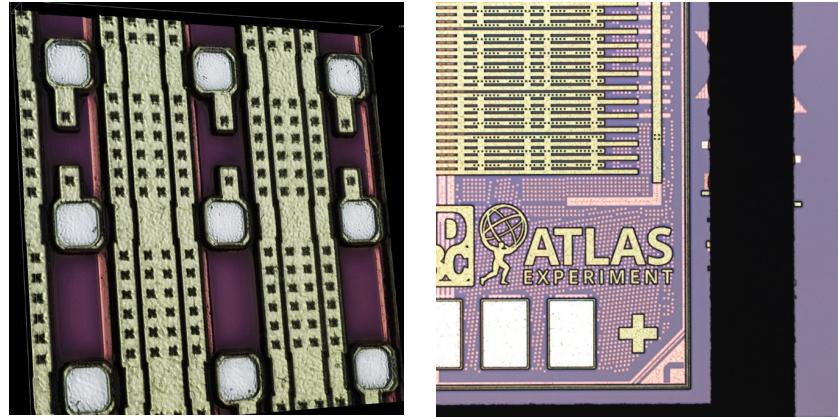


- Received 16 engineering run wafers on the 26th of June
 - 4 reserved for wafer probing sites (Bonn, Glasgow, Paris, Hong Kong)
 - 2 sent for dicing immediately (1 at APD, 1 at DISCO) for loading onto SCCs
 - 1 for Torino (CMS) → help with testing and preparation for CROC v2
 - 9 held at Bonn for probing and early hybridisation
- Currently in the process of testing on SCCs and validating that all chip features work as expected

First Start-Up of ITkPixV2

- Received first ITkPixV2 **diced wafer** at the end of July 2023
- Diced chips look good as expected
- Assembled chips on single-chip testing boards (SCCs)
- First power-up was successful and chip currents are within 10% of expectation

Diced ITkPixV2 wafer

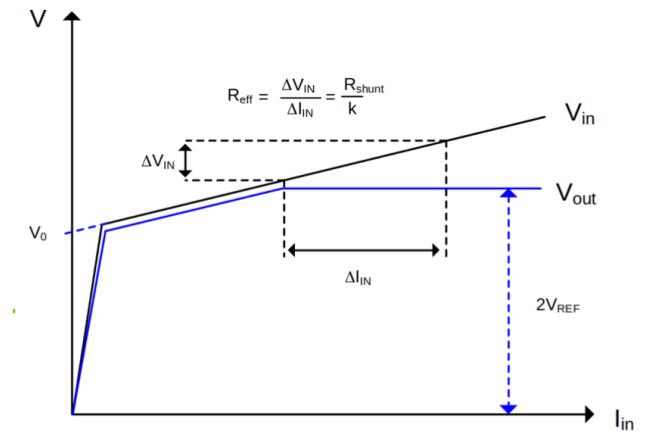


Assembled single chip testing board

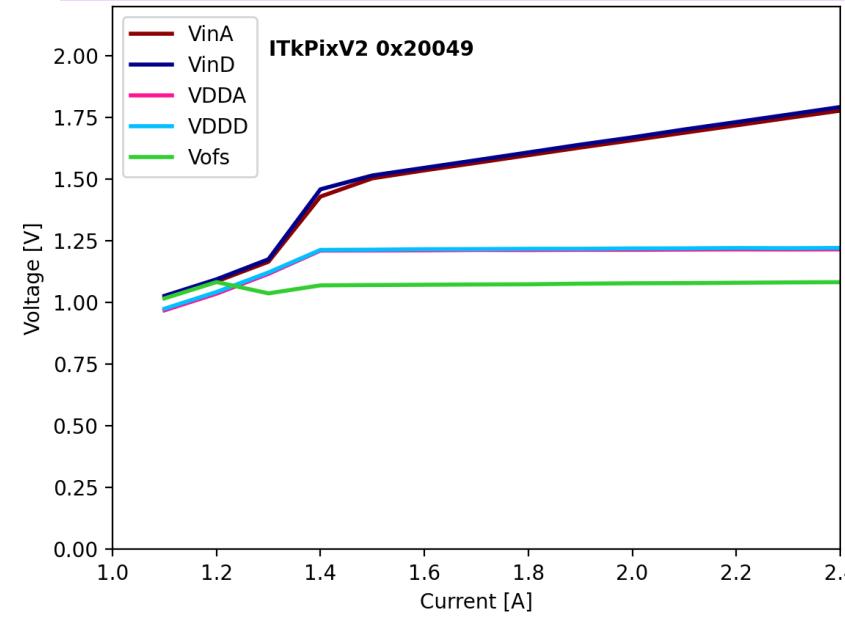
SLDO performance

- ITk modules will be operated in serial powering using a shunt-LDO circuit in the readout chip
- Use **SLDO start-up curves** to characterise chip start-up behaviour
→ Results look as expected for ITkPixV2 and match what was observed for ITkPixVI
- No start-up issues observed down to temperatures of -50 C

Schematic of SLDO VI curve

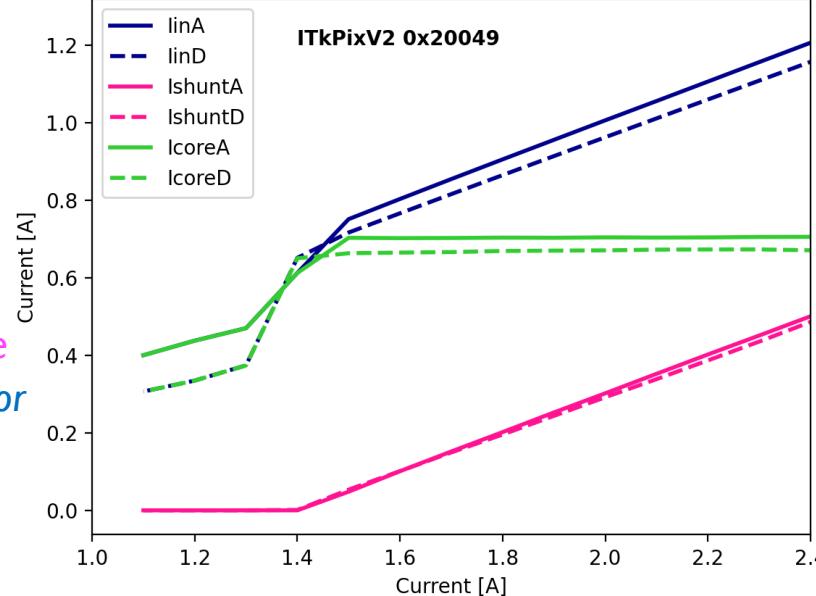


SLDO voltages



V_{inA} – analog input voltage
 V_{inD} – digital input voltage
 V_{DDA} – analog regulator output voltage
 V_{DDD} – digital regulator output voltage
 V_{ofs} – offset voltage

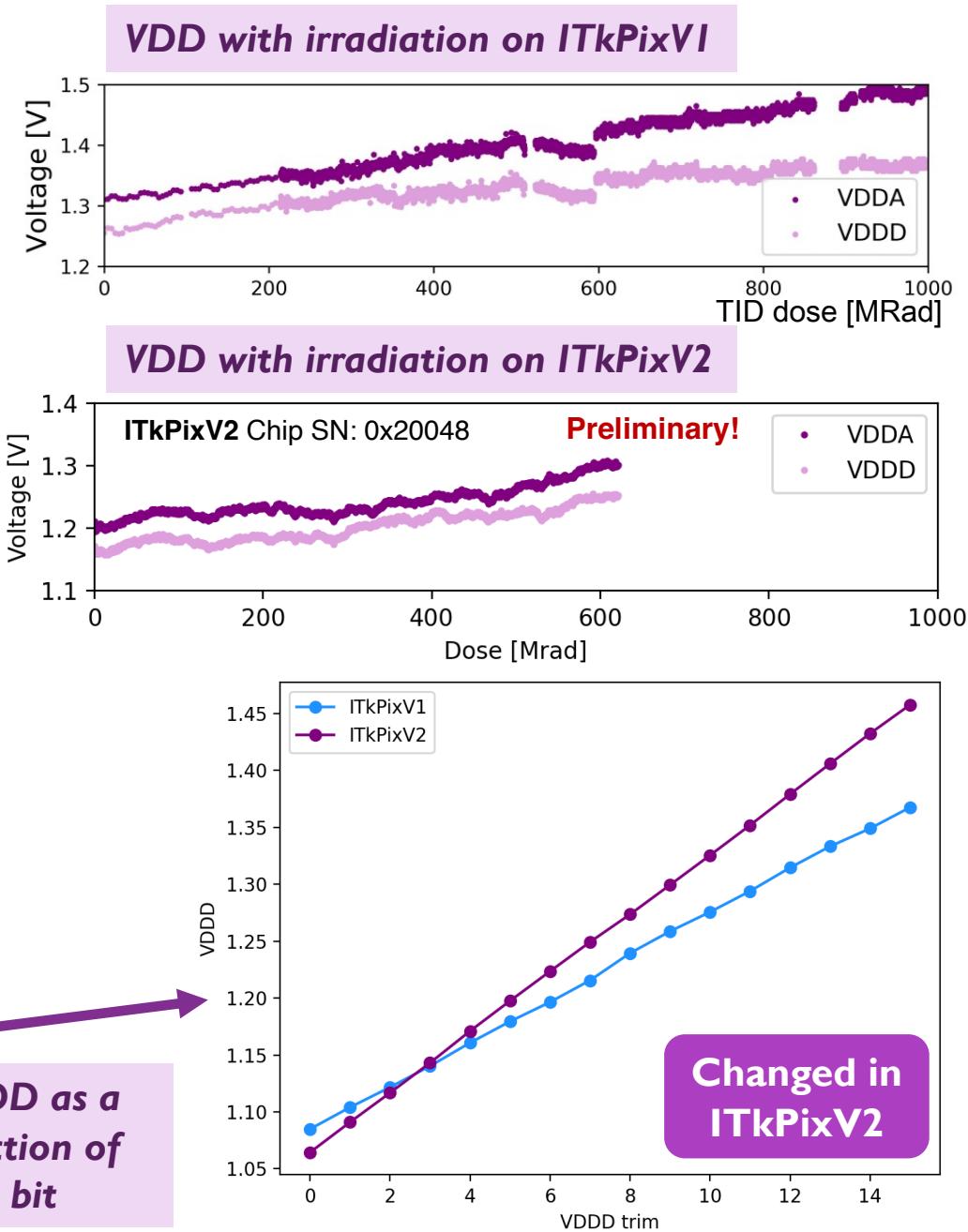
SLDO currents



lin – chip input current
 I_{core} – current consumed by chip
 I_{shunt} – current consumed shunt element

VDD voltages

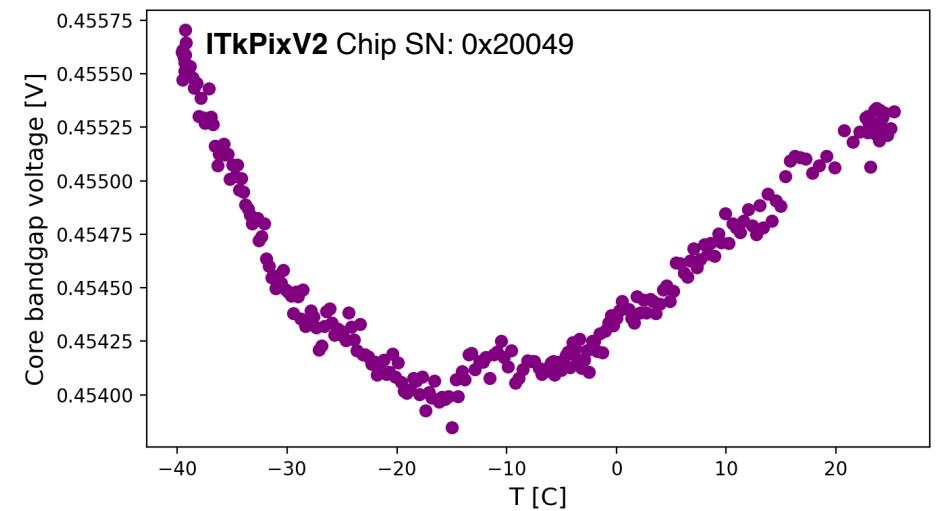
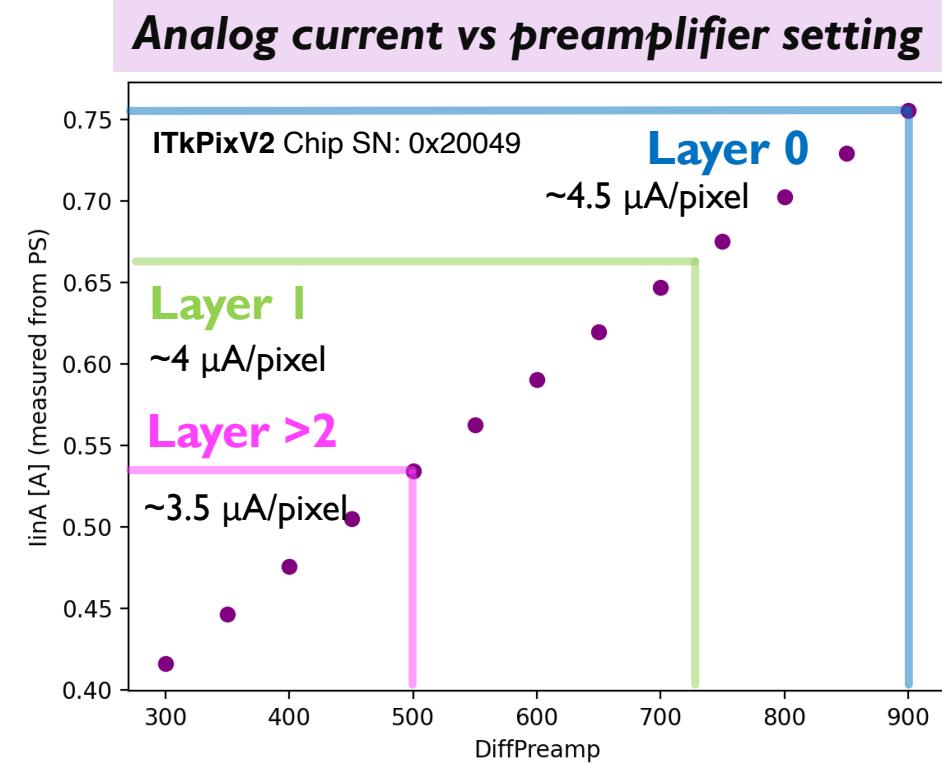
- VDDA/VDDD voltage level can be controlled by chip configuration setting ("trim bits")
 - Operational setting should be **as close as possible to 1.2 V**
 - Saw in irradiations of ITkPixVI that **VDDA/VDDD voltage increases** due to change in bandgap voltages with irradiation
 - VDDA increased significantly more than VDDD (+14% for VDDA, +9% for VDDD after 1 Grad)
- likely caused by increased mismatch of current mirrors caused by non-uniform chip metallisation layers
- Included two related modifications in ITkPixV2 design:
 - More uniform metallisation layers → first irradiation results look promising
 - Larger trim bit size → Larger range of VDDA/VDDD possible, effect as expected



Chip currents

- **Analog input current:** Preamplifier consumes most of the analog current
 - Verified linear behaviour with DAC
 - Different settings intended for different ITk detector layers
 - Lower values in the outer layers of the detector to reduce power consumption (at the expense of more noise & time-walk)
- **Bias network** based on bandgap reference circuits
- Generates reference voltage/currents for analog front-end etc
- Designed with low sensitivity to temperature variations (4% over a 70 °C range)

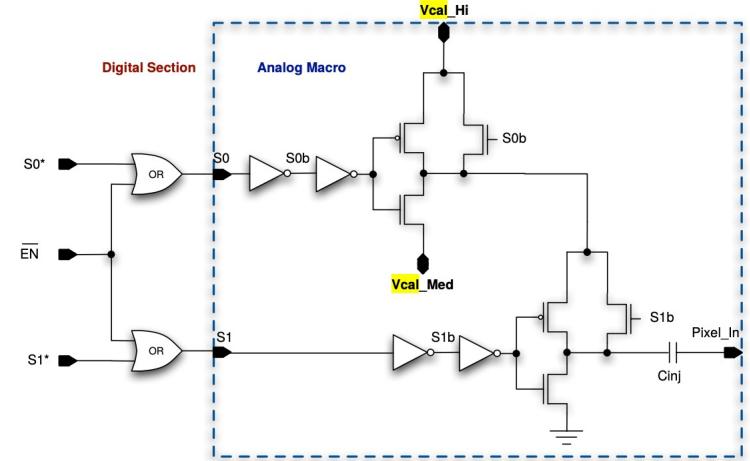
Temperature dependence of core bandgap voltage



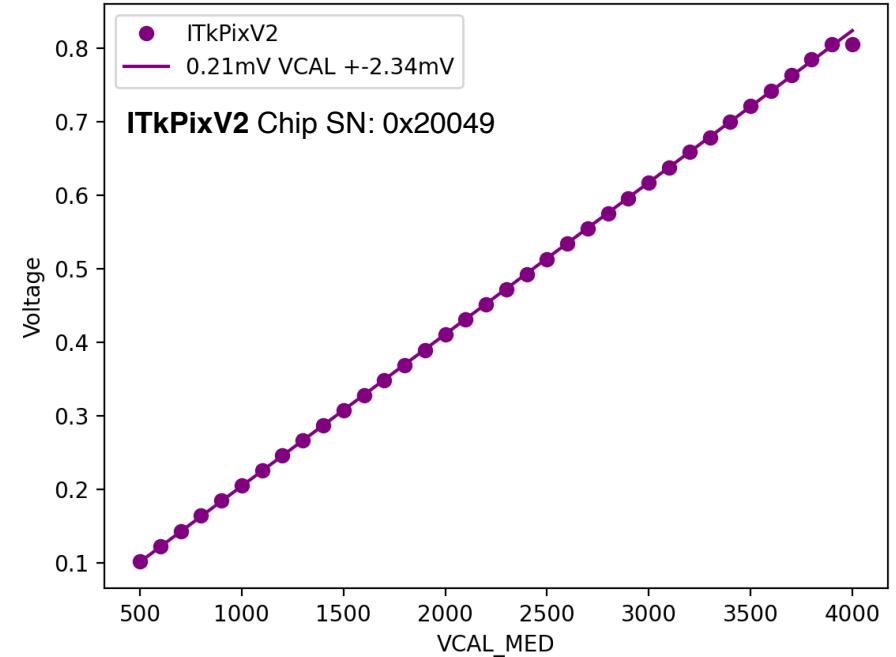
Injection calibrations

- Charge injection circuit implemented in each pixel for characterisation measurements
 - Circuit needs to be calibrated to get conversion from DAC setting to voltage
 - Slope measured to be **~0.2 mV/DAC, consistent with ITkPixV1**
 - Charge injected using **injection capacitor**
 - Injection capacitance can be measured precisely using dedicated circuit in the chip
 - Observe injection capacitance of **7.7 fF**
- Good agreement with expectations (design value 8 fF)

Charge injection circuit



Injection circuit calibration

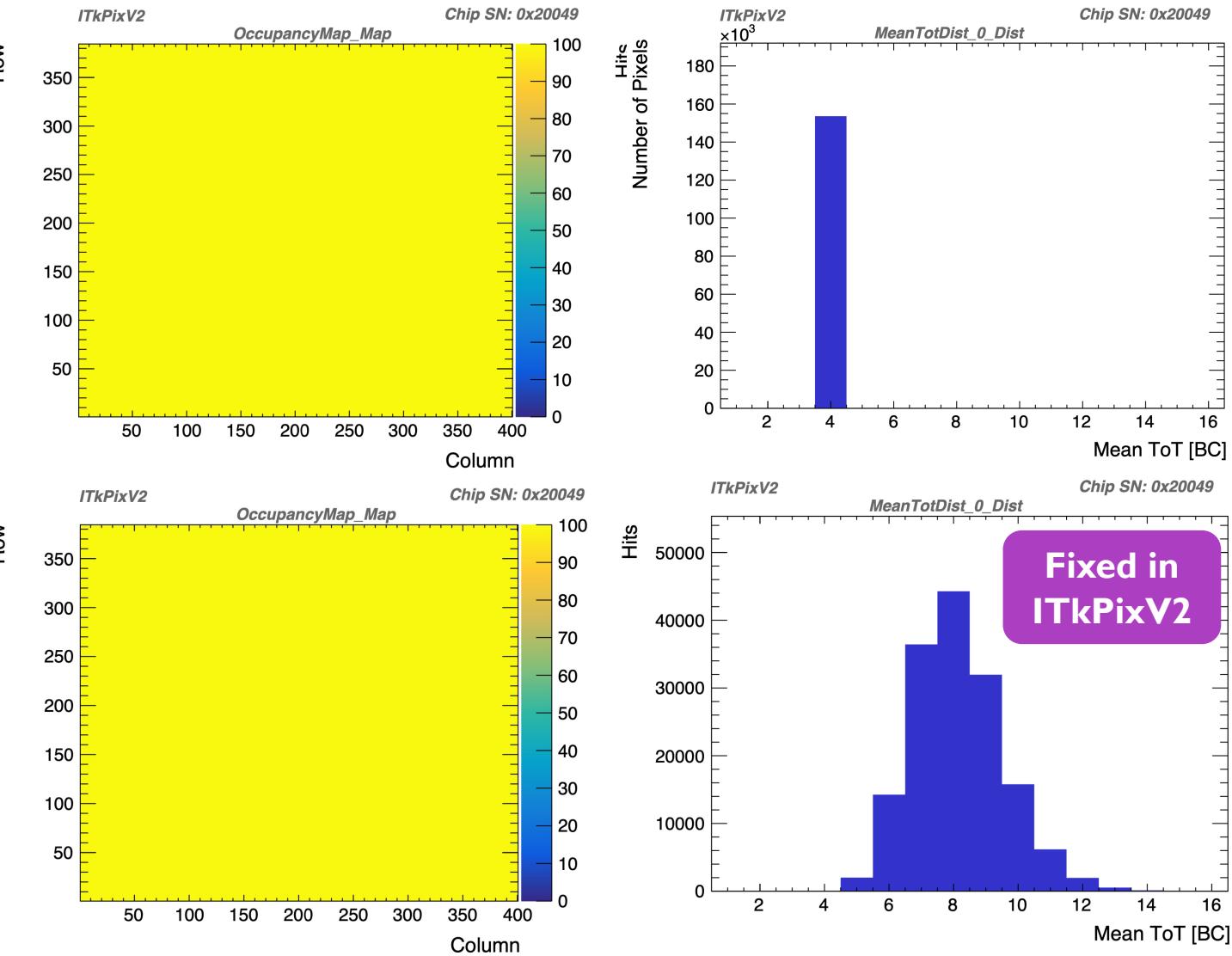


Digital and analog scans

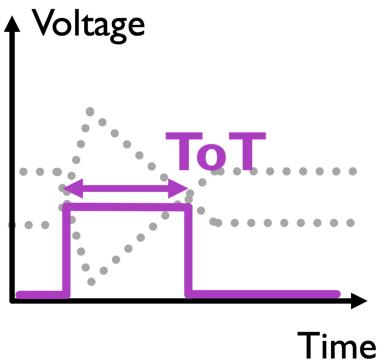
Digital scan

- Inject a charge a certain amount of times, and count how many of the injections each pixel sees
- **Digital scans:**
 - Using digital injections
 - Observe uniform map with observed number of hits matching the expected
 - Very narrow ToT distribution
- **Analog scans:**
 - Using analog injection circuit
 - Observe reasonable ToT distribution → **ToT works in ITkPixV2**

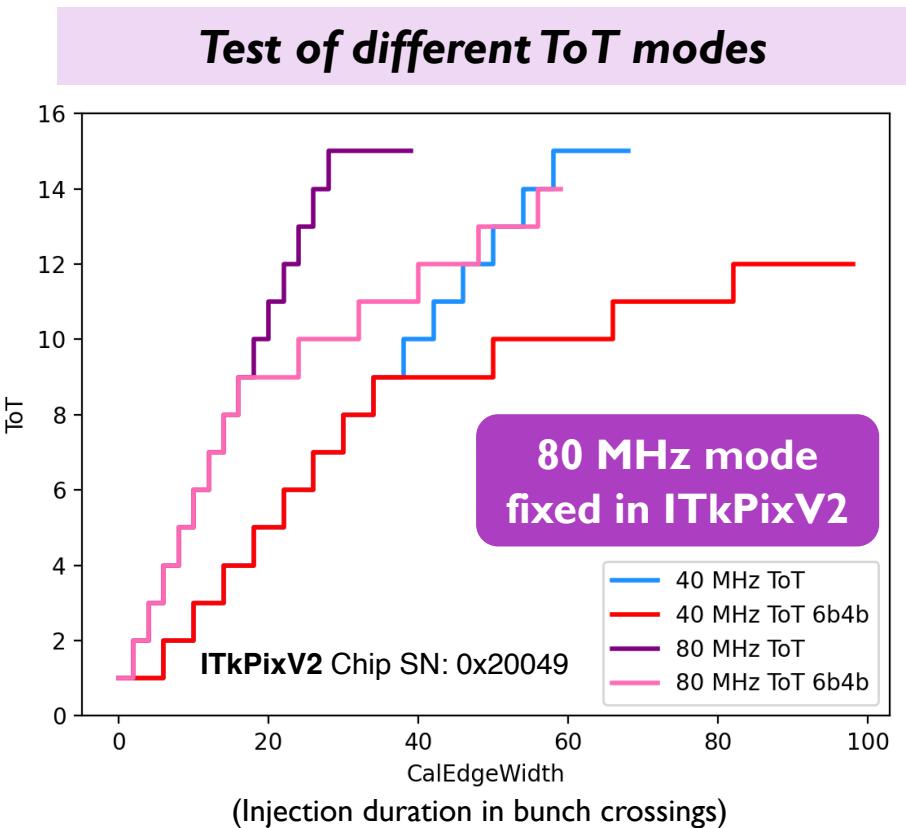
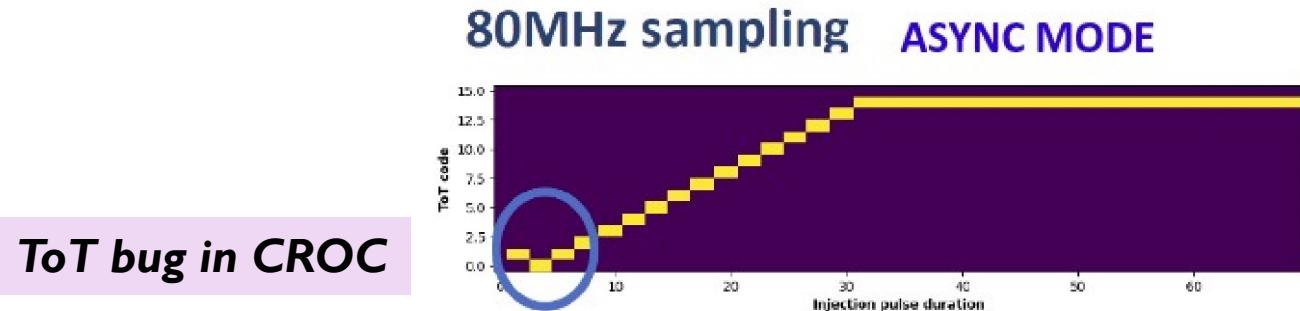
Analog scan



ToT modes in ITkPixV2

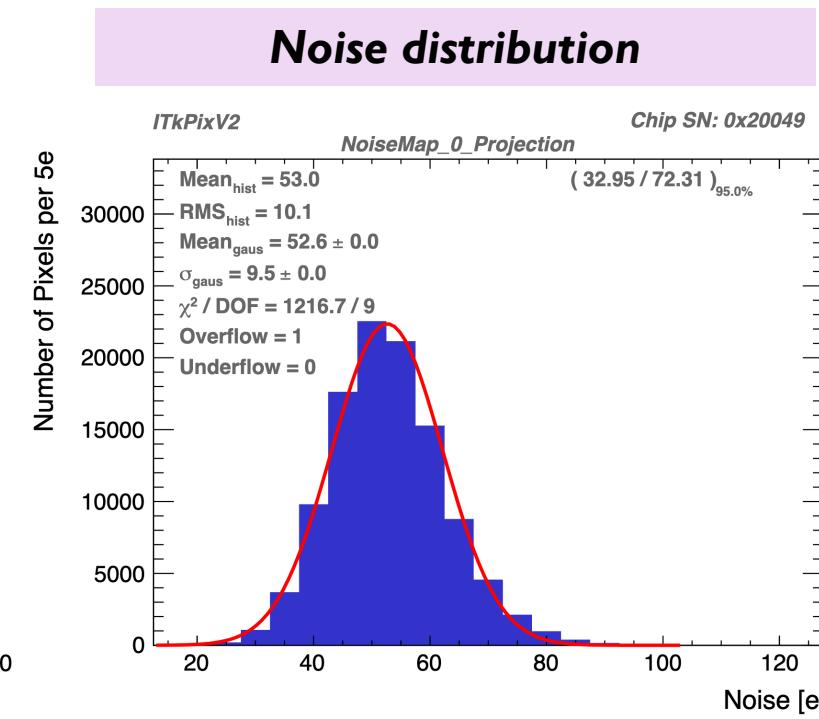
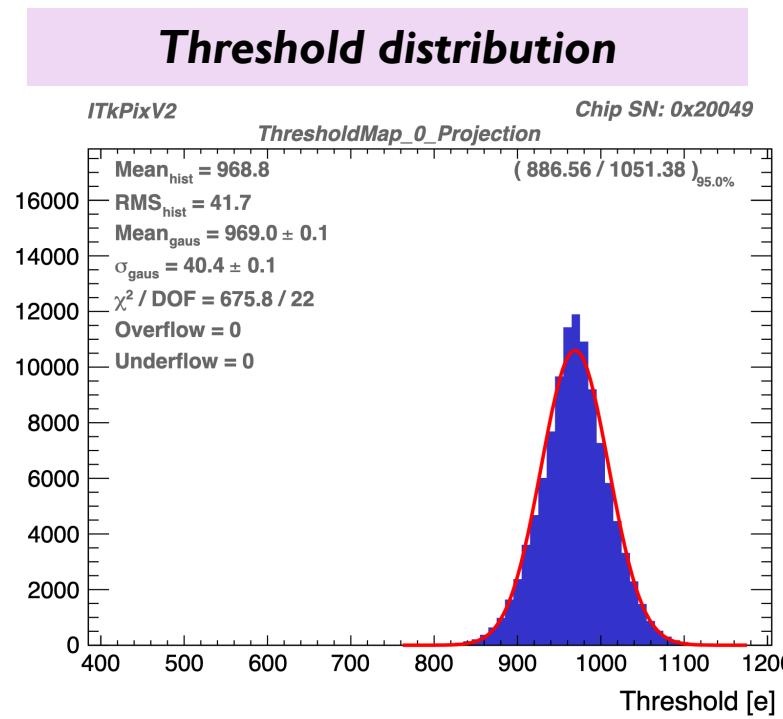
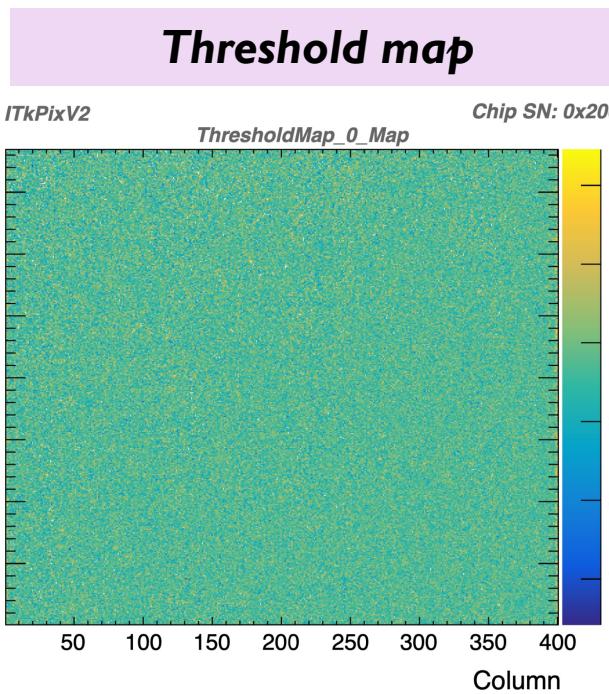


- Different time-over threshold (ToT) modes available in ITkPixV2
- Validate ToT value as a function of injection duration of digital injection
- **80 MHz ToT** has twice the slope of 40 MHz ToT, as expected
→ Additionally, bug fixed for 80MHz ToT which was observed in CMS CROC chip v1
- **6-to-4 bit ToT** available with increased step sizes at longer injections/higher charges
→ **All ToT modes verified to work in ITkPixV2**



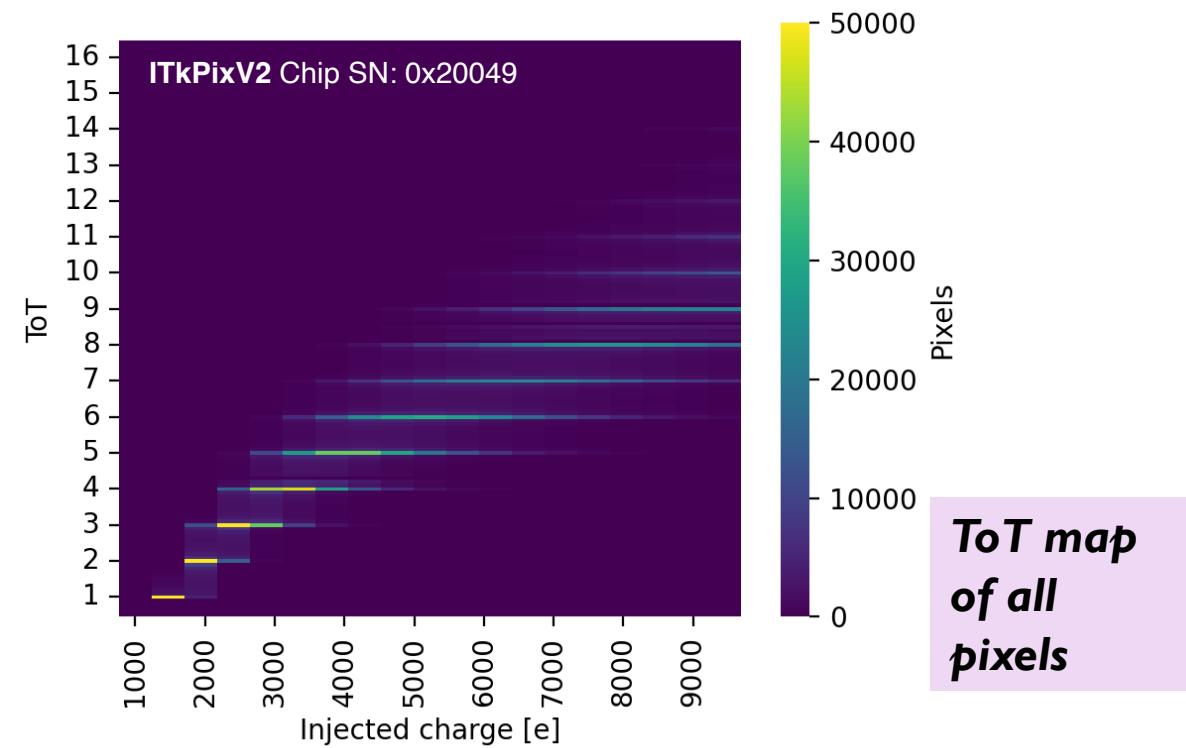
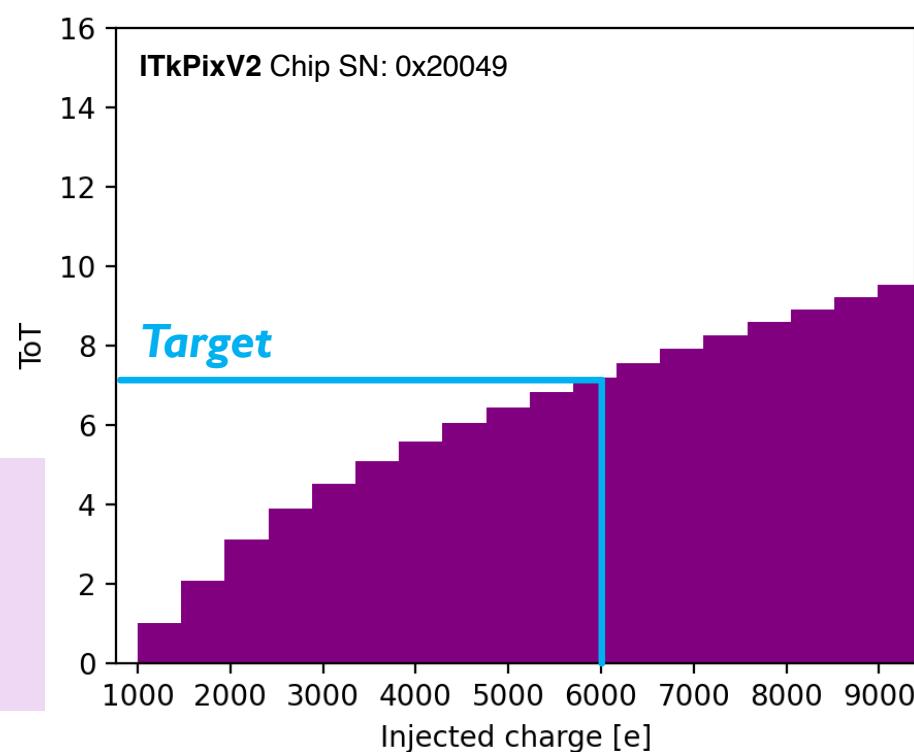
Threshold tuning

- Can tune chip threshold value using global and pixel-specific parameters
- Threshold tuning works as expected in ITkPixV2, tested with targets of 1500e and 1000e
- **Threshold Mean = (968.8 ± 41.7) electrons**
- **Noise Mean = (53.0 ± 10.1) electrons**



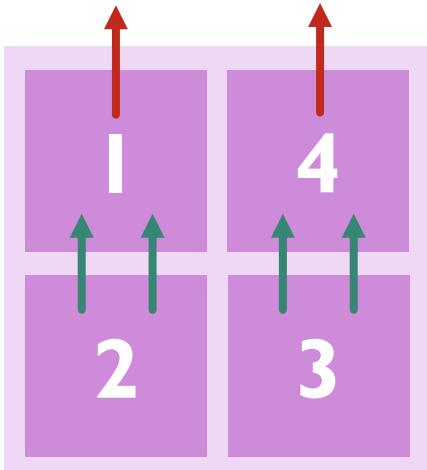
ToT tuning

- With working ToT functionality, it is possible to tune ToT to have a particular ToT at a given charge
- ToT tuning works**, for example with a target of 6000 electrons at a ToT of 7
- Verify ToT tuning by measuring ToT as a function of injected charge

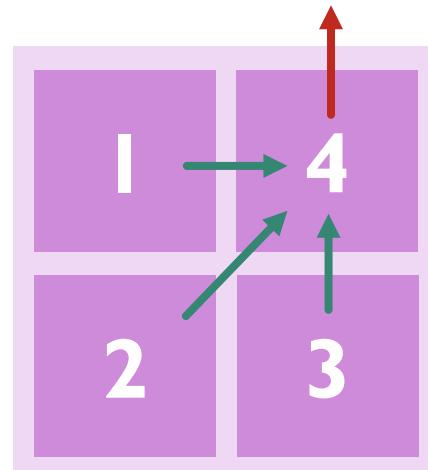


Data merging

- In ITkPixVI data merging did not work properly for all delay values between primary and secondary, due to bug in automatic phase detector
- Fixed in ITkPixV2, and included possibility to manually select phase
- Fix verified in testing in setup with two single chip cards at CERN (not quad modules yet)

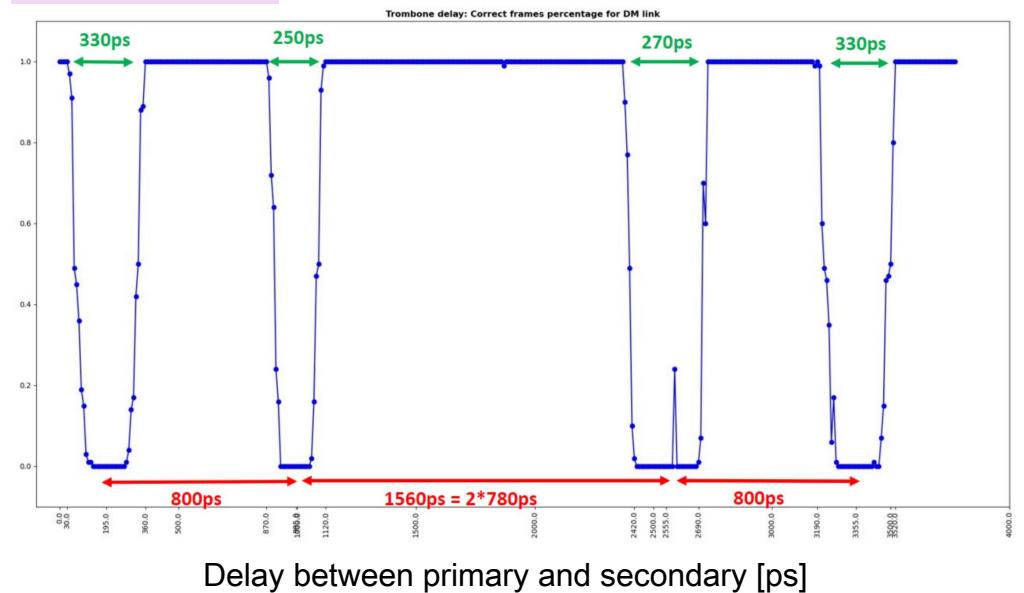


**2 to 1
data
merging**

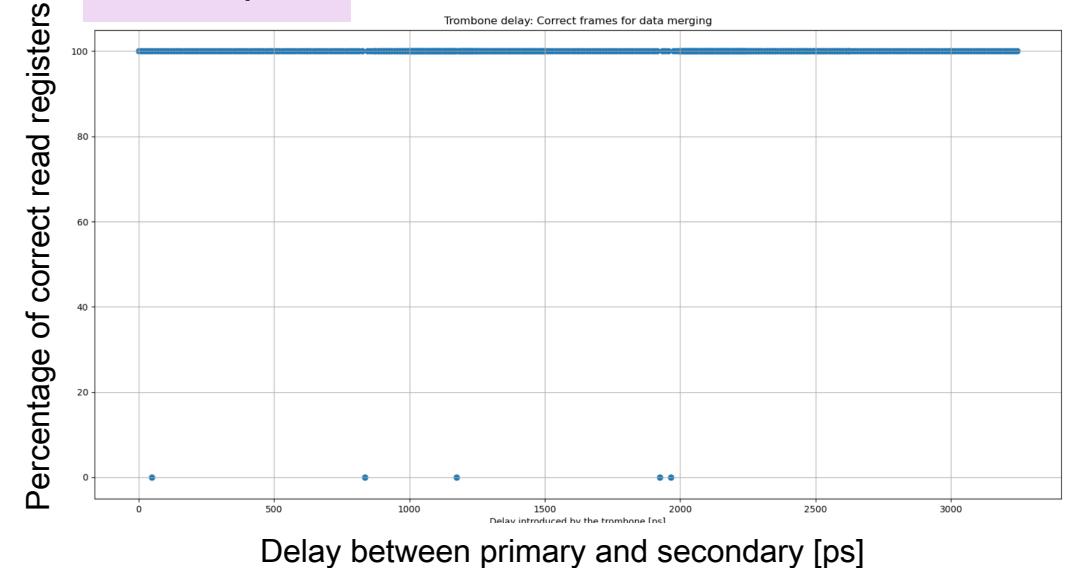


**4 to 1
data
merging**

ITkPixVI.I



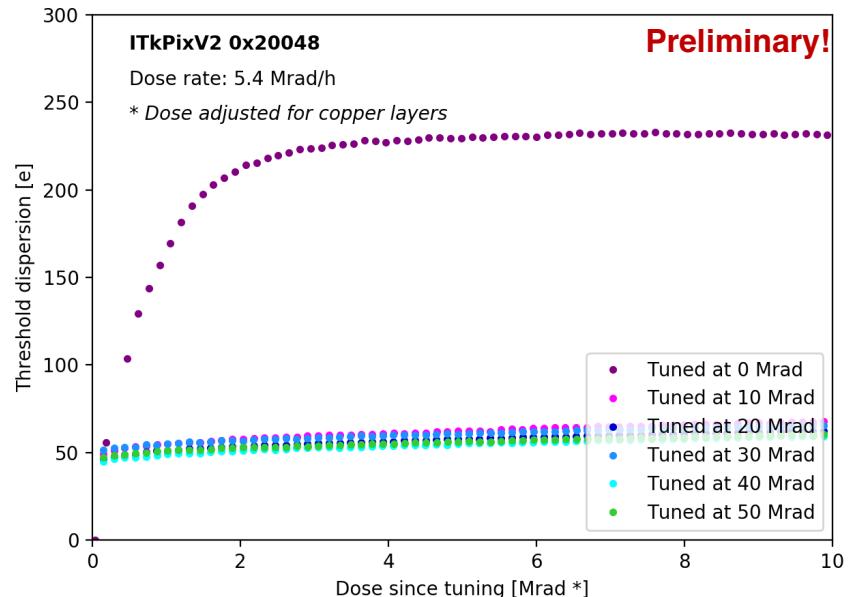
ITkPixV2



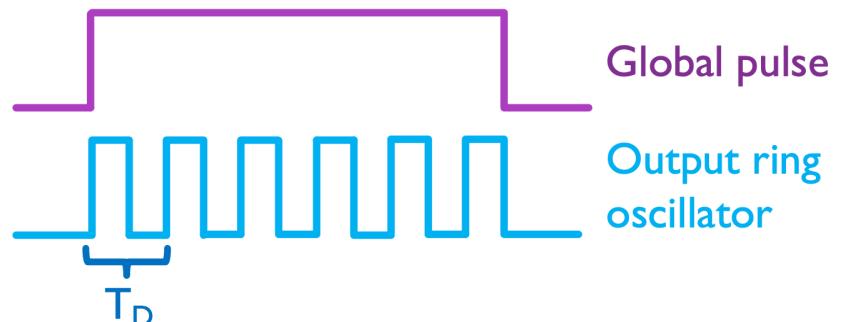
X-ray irradiations

- Characterised in detail the radiation tolerance of the ITkPixVI chip
→ Currently repeating main measurements for ITkPixV2
- So far, results look consistent with ITkPixVI (after irradiation to 500 Mrad at 5 Mrad/h), and no operational issues observed during irradiation
- **Most damage to analog front-end occurs in the beginning of irradiation** → consistent with what was seen for ITkPixVI
- Dedicated **ring oscillators** included in ITkPixV2 to measure damage to digital gates
- 42 ring oscillators made with different logic cells and different transistor sizes (strength 0, 1 and 4)
 - No strength 0 gates used in ITkPixV2 digital logic
 - Too large increase in gate delay (200%) will cause digital logic to fail

Tuned threshold dispersion with irradiation



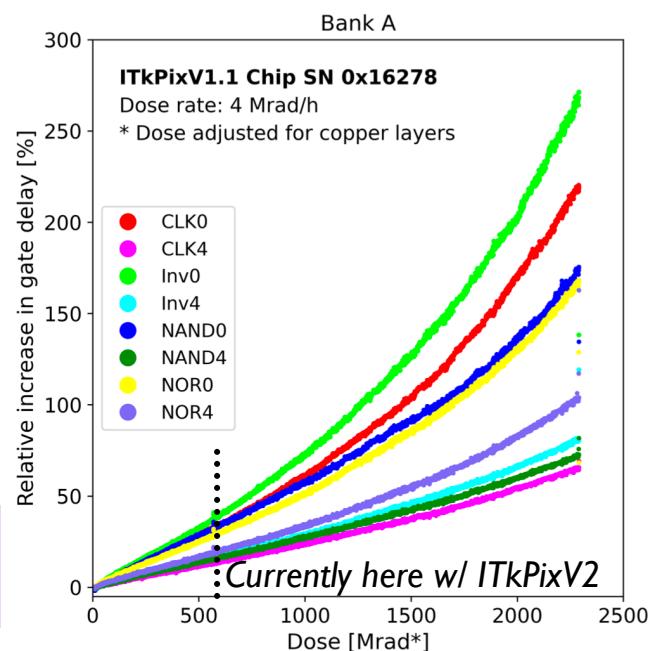
Ring oscillator behaviour



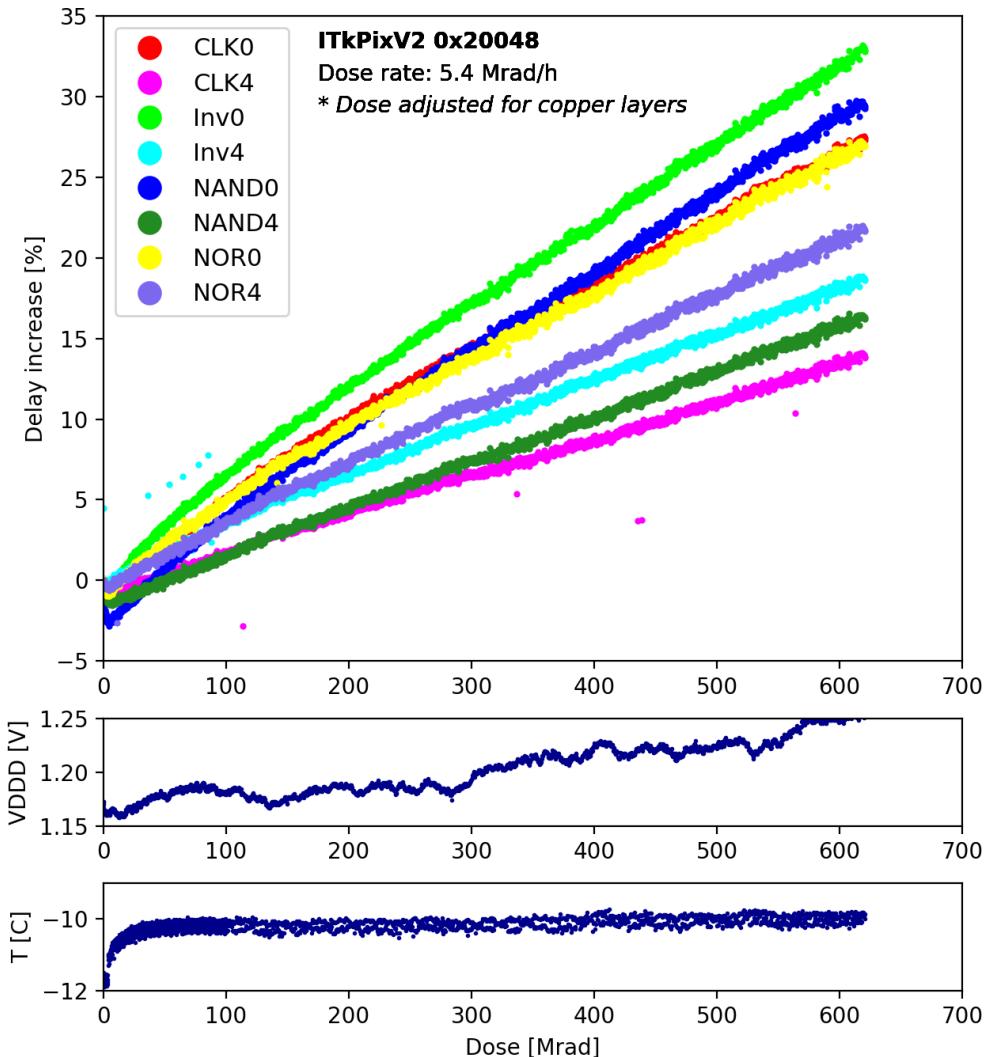
X-ray irradiations

- Digital logic is sensitive to **dose rate effects** → roughly two times more damage at low dose rate
 - Need to irradiate to around 2 Grad to simulate the 1 Grad environment in ITk
- So far, ring oscillator behaviour is **very consistent with ITkPixV1**
- Will reach total target dose in ~ 2 weeks

ITkPixVI
irradiation results



Ring oscillator delay increase with irradiation
for ITkPixV2



Conclusions

- Received first ITkPixV2 engineering run wafers
- Issues:
 - So far, have only found one issue related to aurora protocol, which was confirmed as an RTL bug (introduced during code cleanup) → however, feature (clock compensation) not used nor needed for ATLAS operation
- Open points:
 - Following up on some of the observations from wafer probing → currently checking if we observe something similar in bench testing
- **First tests on ITkPixV2 look promising**, most major design changes verified
- Tested chip functionality performs as expected, some detailed studies still ongoing
- Plan to qualify ITkPixV2 by October 2023 and release order for 400 production wafers (100 already ordered expected to arrive very soon)
- **YARR SW devel branch fully supports ITkPixV2 testing**

Next steps for qualification

- Some bench testing remaining, but mainly missing X-ray irradiations and SEU testing
- X-ray irradiations current ongoing at LBL, Oxford and Bonn
- Currently do not have a slot at a heavy ion facility, currently exploring options:
 - Preferred location are Louvain or GANIL (currently on wait list for Louvain, and waiting to hear back from GANIL), also exploring an option in Sweden
 - there are other options, but would prefer a known facility due to known challenges
 - Protons at CERN are an option, but beam structure makes testing close to impossible
 - Will build digital modules as soon as possible, but will not get hybridized modules in time for qualification

Thank you!

Questions?

ITkPixVI → CROCvI Bug fixes

Item	Note	Tested in ITkPixV2
FE/CORE		
1 New multi-bit TOT latch	Solves the large current and ToT corruption issues found in RD53B-ATLAS	✓
Digital		
2 Precision TOT	Fixed counter reset issue (MSB was not reset)	✓
3 Precision TOT	TOT trigger latency changed from relative to absolute	✓
4 Precision TOT	Output inverted so that TOT "0" is represented by all 1's.	-
5 Data merging input polarity selection	This bit was unconnected in RD53B-ATLAS	✓
6 Self-trigger TAG overlap with Command Decoder Warning/Error TAG	New TAG numbering	□
7 LSB of trigger ID not triplicated	Could lead to a degraded SEU sensitivity (minor issue)	-
8 Missing self-trigger outputs in signal selection for General Purpose Outputs	Fixed. Also added other signals for debug	□
Analog		
9 Added antenna diodes on long wire connecting the top RPOLY T sensor	To possibly solve the issue that the top RPOLY T sensor gives ~50% of expected output voltage	-

ITkPixVI → CROCvI additional features

Item	Details	Tested in ITkPixV2
FE/CORE		
1 Selectable hit sampling mode	Asynch -0, Synchr-1	<input checked="" type="checkbox"/>
2 SEU detection in pixel core (only CMS Core)	4 bit/pixel. Hit OR busses in each column are used	<input type="checkbox"/>
Digital		
3 BX-ID in readout	Include in the readout after the tag	<input type="checkbox"/>
4 LV1ID in readout	Include in the readout after the tag	<input type="checkbox"/>
5 CRC (cyclic redundancy check)	32 bit at the end of event stream	<input type="checkbox"/>
6 SEU counting from Pixel Config. Registers (only CMS)		<input type="checkbox"/>
7 SEU counting from Global Config. registers		<input type="checkbox"/>
8 Dummy Global Config. registers for SEU testing	no TMR, TMR with clock skew, TMR w/o clock skew	-
9 Optional disable of triplicated clocks	For SEU TMR verification and testing	<input type="checkbox"/>
10 Constant serial test pattern	To check output levels during WLT	<input type="checkbox"/>

ITkPixVI → CROCvI changes/improvements

Item	Note	Tested in ITkPixV2
PADFRAME		
1 LVDS CMD receiver common mode	Now 600mV, it was 200 mV. Improved SET robustness	<input type="checkbox"/>
2 LVDS CMD receiver bias current mirror	Improved design for better SET robustness	<input type="checkbox"/>
3 LVDS receiver for Data Merging w/o internal termination	Use same LVDS CMD receiver	<input type="checkbox"/>
Digital		
4 New stream bit changed to End of Stream bit	To clearly identify when all data from an event/stream has been read out	<input checked="" type="checkbox"/>
5 Time resolution of Global Pulse generator	50ns → 25 ns	<input checked="" type="checkbox"/>
Analog		
6 Shunt current mirror for monitoring		<input checked="" type="checkbox"/>
7 Improved circuit to measurement injection cap	Now the measurements of parasitic cap includes also the cap between the terminals and the shield layer, while in RD53B-ATLAS this contribution was only estimated	<input checked="" type="checkbox"/>

CROCv1 → ITkPixV2 bug fixes

RD53B-CMS → RD53C-ATLAS (V11.1) Bug fixes



Tested
in ITkPixV2

Item	Note	
FE/CORE		
1 For ATLAS removed possibility to select sampling mode. Kept only asynchronous	This is to quickly remove the bug introduced with CROCv1, since ATLAS will use only async. The real fix will be done for RD53C-CMS	✓
2 Wrong ToT for short hits in 80 MHz asynch. sampling mode (non-monotonicity)	Side effect of the fix: in synchr. mode, the ToT starts counting from "1" instead of "0"	✓
Digital		
3 High rate chip stuck from SEU in Pixel Core	Fixed in the periphery	□
4 Precision TOT	Fixed issue introduced in RD53B-CMS that prevented the PTOT to work. Not yet implemented in the verification framework	✓
5 Data merger: various fixes, including automatic phase detector	Also added the possibility to manually override the phase choice	✓
6 CLEAR command must not reset Aurora	The CLEAR command used only for fast clear of buffers and not Aurora, since this was causing link loss	□
Analog		
7 RPOLY Tsensor	New biasing scheme to solve the large mismatch between top and bottom sensors observed in RD53B chips	✓
Shuldo		
8 Preregulator	Improved stability for larger load (up to 5 mA, it was 1 mA). Became worse in the RD53B-CMS after the change in the I _{shunt} mirroring	-

CROCv1 → ITkPixV2 changes/improvements

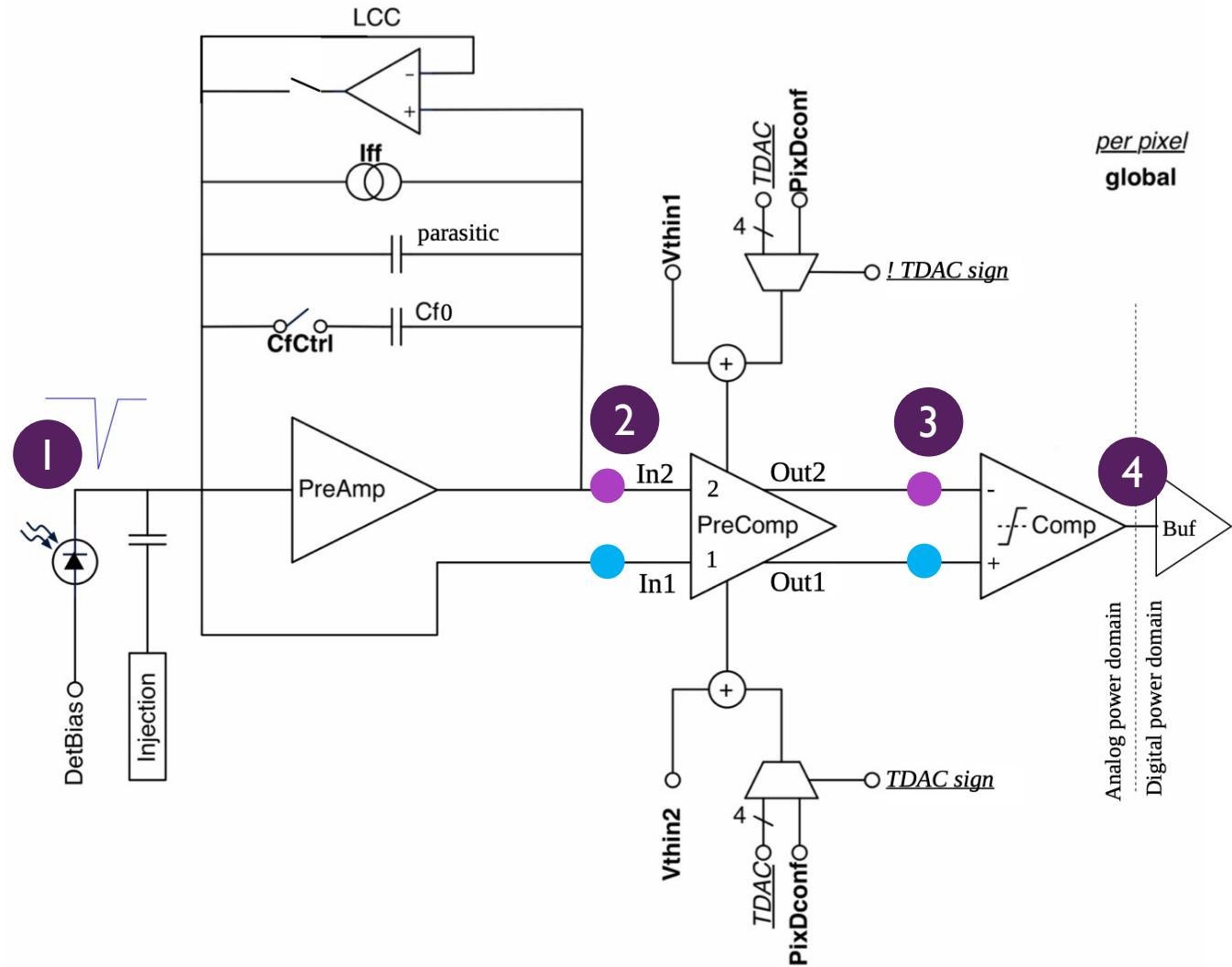
RD53B-CMS → RD53C-ATLAS (V11.1)

**RD
53**

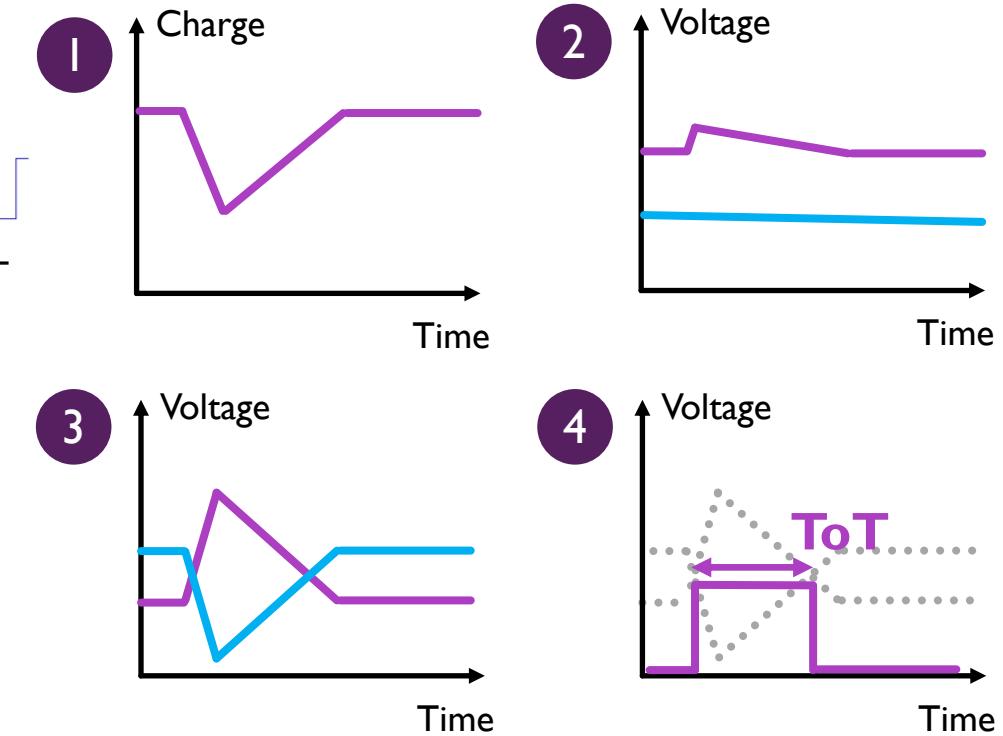
Tested
in ITkPixV2

Item	Note
Digital	
1 IREF TRIM bits read-back	
Analog	
2 New radiation sensor in the centre of the periphery (near the Ring Oscillators). The two near ShLDO are not changed	Made of minimum size PMOS for extended linear range up to 1 Grad
3 Improved uniformity of M8-M9 over current mirrors	Where possible, improved the M8-M9 coverage over various current mirrors used in the bias circuitry, to have more uniform dose during X-ray tests
ShuLDO/Bandgaps	
4 Core Bandgap	Added capacitors to improve SET robustness
5 Preregulator Bandgap	Improvement of startup
6 Voffset amplifier (of the ShLDO)	Increase the region of Vofs voltages where the circuit can operate without any overvoltages
7 Small increase of VREF trimming LSB (19 mV → 25 mV)	Increased capability of VDDA/D setting to 1.2V even after Iref increase by 15% due to TID

ITkPixV2 Differential Front-End

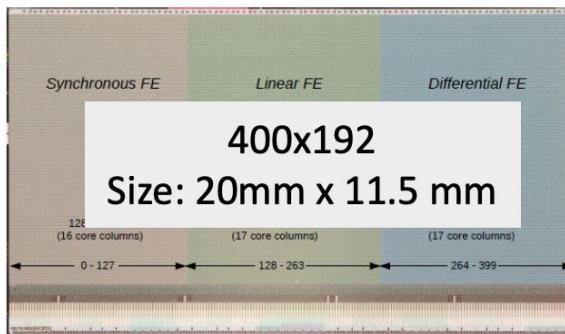


- ITkPixV2 uses a differential front-end to determine ToT information



RD53 chip evolution: RD53A

RD53A



- Pixel chips for the HL-LHC upgrade for ATLAS and CMS have been jointly developed by the RD53 collaboration to cope with the harsh requirements for HL-LHC
- First joint prototype was RD53A, submitted in August 2017
→ Half-sized demonstrator chip with three different architectures
- Based on this, improved RD53B chip, produced in two versions:
ATLAS ITkPixVI and CMS CROC
- Main difference in size and type of front-end used
 - Differential Front-End for ATLAS
 - Linear Front-End for CMS

RD53 chip evolution: RD53B

ITkPixVI.0



ITkPixVI.I

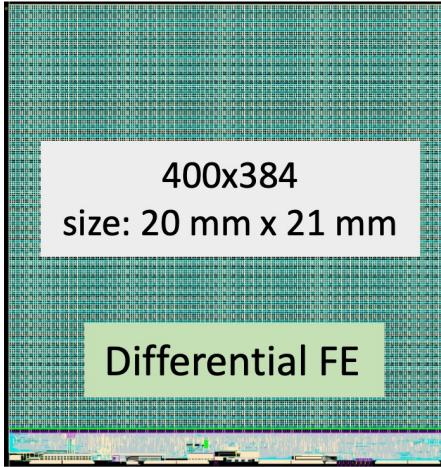
- **ATLAS ITkPixVI** chip submitted in March 2020
- Found a serious issue in the time-over-threshold (ToT) memory
 - Large current for particular configurations of ToT
 - Wrong ToT storage and hit loss
- Fix to the mask on the remaining FE wafers, fixing the issue of large leakage current in ITkPixVI.I (but ToT still not useable), submitted in October 2020
- ITkPixVI.I will be used as the **ITk pre-production readout chip**
- **CMS CROC_vI** chip submitted June 2021, including proper fix to the ToT memory

CROC vI



RD53 chip evolution: RD53C

ITkPixV2

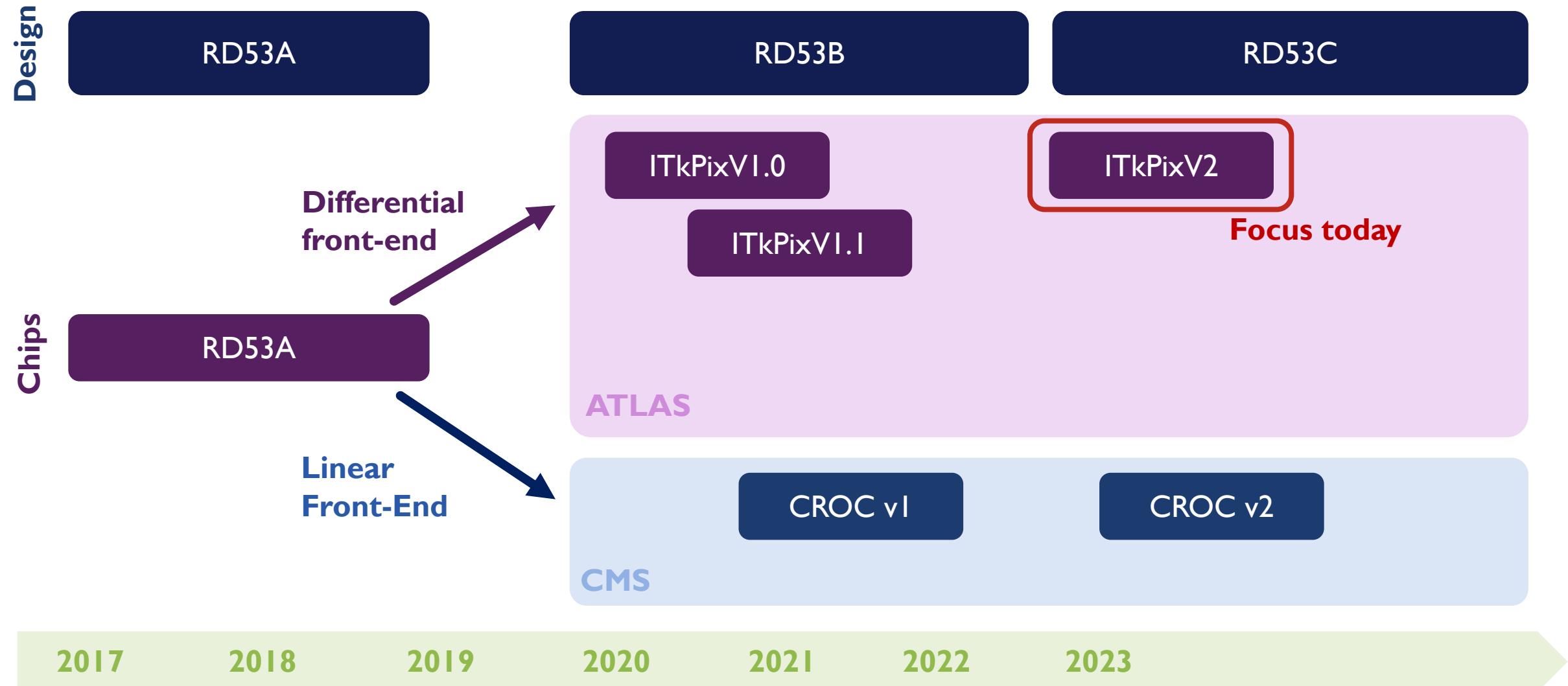


CROC v2



- **ATLAS ITkPixV2** chip submitted in April 2023
- Many small changes to improve:
 - Stability against single-event transients
 - Startup and powering stability
 - Improvements and additional monitoring sensors for temperature and radiation
- Expected to be the final production chip
- Received back engineering run wafers → need to run tests now to decide within a few months if we are happy with the design and would like to produce the remaining wafers
- **CROC v2** to be submitted soon

RD53 chip evolution



2017

2018

2019

2020

2021

2022

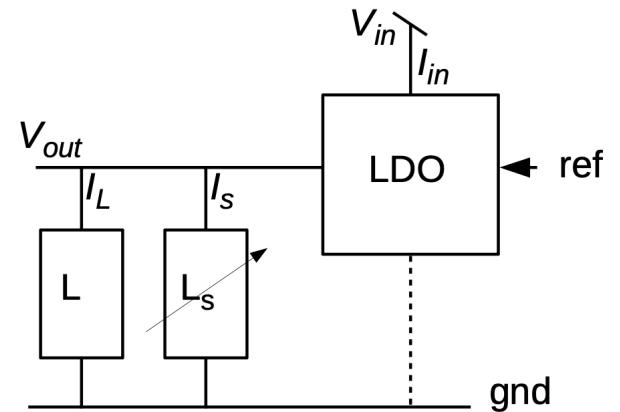
2023

SLDO performance

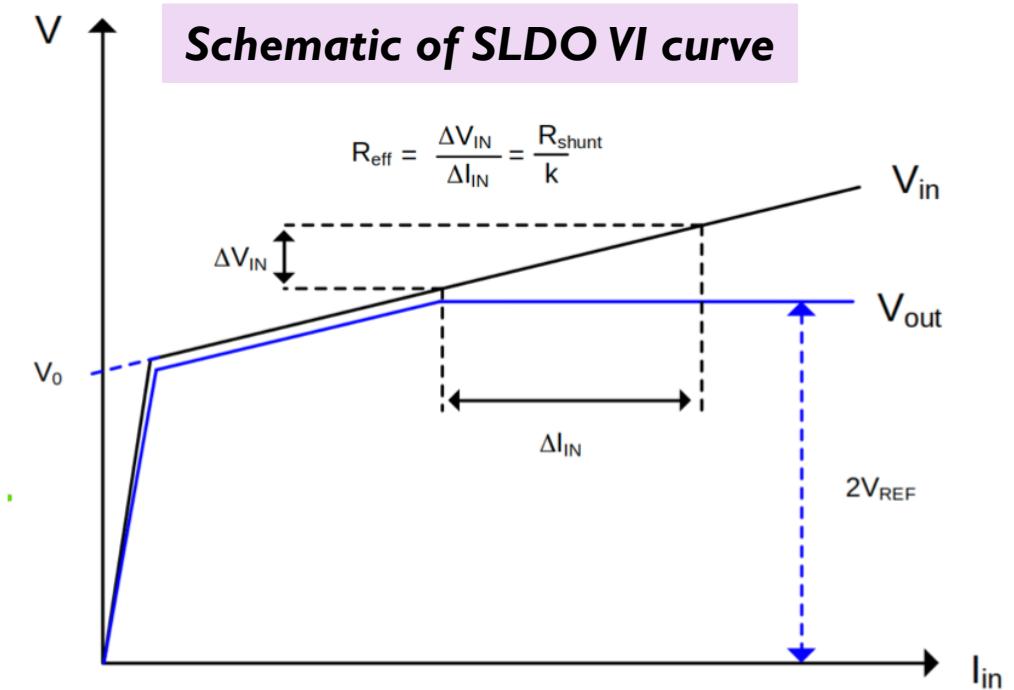
- ITkPixVI modules will be operated in a **serial power configuration**, supplying a constant current
- Motivation: reduce the number of cables and material in the detector
- To allow this, the chip has a **SLDO circuit**, which powers the main load (the chip) and the internal load (shunt element)
- The shunt element is designed such that it achieves the required input current, regardless of what the chip does
- Put in V_{in} which regulates voltage to V_{out}
- Linear behaviour driven by R_{eff}
- Offset voltage V_0 (or V_{ofs}) is set by a separate circuit
- Overall behaviour can be described as:

$$I_{in} = I_L + I_s = \frac{V_{in} - V_0}{R_{eff}} \quad [V_{in} > V_0]$$

Schematic of LDO circuit



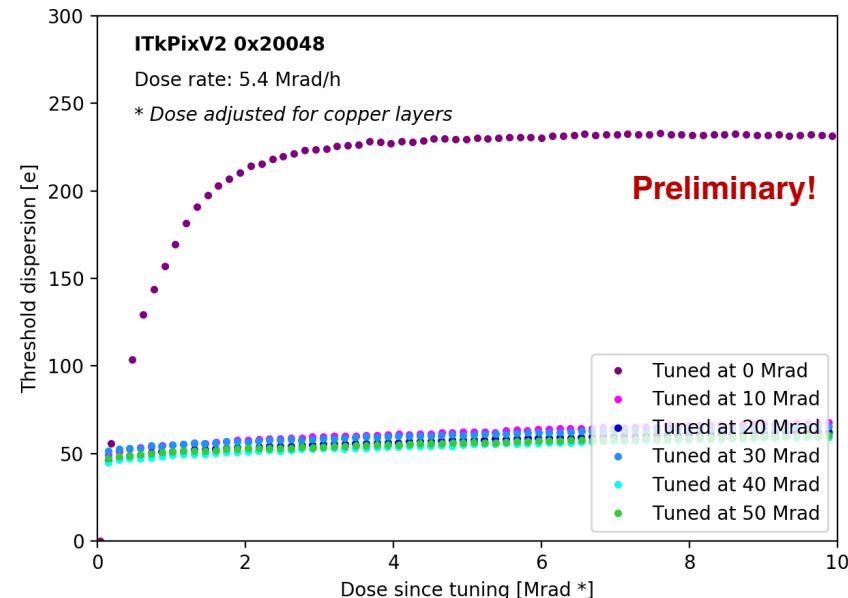
Schematic of SLDO VI curve



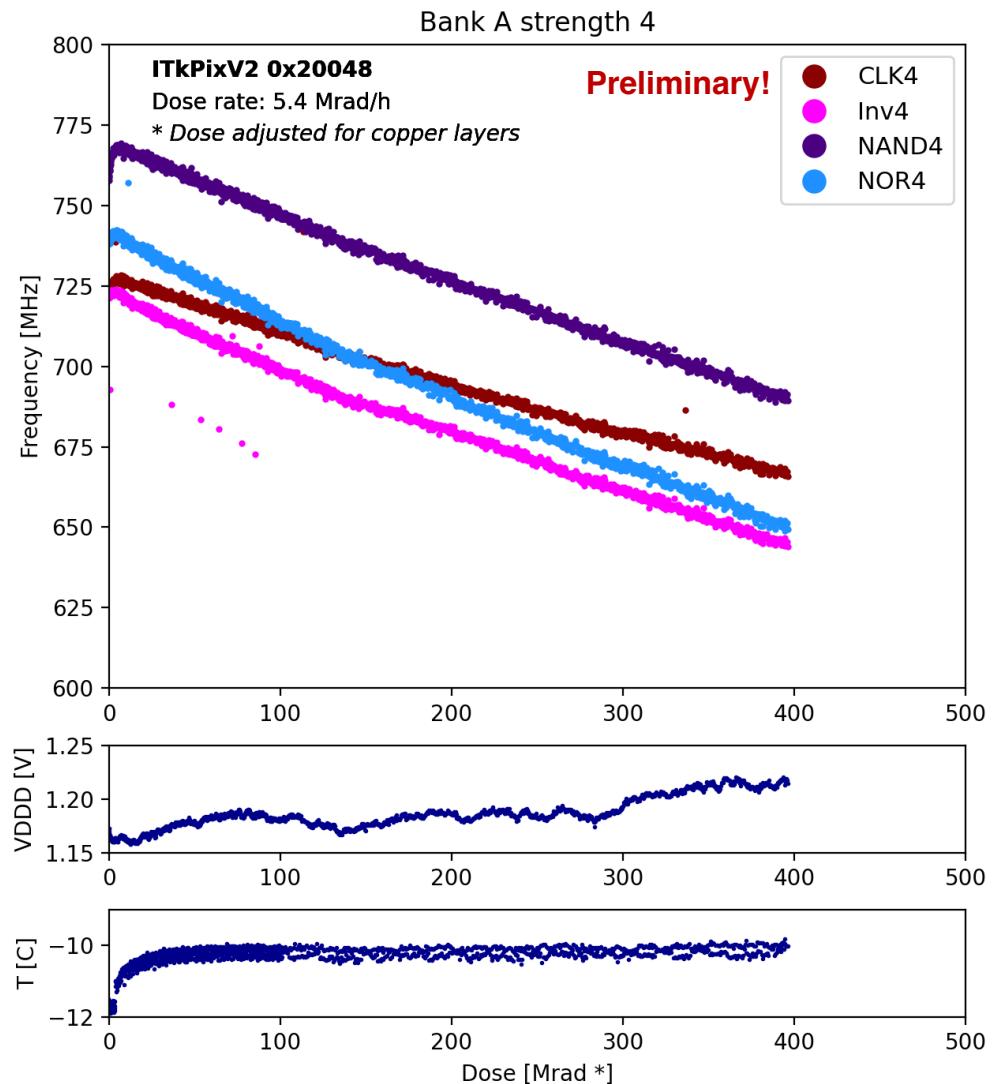
Irradiations

- Characterised in detail the radiation tolerance of the ITkPixVI chip
→ Currently repeating main measurements for ITkPixV2
- So far, results look consistent with ITkPixVI (after irradiation to 400 Mrad at 5 Mrad/h)
- Dedicated ring oscillators to measure damage to digital gates → sensitive to dose rate effects
- Damage to analog front-end is most severe in the beginning of irradiation

Tuned threshold dispersion with irradiation

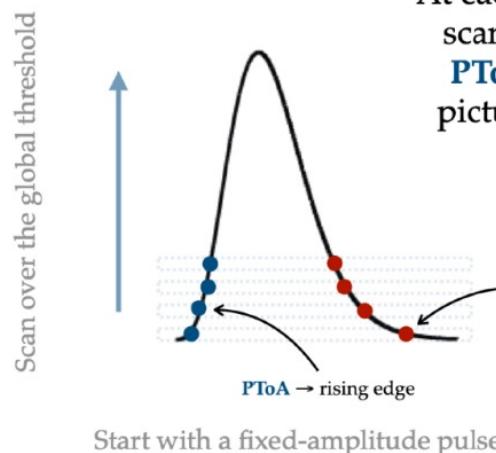


Ring oscillator frequencies with irradiation



FE scope

- ToT in ITkPix-V1 chips is controlled by global registers only. Scan the feedback current DAC to decide configuration for different detector regions
 - Study with **FE scope**: get the profile of analog signal using PToT and ToA
 - ToT to charge conversion can be performed in DAQ software



At each step in the threshold scan, sample each pixel's **PToA** and **PToT** to get a picture of the pulse shape

