Module Development for the ATLAS ITk Pixel Detector

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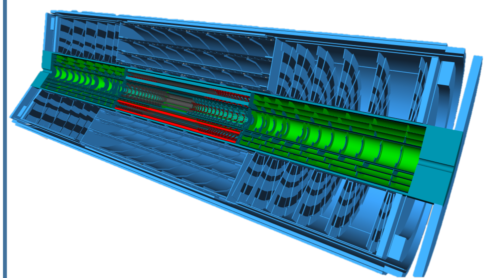
On behalf of the ATLAS ITk collaboration

Introduction

The ATLAS experiment will upgrade its tracking detector during the Phase-II LHC shutdown to take advantage of the increased luminosity of the HL-LHC, with data-taking expected to start by 2027.

The upgraded tracker will consist of a barrel of concentric layers (5 pixel + 4 strip, with several endcap rings) and will likely cover an extended eta[1] range. It is foreseen to cover up to |eta|<4.0. Substantial developments are taking place in the area of silicon hybrid module technologies to optimize their assembly and integration techniques in order to acquire the necessary expertise for the detector's commissioning.



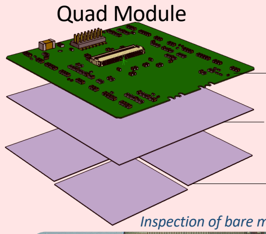
Proposed layout for the ITK detector[2], 1 m in radius and 6 m in length. The silicon sensors shown as red/blue/green cells are secured onto detector-long support staves.

To validate the numerous production, assembly, integration tests and wider infrastructure necessary in preparation for the commissioning of the ITk[3], the first stages of these developments are being conducted using RD53A[4,5] hybrid modules. Diced to match the final production sensor size (ITkPixV2[6]), these will assist towards optimizing the tooling and testing infrastructure needed for the final commissioning stage.

Assembly

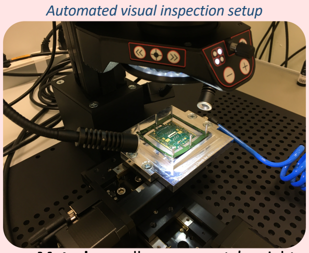
A module consists of a silicon sensor bump-bonded to a front-end (FE) chip (forming a bare module) glued to a flexible PCB that relays the data and power connections to dedicated pigtail cables.

Quad Module

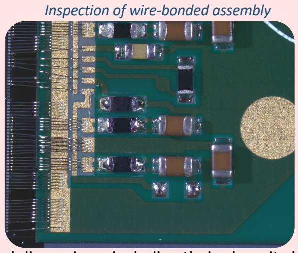


The module assembly process comprises of several key stages:

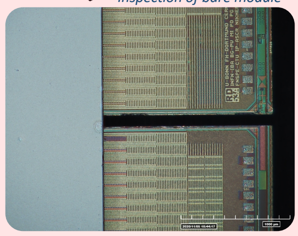
- **Visual Inspection**: assessing all components upon reception and at every assembly and testing stage to ensure no defects are present.



Automated visual inspection setup

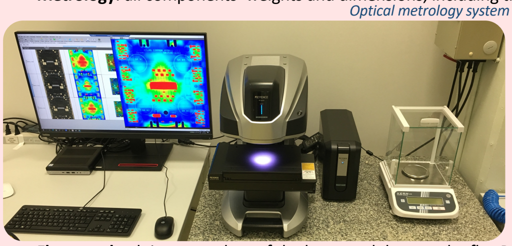


Inspection of wire-bonded assembly

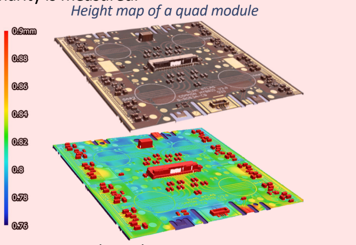


Inspection of bare module

- **Metrology**: all components' weights and dimensions, including their planarity is measured.



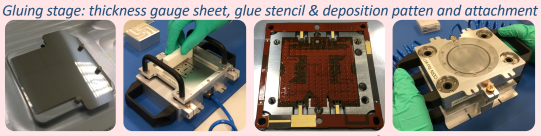
Optical metrology system



Height map of a quad module

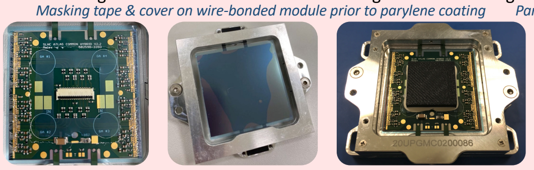
- **Flex-attach**: gluing procedure of the bare module onto the flex PCB using custom-made tooling.

Assembly Tooling

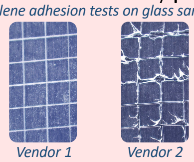


Gluing stage: thickness gauge sheet, glue stencil & deposition patten and attachment

Following the flex-attach stage the module is **wire-bonded** using aluminium wedge wire-bonds followed by **parylene coating**.



Masking tape & cover on wire-bonded module prior to parylene coating

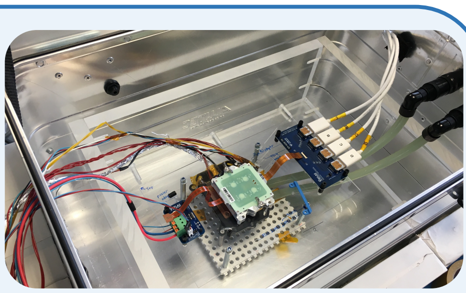


Parylene adhesion tests on glass samples

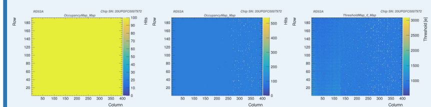
Testing

In order to develop the necessary testing infrastructure for the electrical qualification of each assembled module, a phased approach has been adopted across the collaboration to achieve these different testing capabilities, including:

- **Performing scans and tunings** on the FEs.

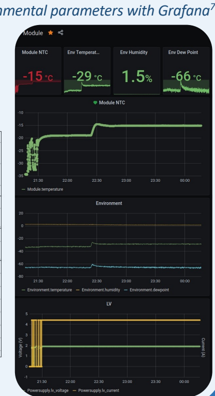


Electrical testing setup for quad RD53A assemblies

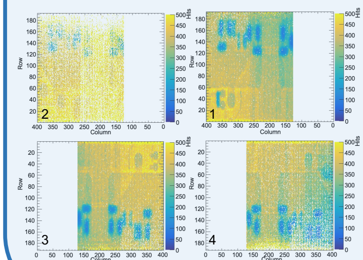


Digital, analog and threshold scans

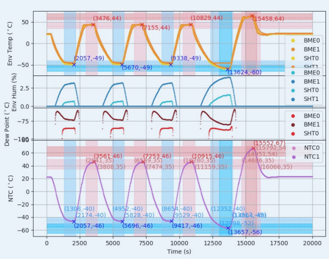
- **Monitoring** HV/LV voltages and currents, environmental temperature, humidity, dew point & module NTC temperature. This includes software interlocks which can for instance alert for module temperatures > 40°C and leakage current < −1 μA.
- **Thermal cycling** to ensure operation of the module after 10 cycles down to -45°C.
- **Source scans** to display the functionality of unmasked pixels.



Monitoring of module powering and environmental parameters with Grafana[7]



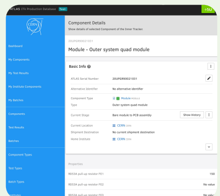
54 MBq ^{90}Sr source scan over 1h at 50kHz trigger rate



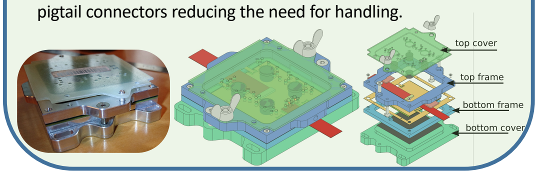
Thermal cycling profiles

Tools facilitating a global production

- A **database** has been developed to trace all components and assemblies along with each of their inspection & measurement results.



- In order to transport assemblies securely between different sites **module carrier** has been designed to safely house wire-bonded assemblies all whilst allowing electrical testing to continue via pigtail connectors reducing the need for handling.



Bibliography

[1]Eta: pseudo-rapidity = $-\ln\left(\tan\frac{\theta}{2}\right)$, where θ is the angle between a particle and the beam axis.
[2]Technical Design Report ATLAS Inner Tracker Pixel Detector, CERN, ATLAS Collaboration, 2017
[3]RD53A: The RD53A Integrated Circuit cds.cern.ch/record/2287593
[4]RD53 collaboration rd53.web.cern.ch
[5]See Talk by M. Standke on RD53 wafer testing for the ATLAS ITk pixel detector
[6]See Talk by F. M. Sanchez on ATLAS ITk Pixel Detector Overview
[7]Grafana Labs grafana.com

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