Laboratory 4:

**AD-DA Conversion**

In this laboratory we will investigate different aspects of analog to digital, and, digital to analog signal conversion, plus compare related effects, like aliasing and quantisation noise between practical implementation and theory.

We use a HW board containing an analog to digital converter (ADC), which samples and quantizes an analog input signal x(t), with a given number of bits (resolution) and generates the discrete signal output xS[n] . The sampling frequency Fs is a constant and known parameter. Before the ADC an anti-aliasing filter can be deployed (we will see what for).

On the other side the discrete signal xS[n] is converted back to an analog signal by a digital to analog converter (DAC). The DAC has a zero-order-holder and is often combined with an anti-imaging or reconstruction filter delivering the reconstructed analog signal xR(t) .

The block diagram of this HW board is shown below in figure 1. The detailed schematics is provided in the annex.



**Figure 1:** Block diagram of the AD-DA hardware board

Then follow the tasks described below, paying attention to the recommended setups.

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| SETUP-GENERAL: Power + FuGe to Osc. |
| * Connect the board supply: ground plus a DC voltage in range [+5, +10] V * Connect the output of the signal generator (FuGe) to the input VIN of the board, and also to the channel 1 (CH1) input at the oscilloscope. * Plus connect the output VOUT of the board to the channel 2 of the oscilloscope. |
| SETUP-A: BOARD |
| * Put jumpers in position: CLK\_INT, VREF\_INT, VIN\_OFFSET, plus anti-imaging jumper open (filter inactive), and anti-aliasing jumper open (filter inactive) * set all 12 DIP switches on (ADC using its maximum resolution of 12 bits). |
| SETUP-A: FUNCTION GENERATOR & OSCILLOSCOPE SETUP |
| * Generate with the FuGe a sinusoidal signal x(t) with f0=50 kHz and amplitude   2.0 Vpp . The dynamic range („Aussteuerbereich“) of the ADC is about ca. 5 Vpp . |
| QUESTIONS |
| 1. Control the input (CH1) and ouput (CH2) signals in the oscilloscope. The ouput signal is discrete in both time and amplitude values. How can you explain the delay between input and output signals? Why is the output signal always slightly changing? |
| 1. Determine the sampling period Ts, and the corresponding sampling frequency Fs.   You can freeze the display of the oscilloscope (toggle between run/single measurement) to easy your observation. |
| SETUP-B: FUNCTION GENERATOR & DIP-SWITCHES |
| Lower now the frequency of VIN to . f0 = 1 kHz and set the amplitude to 5.0 Vpp.  Check if your output is saturating. In case yes, reduce slightly the amplitude to avoid saturation. Then set the DIP switches one by one in off position, starting by the LSB and evolving towards the MSB. |
| QUESTION |
| 1. Observe the changes in VOUT and explain why these changes happen.   Set all 12 DIP switches in the ON position again. |

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| SETUP-C: FUNCTION GENERATOR |
| Change again the frequency of VIN to . f0 = 100 kHz and keep the amplitude at (or almost) 5.0 Vpp. |
| QUESTIONS |
| 1. Observe now the spectrum of the input signal VIN. and of the output signal VOUT .  Which are the new frequency components of VOUT in comparison to VIN ?  The spectrum of VOUT contains the original frequency of VIN, plus copies of it (image frequencies) shifted around multiples of Fs.   Note down the frequency components (original plus images) in the frequency range from 0 Hz till 5 MHz. Verify the position of the image components compared to the multiples of Fs. |
| 1. Which other frequency of VIN do you expect to produce the same output spectrum at VOUT? Verify your expectation with a measurement.  Is the frequency value of VIN that you set larger than Fs/2 ?  The effect you are observing here (that the original frequency of VIN appears distorted at VOUT) is called aliasing. |
| 1. Change again the frequency of VIN to . f0 = 100 kHz and keep the amplitude at (or almost) 5.0 Vpp. And **change the shape to a ramp function**.  The DAC contains a zero-order-holder (ZOH), which is a filter taking each input value of the DAC and holding it constant until the next sample arrives.   In the time domain the response of the ZOH to a single impulse is a rectangular pulse with width Ts . Therefore the response of the ZOH in the frequency domain corresponds to a sinc shaped spectrum.   Where are the zero-crossings of the ZOH sinc shaped spectrum? Can you observe them in the spectrum of VOUT ? |

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| SETUP-D: FUNCTION GENERATOR & DIP-SWITCHES & FILTERS |
| Set again a sine shaped VIN with frequency f0 = 100 kHz and keep the amplitude at (or almost) 5.0 Vpp . Set again the DIP switches one by one in off position, starting by the LSB and observe this time the effect in the frequency domain. |
| QUESTIONS |
| 1. Observe the new frequency components raising as the quantisation noise increases. The range between the maximum signal amplitude, and the maximum noise amplitude (in the frequency domain) is called SFDR (spurious free dynamic range).   Verify that the SFDR in the frequency range from [0…Fs/2] changes by 6dB per bit, as you change the resolution of VOUT . You will only be able to observe this effect for the 8 MSBs, because the oscilloscope numerical calculation has a limited resolution of 8 bits.   The overall signal quality is measured with the signal to noise ratio (SNR). The SNR of VOUT also changes with 6dB / bit used in the quantisation of VIN.  HINT: In the FFT options you can select type: “Peak-Hold” to facilitate the SFDR measure.   Set all 12 DIP switches in the ON position again. And the FFT type back to “sample”. |
| 1. Close now the jumper at the output of the DAC, setting the anti-imaging filter (passive RC ) with a cut off frequency of fc = 100 kHz (R = 50Ω, C = 33nF), and control the changes in the spectrum of VOUT . |
| 1. Set now the frequency of VIN to 900kHz, and observe VOUT both in time and frequency domain.   As commented above the effect observed here is called aliasing and it implies the distortion of the frequency contents of the input signal being sampled, when these frequency contents are above Fs/2.   There are basically 2 ways to prevent aliasing. One is to select a higher sampling frequency (which is not always possible for a given hardware), and the other is to deploy an anti-aliasing filter (AAF).   The anti-aliasing filter is placed before the ADC and limits the bandwidth to the ADC input signal. In this board the anti-aliasing filter has a cut off frequency of fc = 50 kHz.   Close now the jumper setting the anti-aliasing filter active, and control VOUT in time and frequency domain. |
| 1. Lower again the frequency of VIN to 100kHz, and observe VOUT both with and without the anti-aliasing filter. Does the AAF have a significant effect for this input frequency? |

Some further ideas if you still have time:

* Keep the frequency of VIN to 100kHz .   
  Open the jumpers of the anti-image and anti-aliasing filters (inactive position).  
     
  Set the jumper to CLK\_EXT, and connect a second FuGe in the clock-input.   
    
  Start with a clock frequency of 1MHz and lower it towards 100kHz, while observing the influence at VOUT both in time and frequency domains. The clock signal should have an amplitude toggling between 0V and 5V.
* The ADC has besides VIN two further inputs, VREF (reference voltage) and VCLOCK (determining the sampling period).   
    
  What is VREF needed for?   
  What is the influence of a clock jitter (clock period uncertainty) for the ADC performance?  
  You can study the ADC datasheet to check for answers.

