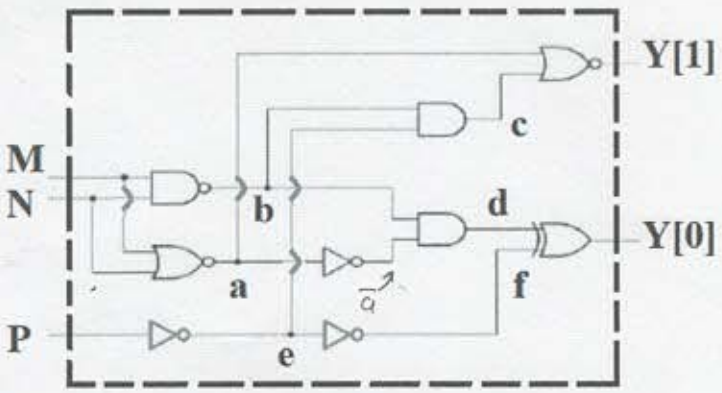
CSUS CPE166 Dummy Exercise Student Name: David Quintanilla

You need to upload the solution in multi-page PDF or WORD file format on the canvas course website.
You must write down your name on your solution sheets.

1. Complete the Verilog HDL design for the circuit below.



module ex1 (M, N, P, Y);

input M, N, P ;

output [1:0] Y ;

wire a, b, e, c, d, f ;

assign a = ~(M|N) ;

assign b = ~(M&N) ;

assign c = B&E ;

assign d = B&~A ;

assign e = ~P ;

assign f = ~E ;

assign Y[1] = ~(A|C) ;

assign Y[0] = D^E ;

endmodule

2. Write a testbench for the above circuit. You must generate testing cases for all possible values of M, N, and P.

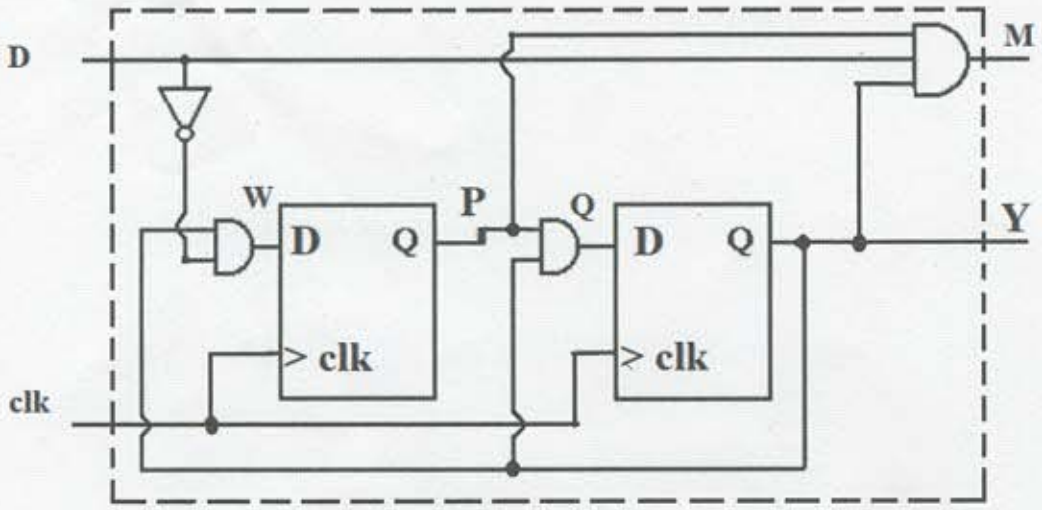
```
`timescale 1ns/1ps

module ex1_tb();

Reg M N P;
wire [1:0] Y

  ex1 uut(.m(M), .N(N), .P(P));

Initial begin

      M=0; N=0; P=0;
      #5
      M=0; N=0; P=1;
      #5
      M=0; N=1; P=0;
      #5
      M=0; N=1; P=1;
      #5
      M=1; N=0; P=0;
      #5
      M=1; N=0; P=1;
      #5
      M=1; N=1; P=0;
      #5
      M=1; N=1; P=1;
      #5
      M=0; N=0; P=0;
end

initial $Monitor($time, "M=%b, N=%b, P=%b" M,N,D);

end module
```

3. Design a counter circuit in Veirlog. The counter counts from 0 to 220 and then repeats.

```
module counter();

Interj;

inital begin

where (1'b0) begin
 for(j=0; j<=220; j+1)
   #1 display("counter= %d", j);
  end
 end
end
```

endmodule

4. Design the following circuit in Verilog.



module ex4 (D, clk, M, Y);

```
input D, clk;
output M, Y;
wire (W, P, Q);

assign W = (~D) & Q);
assign Q = (P & Q);
assign P = Q;

always @(posedge clk)
  if
```

5. Write a testbench for the circuit in the problem 4.

module ex4_tb;

```
module ex4_tb;

  reg d, clk
  wire m, y;

  ex4 (d, clk, my)

initial clk = 1'b0
always #6 clk = ~clk;
initial
 begin
   d= 1'b0;
   #14 d = 1'b1;
   #5 d = 1'b0;
   #6 d = 1'b1;
   #16 d = 1'b0;
   #10 d = 1'b1;
   #12 d = 1'b1;
   #10 d = 1'b0;
   #18 d = 1'b1;
  #10 d = 1'b0;
  #10 d = 1'b0;
  #10 $stop;
end
initial $monitor ($time, " d=%d, clk= %d, m=%d, y=%d", d, clk, m, y);
endmodule
```