	ntanilla									
Instruction:	Mov DX, 0	120								
Address:	CS	100		Operation:			st.: DX		Source:	120
Instruction	Format		to register (g:immedia	alternate er	coding)					
Instruction	Format	w=1	reg DX=01		data=2	001h				
Binary:	1011	1010								
Hex:	BA2001									
Instruction	Mov AX, [0	200]								
Address:	CS	103		Operation:	Mov	De	st.: AX		Source:	[0200]
Instruction	Format	Memory to 1010 001v	AX v "full displa	cement"						_
Binary:	1010	w = 1	0002h							
	A	1	2							
Hex:	A10002		`							
Instruction:	Mov BX [02	204]								
Address:	cs	: 0106		Operation:	Mov	De	st.: BX		Source:	[0204]
		4000 404								
Instruction	Format	1000 101w	: mod reg	m: BX				_		
		w = 1	mod = 00	reg = 011	r/m = 11	10				
Binary:	1000	1011	0001	1110	0204h					
Uew.	9D4E0402									
	8B1E0402									
	8B1E0402 Sub AX, B		,							
Instruction				Operation:	Sub	De	st.: AX	1	Source:	BX
Instruction:	Sub AX, B	X	v: 11 AX, B		Sub	De	st.: AX	1	Sou <mark>ce:</mark>	ВХ
	Sub AX, B	X 10A 0010 100w		x		De	st.: AX]	Sou <mark>ce:</mark>	BX
Instruction: Address:	Sub AX, B	X 10A 0010 100w w = 1	reg1 = 01	x reg2 = 00	0	De	st.: AX]	Soulce:	BX
Instruction: Address: Instruction Binary:	Sub AX, B	X 10A 0010 100w w = 1	reg1 = 01	x reg2 = 00	0	De	st.: AX		Soutce:	BX
Instruction: Address: Instruction Binary:	Sub AX, B	X 10A 0010 100w w = 1	reg1 = 01	x reg2 = 00	0	De	st.: AX		Soulce:	BX
Instruction: Address: Instruction Binary: Hex:	Sub AX, B	X 10A 0010 100w w = 1 1001	reg1 = 01	x reg2 = 00	D	De	st.: AX		Soulce:	BX
Instruction: Address: Instruction Binary:	Sub AX, B CS Format 0010 29D8	X 10A 0010 100w w = 1 1001	reg1 = 01	X reg2 = 000 1000	0 I Jump	Dest	st.: AX	}	Sou <mark>tce:</mark>	BX
Instruction: Address: Instruction Binary: Hex:	Sub AX, B CS Format 0010 29D8 JGE 0116 CS	X 10A 0010 100w w = 1 1001	reg1 = 01 1101	X reg2 = 00 1000 Conditiona Operation	0 I Jump			}	Soulce:	BX
Instruction Address: Instruction Binary: Hex: Instruction	Sub AX, B CS Format 0010 29D8 JGE 0116 CS	X 10A 0010 100w w = 1 1001 010C	reg1 = 01 1101 8-bit displa	X reg2 = 00 1000 Conditiona Operation	0 I Jump			}	Soulce:	BX
Instruction Address: Instruction Binary: Hex: Instruction	Sub AX, B CS Format 0010 29D8 JGE 0116 CS	X 10A 0010 100w w = 1 1001 010C 0111 tttn : tttn = 1101	reg1 = 01 1101 8-bit displa	X reg2 = 00 1000 Conditiona Operation	0 I Jump			}	Soulce:	BX