AIM: Realization of Boolean algebra using gates.

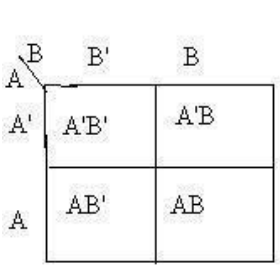
LEARNING OBJECTIVES: Students will

1. Learn to minimize and design combinational logic.
2. Understand the relationships between combination logic and Boolean algebra, and between sequential logic and finite state machines.

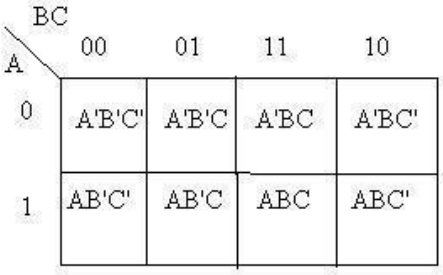
TOOLS/SOFTWARE REQUIRED:
Logic gates (IC) trainer kit.
Connecting patch chords.
IC 7400, IC 7402, IC 7404, IC 7406, IC 7408, IC 7432, IC 7486.

RELATED THEORY:
Canonical Forms (Normal Forms): Any Boolean function can be written in disjunctive normal form (sum of min-terms) or conjunctive normal form (product of max-terms). A Boolean function can be represented by a Karnaugh map in which each cell corresponds to a minterm. The cells are arranged in such a way that any two immediately adjacent cells correspond to two minterms of distance 1. There is more than one way to construct a map with this property.

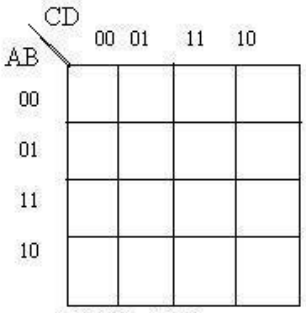
Karnaugh Maps:
The K-Map for 2, 3, 4 and 5 variable is shown in the following figure.



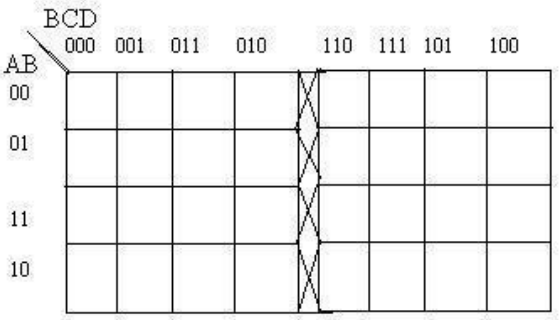
2 Variable K-Map



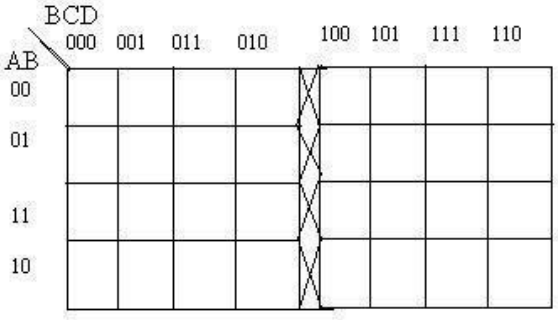
3 Variable K-Map



4 Variable K-Map



Reflection (Gray Code) 5 Variable K-Map



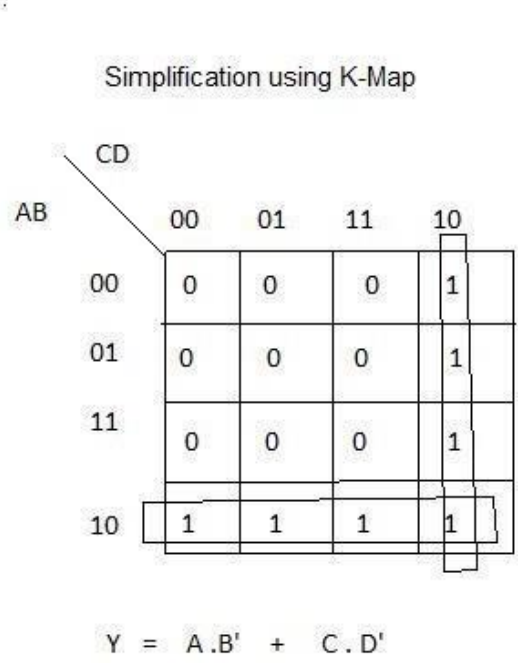
Overlay 5 Variable K-Map

Realization of SOP Boolean expression:

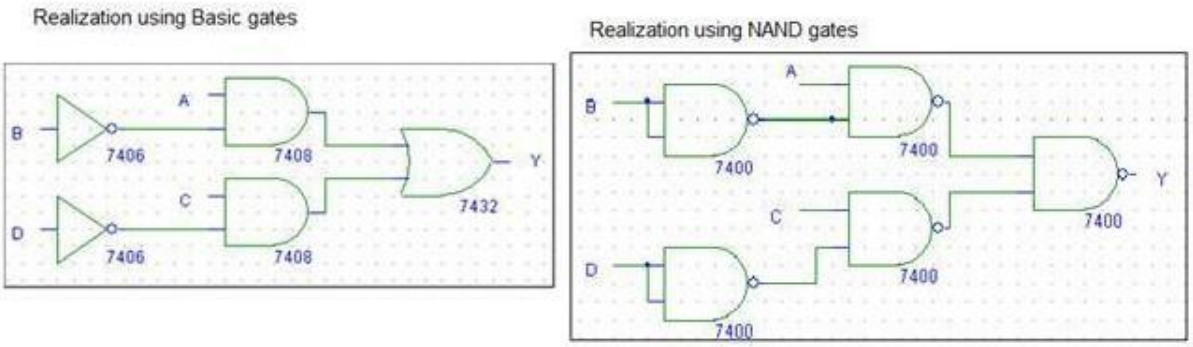
1). Y= A’B’CD’ + A’BCD’ + ABCD’ + AB’CD’ + AB’C’D’ + AB’C’D + AB’CD

The figure below shows the truth table of the above function and on the right of TT is the K-Map simplification of the above logic function in SOP form.

inputs				O/P
A	B	C	D	O
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0



Realization of Sum of Product Equations



Product of Sum Logic Equations

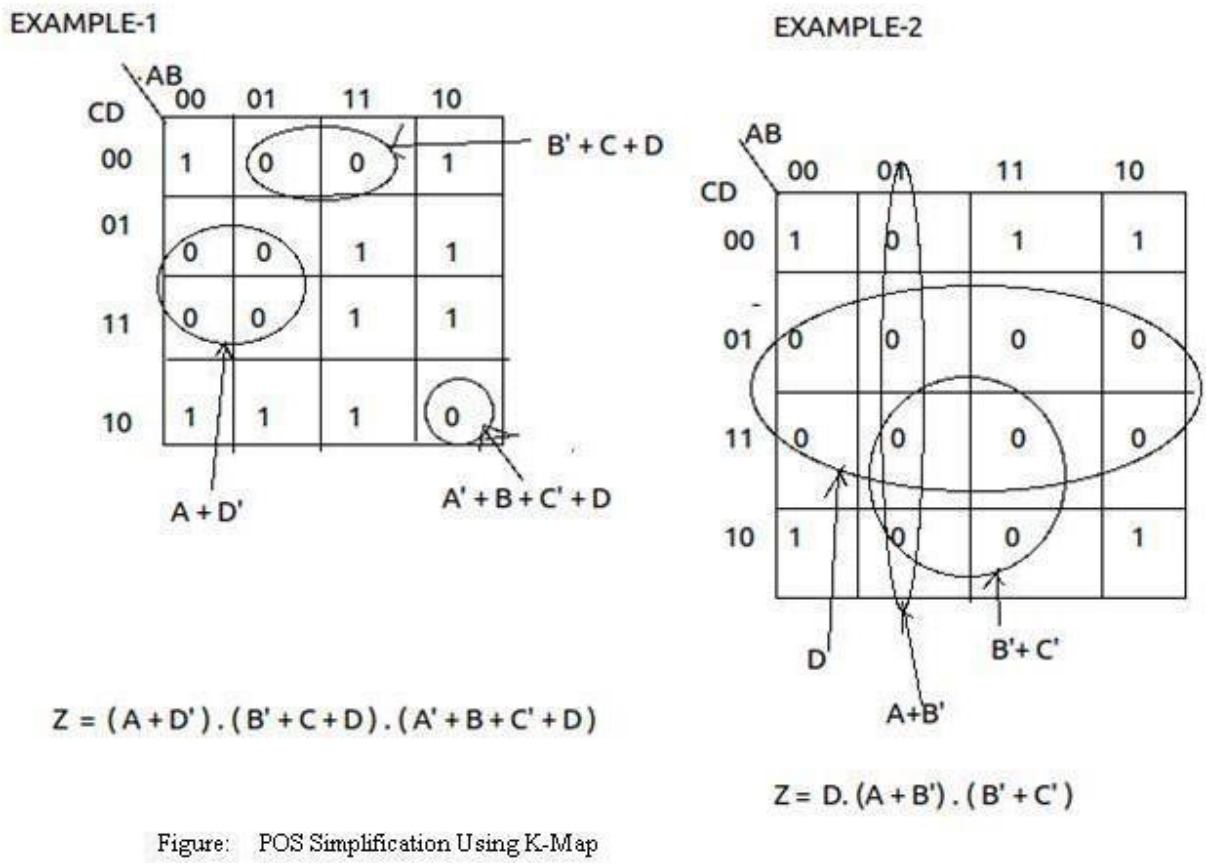


Figure: POS Simplification Using K-Map

Rules for Grouping:

Same as for sum-of-products, except that zero's are grouped instead of ones. Resulting Sum Terms:

1.If variable X has value 0 for all squares in the group, then the literal X is in the sum term.

2.If variable X has value 1 for all squares in the group, then the literal X' is in the sum term.

3.If variable X has value 0 for some squares in the group and value 1 for the others, then that variable does not appear in the sum term.

Prime Implicate: Maximal grouping of zeros b>Verification:

Result:- Hence, given Boolean Expression is implemented by the Logic Gates. SOP Equation

1). Y= AB' + CD'

POS equation

(i) D.(A+B').(B'+C')

(ii) (A+D'). (B'+C+D). (A'+B+C'+D)

PROCEDURE:

1. Check the components for their working.

2. Insert the appropriate IC into the IC base.

3. Make connections as shown in the circuit diagram.

4. Provide the input data via the input switches and observe the output on output LEDs.

RESULTS AND DISCUSSION:

Hence given Boolean Expression is implemented by the Logic Gates.

SOP EQUATION:-

Y = AB’ + CD’

POS EQUATION:-

➔ D.(A+B’).(B’+C’)
➔ (A+D’).(B’+C+D).(A’+B+C’+D)

CONCLUSION: Thus realised the Boolean algebra using gates.

LAB OUTCOMES: Students will be able to

1. Minimize the Boolean algebra and design it using logic gates.
2. Analyse and design combinational circuit.

COURSE OUTCOMES: Students will be able to

1. Represent numbers and perform arithmetic operations.
2. Minimize the Boolean expression using Boolean algebra and design it using logic gates