An ultra-low power RISC-V processor pipeline structure

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Abstract: With the rapid development of communication and chip technology, the Internet of Things will be an important part of the next generation of information technology and a powerful driving force for the process of intelligent life. Ultra-low-power microcontrollers play an integral role in IoT's end-device applications. Based on the design goal of ultra-low power embedded applications, a processor pipeline architecture based on RISC-V instruction set architecture is proposed. Considering the compromise between power consumption and performance, a two-stage sequential pipeline is adopted as the main component. , supplemented by a pipeline structure with variable length of other components. The logic function of the microcontroller is verified in the VCS environment. At the same time, the SMIC180 process library is used to complete the simulation in the DC environment, and the area ratio report of the microcontroller is obtained. Finally, by running the running subroutine test and comparing it with the ARM Cortex-M microcontroller, the comparison results show that this work can also be applied to the low-power scene of IoT.

Keywords: pipeline structure low power RISC-V architecture RISC-V processor

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An ultra-low-power processor pipeline-structure

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Abstract: With the rapid development of communication and chip technology, IoT will be an important part of the next generation of information technology, a powerful driving force to promote the intelligent process of our lives. Among the IoT terminal applications, ultra-low-power microcontroller plays An indispensable role. Based on the design goal of ultra-low-power embedded applications, this paper proposes a pipeline structure of a processor based on RISC-V instruction set architecture. Taking into account the compromise between power consumption and performance, the main body Uses a two-stage pipeline, and was supplemented by a pipeline structure with variable length of other components. The logic function of the microcontroller is verified in the VCS environment. At the same time,The area ratio report of the microcontroller is

obtained by using the SMIC180 process library to complete the simulation in the DC environment. Finally, by running the running subroutine test and comparing it with the ARM Cortex-M microcontroller, the comparison results show that this work Can also be applied to the low-power scene of IoT.

Key words : pipeline-structure;ultra-low-power;RISC-V architecture;RISC-V processor

0 Preface

After decades of evolution in processor design technology and the development of large-scale integrated circuit design techniques, the hardware scheduling capabilities of high-performance processors are already very strong, and the main frequency is already very high, so hardware designers hope that the instruction set can be structured and simplified, and higher frequency so as to design a more low-power processors. On the other hand, for IoT (Internet of Thing) applications such as wearable systems and healthcare [1-2] and other IoT applications such as Smart City [3], Intelligent Transportation [4] processors for low power consumption and The requirements for small areas are higher. However, due to commercial reasons and intellectual property protection, traditional instruction set architectures such as the ARM and X86 architectures require high licensing fees. The open source instruction set architecture RISC-V [5] architecture is a new instruction set architecture, a live, patent-free, history-free instruction set architecture, and is released under the BSD license. The RISC-V instruction set architecture is extremely simple, modular, and customizable. This also enables the RISC-V instruction set architecture to build microprocessors in virtually any field by combining or extending instruction sets, such as cloud computing, storage, parallel computing, virtualization/containers, MCUs, application processors, and DSP processors. .

1 Overall structure design of Hummingbird E203

The structure diagram of the E203 processor core is shown in Figure 1. The first stage of the pipeline is "finger" (completed by the IFU). "Decode" (completed by EXU), "Execute" (completed by EXU), and "Write Back" (completed by WB) are all in the same clock cycle, at the second level of the pipeline. The "access" (completed by LSU) phase is in the third-stage pipeline after the EXU, but the result of the LSU write still needs to be written back to the general register bank (Register File, Regfile) through the WB module. Therefore, strictly speaking, Hummingbird E203 is a variable length pipeline structure . However, the sequential body of the Hummingbird E203 processor core is the "finger" in the first level and the "execution" and "write back" in the second level. Therefore, the pipeline length of the Hummingbird E203 processor core is not strictly defined in this paper. Second level.

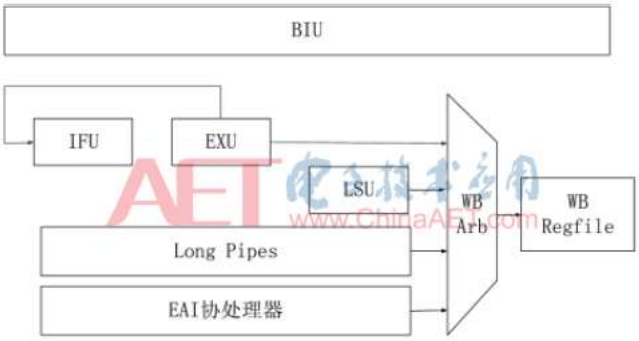

图 1 E203 处理器核的结构示意图

2 Hummingbird E203 unit design

2.1 Design of the fetching finger (IFU) unit

The IFU micro-architecture is shown in Figure 2. The Mini-Decode module is mainly used to decode the retrieved instructions. The Simple-BPU module is mainly used for branch prediction of the branch jump instruction found after the retrieved instruction is decoded by the Mini-Decode module. The PC generation logic is used to generate the next PC to be fetched. Address judgment and ICB bus control access the ITCM

Mr. Zhou Zucheng, a retire
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or BIU based on the PC's address. The ITCM is stored as an instruction, and if the address of the instruction fetch does not fall within the interval in which the ITCM is located, the IFU will access the external memory through the BIU.

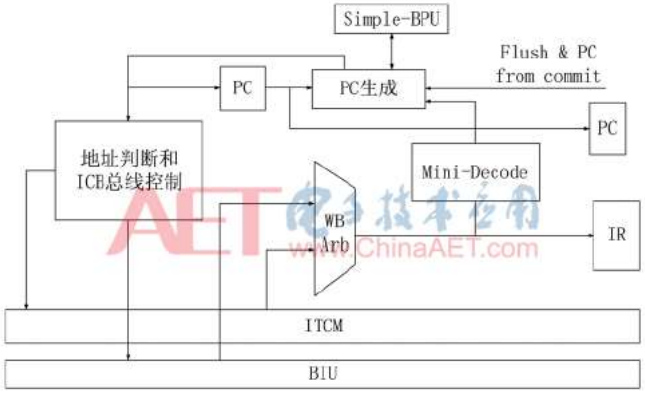

图 2 IFU 微架构示意图

After the IFU fetches the instruction, it will place it in the IR (Instruction Register) register that interfaces with the EXU unit. The PC value of this instruction will also be placed in the PC register that interfaces with the EXU unit. The EXU unit will use this IR and PC for subsequent execution.

2.2 Implementation (EXU) unit design ideas

The EXU micro-architecture is shown in Figure 3. The functions of the EXU unit are mainly: decoding and dispatching the IFU through the register to the EXU; reading the Regfile through the decoded operand register index; maintaining the data dependency of the instruction ; dispatch the instruction to a different arithmetic unit; deliver the instruction; write the result of the instruction operation back to Regfile.

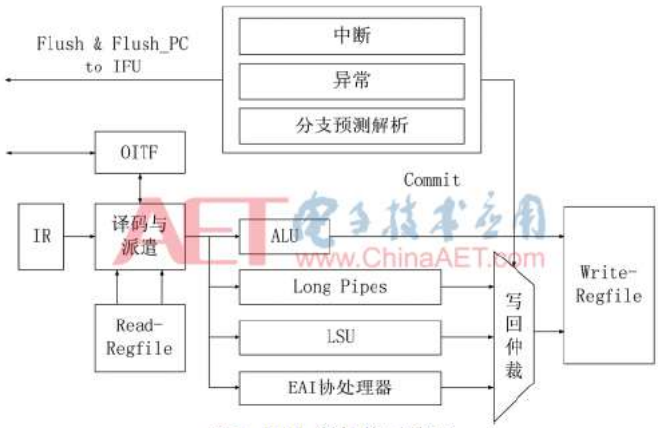

图 3 EXU 微架构示意图

2.2.1 Decoding and Dispatch Module

译码(Decode)模块主要用于将IFU通过IR寄存器发送给EXU的指令进行译码。译码模块完全由组合逻辑组成，其主要逻辑即根据RISC-V指令的编码规则进行译码，产生不同的指令类型信息、操作数寄存器索引等。

蜂鸟E203是简单的两级流水线架构，派遣(Dispatch)发生在流水线的执行阶段，表示指令经过译码且从寄存器组中读取了操作数之后被派遣到不同的运算单元(ALU、Long Pipes、LSU和EAI)执行的过程。

2.2.2 整数通用寄存器模块

整数通用寄存器组(Integer Register File，简称Integer-Regfile)模块主要用于实现RISC-V架构定义的整数通用寄存器组，其微架构如图4所示。RISC-V的整数指令都是单操作数或两操作数指令，且蜂鸟E203属于单发射(一次发射派遣一条指令)的微架构，因此Integer-Regfile模块只需要支持最多两个读端口。同时，蜂鸟E203的写回策略是按顺序每次写回一条指令的微架构，因此Integer-Regfile模块只用支持一个端口。

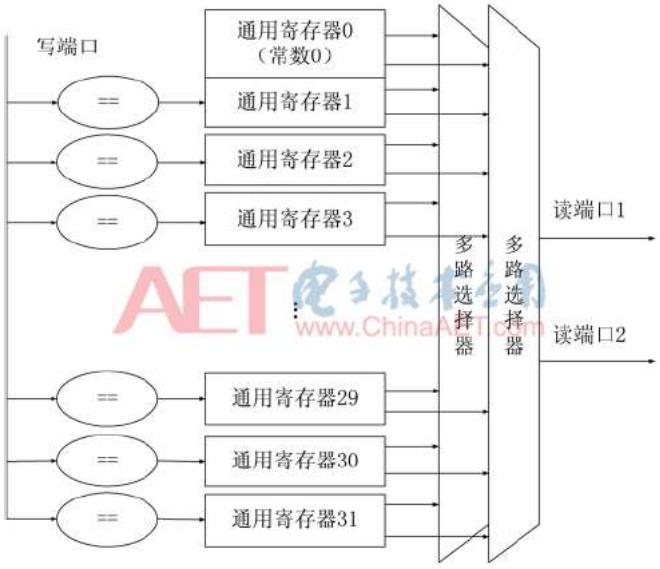

图 4 Integer-Regfile 微架构示意图

2.2.3 ALU模块

如图5所示，蜂鸟E203的ALU单元包括5个功能子单元。普通ALU运算主要负责普通的ALU指令（逻辑运算、加减法移位等指令）的执行；访问地址生成主要负责Load、Store和“A”扩展指令的地址生成；分支预测解析主要负责Branch和Jump指令的结果解析和执行；CSR读写控制主要负责CSR指令的执行；多周期乘除法器主要负责乘法和除法指令的执行。以上5个功能子单元只负责具体指令执行的控制，它们均共享一份实际的运算数据通路，因此主要数据通路的面积开销只有一份，这也是蜂鸟E203追求低功耗和小面积的一大亮点。

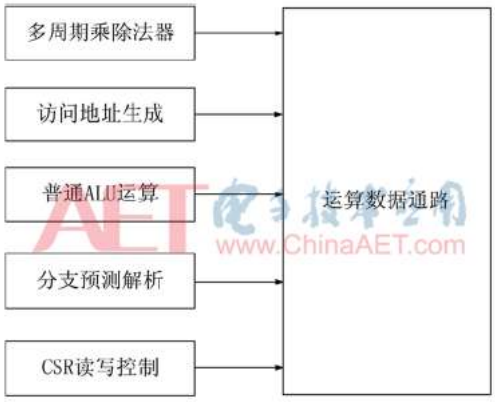

图 5 ALU 框图

2.2.4 状态寄存器（CSR）模块

RISC-V架构中定义了一些控制和状态寄存器(Control and Status Register，CSR)，用于配置或记录一些运行的状态。CSR寄存器是处理器核的内部寄存器，使用其自己的地址编码空间，与存储器寻址的地址区间完全无关系。蜂鸟E203的EXU单元中的CSR寄存器模块主要用于实现蜂鸟E203所支持的寄存器功能。如在ALU模块中的CSR读写寄存器模块会产生CSR读写控制信号。

2.2.5 OITF模块

OITF本身只是一个先进先出的FIFO，FIFO的默认深度是2个表项。如图6所示，每条指令在派遣时，都会将本指令的源操作数寄存器索引和结果寄存器索引与OITF中的各个表项进行对比，从而判断本指令是否已经派遣出以及检查其是否与尚未写回的长指令产生RAW和WAW相关性。在整个过程中，由于蜂鸟E203主要侧重于低功耗和小面积，因此只采用了阻塞流水线而未使用快速旁路的方法。

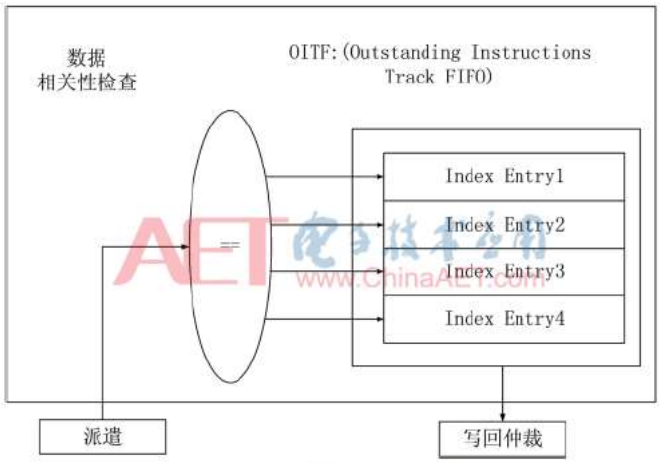

图 6 OITF 微架构示意图

2.2.6 交付（Commit）模块

RISC-V指令集架构具有指令没有条件码和所有的运算指令都不会产生异常这两个显著的特点，因此可以大幅度简化“交付”的硬件实现。无论是单周期指令还是多周期指令，在蜂鸟E203处理器中都将“交付”安排在“执行”阶段。

2.2.7 写回仲裁（WB-Arb）模块

蜂鸟E203处理器的写回策略是一种因地制宜的混合策略。其核心思想是将指令划分为单周期指令和长指令两大类；以及将长指令的“交付”和“写回”分开，使得即便执行了多周期指令，仍然不会阻塞流水线，让后续的单周期指令仍然能够顺利地写回和交付。

如图3所示，蜂鸟E203处理器有两级写回仲裁模块，其一是最终写回仲裁，主要用于仲裁所有单周期指令的写回（来自ALU模块）和所有长指令的写回（来自长指令写回仲裁模块），仲裁采用优先级仲裁的方式。在没有长指令写回的空闲周期，单周期指令可以随便写回。而对于长指令的写回，则由OITF和长指令写回仲裁模块协同完成所有长指令的写回操作。

3 综合仿真分析与跑分测试

表1为蜂鸟E203 CPU的面积分布占比报告，其中CPU核的面积为233 329.695 5 μm^2，占整个CPU面积的93.5%，CPU的其他部分的面积为16 334.17 μm^2，占整个CPU的6.5%。

表 1 CPU 面积分布占比

模块		面积/μm^2	百分比/%
CPU	Core	233 329.695 5	93.5
	Others	16 334.17	6.5
Total		249 663.865 5	100

表2为CPU核的面积分布占比报告，BIU单元、EXU单元、IFU单元和LSU单元的面积占比分别为6.2%、73.2%、9.8%和4.3%，合计为CPU核的面积占比即93.5%。

表 2 Core 面积分布占比

模块		面积/μm^2	百分比/%
Core	BIU	15 547.661 3	6.2
	IFU	24 357.31 5	9.8
	EXU	182 686.430 4	73.2
	LSU	10 710.067 4	4.3
Total		233 329.695 5	93.5

表3为EXU单元的面积占比报告，译码、整数通用寄存器组、状态寄存器、派遣、ALU、交付、OITF、长指令写会仲裁、最终写回仲裁模块的面积占比分别为1.5%、36.5%、11.8%、0.6%、16.6%、2.5%、2.9%、0.4%和0.3%，合计为EXU单元的面积占比即73.2%。

表 3 EXU 面积分布占比

模块		面积/μm²	百分比/%
EXU	译码	3 763.200 1	1.5
	整数通用寄存器组	91 014.876 5	36.5
	状态寄存器	29 501.607 1	11.8
	派遣	1 569.254 4	0.6
	ALU	41 494.925 6	16.6
	交付	6 305.241 7	2.5
	OITF	7 257.331 4	2.9
	长指令写回仲裁	967.142 4	0.4
	最终写回仲裁	773.337 6	0.3
Total		182 686.430 4	73.2

对表1、2、3中的数据分析可以得出，蜂鸟E203在满足一定性能的情况下达到了小面积的设计目的。

另外，为了衡量蜂鸟E203处理器的性能，本文通过跑分程序（Benchmarks）对其进行了跑分测试，并与ARM Cotex-M0+处理器进行比较。从表4可以看出，蜂鸟E203性能均不逊色于ARM的Cotex-M0+处理器(M0+是ARM面积最小的处理器核)。

表 4 E203 和 ARM Cotex-M0+的跑分比较

Benchmarks	ARM Cotex-M0+	E203
Dhrystone(DMIPS/MHz)	0.94(official) 1.31(Max options)	1.23
Coremarks(Coremark/MHz)	2.42	2.14

4 结论

本文介绍了一种RISC-V处理器流水线架构，综合仿真和跑分测试结果表明蜂鸟E203可面向极低功耗与极小面积的场景，非常适合于替代传统的8051内核或者Cortex-M系列内核应用于IoT或其他低功耗场景。

参考文献

[1] ISLAM S M R，KWAK D，KABIR M H，et al.The Internet of Things for health care: a comprehensive survey[J].IEEE Access，2017，3：678-708.

[2] LAPLANTE P A，LAPLANTE N.The Internet of Things in healthcare: potential applications and challenges[J].IT Professional，2016，18(3)：2-4.

[3] ZANELLA A，BUI N，CASTELLANI A，et al.Internet of Things for smart cities[J].IEEE Internet of Things Journal，2014，1(1)：22-32.

[4] LU N，CHENG N，ZHANG N，et al.Connected vehicles：solutions and challenges[J].IEEE Internet of Things Journal，2014，1(4)：289-299.

[5] WATERMAN A，LEE Y，PATTERSON D A，et al.The RISC-V instruction set manual, volume I：base user-level ISA[J].Eecs Department，2011，7(9)：475.

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Implementation of FPGA-based Shift Register Pipeline Structure FFT Processor

A 12-bit 50MS/s CMOS pipelined A/D converter [Figure]

A 6.4 ppm/°C low power bandgap reference design

Low-power implementation method of half-band filter

Structure Design and FPGA Implementation of a Low Storage Capacity Turbo Code Decoder

Design of High Integrated Low Power High Order Active Low Pass Filter Based on Monolithic MO-

Toshiba Introduces Low-Power Brushed DC Motor Driver IC New Motor Driver ICs in a Compatible