Thermal Design Concepts

Prof. Kurian Polachan, IIIT-B

Energy Usage

E_i

(AC Mains, Battery …)

Work

(Processing, Amplification …)

Energy Efficiency

For Any System, Work Done < E_i

Work Done = $\eta E_i \mid \eta < 1$

Energy Efficiency

E_i →  → Work

Work Done = $\eta\, E_i \mid \eta < 1$

for i5, $\eta \sim 70\%$

Wasted Energy

for i5, $\eta \sim 70\%$

100 Wh → → **η100 Wh = 70 Wh**

$$\underbrace{(1-\eta)100\text{ Wh} = 30\text{ Wh}}_{\text{Wasted}}$$

Heat Dissipation

100 Wh → 

→ η100 Wh = 70 Wh

$\underbrace{(1-\eta)\text{100 Wh} = \text{30 Wh}}_{}$ Wasted

Wasted Energy → Dissipated as Heat

Temperature Rise

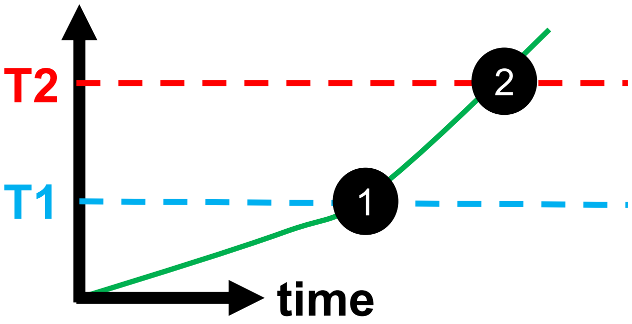
Wasted Energy → Dissipated as Heat

IC Temperature Rises

The Problem

Temperature Rise Leads to,

1. Reduced Performance
2. Permanent Damage



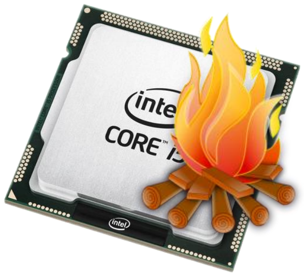
Quantify Temp Rise

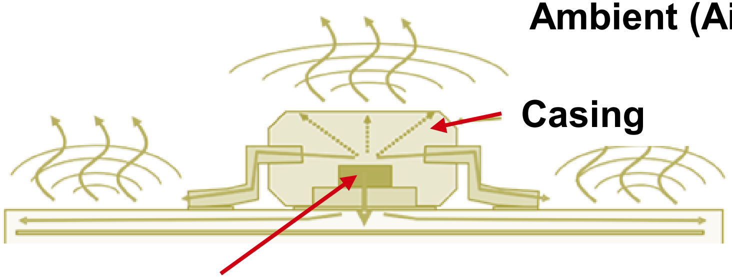
IC Temperature Rises

But, How much ?

The Need for Thermal Modeling

Heat Flow



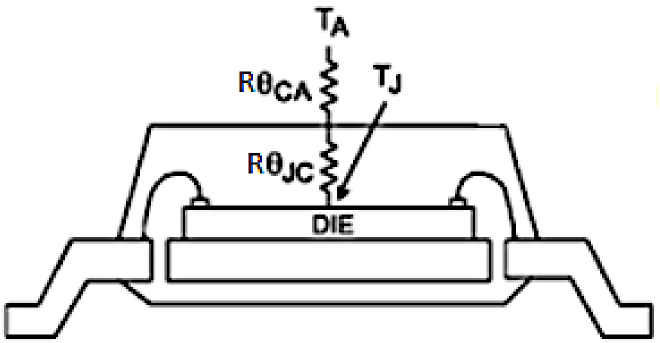


Die $\xrightarrow[\text{Flow}]{\text{Heat}}$ Casing $\xrightarrow[\text{Flow}]{\text{Heat}}$ Ambient

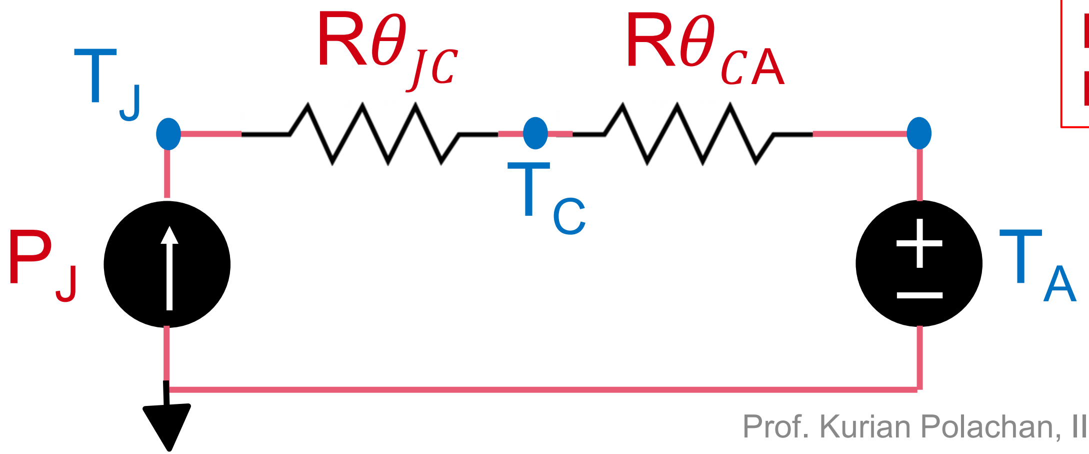
(T_J°) (T_C°) (T_A°)

$$\boxed{T_J° > T_C° > T_A°}$$

Thermal Model



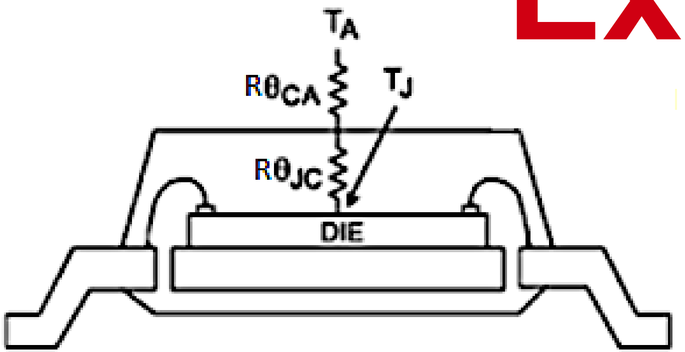
Die (T_J°) $\xrightarrow{\text{Heat Flow}}$ Casing (T_C°) $\xrightarrow{\text{Heat Flow}}$ Ambient (T_A°)

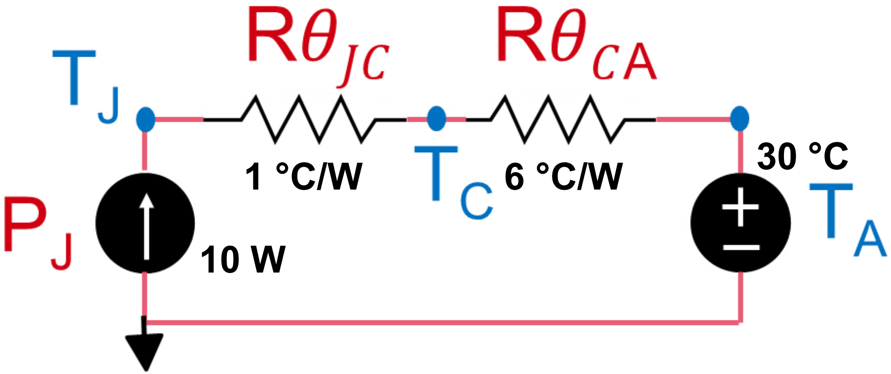


$R\theta$ → thermal resistance (°C/W)
P_J → power dissipated at die (W)

$$T_J = P_J\,(R\theta_{JC} + R\theta_{CA}) + T_A$$

Example





$$T_J = P_J\,(R\theta_{JC} + R\theta_{CA}) + T_A$$

$R\theta_{JC}$ = 1 °C/W
$R\theta_{CA}$ = 6 °C/W
P_J = 10 W
T_A = 30 °C

$T_J = 10*1 + 10*6 + 30 =$ 100 °C

What if the rated max T_J of the die is 80 °C ?

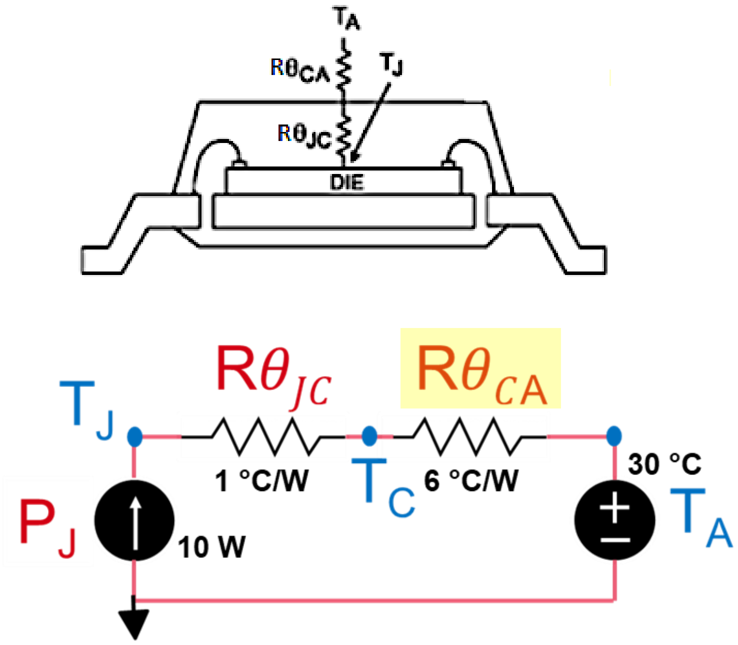
Solution – Use Heat Sink !

Heat Sink

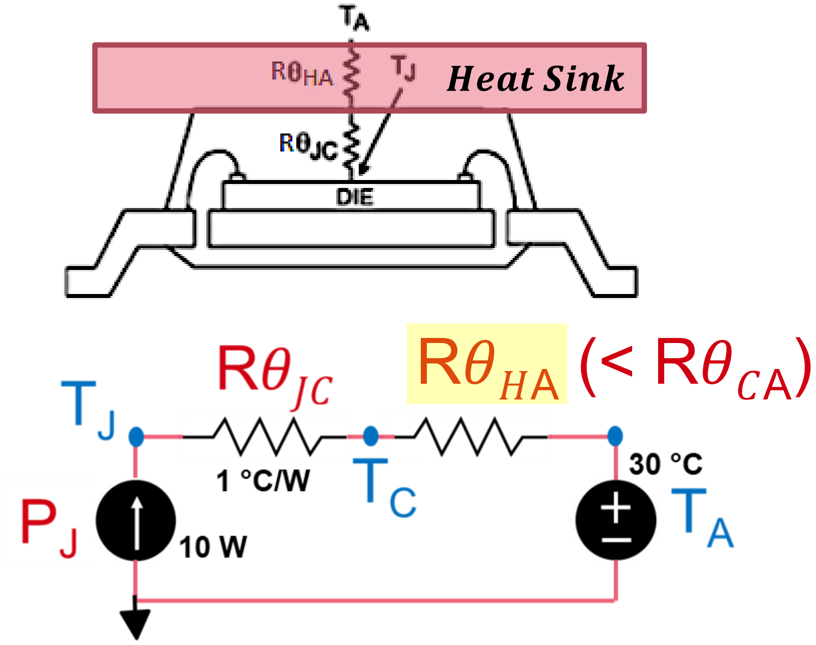
Heat sink improves the heat transfer from the die to ambient → lower T_J.

But how ?

Thermal Model with HS

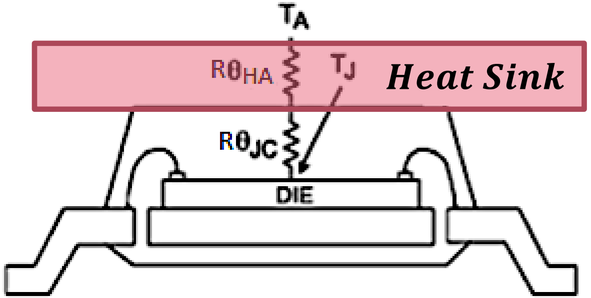


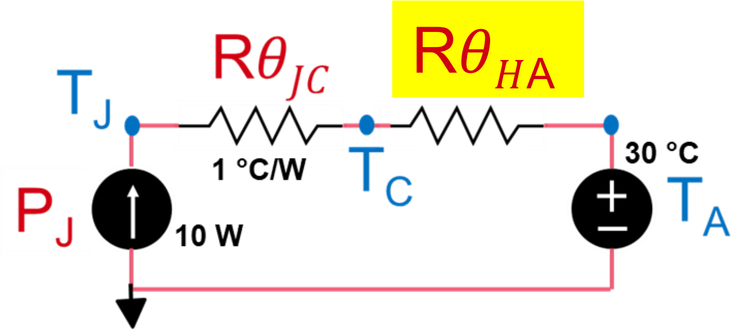
$T_J = 10*1 + 10*6 + 30 =$ **100 °C**



$T_J = 10*1 + 10*(R\theta_{HA}) + 30 <$ **100 °C**

Design of HS





$R\theta_{JC}$ = 1 °C/W
$R\theta_{CA}$ = 6 °C/W
P_J = 10 W
T_A = 30 °C
Rated max T_J of the die is 80 °C.

$$T_J = 10*1 + 10*(R\theta_{HA}) + 30 = 80\ °C$$

Required $R\theta_{HA}$ = **4** °C/W

Select a HS with $R\theta_{HA}$ = 4 °C/W.

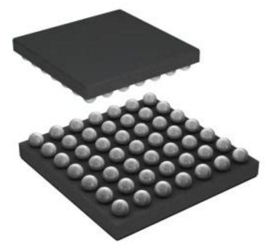
PSoC® 4: PSoC 4100_BLE Family Datasheet Programmable System-on-Chip (PSoC®)

E.g., PSoC

Table 56 Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	–	–40	25.00	105	°C
T_J	Operating junction temperature	–	–40	–	125	°C
T_{JA}	Package θ_{JA} (56-pin QFN)	–	–	16.9	–	°C/watt
T_{JC}	Package θ_{JC} (56-pin QFN)	–	–	9.7	–	°C/watt
T_{JA}	Package θ_{JA} (76-ball WLCSP)	–	–	20.1	–	°C/watt
T_{JC}	Package θ_{JC} (76-ball WLCSP)	–	–	0.19	–	°C/watt
T_{JA}	Package θ_{JA} (76-ball Thin WLCSP)	–	–	20.9	–	°C/watt
T_{JC}	Package θ_{JC} (76-ball Thin WLCSP)	–	–	0.17	–	°C/watt
T_{JA}	Package θ_{JA} (68-ball WLCSP)		–	16.6	–	°C/watt
T_{JC}	Package θ_{JC} (68-ball WLCSP)		–	0.19	–	°C/watt
T_{JA}	Package θ_{JA} (68-ball Thin WLCSP)		–	16.6	–	°C/watt
T_{JC}	Package θ_{JC} (68-ball Thin		–	0.19	–	°C/wat

56-Pin QFN
Ref: DigiKey



49-Ball WLCSP
Ref: DigiKey

Reading

- What is a thermal capacitance ?
- Does thermal capacitance affect heat sink design ?
- MacBook Air and MacBook Pro (What is the difference ?)