V12 REVISION HISTORY

ECR#: ECR-001-CLVESBMS

Sheet Name	Design Change Description
AFE	J17 added for Relay interface VC14 taken out to 14th cell BST82,215,Q19, manufacturer changed to "Nexperia" Relay driver cirucuit included
Charge _ Discharge	C132, D77,R236,R237 to be populated C7 changed to 10uF,35V,1206 R208 value changed to 60.4K Pow er Sw itch added between 12V and MOSFET driver D78 removed D7 changed to 0E BST82,215,Q34, manufacturer changed to "Nexperia" R219, gate resistor in Discharge path changed to 300K Series Gate Resistors added to charge & discahrge MOSFETs Load Sw itch, TPS22810TDBVRQ1, added to pow er MOSFET drivers "I_SENSE_UC" signal given to U24-In2- pin through a 0E Resistor 0E added between U24-1 and U24-8, "OUTA" label to U24-6 removed Buffer added to disable Relay in SC R230 changed to 1M
PreCHG _ PreDSG	Precharge Resistors changed to "H5WI*5KV J 150R" D71 removed
Cell Balancing	Updated to 15 cell configuration
Host uC	PC9 multiplexed with "SOC_LED4" and "UC_PV_S_EN_DO_M" J18, current sense I/P conn., for Relay application, added with I_SENSE given to PA6 PA4 given to Load sw itch enable of MOSFET drivers 0E added across U19 for bypass option 0E added to VBAT pin to pow er from coin cell "CMI-1210-92T", 12V Buzzer added as an option R232 changed to 0E 10K added across Buzzer pins
Isolated_CAN	0E added to coin cell to feed VBAT of controller as an option "ISO2_GND" and "GND" options given to Coin cell return through 0E resistors
Temp Sensor_DAC_Speed_Monitor	Bypass option provided for Opto-Isolator of Speed monitor circuit R123 changed to 0E R86 made DNP
Pow ersupply	Pow ersupply IC changed to "LM5164DDAR" "TPS7B8133QDRVRQ1" - 12V to 5V converter added J19 added across R19 to connect reserve battery sw itch
Connectors_Mechanical_Parts	Aluminium Extrusion Heatsink (68x11.5x19.92) provisioned JTAG header changed to "FTSH-105-01-L-DV-K"

Variant	Configuration	Application
48V28Ah	15SLFP	2W/3W BMS

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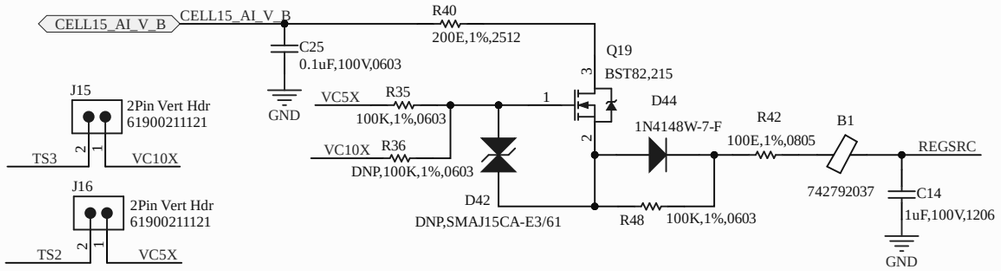
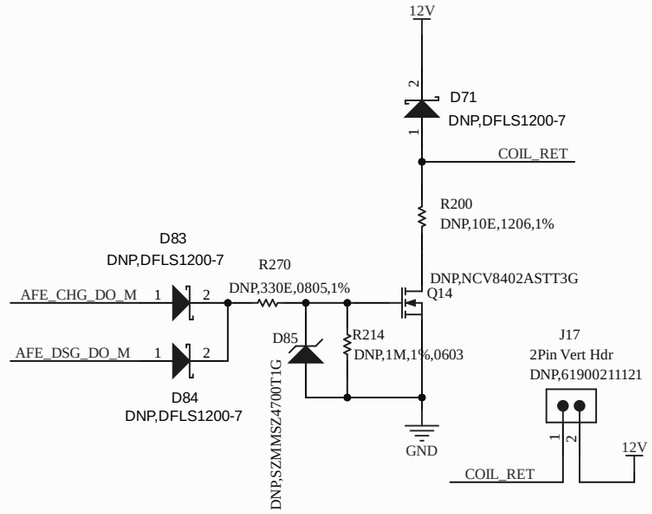
Document Number : 1 Size: A4

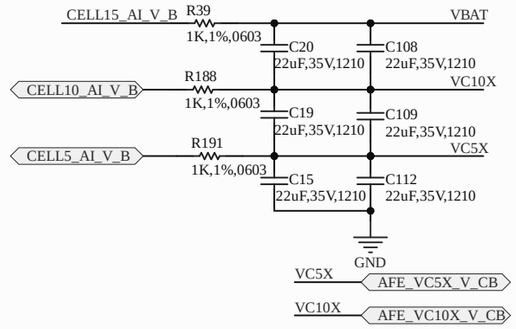
Title : EVB48V-V1 Full.PrjPcb

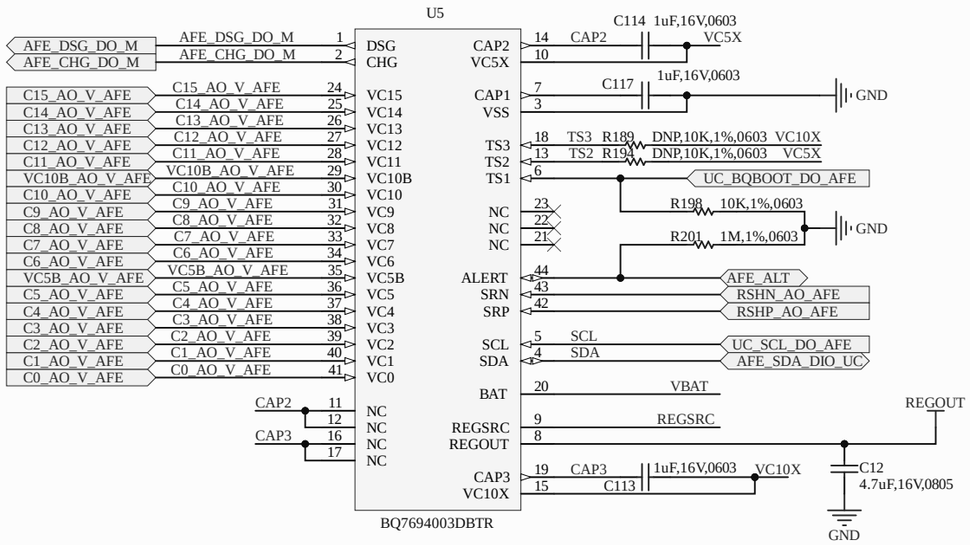
Revision	Issue	Date	Design Status	Drawn By	Approved By
1.2		04-10-2021	Under Development	Bharani Latha R	Devarajan S

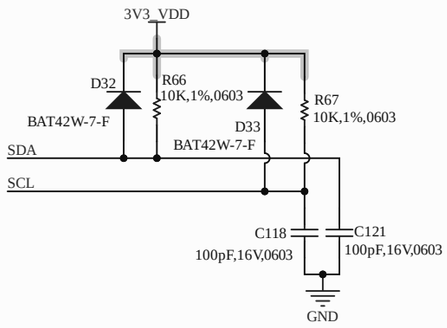
Sheet Title : Rev_History.SchDoc Printed : Sheet 1 of 14











BQ76940 Pin Cell Input	13 Cells	14 Cells	15 Cells
VC15–VC14	CELL 13	CELL 14	CELL 15
VC14–VC13	short	short	CELL 14
VC13–VC12	CELL 12	CELL 13	CELL 13
VC12–VC11	CELL 11	CELL 12	CELL 12
VC11–VC10b	CELL 10	CELL 11	CELL 11
VC10–VC9	CELL 9	CELL 10	CELL 10
VC9–VC8	short	CELL 9	CELL 9
VC8–VC7	CELL 8	CELL 8	CELL 8
VC7–VC6	CELL 7	CELL 7	CELL 7
VC6–VC5b	CELL 6	CELL 6	CELL 6
VC5–VC4	CELL 5	CELL 5	CELL 5
VC4–VC3	CELL 4	CELL 4	CELL 4
VC3–VC2	CELL 3	CELL 3	CELL 3
VC2–VC1	CELL 2	CELL 2	CELL 2
VC1–VC0	CELL 1	CELL 1	CELL 1

BQ76930 to be populated in U5 for 7 Cell Configuration

BQ76930 Pin Cell Input	7 Cells
VC10–VC9	CELL 7
VC9–VC8	short
VC8–VC7	short
VC7–VC6	CELL 6
VC6–VC5b	CELL 5
VC5–VC4	CELL 4
VC4–VC3	short
VC3–VC2	CELL 3
VC2–VC1	CELL 2
VC1–VC0	CELL 1

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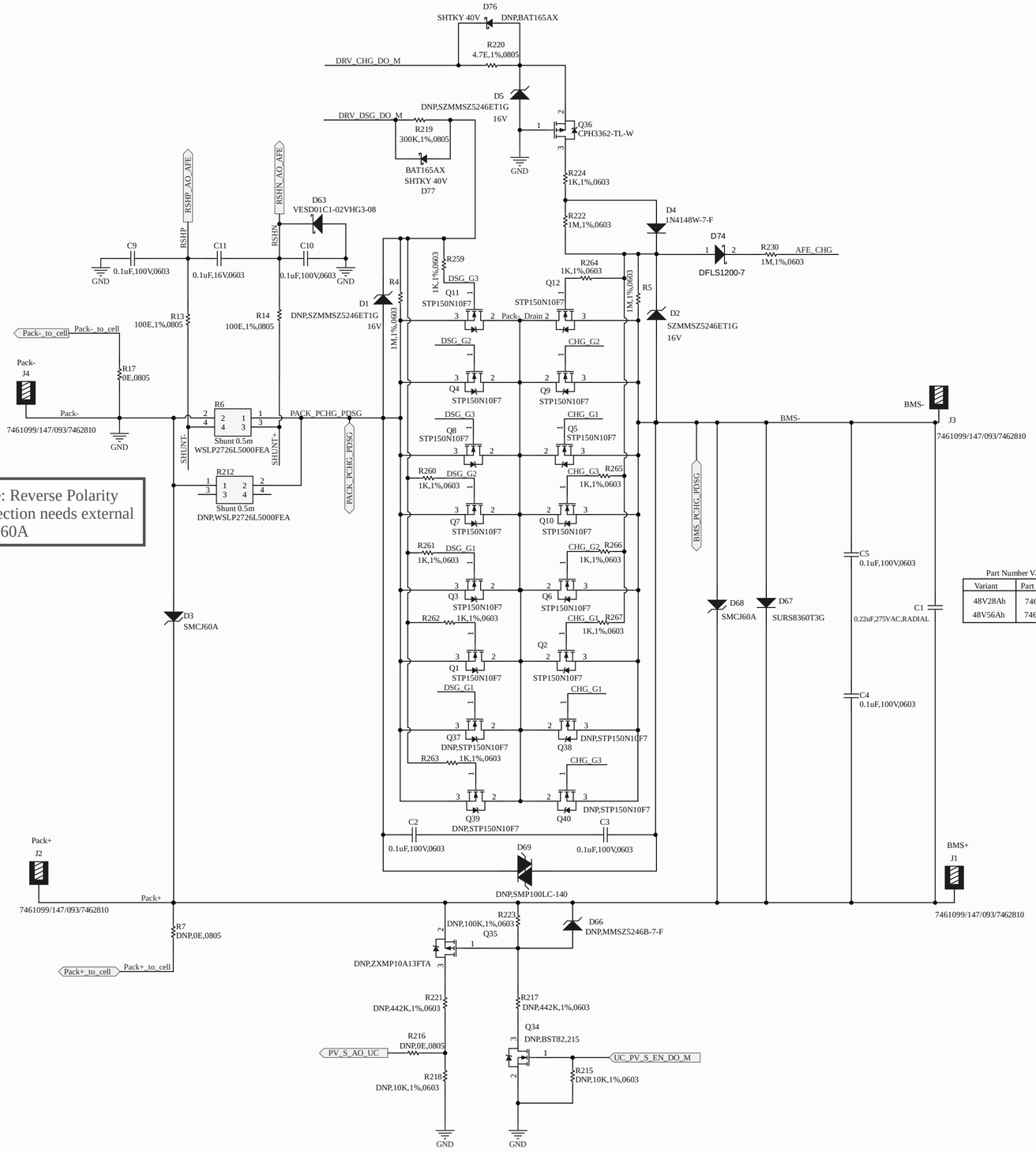
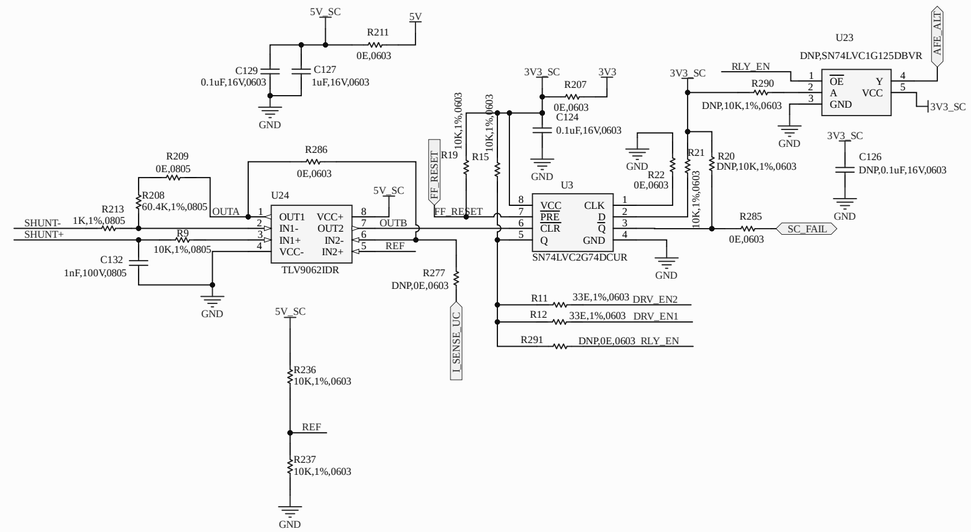
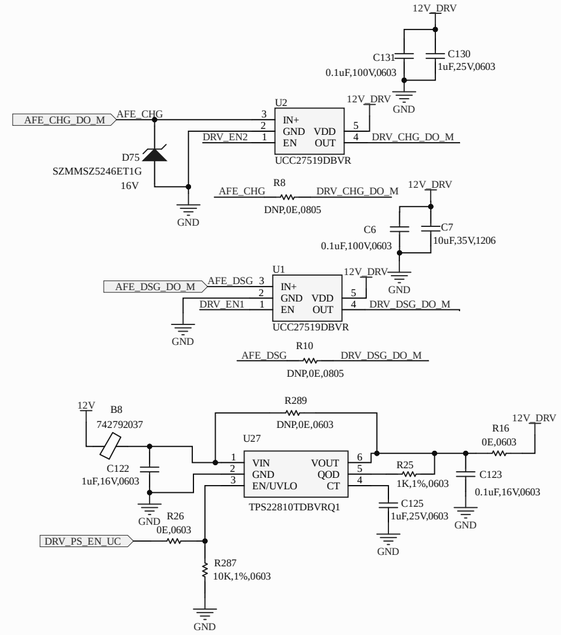
Title : EVB48V-V1 Full.PrjPcb

Revision	Issue	Date	Design Status	Drawn By	Approved By
1.2		04-10-2021	Under Development	Bharani Latha R	Devarajan S

Sheet Title : AFE.SchDoc Printed : Sheet 2 of 14







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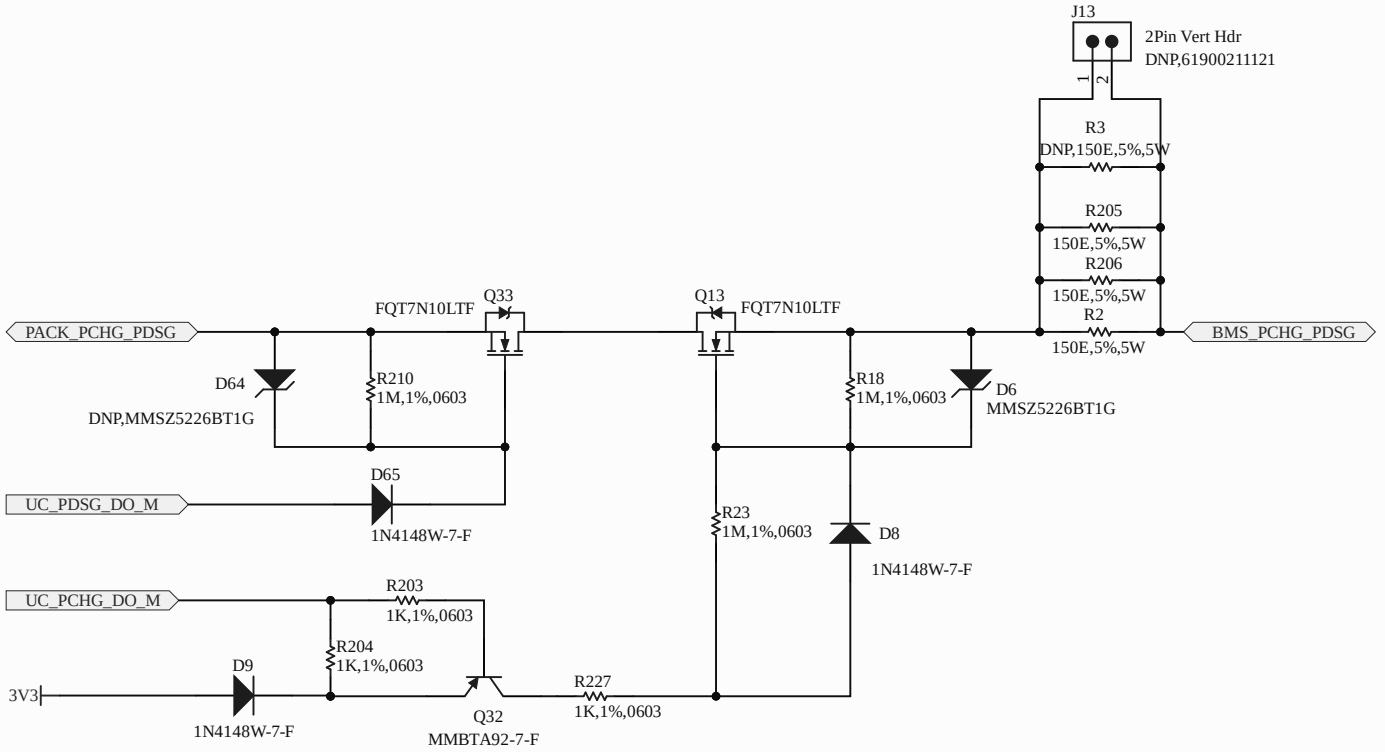
Sheet Title :	Charge _ Discharge.SchDoc		Printed :	Sheet 3 of 14	



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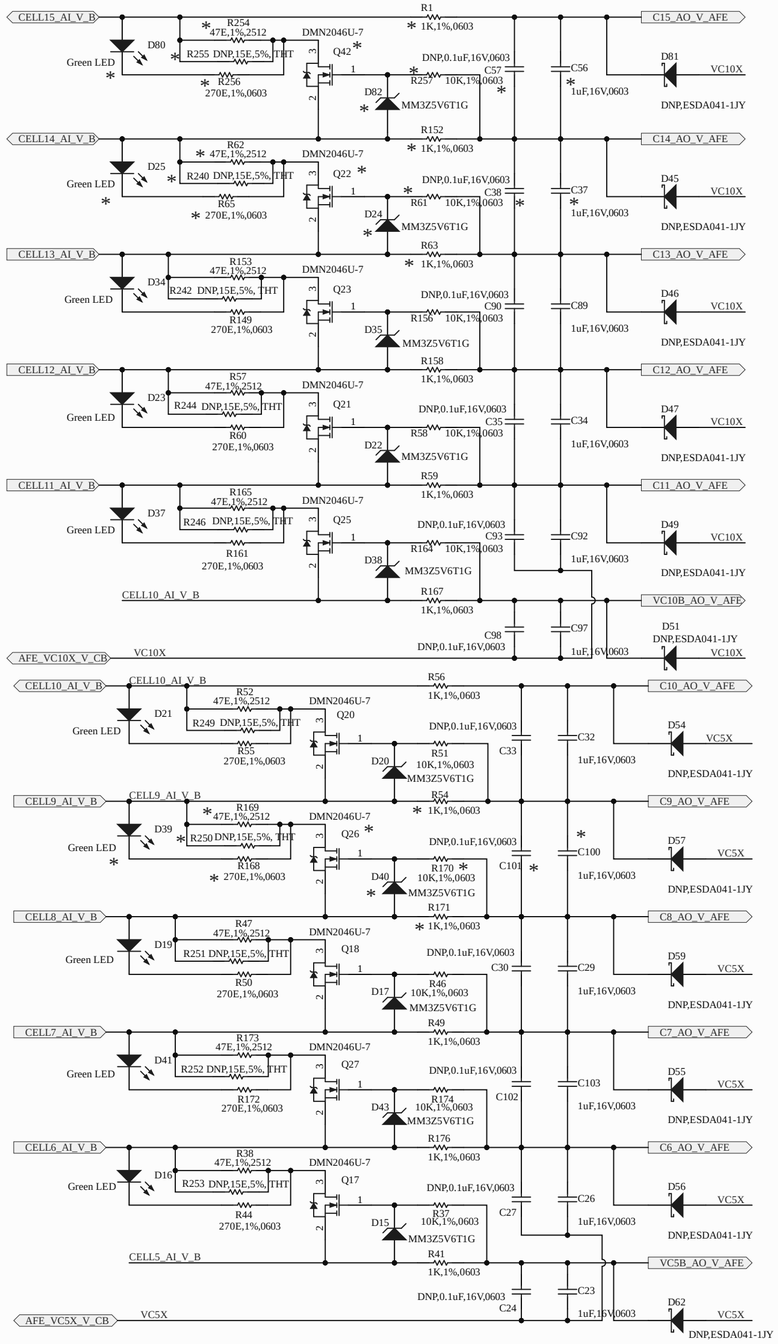

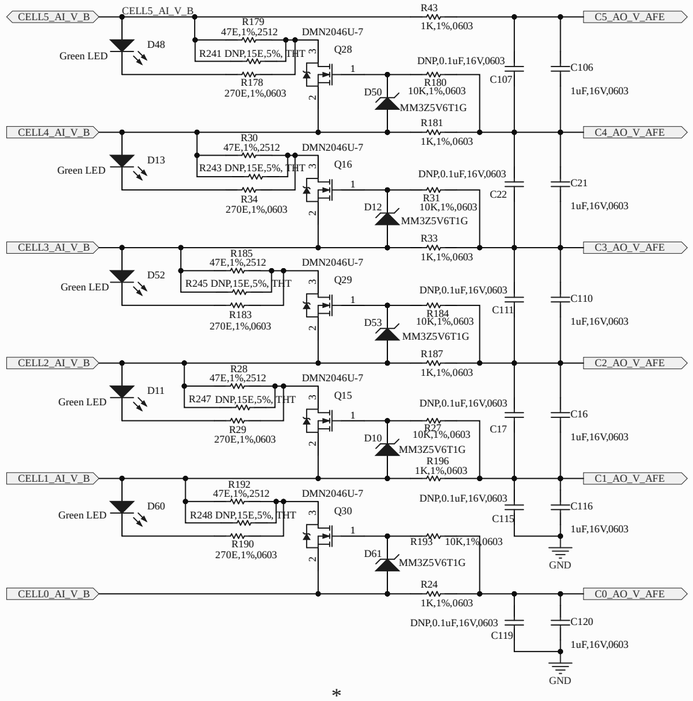

*

Connector J5 PIN	Assembly Options		
	13 Cells	14 Cells	15 Cells
1	Connect to Cell0	Connect to Cell0	Connect to Cell0
2	Connect to Cell1	Connect to Cell1	Connect to Cell1
3	Connect to Cell2	Connect to Cell2	Connect to Cell2
4	Connect to Cell3	Connect to Cell3	Connect to Cell3
5	Connect to Cell4	Connect to Cell4	Connect to Cell4
6	Connect to Cell5	Connect to Cell5	Connect to Cell5
7	NC	NC	NC
8	Connect to Cell6	Connect to Cell6	Connect to Cell6
9	Connect to Cell7	Connect to Cell7	Connect to Cell7
10	Populate R269	Connect to Cell8	Connect to Cell8
11	Connect to Cell8	Connect to Cell9	Connect to Cell9
12	Connect to Cell9	Connect to Cell10	Connect to Cell10
13	NC	NC	NC
14	Connect to Cell10	Connect to Cell11	Connect to Cell11
15	Connect to Cell11	Connect to Cell12	Connect to Cell12
16	Populate R268	Populate R268	Connect to Cell13
17	Connect to Cell12	Connect to Cell13	Connect to Cell14
18	Connect to Cell13	Connect to Cell14	Connect to Cell15

*

Ref des	Assembly Options			
	7 Cells	13 Cells	14 Cells	15 Cells
D25		DNP	DNP	Populate
R62		DNP	DNP	Populate
R240		DNP	DNP	DNP
R65		DNP	DNP	Populate
Q22		DNP	DNP	Populate
D24		DNP	DNP	Populate
R61		DNP	DNP	Populate
R63		Populate	Populate	Populate
R152		DNP	DNP	Populate
C38		0E	0E	Populate
C37		DNP	DNP	DNP
D80		Populate	Populate	Populate
R254		Populate	Populate	Populate
R255		DNP	DNP	DNP
R256		Populate	Populate	Populate
Q42		Populate	Populate	Populate
D82		Populate	Populate	Populate
R257		Populate	Populate	Populate
R1		Populate	Populate	Populate
C57		DNP	DNP	DNP
C56		Populate	Populate	Populate
D39		DNP	Populate	Populate
R169		DNP	Populate	Populate
R250		DNP	DNP	DNP
R168		DNP	Populate	Populate
Q26		DNP	Populate	Populate
D40		DNP	Populate	Populate
R170		DNP	Populate	Populate
R171		Populate	Populate	Populate
R54		DNP	Populate	Populate
C101		DNP	DNP	DNP
C100		0E	Populate	Populate

esmito	Document Number : 5		Size: A4	
	Title : EVB48V-V1 Full.PrjPcb			
Revision	Issue	Date	Design Status	Drawn By	Approved By
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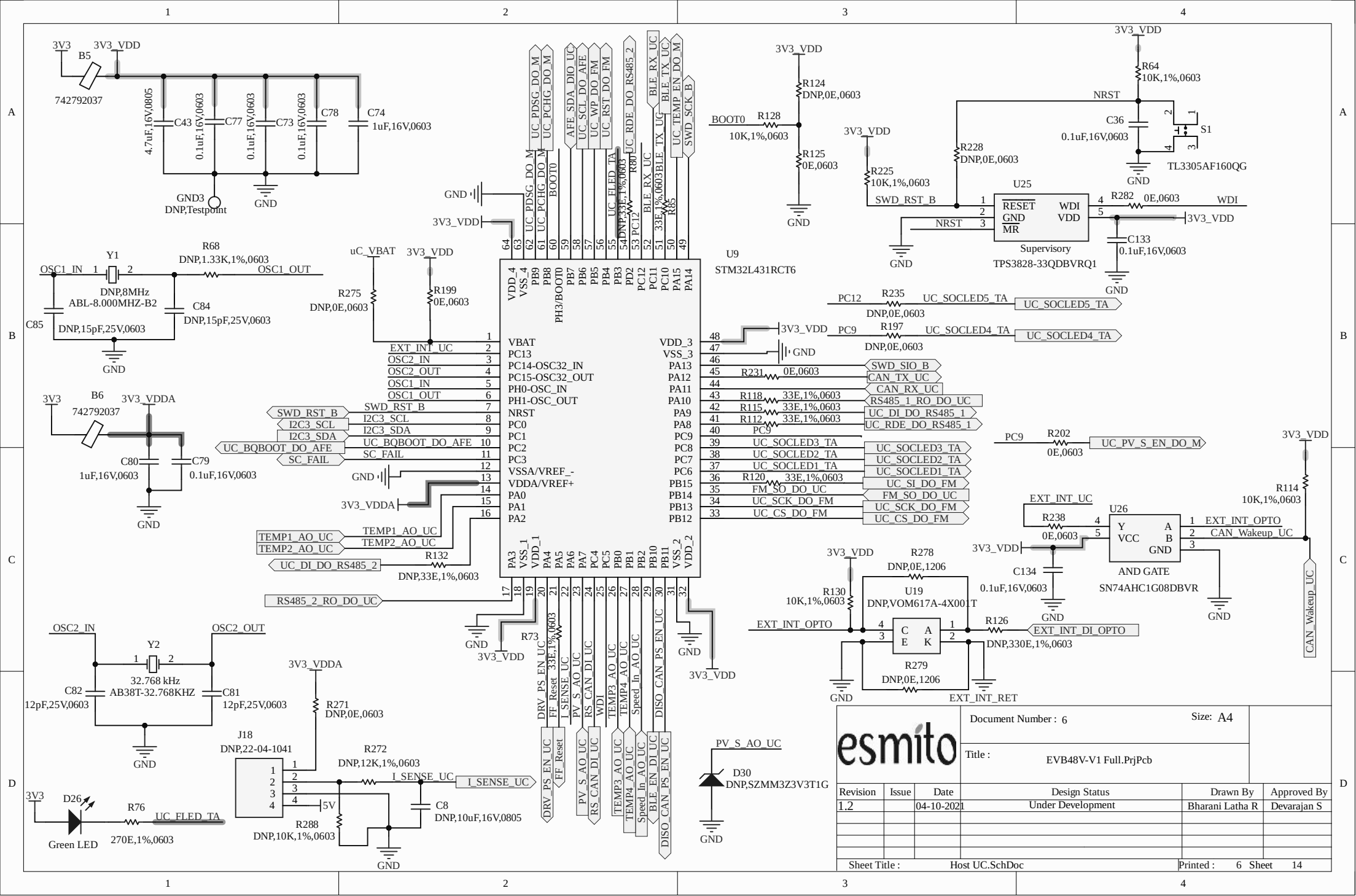
Sheet Title :	Cell Balancing.SchDoc		Printed :	Sheet 5 of 14	


3V3
3V3_VDD
B5
742792037
C43
4.7uF,16V,0805
C77
0.1uF,16V,0603
C73
0.1uF,16V,0603
C78
0.1uF,16V,0603
C74
1uF,16V,0603
GND3
DNP,Testpoint
GND
U9
STM32L431RCT6
VBAT
PC13
PC14-OSC32_IN
PC15-OSC32_OUT
PH0-OSC_IN
PH1-OSC_OUT
NRST
PC0
PC1
PC2
PC3
VSSA/VREF_-
VDDA/VREF+
PA0
PA1
PA2
VDD_4
VSS_4
PB9
PB8
PH3/BOOT0
PB7
PB6
PB5
PB4
PB3
PD2
PC12
PC11
PC10
PA15
PA14
VDD_3
VSS_3
PA13
PA12
PA11
PA10
PA9
PA8
PC9
PC8
PC7
PC6
PB15
PB14
PB13
PB12
PA3
VSS_1
VDD_1
PA4
PA5
PA6
PA7
PC4
PC5
PB0
PB1
PB2
PB10
PB11
VSS_2
VDD_2
UC_PDSG_DO_M
UC_PCHG_DO_M
BOOT0
AFE_SDA_DIO_UC
UC_SCL_DO_AFE
UC_WP_DO_FM
UC_RST_DO_FM
UC_FLED_TA
UC_RDE_DO_RS485_2
BLE_RX_UC
BLE_TX_UC
UC_TEMP_EN_DO_M
SWD_SCK_B
R124
DNP,0E,0603
R128
10K,1%,0603
R125
0E,0603
R64
10K,1%,0603
NRST
C36
0.1uF,16V,0603
S1
TL3305AF160QG
R225
10K,1%,0603
SWD_RST_B
R228
DNP,0E,0603
U25
RESET
GND
MR
WDI
VDD
Supervisory
TPS3828-33QDBVRQ1
R282
0E,0603
WDI
C133
0.1uF,16V,0603
Y1
OSC1_IN
OSC1_OUT
DNP,8MHz
ABL-8.000MHZ-B2
R68
DNP,1.33K,1%,0603
C84
DNP,15pF,25V,0603
C85
DNP,15pF,25V,0603
uC_VBAT
R275
DNP,0E,0603
R199
0E,0603
EXT_INT_UC
OSC2_IN
OSC2_OUT
OSC1_IN
OSC1_OUT
PC12
R235
DNP,0E,0603
UC_SOCLED5_TA
PC9
R197
DNP,0E,0603
UC_SOCLED4_TA
R231
0E,0603
SWD_SIO_B
CAN_TX_UC
CAN_RX_UC
R118
33E,1%,0603
RS485_1_RO_DO_UC
R115
33E,1%,0603
UC_DI_DO_RS485_1
R112
33E,1%,0603
UC_RDE_DO_RS485_1
R120
33E,1%,0603
UC_SI_DO_FM
FM_SO_DO_UC
UC_SCK_DO_FM
UC_CS_DO_FM
B6
742792037
C80
1uF,16V,0603
C79
0.1uF,16V,0603
SWD_RST_B
I2C3_SCL
I2C3_SDA
UC_BQBOOT_DO_AFE
SC_FAIL
TEMP1_AO_UC
TEMP2_AO_UC
R132
DNP,33E,1%,0603
UC_DI_DO_RS485_2
RS485_2_RO_DO_UC
UC_SOCLED3_TA
UC_SOCLED2_TA
UC_SOCLED1_TA
PC9
R202
0E,0603
UC_PV_S_EN_DO_M
R114
10K,1%,0603
U26
AND GATE
SN74AHC1G08DBVR
EXT_INT_OPTO
CAN_Wakeup_UC
C134
0.1uF,16V,0603
R278
DNP,0E,1206
U19
DNP,VOM617A-4X001T
R130
10K,1%,0603
R126
DNP,330E,1%,0603
EXT_INT_DI_OPTO
R279
DNP,0E,1206
EXT_INT_RET
OSC2_IN
OSC2_OUT
Y2
32.768 kHz
AB38T-32.768KHZ
C82
12pF,25V,0603
C81
12pF,25V,0603
R73
33E,1%,0603
DRV_PS_EN_UC
FF_Reset
I_SENSE_UC
PV_S_AO_UC
RS_CAN_DI_UC
WDI
TEMP3_AO_UC
TEMP4_AO_UC
Speed_In_AO_UC
DISO_CAN_PS_EN_UC
BLE_EN_DI_UC
R271
DNP,0E,0603
J18
DNP,22-04-1041
R272
DNP,12K,1%,0603
5V
C8
DNP,10uF,16V,0805
R288
DNP,10K,1%,0603
D26
Green LED
R76
270E,1%,0603
PV_S_AO_UC
D30
DNP,SZMM3Z3V3T1G
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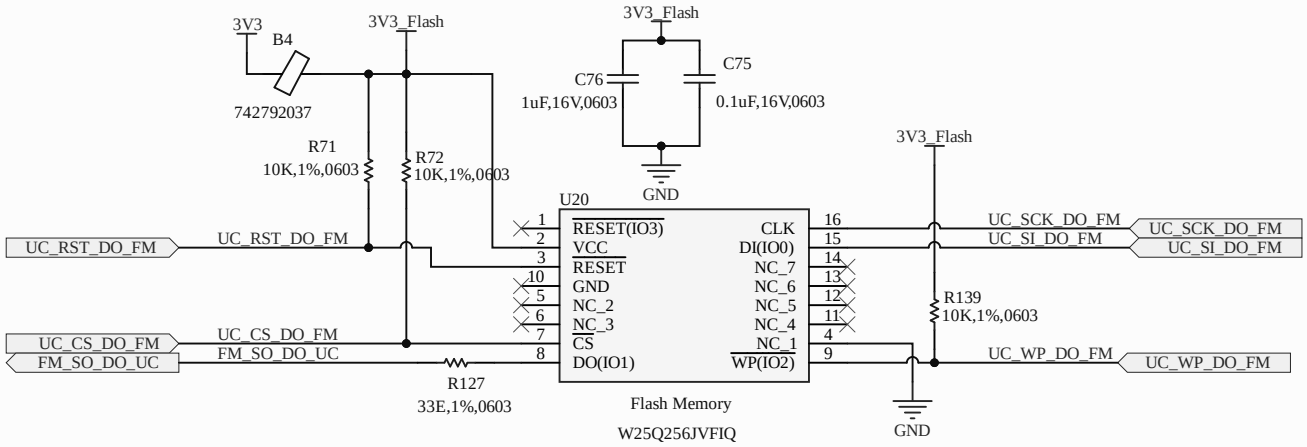
Document Number : 6
Size: A4
Title : EVB48V-V1 Full.PrjPcb
Revision
Issue
Date
Design Status
Drawn By
Approved By
1.2
04-10-2021
Under Development
Bharani Latha R
Devarajan S
Sheet Title : Host UC.SchDoc
Printed : 6 Sheet 14



Flash Part Number

Variant	
EV	ES
W25Q256JVFIQ	W25Q64JVSFIQ W25Q128JVFIQ

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Title : EVB48V-V1 Full.PrjPcb

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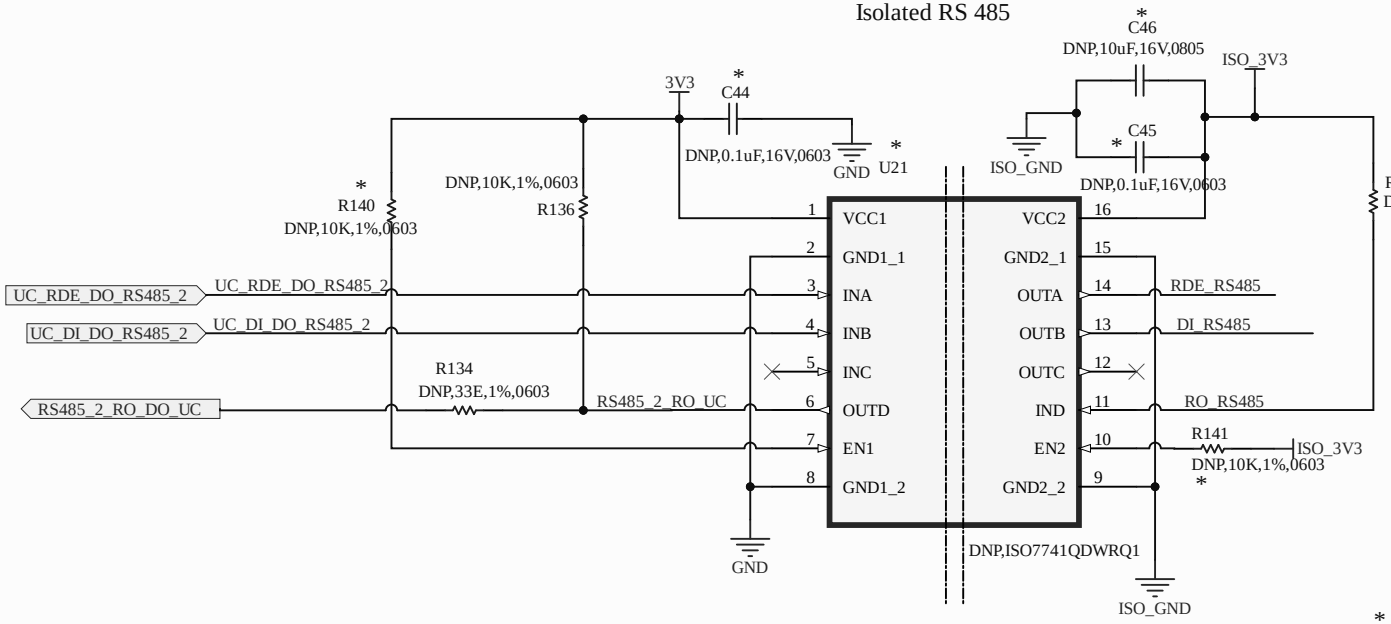
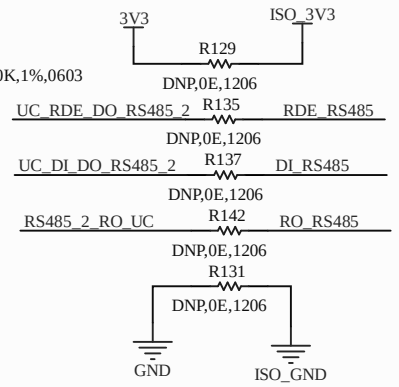
1.2		04-10-2021	Under Development	Bharani Latha R	Devarajan S

Sheet Title : Flash Memory.SchDoc Printed : Sheet 7 of 14

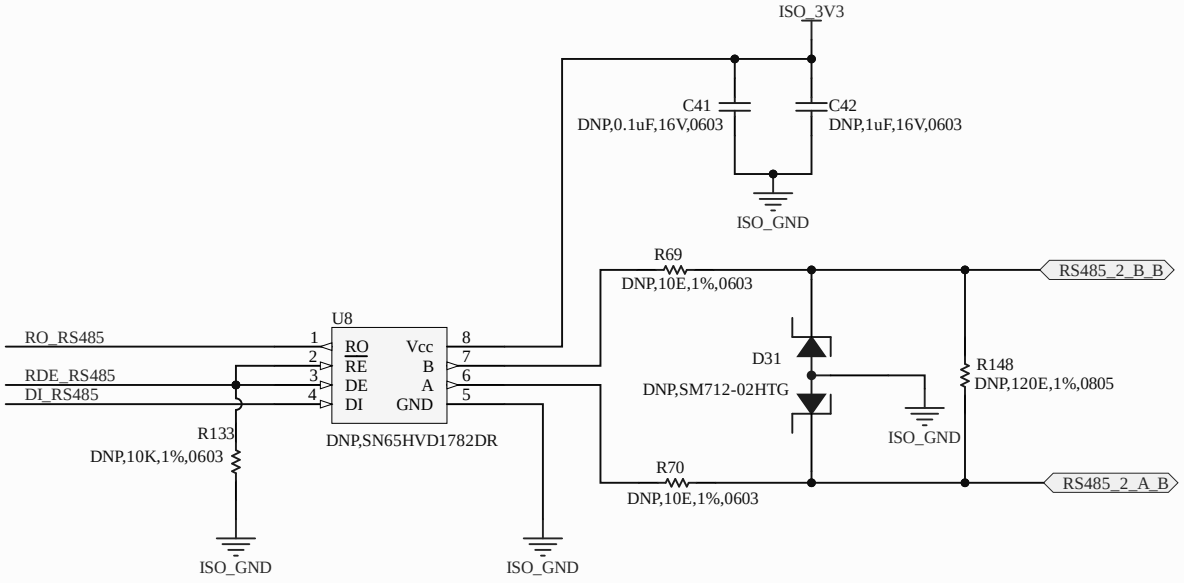
Isolated RS 485



Bypass option to unmount Isolated Rs 485



∗ To unmount these parts when using Bypass option



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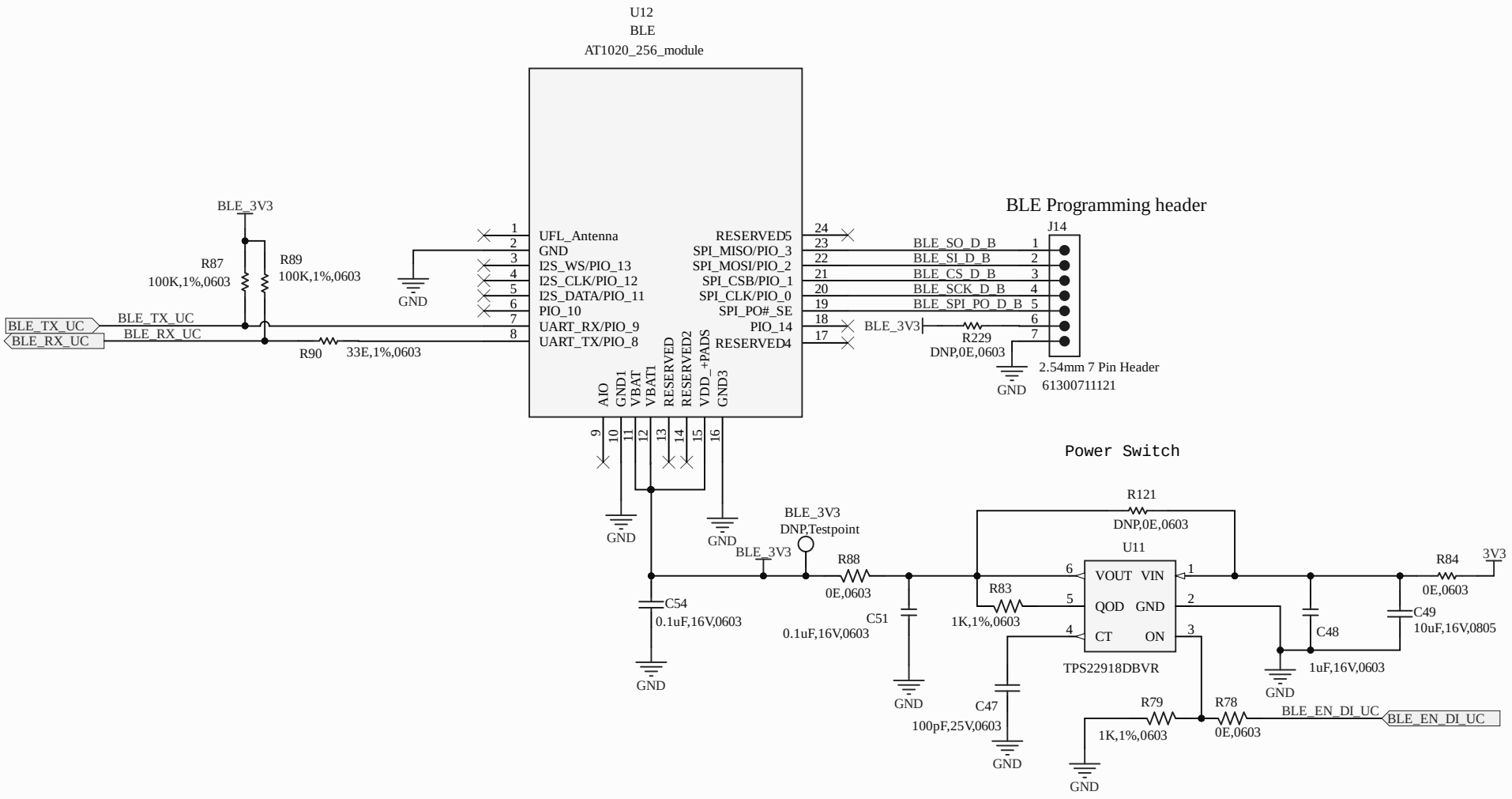
Sheet Title :			Isolated_RS485.SchDoc	Printed :	Sheet 8 of 14



Note: BLE Section to be mount for EV variant only

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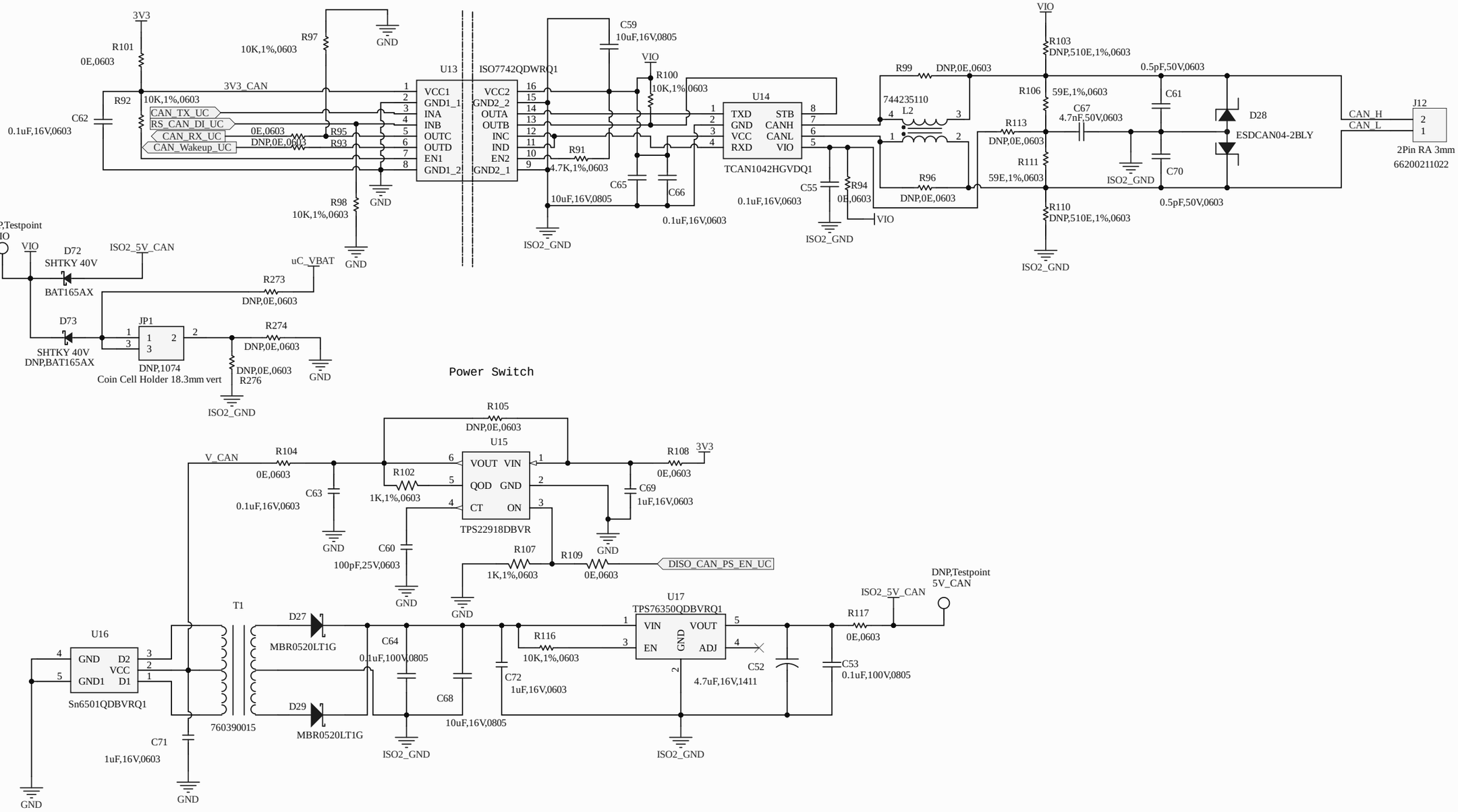
Sheet Title :		BLE.SchDoc	Printed :		Sheet 9 of 14



Note: CAN Section to be mount for EV variant only

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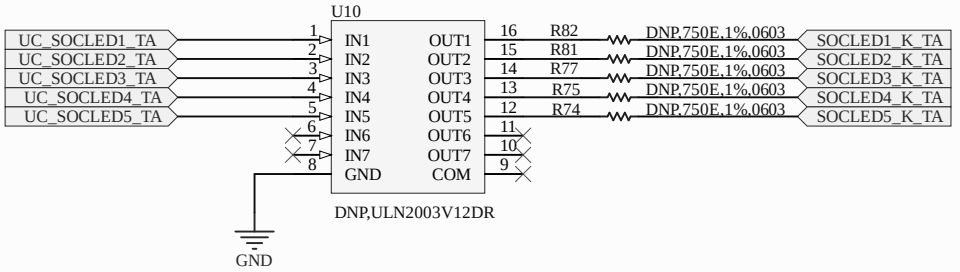
Revision	Issue	Date	Details	Drawn By	Approved By
1.2		04-10-2021	Under Development	Bharani Latha R	Devarajan S
Sheet Title :			Isolated_CAN.SchDoc	Printed :	Sheet 10 of 14

SOC LED Driver



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Document Number : 11 Size: A4

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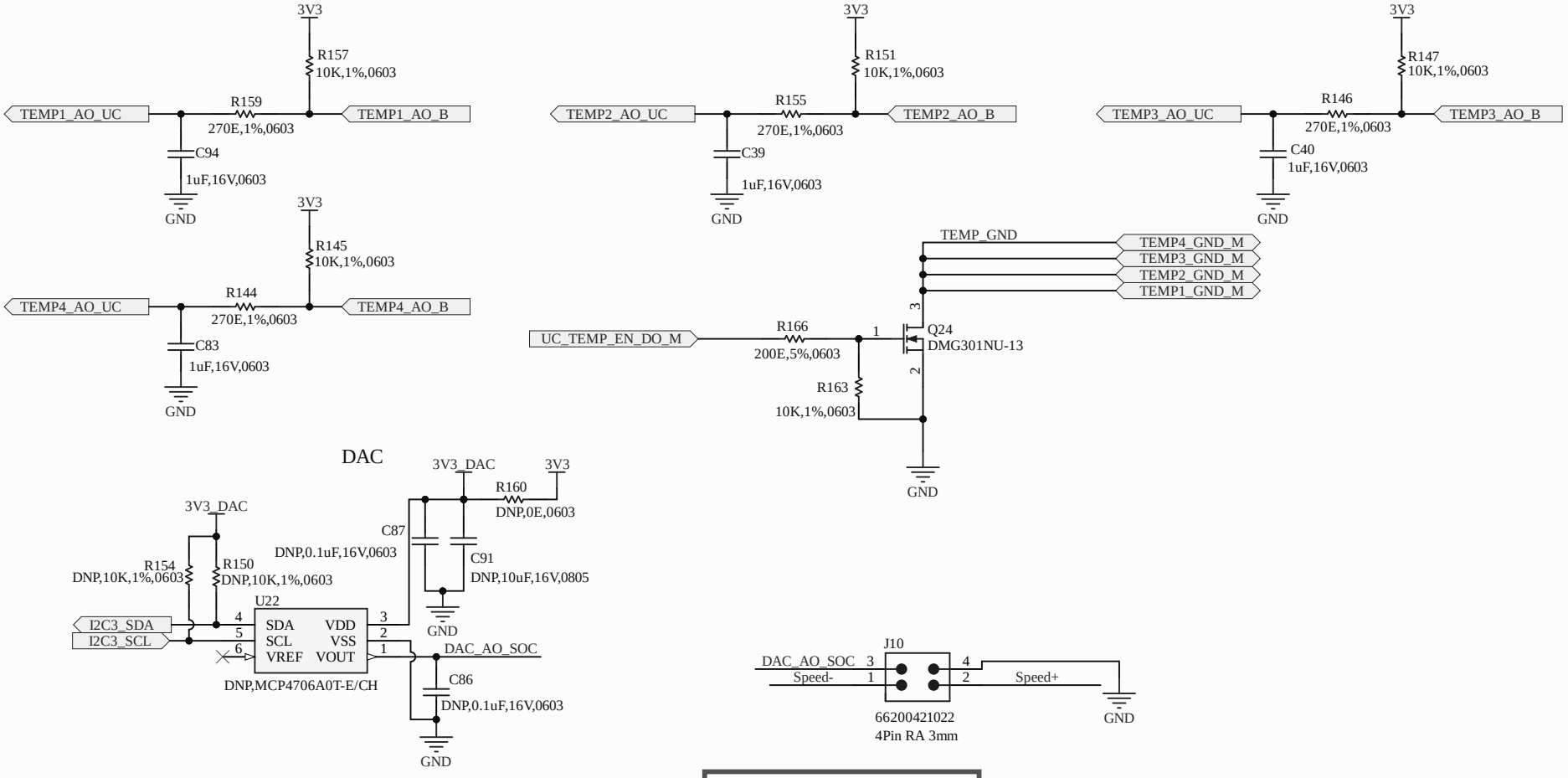
Sheet Title : SOC Led.SchDoc Printed : Sheet 11 of 14



Note:
Hall Sensor signal is +3.3V LVTTL or LVCMOS compliant

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Document Number : 12 Size: A4

Title : EVB48V-V1 Full.PrjPcb

Revision	Issue	Date	Details	Drawn By	Checked By
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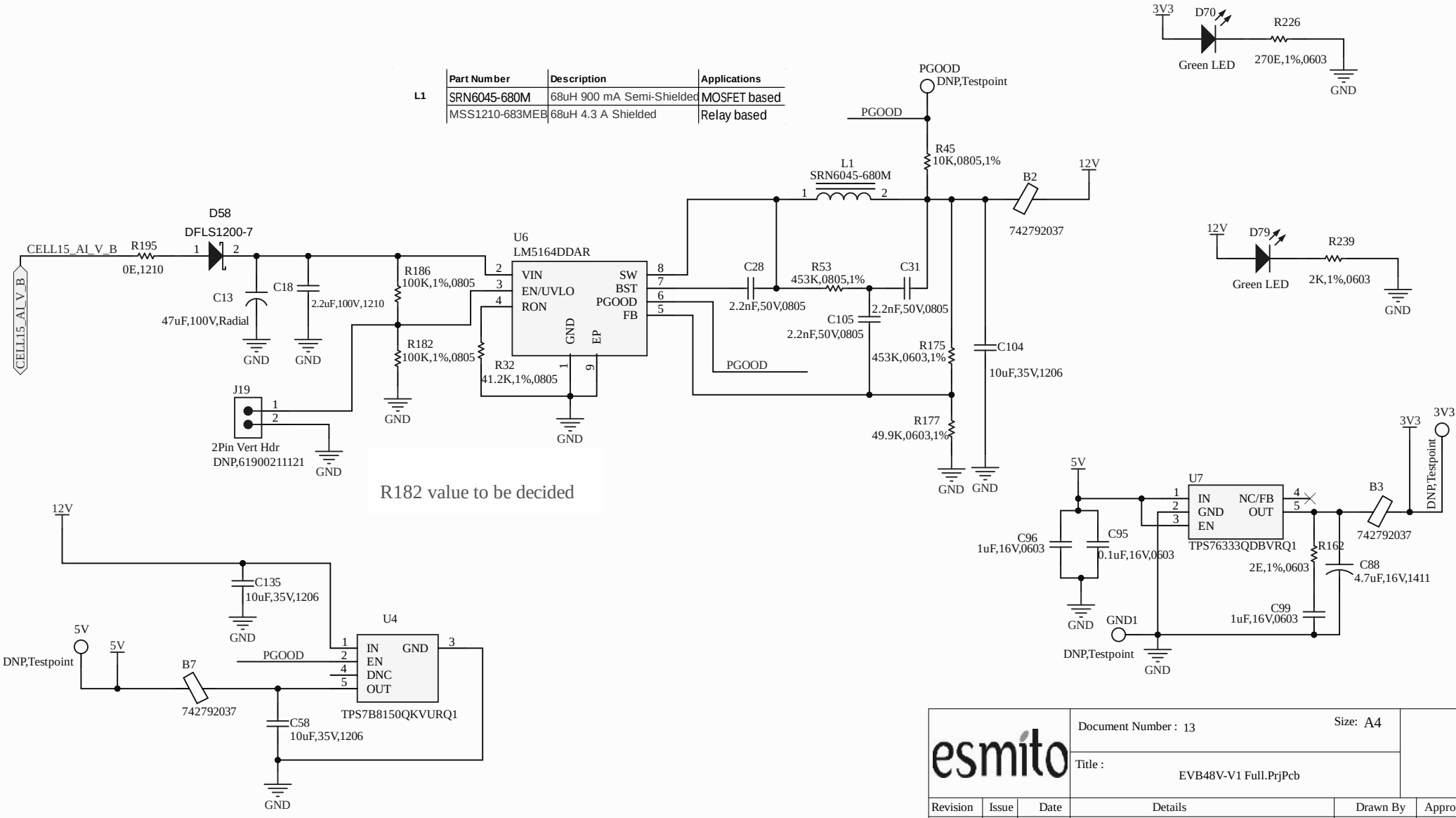
Sheet Title : Temp Sensor_DAC_Speed_Monitor.SchDoc Printed : Sheet 12 of 14



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Revision	Issue	Date	Details	Drawn By	Approved By
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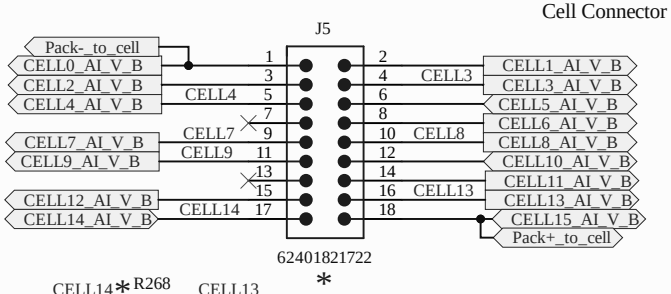
Sheet Title :	Power Supply.SchDoc	Printed :	Sheet 13 of 14

Cell Connector



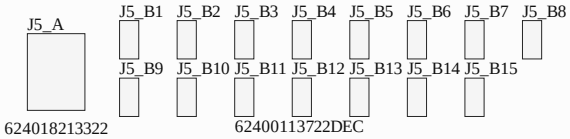
CELL14 * R268 CELL13
DNP,0E,0603

CELL9 * R269 CELL8
DNP,0E,0603

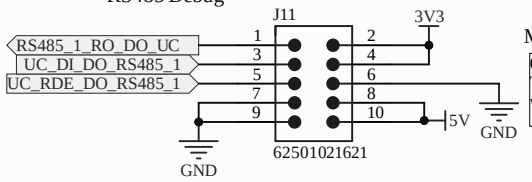
CELL8 * R280 CELL7
DNP,0E,0603

CELL4 * R281 CELL3
DNP,0E,0603

Mating Part & Crimp for Cell Connector, J5



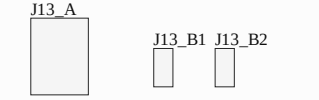
RS485 Debug



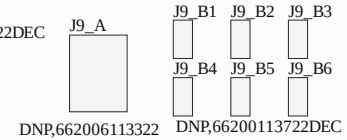
Mating Part for RS485 Debug, J11

62501023021
To use with external RS485 adapter with mating cable assembly

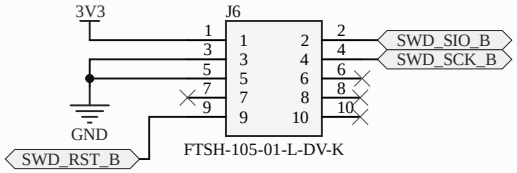
Mating Part & Crimp for Pre-charge conn.J13



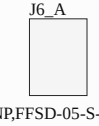
Mating Part & Crimp for SoC, J9



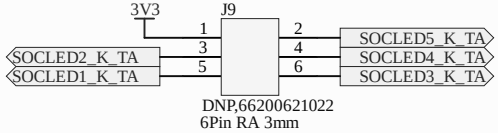
JTAG header



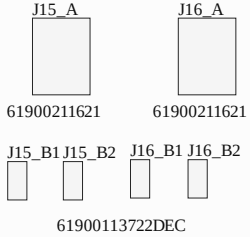
Mating Part for J6



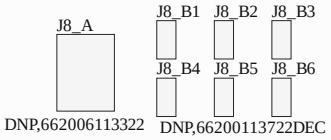
SOC LED Connector



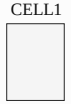
Mating Part & Crimp for Temp. sensor conn. J15,J16



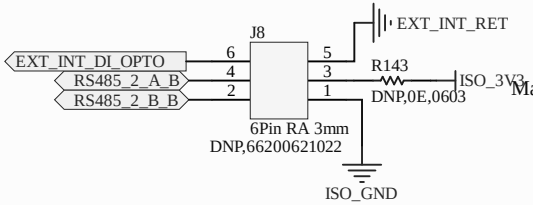
Mating Part & Crimp for RS485, J8



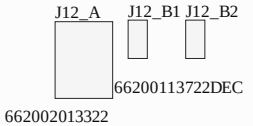
CELL for JP1



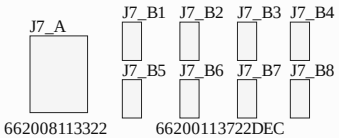
Isolated RS485 Connector



Mating Part & Crimp for CAN, J12

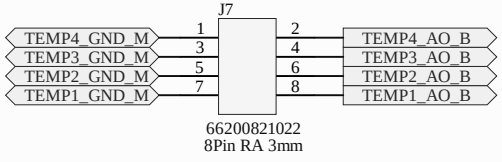


Mating Part & Crimp for J7

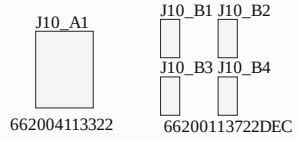


MOSFET HEATSINK

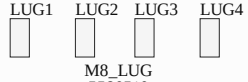
Temp. Measurement Connector

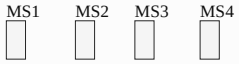


Mating Part & Crimp for SPEED, J10



LUG & Screw for Power Terminals J1,J2,J3 & J4





PCB1
PCB 4 Layers 1.6mm, 70microns
PCB 1.6mm

PCB2
PCB 4 Layers 2.5mm, 70microns
DNP,PCB 2.5mm

esmito

Document Number : 14
Size: A4
Title : EVB48V-V1 Full.PrjPcb

Revision	Issue	Date	Details	Drawn By	Checked By
1.2		04-10-2021	Under Development	Bharani Latha R	Devarajan S

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