Sample-Boost-Latch Based Offset Tolerant Sense Amplifier for Subthreshold SRAMs

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1. Motivation

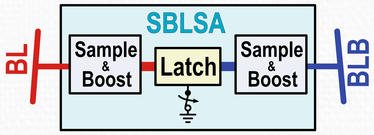
- Low-voltage, high-speed & reliable SRAMs in high demand for SoCs
- Sense Amplifier (SA) offset play a vital role in dictating SRAM energy
- For every 1 mV of Std_{OS} in SA, requires 10 mV of highly capacitive bitline discharge for 6σ SRAM read yield [Abu-Rahma, CICC 2011]

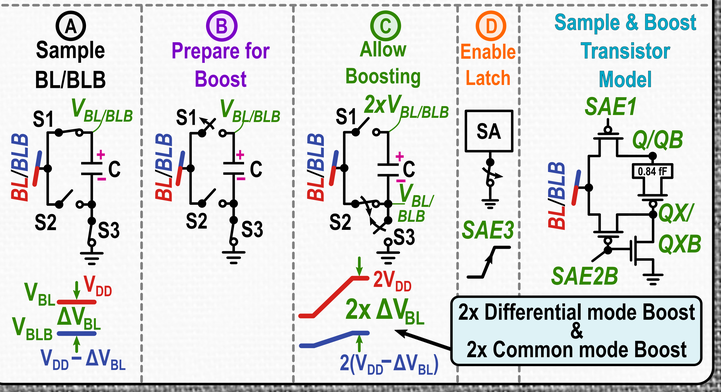
2. Problem Statement

- Improve both offset tolerance & reliable sub-threshold operation for low-voltage SRAM SAs across wider PVT range
- Targeted Applications: IoT devices, Bio-implantable SoCs, Battery operated sensory ICs

3. Sample-Boost-Latch (SBL) Concept

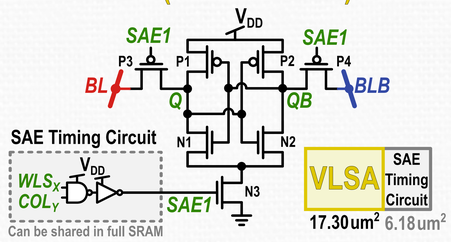
- Boosting on local, low capacitive nodes of the latching element
- Differential mode boosting for mismatch tolerance
- Common mode boosting for low-voltage operation



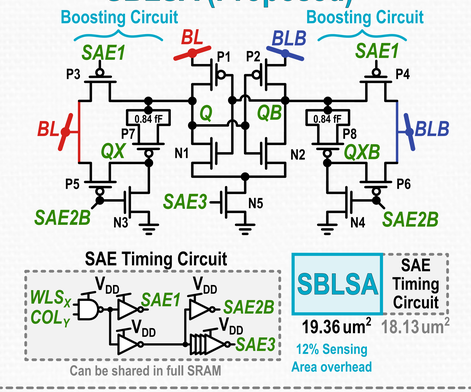


4. Implemented SAs on Chip

VLSA (Conventional)

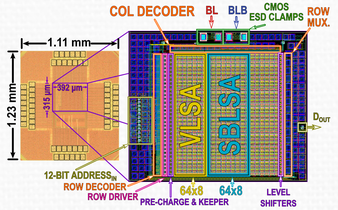


SBLSA (Proposed)

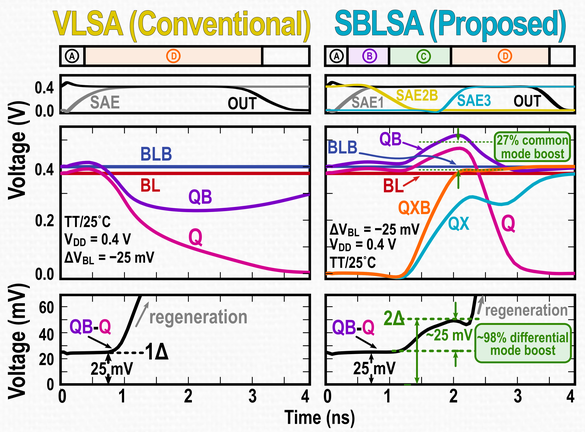


Die Photo

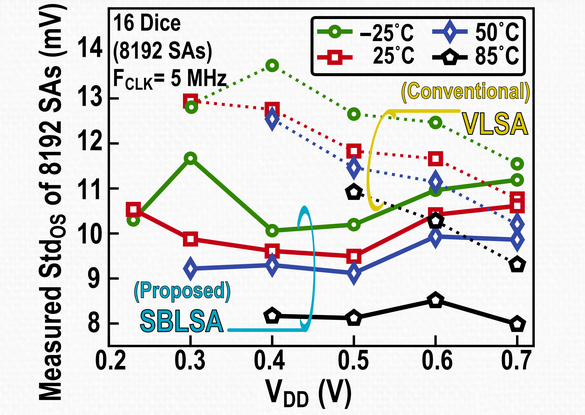
65nm-GP CMOS



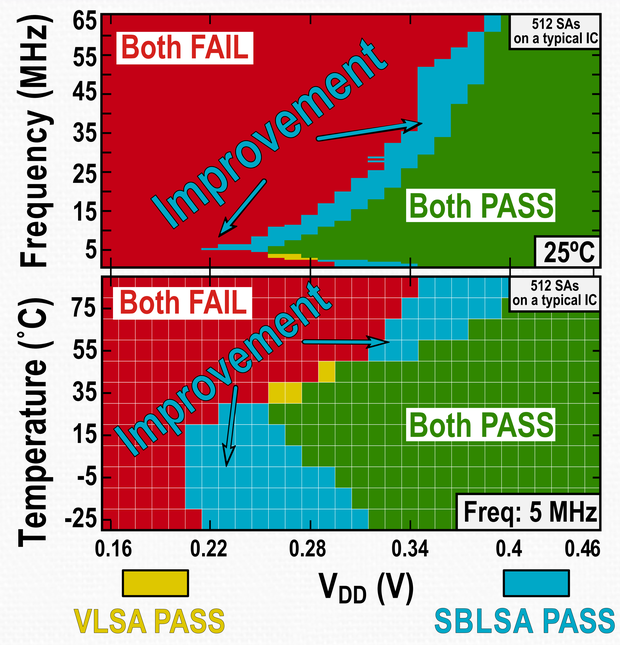
5. Transient Simulations (PLS)



6. Measured Offset Statistics



7. Measured Shmoo Plots



8. Results in 65nm-GP CMOS

- Standard deviation of offset (Std_{OS}) reduced by 23.3%
  - measured across 16 ICs (total 8192 SAs of each)
- Sensing Delay reduced by 38.5%
- Minimum Supply required ($V_{DD\text{-}min}$): 230 mV at 25 ºC
- Minimum Supply required ($V_{DD\text{-}min}$): 350 mV for -25 ºC to 85 ºC