# Dhruv Patel

dhruv.patel@isl.utoronto.ca | webpage | LinkedIn | Google Scholar

## EDUCATION

**UNIVERSITY OF TORONTO**
Master of Applied Science - Electrical Engineering
Sept 2016 - Present | Toronto, ON
Supervisor: Prof. Tony Chan Carusone

- Research Area: CMOS Optical Receiver

**UNIVERSITY OF WATERLOO**
Bachelor of Applied Science Honours Electrical Engineering, Co-op Program - With Distinction
Sept 2011 - April 2016 | Waterloo, ON

- Final Year Project: PowerSmart - Enabling IoT with AC power-line communication

## PUBLICATIONS

**REFEREED JOURNAL PAPERS:**

[J1] **D. Patel** and M. Sachdev, "0.23-V Sample-Boost-Latch-Based Offset Tolerant Sense Amplifier," in **IEEE Solid-State Circuits Letters**, vol. 1, no. 1, pp. 6-9, Jan. 2018.

**REFEREED CONFERENCE PAPERS:**

[C1] **D. Patel**, D. Wright and M. Sachdev, "Sense amplifier offset characterisation and test implications for low-voltage SRAMs in 65 nm," in 2018 IEEE 23rd **European Test Symposium (ETS)**, Bremen, 2018, pp. 1-6.

**REFEREED POSTERS & PRESENTATIONS:**

[P1] **Dhruv Patel** and Manoj Sachdev, "Sample-Boost-Latch Based Offset Tolerant Sense Amplifier for Sub-threshold SRAMs" **IEEE 2018 International Solid-State Circuits Conference (ISSCC) Student Research Preview**.

## RESEARCH EXPERIENCE

**CMOS OPTICAL RECEIVER FRONT-END** | MASc. Graduate Research Assistantship
Sept 2016 - Present | Toronto, ON
Supervisors: Prof. Tony Chan Carusone

- Designing Optical Receiver Front-end for PAM-4 fiber-optic communications
- Second order system optimization with Gain-BW-noise trade-offs and peak-distortion analysis

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**SRAM CIRCUITS - VLSI** | BASc. Undergraduate Research Assistantship
Sept 2015 - Aug 2016 | Waterloo, ON
Supervisors: Prof. Manoj Sachdev, Dr. Adam Neale, Dr. Derek Wright

- Taped-out low-voltage and offset reducing Sense-amplifiers in 65 nm
- Schematics, layout and simulations of 65 nm SRAM cells and Sense Amplifiers in Cadence Virtuoso
- Characterizing Sense Amplifier ICs in CMOS design and reliability laboratory

- 4-layer PCB Design for Sense Amplifier IC for characterization purposes
- Took graduate level CMOS digital design course; Project: 16-bit 1GHz adder design in cadence

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**POWER-LINE TRANSCEIVER DESIGN** | BASc. Undergraduate Research Assistantship
8 months | Jan 2015 - Aug 2015 | Waterloo, ON
Supervisors: Prof. Vincent Gaudet

- Assisted in automotive DC power-line communication (PLC) research
- Schematics and PCB designs of transmitter and receiver analog-front-end (AFE) boards
- Prototyped and characterized AFE transceivers in microelectronic laboratory
- Performed substantial circuit simulations and component selections for the AFE circuitry

## WORK EXPERIENCE

**APPLE INC.** | Sensing Systems Hardware Intern
5 months | Aug 2014 - Dec 2014 | Cupertino, CA

- Optical Characterizations of CMOS SPAD arrays and VCSELs in optoelectronics laboratory
- Executed extensive statistical analysis of sensor test data for modelling purposes with python
- Architected Robotic control software for automating sensor characterizations with python and Java
- Involved in System level and PCB level designs of Optical sensor prototypes

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**ARISTA NETWORKS** | Hardware Design Engineering Intern
4 months | Jan 2014 - April 2014 | Santa Clara, CA

- Contributed in PCB designs for 40Gb/s Network Switches
- Designed and simulated matched 156 MHz clock fanout interfaces with HSpice and ADS
- Simulated power planes and optimized component placements for efficient power delivery
- Performed spectrum analysis for selecting Crystal Oscillators with lowest EMI
- Eye characterizations and tuning for Jitter and Power reduction
- Developed JTAG boundary scan test on Network Switches
- Characterized Airflow and Pressure inside the Network Switch chassis for better fan selection

**BLACKBERRY** | Hardware Verification Engineering Intern
4 months | May 2013 - Aug 2013 | Waterloo, ON

- Verified high-speed interfaces across baseband and application processors in GBit/sec class
- Analyzed signal eye diagrams and jitter measurements for signal integrity verification purposes
- Automated oscilloscopes, temperature chambers and frequency counters for chip testing in python
- Performed current drive optimization and noise analysis on baseband ICs
- Developed software in C for throughput measurements on USB and µSD interfaces
- Performed USB 2.0 electrical compliance tests according to USB protocol specifications
- Tested functionalities of Blackberry handheld devices using NI LabVIEW

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**CHRISTIE DIGITAL** | Electrical Engineering - Intern
4 months | Sept 2012 - Dec 2012, Kitchener, ON

- Contributed to flight-simulator Projector's PCB designs
- Lead projector's harness designs: component selections, prototype building and finalizing designs
- Involved in Electro-Optical/Mechanical algorithm development and validation
- Performed net list checks, signal integrity and brought-up PCBs according to test plans
- Optimized Light Sensor sampling time by modifying existing amplification circuitry

**TDA INC.** | Programmer - Intern
4 months | Jan 2012 - April 2012, Burlington, ON

- Developed scantron scanning software from scratch in C# and VB.net
- Designed Call Information System for VOIP to search call records from the database in VB.Net

## VOLUNTEERING ACTIVITIES & SOCIETY MEMBERSHIPS

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| 2018 | Engineer in Residence (EIR) volunteer at Briarcrest Junior School |
| 2018 | IEEE International Solid-State Circuit Conference (ISSCC) Volunteering Team |
| 2013-2014 | UofW Application Specific Integrated Circuit (ASIC) group |
| 2013-2014 | UofW Badminton Club |
| 2012-Present | IEEE Student Membership:<br>(2016-Present): SSCS, CAS, Photonics, Nanotechnology, Sensors |

## SCHOLARSHIPS & AWARDS

2018 Edward S. Rogers Sr. Graduate Scholarships (UofT: MASc.)
2017 Queen Elizabeth Graduate Scholarship in Science and Technology (UofT: MASc.)
2016 NSERC Undergraduate Student Research Award (SRAM: VLSI)
2016 Distinguished Final Year Capstone Design Project Award (PowerSmart)
2016 Undergraduate Research Assistantship Award (SRAM: VLSI)
2015 NSERC Undergraduate Student Research Award (SRAM: VLSI)
2015 Undergraduate Research Assistantship Award (Power-Line Tx/Rx Design) x2
2011 University of Waterloo Merit Scholarship
2011 Queen Elizabeth II Aiming for the Top Scholarship

## COMPLETED MAJOR COURSEWORK

**UNDERGRADUATE**

Integrated Digital Circuits
Electronic Devices
EM Fields and Waves
Analog Control Systems
Embedded Microprocessor Systems
Integrated Analog Electronics
Geometric and Physical Optics
Microelectronic Circuits I and II
Analog and Digital Communication
RF and Microwave Circuits
Power Electronic Converters
Probability Theory and Random Access
Photonics Devices and Systems

**GRADUATE**

Digital Integrated Circuits
VLSI Design Methodology
Integrated Circuits for Wireless Communications
Analog Circuit Design I
High Frequency Integrated Circuits
Integrated Circuits for Digital Communications

## TEACHING ASSISTANTSHIP

ECE 334-Digital Electronics: Lab sessions for 3rd Yr. undergrad students (2016, 2017)
ECE 231-Introductory Electronics: Lab sessions for 2nd Yr. undergrad students (2018)

## EXPERTISE

**HARDWARE TOOLS**

- Electronics Instruments: High-end Oscilloscopes, Spectrum Analyzers, VNA, Current Probes, Power Supplies, Pattern Generators, Frequency Counters, Logic Analyzers
- Optical Instruments: Spectrometers, Solar simulators, Lasers and precision stages/apertures
- Communication Protocols: I2C, USB, SPI, JTAG, GPIB
- Solid PCB design and soldering skills

**SOFTWARE TOOLS**

- EE tools: Cadence Virtuoso (Schematics/Layout), Cadence Allegro/Orcad, Ltspice, HSpice, Advanced Design System, Labview, Altium, Eagle, Qurtus, Hyperlynx Power-Integrity
- Programming: Java, C, C#, C++, Matlab, Python, VHDL, Verilog, Assembly, .NET, Html, CSS
- Publishing Presentation tools: Latex, MS office suit