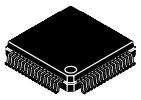


MC33771B

Battery cell controller IC

Rev. 3.0 — 6 December 2017

Data sheet: product preview
COMPANY CONFIDENTIAL

1 General description

The 33771 is a SMARTMOS lithium-ion battery cell controller IC designed for automotive applications, such as hybrid electric (HEV) and electric vehicles (EV) along with industrial applications, such as energy storage systems (ESS) and uninterruptible power supply (UPS) systems.

The device performs ADC conversions of the differential cell voltages and current, as well as battery coulomb counting and battery temperature measurements. The information is digitally transmitted through the SPI or transformer isolation to a microcontroller for processing.

2 Features

- 9.6 V ≤ V_{PWR} ≤ 61.6 V operation, 75 V transient
- 7 to 14 cells management
- Isolated 2.0 Mbps differential communication or 4.0 Mbps SPI
- Addressable on initialization
- 0.8 mV maximum total voltage measurement error
- Synchronized cell voltage/current measurement with coulomb count
- Total stack voltage measurement
- Seven GPIO/temperature sensor inputs
- 5.0 V at 5.0 mA reference supply output
- Automatic over/undervoltage and temperature detection routable to fault pin
- Integrated sleep mode over/undervoltage and temperature monitoring
- Onboard 300 mA passive cell balancing with diagnostics
- Hot plug capable
- Detection of internal and external faults, as open lines, shorts, and leakages
- Designed to support ISO 26262, up to ASIL D safety capability
- Fully compatible with the MC33772 for a maximum of six cells
- Qualified in compliance with AECQ-100

3 Simplified application diagram

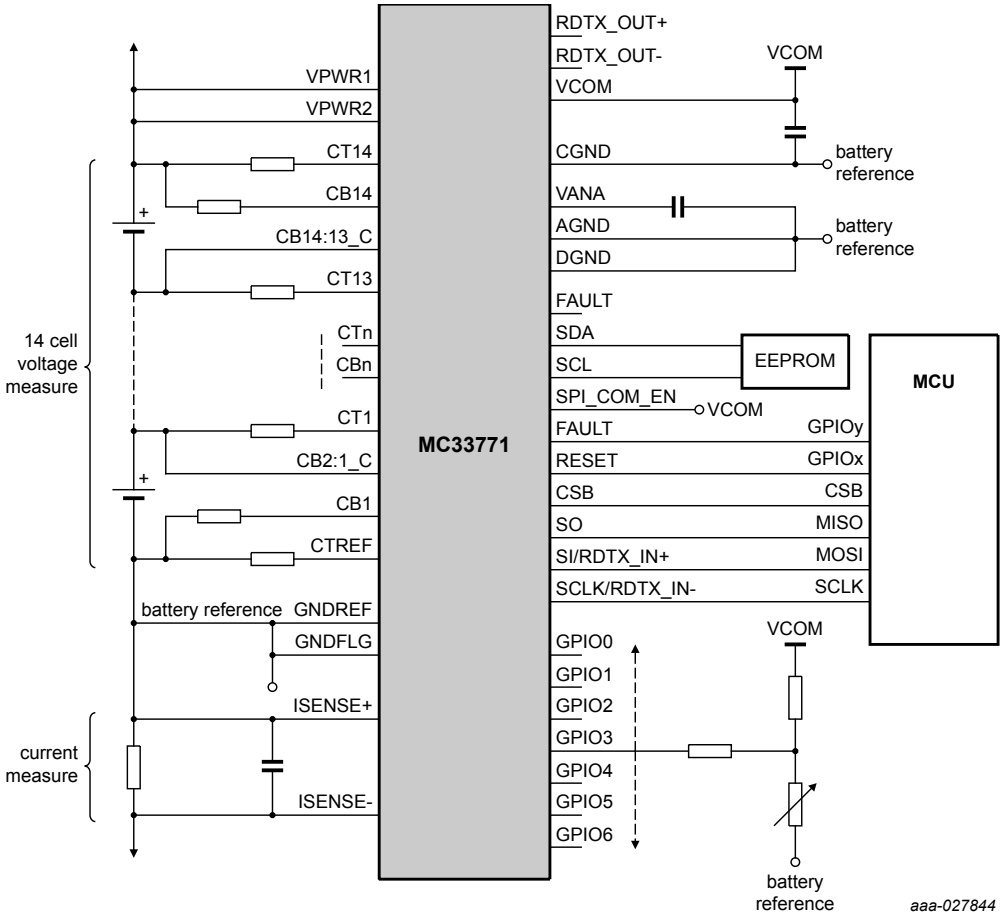


Figure 1. Simplified application diagram, SPI use case

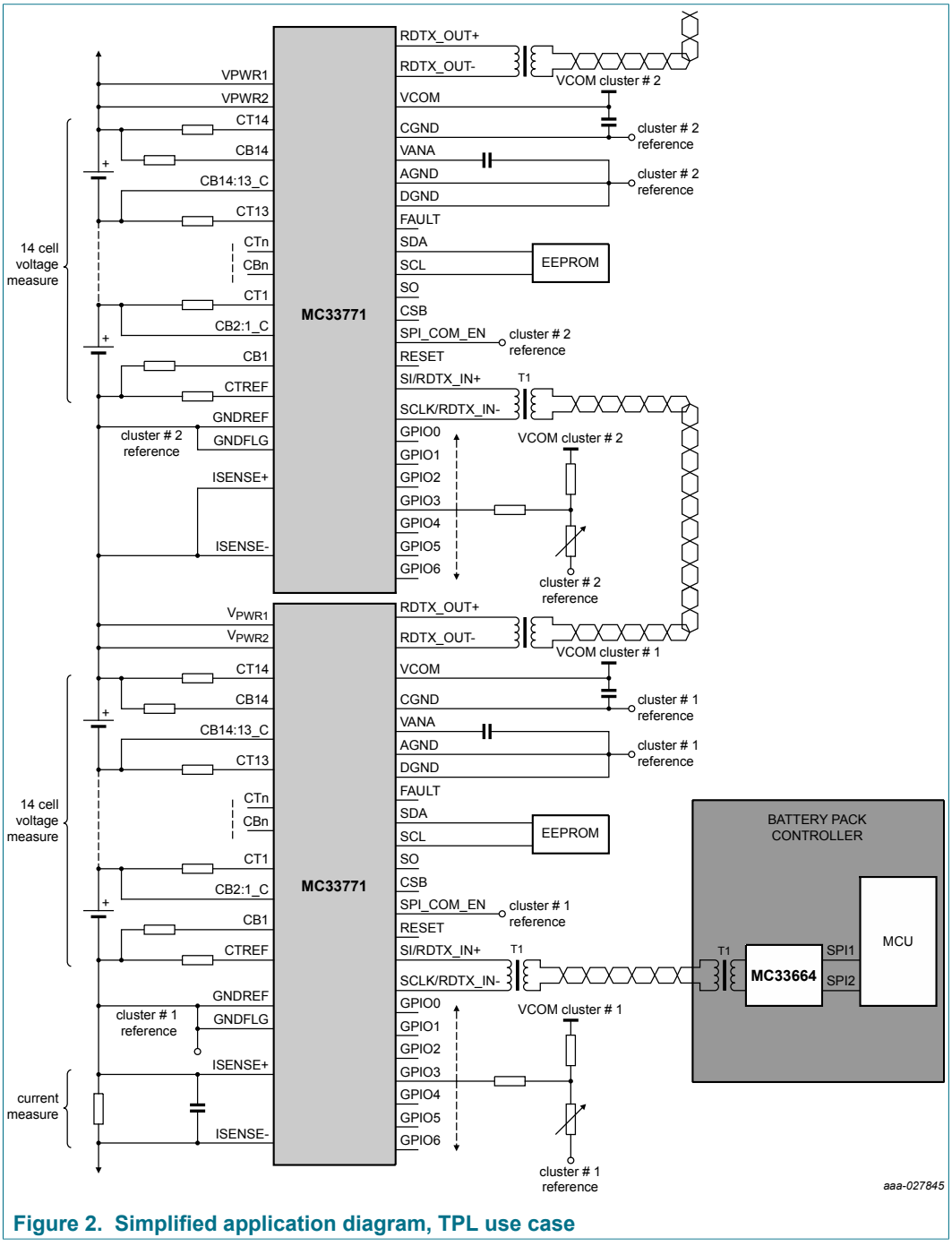


Figure 2. Simplified application diagram, TPL use case

4 Applications

- Automotive: 48 V and high-voltage battery packs
- E-bikes, e-scooters
- Energy storage systems
- Uninterruptible power supply (UPS)

5 Ordering information

5.1 Part numbers definition

PC33771B x y z AE/R2

Table 1. Part number breakdown

Code	Option	Description
	PC	Prototype
	33	Auto
	771	Series/product family
	B	Silicon version
x	SPI	x = S (SPI communication type)
	TPL	x = T (TPL communication type)
y	A	y = A (Advanced)
	B	y = B (Basic)
	P	y = P (Premium)
z	1	z = 1 (7 to 14 channels)
	2	z = 2 (7 to 8 channels)
	AE	Package suffix
	R2	Tape and reel indicator

5.2 Part numbers list

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com.

Table 2. Advanced orderable part table

Temperature range is −40 to 105 °C
Package type is 64-pin LQFP-EP

Orderable part	# of channels	OV/UV	Precision GPIO as temperature channels and OT/UT	Current channel or coulomb count
SPI communication protocol				
PC33771BSA1AE	7 to 14	Yes	Yes	No
PC33771BSA2AE	7 to 8	Yes	Yes	No
TPL differential communication protocol				
PC33771BTA1AE	7 to 14	Yes	Yes	No
PC33771BTA2AE	7 to 8	Yes	Yes	No

Table 3. Basic orderable part table

Temperature range is −40 to 105 °C
Package type is 64-pin LQFP-EP

Orderable part	# of channels	OV/UV	Precision GPIO as temperature channels and OT/UT	Current channel or coulomb count
SPI communication protocol				
PC33771BSB1AE	7 to 14	Yes	No	No
PC33771BSB2AE	7 to 8	Yes	No	No
TPL differential communication protocol				
PC33771BTB1AE	7 to 14	Yes	No	No
PC33771BTB2AE	7 to 8	Yes	No	No

Table 4. Premium orderable part table

Temperature range is −40 to 105 °C
Package type is 64-pin LQFP-EP

Orderable part	# of channels	OV/UV	Precision GPIO as temperature channels and OT/UT	Current channel or coulomb count
SPI communication protocol				
PC33771BSP1AE	7 to 14	Yes	Yes	Yes
PC33771BSP2AE	7 to 8	Yes	Yes	Yes
TPL differential communication protocol				
PC33771BTP1AE	7 to 14	Yes	Yes	Yes
PC33771BTP2AE	7 to 8	Yes	Yes	Yes

6 Internal block diagram

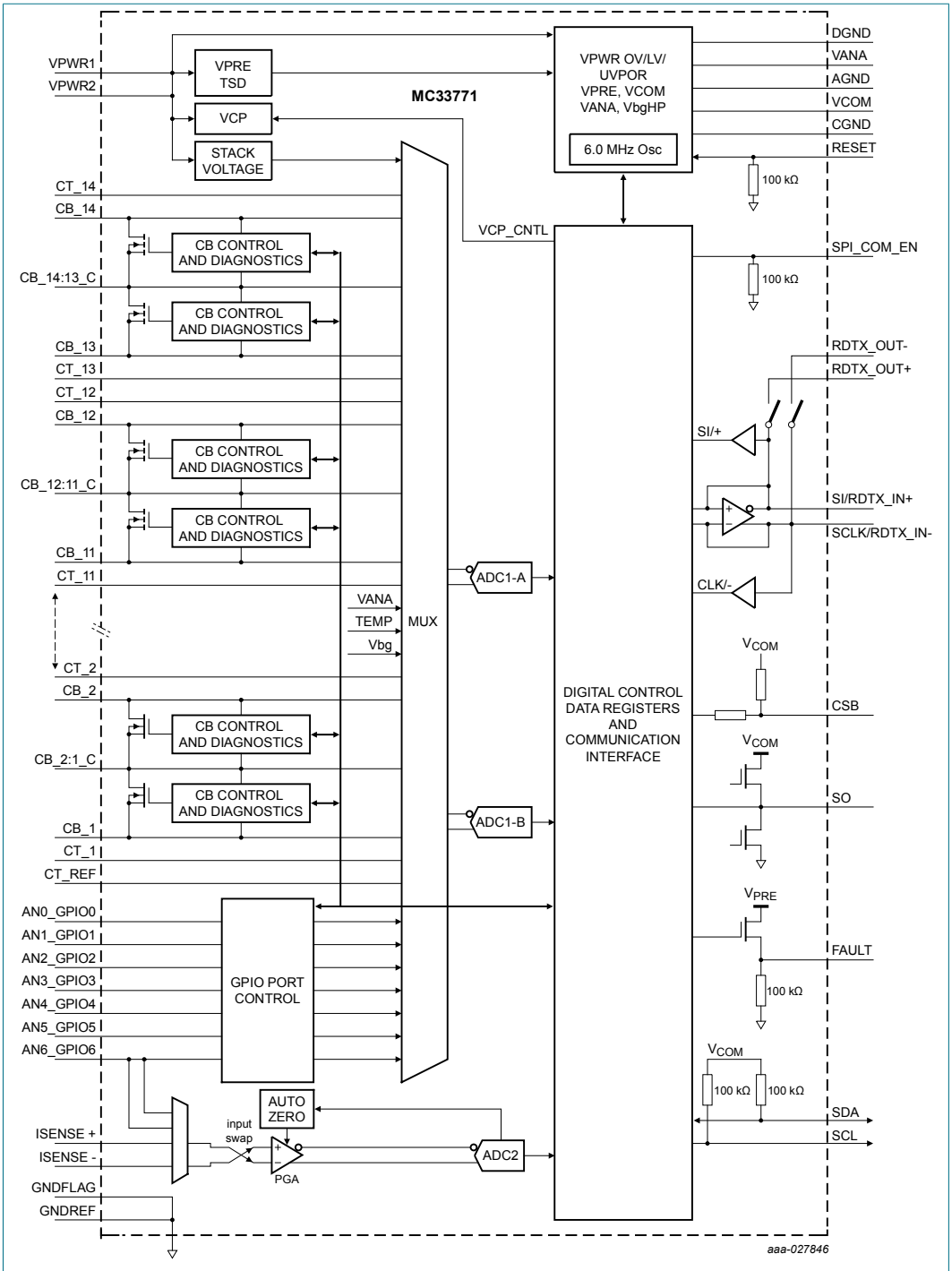


Figure 3. Simplified internal block diagram

7 Pinning information

7.1 Pinout diagram

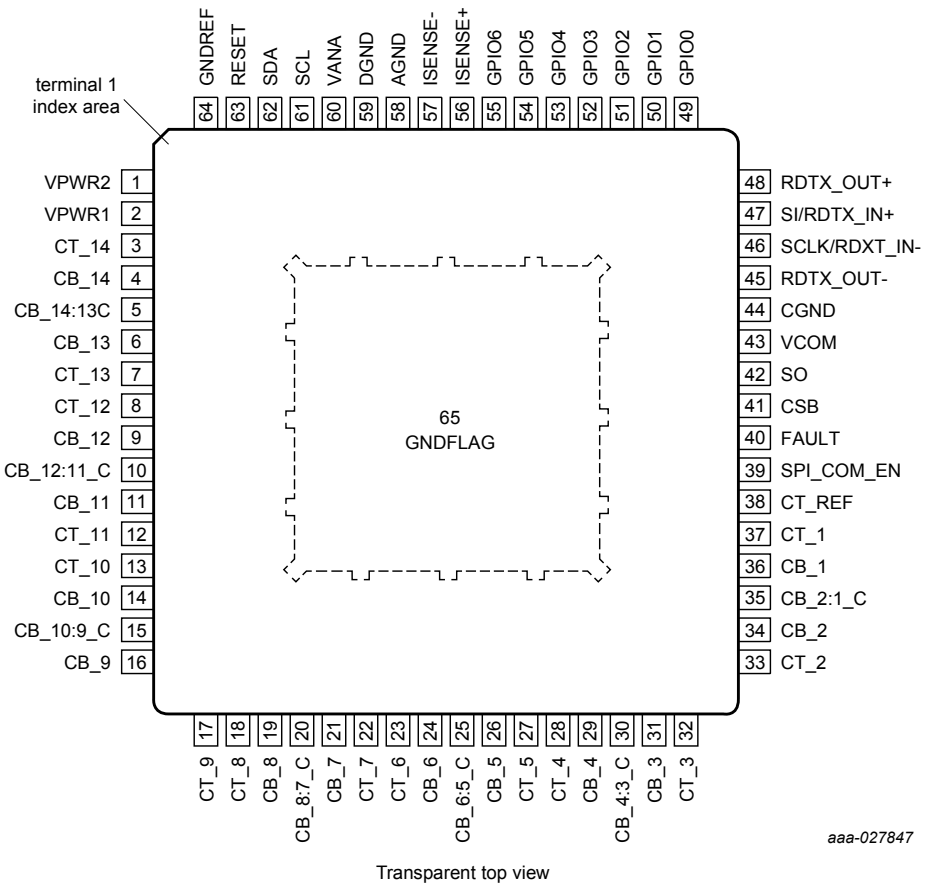


Figure 4. Pinout diagram

7.2 Pin definitions

For a detailed description of each pin, see Section 9 "Functional description".

Table 5. Pin definitions

Pin number	Pin name	Pin function	Definition
1	VPWR2	Input	Power input to the 33771
2	VPWR1	Input	Power input to the 33771
3	CT_14	Input	Cell pin 14 input. Terminate to LPF resistor.
4	CB_14	Output	Cell balance driver. Terminate to cell 14 cell balance load resistor.
5	CB_14:13_C	Output	Cell balance 14:13 common. Terminate to cell 14 and 13 common pin.
6	CB_13	Output	Cell balance driver. Terminate to cell 13 cell balance load resistor.

Pin number	Pin name	Pin function	Definition
7	CT_13	Input	Cell pin 13 input. Terminate to LPF resistor.
8	CT_12	Input	Cell pin 12 input. Terminate to LPF resistor.
9	CB_12	Output	Cell balance driver. Terminate to cell 12 cell balance load resistor.
10	CB_12:11_C	Output	Cell balance 12:11 common. Terminate to cell 12 and 11 common pin.
11	CB_11	Output	Cell balance driver. Terminate to cell 11 cell balance load resistor.
12	CT_11	Input	Cell pin 11 input. Terminate to LPF resistor.
13	CT_10	Input	Cell pin 10 input. Terminate to LPF resistor.
14	CB_10	Output	Cell balance driver. Terminate to cell 10 cell balance load resistor.
15	CB_10:9_C	Output	Cell balance 10:9 common. Terminate to cell 10 and 9 common pin.
16	CB_9	Output	Cell balance driver. Terminate to cell 9 cell balance load resistor.
17	CT_9	Input	Cell pin 9 input. Terminate to LPF resistor.
18	CT_8	Input	Cell pin 8 input. Terminate to LPF resistor.
19	CB_8	Output	Cell balance driver. Terminate to cell 8 cell balance load resistor.
20	CB_8:7_C	Output	Cell balance 8:7 common. Terminate to cell 8 and 7 common pin.
21	CB_7	Output	Cell balance driver. Terminate to cell 7 cell balance load resistor.
22	CT_7	Input	Cell pin 7 input. Terminate to LPF resistor.
23	CT_6	Input	Cell pin 6 input. Terminate to LPF resistor.
24	CB_6	Output	Cell balance driver. Terminate to cell 6 cell balance load resistor.
25	CB_6:5_C	Output	Cell balance 6:5 common. Terminate to cell 6 and 5 common pin.
26	CB_5	Output	Cell balance driver. Terminate to cell 5 cell balance load resistor.
27	CT_5	Input	Cell pin 5 input. Terminate to LPF resistor.
28	CT_4	Input	Cell pin 4 input. Terminate to LPF resistor.
29	CB_4	Output	Cell balance driver. Terminate to cell 4 cell balance load resistor.
30	CB_4:3_C	Output	Cell balance 4:3 common. Terminate to cell 4 and 3 common pin.
31	CB_3	Output	Cell balance driver. Terminate to cell 3 cell balance load resistor.
32	CT_3	Input	Cell pin 3 input. Terminate to LPF resistor.
33	CT_2	Input	Cell pin 2 input. Terminate to LPF resistor.

Pin number	Pin name	Pin function	Definition
34	CB_2	Output	Cell balance driver. Terminate to cell 2 cell balance load resistor.
35	CB_2:1_C	Output	Cell Balance 2:1 common. Terminate to cell 2 and 1 common pin.
36	CB_1	Output	Cell balance driver. Terminate to cell 1 cell balance load resistor.
37	CT_1	Input	Cell pin 1 input. Terminate to LPF resistor.
38	CT_REF	Input	Cell pin REF input. Terminate to LPF resistor.
39	SPI_COM_EN	Input	SPI communication enable, pin must be high for the SPI to be active
40	FAULT	Output	Fault output dependent on user defined internal or external faults. If not used, it must be left open.
41	CSB	Input	SPI chip select
42	SO	Output	SPI serial output
43	VCOM	Output	Communication regulator output. Decouple with 2.2 µF ceramic.
44	CGND	Ground	Communication decoupling ground. Terminate to GNDREF
45	RDTX_OUT-	I/O	Receive/transmit output negative
46	SCLK/RDTX_IN-	I/O	SPI clock or receive/transmit input negative
47	SI/RDTX_IN+	I/O	SPI serial input or receiver/transmit input positive
48	RDTX_OUT+	I/O	Receive/transmit output positive
49	GPIO0	I/O	General purpose analog input or GPIO or wake-up or fault daisy chain
50	GPIO1	I/O	General purpose analog input or GPIO
51	GPIO2	I/O	General purpose analog input or GPIO or conversion trigger
52	GPIO3	I/O	General purpose analog input or GPIO
53	GPIO4	I/O	General purpose analog input or GPIO
54	GPIO5	I/O	General purpose analog input or GPIO
55	GPIO6	I/O	General purpose analog input or GPIO
56	ISENSE+	Input	Current measurement input+
57	ISENSE-	Input	Current measurement input−
58	AGND	Ground	Analog ground, terminate to GNDREF
59	DGND	Ground	Digital ground, terminate to GNDREF
60	VANA	Output	Precision ADC analog supply. Decouple with ceramic 47 nF ceramic capacitor to AGND.
61	SCL	I/O	I^2C clock
62	SDA	I/O	I^2C data

Pin number	Pin name	Pin function	Definition
63	RESET	Input	RESET is an active high input. RESET has an internal pull down. If not used, it can be tied to GND.
64	GNDREF	Ground	Ground reference for device. Terminate to reference of battery cluster.
65	GNDFLAG	Ground	Device flag. Terminate to lowest potential of battery cluster.

8 General product characteristics

8.1 Ratings and operating requirements relationship

The operating voltage range pertains to the VPWR pins referenced to the AGND pins.

Table 6. Ratings vs. operating requirements

Fatal range **Permanent failure may occur** V_{PWR} < −0.3 V	**Lower limited operating range** 7.6 V ≤ V_{PWR} < 9.6 V **No permanent failure, but IC functionality is not guaranteed** **Reset range:** 0.0 V ≤ V_{PWR} < 7.6 V	**Normal operating range** **100 % functional** 9.6 V ≤ V_{PWR} ≤ 61.6 V	**Upper limited operating range** 61.6 V < V_{PWR} ≤ 75 V **IC parameters maybe out of specification. Detection of V_{PWR} overvoltage is functional**	**Fatal range** **Permanent failure may occur** 75 V < V_{PWR}
	Handling range - no permanent failure			

In both upper and lower limited operating range, no information can be provided about IC performance. Only the detection of V_{PWR} overvoltage is guaranteed in the upper limited operating range.

Performance in normal operating range is guaranteed only if there is a minimum of seven battery cells in the stack.

8.2 Maximum ratings

Table 7. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Max.	Unit
Electrical ratings				
VPWR1, VPWR2	Supply input voltage	−0.3	75	V
CT14	Cell terminal voltage	−0.3	75	V
VPWR to CT14	Voltage across VPWR1,2 pins pair and CT14 pin	−10	10.5	V
CT_N to CT_{N-1}	Cell terminal differential voltage [1]	−0.3	6.0	V
$CT_{N(CURRENT)}$	Cell terminal input current	—	±500	µA
CB_N to $CB_{N:N-1\_C}$ $CB_{N:N-1\_C}$ to CB_{N-1}	Cell balance differential voltage	—	10	V
CB_{N-1_C} to CTn-1	Cell balance input to cell terminal input	−10	+10	V
VISENSE	ISENSE+ and ISENSE– pin voltage	−0.3	2.5	V
VCOM	Maximum voltage may be applied to VCOM pin from external source	—	5.8	V
VANA	Maximum voltage may be applied to VANA pin	—	3.1	V
V_{DIG}	Maximum voltage to digital pins CSB, SO, SDA, RESET, GPIOx	−0.3	VCOM + 0.5	V
$V_{GPIO5,6}$	Maximum voltage for GPIO5 and GPIO6 pins used as current input	−0.3	2.5	V
FAULT	Maximum applied voltage to pin	−0.3	7.0	V
V_{COMM}	Maximum voltage to pins RDTX_OUT+, RDTX_OUT–, SI/ RDTX_IN+, CLK/RDTX_IN–	−10.0	10.0	V
f_{SPI}	SPI frequency (SPI mode)	—	4.2	MHz
BR_{TPL}	Transformer communication bit rate (TPL mode)	1.9	2.1	Mbps
f_{TPL}	Transformer signal frequency (TPL mode)	3.8	4.2	MHz

Symbol	Description (rating)	Min.	Max.	Unit
V_{ESD}	ESD voltage Human body model (HBM) Charge device model (CDM) Charge device model corner pins (CDM)	 — — —	 ±2000 ±500 ±750	V
V_{ESD}	ESD voltage (VPWR1, VPWR2, CTx, CBx, GPIOx, ISENSE+, ISENSE−, RDTX_OUT+, RDTX_OUT−, SI/RDTX_IN+, CLK/RDTX_IN−) [2] Human body model (HBM)	 —	 ±4000	V

[1] Adjacent CT pins may experience an overvoltage which exceeds their maximum rating during OV/UV functional verification test or during open line diagnostic test. Nevertheless, the IC is completely tolerant to this special situation.

[2] ESD testing is performed in accordance with the human body model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the charge device model (CDM) (C_{ZAP} = 4.0 pF).

8.3 Thermal characteristics

Table 8. Thermal ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Max.	Unit
Thermal ratings				
 T_A T_J	Operating temperature Ambient Junction	 −40 −40	 +105 +150	°C
T_{STG}	Storage temperature	−55	+150	°C
T_{PPRT}	Peak package reflow temperature [1] [2]	—	260	°C
Thermal resistance and package dissipation ratings				
$R_{\Theta JB}$	Junction-to-board (bottom exposed pad soldered to board) 64 LQFP EP [3]	—	10	°C/W
$R_{\Theta JA}$	Junction-to-ambient, natural convection, single-layer board (1s) 64 LQFP EP [4] [5]	—	59	°C/W
$R_{\Theta JA}$	Junction-to-ambient, natural convection, four-layer board (2s2p) 64 LQFP EP [4] [5]	—	27	°C/W
$R_{\Theta JCTOP}$	Junction-to-case top (exposed pad) 64 LQFP EP [6]	—	14	°C/W
$R_{\Theta JCBOTTOM}$	Junction-to-case bottom (exposed pad) 64 LQFP EP [7]	—	0.97	°C/W
ΨJT	Junction to package top, natural convection [8]	—	3	°C/W

[1] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.

[2] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts (MC33xxxD enter 33xxx), and review parametrics.

[3] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[4] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[5] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.

[6] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1), with the cold plate temperature used for the case temperature.

[7] Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.

[8] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letter (Ψ) is not available, the thermal characterization parameter is written as Psi-JT.

8.4 Electrical characteristics

Table 9. Static and dynamic electrical characteristics

Characteristics noted under conditions 9.6 V ≤ V_{PWR} ≤ 61.6 V, −40 °C ≤ T_A ≤ 105 °C, GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 56 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Power management					
$V_{PWR(FO)}$	Supply voltage Full parameter specification	9.6	—	61.6	V
I_{VPWR}	Supply current (base value) Normal mode, cell balance OFF, ADC inactive, SPI communication inactive, IVCOM = 0 mA Normal mode, cell balance OFF, ADC inactive, TPL communication inactive, IVCOM = 0 mA	— —	5.4 8.0	8.5 10.0	mA
$I_{VPWR(TPL\_TX)}$	Supply current adder when TPL communication active	—	50	—	mA
$I_{VPWR(CBON)}$	Supply current adder to set all 14 cell balance switches ON	—	0.97	—	mA
$I_{VPWR(ADC)}$	Delta supply current to perform ADC conversions (addend) [1] ADC1-A,B continuously converting ADC2 continuously converting	 — —	 3.0 1.4	 5.0 2.0	mA
$I_{VPWR(SS)}$	Supply current in sleep mode and in idle mode, communication inactive, cell balance off, oscillator monitor on [2] SPI mode (25 °C) SPI mode (−40 °C to 60 °C) SPI mode (105 °C) TPL mode (25 °C) TPL mode (−40 °C to 60 °C) TPL mode (105 °C)	 — — — — — —	 40 — — 68 — —	 — 75 100 — 90 130	µA
$I_{VPWR(CKMON)}$	Clock monitor current consumption	—	10.9	—	µA
V_{VPWR_CT}	Voltage drop across CT14 and VPWR without accuracy degradation [3] 3.0 V ≤ V_{CELL} 2.5 V ≤ V_{CELL}< 3.0 V V_{CELL} < 2.5 V	 −3.0 −2.0 −1.5	 — — —	 3.0 2.0 1.5	V
$V_{PWR(OV\_FLAG)}$	V_{PWR} overvoltage fault threshold (flag)	62	65	68	V
$V_{PWR(LV\_FLAG)}$	V_{PWR} low-voltage warning threshold (flag)	11.7	12	12.3	V
$V_{PWR(UV\_POR)}$	V_{PWR} undervoltage shutdown threshold (POR)	7.6	8.5	9.6	V
$V_{PWR(HYS)}$	V_{PWR} UV hysteresis voltage	100	200	—	mV
$t_{VPWR(FILTER)}$	V_{PWR} OV, LV filter	—	50	—	µs
VCOM power supply					
V_{COM}	VCOM output voltage	4.9	5.0	5.2	V
I_{VCOM}	VCOM output current allocated for external use	—	—	5.0	mA
$V_{COM(UV)}$	VCOM undervoltage fault threshold	4.2	4.4	4.6	V
V_{COM_HYS}	VCOM undervoltage hysteresis	—	100	—	mV
$t_{VCOM(FLT\_TIMER)}$	VCOM undervoltage fault timer	—	10	—	µs
$t_{VCOM(RETRY)}$	VCOM fault retry timer	—	10	—	ms
$V_{COM(OV)}$	VCOM overvoltage fault threshold	5.4	—	5.9	V
$I_{LIM(OC)}$	VCOM current limit	65	—	140	mA
$R_{VCOM(SS)}$	VCOM sleep mode pull-down resistor	1.0	2.0	5.0	kΩ
t_{VCOM}	VCOM rise time (CL = 2.2 µF ceramic X7R only) [4]	—	—	400	µs
VANA power supply					
V_{ANA}	VANA output voltage (not used by external circuits) Decouple with 47 nF X7R 0603 or 0402	2.6	2.65	2.7	V
$V_{ANA(UV)}$	VANA undervoltage fault threshold	2.28	2.4	2.5	V
V_{ANA_HYS}	VANA undervoltage hysteresis	—	50	—	mV
$V_{ANA(FLT\_TIMER)}$	VANA undervoltage fault timer	—	11	—	µs
$V_{ANA(OV)}$	VANA overvoltage fault threshold	2.77	2.8	2.85	V
$t_{VANA(RETRY)}$	VANA fault retry timer	—	10	—	ms

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{LIM(OC)}$	VANA current limit	5.0	—	10	mA
R_{VANA_RPD}	VANA sleep mode pull-down resistor	—	1.0	—	kΩ
t_{VANA}	VANA rise time (CL = 47 nF ceramic X7R only) [4]	—	—	100	µs
ADC1-A, ADC1-B					
$CTn_{(LEAKAGE)}$	Cell terminal input leakage current	—	10	100	nA
$CTn_{(FV)}$	Cell terminal input current - functional verification	—	0.365	0.5	mA
CT_N	Cell terminal input current during conversion	—	50	—	nA
R_{PD}	Cell terminal open load detection pull-down resistor	850	950	3300	Ω
V_{VPWR_RES}	VPWR terminal measurement resolution	—	2.44141	—	mV/LSB
V_{VPWR_RNG}	VPWR terminal measurement range	9.6	—	75	V
$VPWR_{TERM\_ERR}$	VPWR terminal measurement accuracy	−0.5	—	0.5	%
V_{CT_RNG}	ADC differential input voltage range for CTn to CTn-1	0.0	—	4.85	V
$V_{CT\_ANx\_RES}$	Cell voltage and ANx resolution in 15-bit MEAS_xxxx registers	—	152.58789	—	µV/LSB
$V_{ERR33RT}$	Cell voltage measurement error V_{CELL} = 3.3 V, T_A = 25 °C [5] [6]	−0.8	±0.4	0.8	mV
V_{ERR_1}	Cell voltage measurement error [5] [6] 0 V ≤ V_{CELL} ≤ 1.5 V, −40 °C ≤ T_A ≤ 60 °C (or −40 °C ≤ T_J ≤ 85 °C)	−1.5	±0.4	1.5	mV
V_{ERR_2}	Cell voltage measurement error [5] 1.5 V ≤ V_{CELL} ≤ 2.7 V, −40 °C ≤ T_A ≤ 60 °C (or −40 °C ≤ T_J ≤ 85 °C)	−2.0	±0.4	2.0	mV
V_{ERR_3}	Cell voltage measurement error [5] 2.7 V ≤ V_{CELL} ≤ 3.7 V, −40 °C ≤ T_A ≤ 60 °C (or −40 °C ≤ T_J ≤ 85 °C)	−2.0	±0.5	2.0	mV
V_{ERR_4}	Cell voltage measurement error [5] 3.7 V ≤ V_{CELL} ≤ 4.3 V, −40 °C ≤ T_A ≤ 60 °C (or −40 °C ≤ T_J ≤ 85 °C)	−2.8	±0.7	2.8	mV
V_{ERR_5}	Cell voltage measurement error [5] 1.5 V ≤ V_{CELL} ≤ 4.5 V, −40 °C ≤ T_A ≤ 105 °C (or −40 °C ≤ T_J ≤ 125 °C)	−4.5	±0.7	4.5	mV
$V_{ERR33RTA}$	Cell voltage measurement error after aging, V_{CELL} = 3.3 V, T_A = 25 °C [5] [7]	−1.5	±0.5	1.5	mV
V_{ERR_1A}	Cell voltage measurement error [5] [6] [7] after aging, 0 V ≤ V_{CELL} ≤ 1.5 V, −40 °C ≤ T_A ≤ 60 °C (or −40 °C ≤ T_J ≤ 85 °C)	−2.0	±0.5	2.0	mV
V_{ERR_2A}	Cell voltage measurement error [5] [7] after aging, 1.5 V ≤ V_{CELL} ≤ 2.7 V, −40 °C ≤ T_A ≤ 60 °C (or −40 °C ≤ T_J ≤ 85 °C)	−2.5	±0.5	2.5	mV
V_{ERR_3A}	Cell voltage measurement error [5] [7] after aging, 2.7 V ≤ V_{CELL} ≤ 3.7 V, −40 °C ≤ T_A ≤ 60 °C (or −40 °C ≤ T_J ≤ 85 °C)	−3.2	±0.4	3.2	mV
V_{ERR_4A}	Cell voltage measurement error [5] [7] after aging, 3.7 V ≤ V_{CELL} ≤ 4.3 V, −40 °C ≤ T_A ≤ 60 °C (or −40 °C ≤ T_J ≤ 85 °C)	−3.9	±0.7	3.9	mV
V_{ERR_5A}	Cell voltage measurement error [5] [7] after aging, 1.5 V ≤ V_{CELL} ≤ 4.5 V, −40 °C ≤ T_A ≤ 105 °C (or −40 °C ≤ T_J ≤ 125 °C)	−6.0	±0.7	6.0	mV
V_{ANx_ERR}	Magnitude of ANx error in the whole measurement range: [5] [7] Ratiometric measurement Absolute measurement after soldering and aging, input in the range [1.0, 4.5] V Absolute measurement after soldering and aging, input in the range [0, 4.85] V, for −40 °C < T_A < 60 °C) Absolute measurement after soldering and aging, input in the range [0, 4.85] V, for −40 °C < T_A < 105 °C)	 — — −8.0 −11	 — — — —	 16 10 8.0 11	mV
t_{VCONV}	Single channel net conversion time 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	 — — — —	 6.77 9.43 14.75 25.36	 — — — —	µs
V_{V_NOISE}	Conversion noise 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	 — — — —	 1800 1000 600 400	 — — — —	µVrms

Symbol	Parameter	Min.	Typ.	Max.	Unit
ADC2/current sense module					
V_{INC}	ISENSE+/ISENSE− input voltage (reference to GNDREF)	−300	—	300	mV
V_{IND}	ISENSE+/ISENSE− differential input voltage range	−150	—	150	mV
$V_{ISENSEX(OFFSET)}$	ISENSE+/ISENSE− input voltage offset error [8] [9]	—	—	0.5	µV
$I_{SENSEX(BIAS)}$	ISENSE+/ISENSE− input bias current	−100	—	100	nA
$I_{SENSE(DIF)}$	ISENSE+/ISENSE− differential input bias current	−5.0	—	5.0	nA
$I_{GAINERR}$	ISENSE error including nonlinearities [9]	−0.5	—	0.5	%
I_{ISENSE_OL}	ISENSE open load injected current [10]	109	130	151	µA
V_{ISENSE_OL}	ISENSE open load detection threshold	340	460	600	mV
V_{2RES}	Current sense user register resolution	—	0.6	—	µV/LSB
V_{PGA_SAT}	PGA saturation half-range Gain = 256 Gain = 64 Gain = 16 Gain = 4	 — — — —	 4.9 19.5 78.1 150.0	 — — — —	mV
V_{PGA_ITH}	Voltage threshold for PGA gain increase Gain = 256 Gain = 64 Gain = 16 Gain = 4	 — — — —	 — 2.344 9.375 37.50	 — — — —	mV
V_{PGA_DTH}	Voltage threshold for PGA gain decrease Gain = 256 Gain = 64 Gain = 16 Gain = 4	 — — — —	 4.298 17.188 68.750 —	 — — — —	mV
t_{AZC_SETTLE}	Time to perform auto-zero procedure after enabling the current channel	—	200	—	µs
t_{ICONV}	ADC conversion time including PGA settling time 13 bit resolution 14 bit resolution 15 bit resolution 16 bit resolution	 — — — —	 19.00 21.67 27.00 37.67	 — — — —	µs
V_{I_NOISE}	Noise at 16 bit conversion [8]	—	3.01	—	µVrms
V_{I_NOISE}	Noise error at 13 bit conversion	—	8.33	—	µVrms
ADC_{CLK}	ADC2 and ADC1-A,B clocking frequency	5.7	6.0	6.3	MHz
Diagnostic thresholds					
V_{OL_DETECT}	Cell terminal open load V detection threshold [11] 1.5 V ≤ V_{CELL} ≤ 2.7 V 2.5 V ≤ V_{CELL} ≤ 3.7 V 2.5 V ≤ V_{CELL} ≤ 4.3 V	 — — —	 50 100 150	 — — —	mV
V_{LEAK}	Cell terminal leakage detection level [5]	−27	—	27	mV
V_{REF_DIAG}	ISENSE diagnostic reference with PGA having gain 4	124	127	130	mV
V_{OFF_DIAG}	ISENSE diagnostic common mode offset voltage [12]	—	—	37.2	µV
V_{REF_ZD}	Precision diagnostic zener reference for cell voltage channel functional verification	4.45	4.6	4.85	V
V_{CVFV}	Cell voltage channel functional verification allowable error in CT verification measurement [5] [13]	−22	—	6.0	mV
V_{BGP}	Voltage reference used in ADC1-A,B functional verification	—	1.18	—	V
$ADC1a_{FV}$, $ADC1b_{FV}$	ADC1-A and ADC1-B functional verification Maximum tolerance between ADC1-A, B and diagnostic reference (1.5 V ≤ V_{CELL} ≤ 4.3 V)	−5.25	—	5.25	mV
CTx_UV_TH	Undervoltage functional verification threshold in diagnostic mode [11] 1.5 V ≤ V_{CELL} ≤ 2.7 V 2.5 V ≤ V_{CELL} ≤ 3.7 V 2.5 V ≤ V_{CELL} ≤ 4.3 V	 390 650 1200	 — — —	 — — —	mV
CTx_OV_TH	Overvoltage functional verification threshold in diagnostic mode [11] 1.5 V ≤ V_{CELL} ≤ 2.7 V 2.5 V ≤ V_{CELL} ≤ 3.7 V 2.5 V ≤ V_{CELL} ≤ 4.3 V	 — — —	 — — —	 1800 4000 4000	mV
Cell balance drivers					

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{DS(CLAMP)}$	Cell balance driver VDS active clamp voltage	10	11	12	V
$V_{OUT(FLT\_TH)}$	Output fault detection voltage threshold Balance off (open load) Balance on (shorted load)	 0.3	 0.55	 0.75	V
R_{PD_CB}	Output OFF open load detection pull-down resistor Balance off, open load detect disabled	 1.7	 2.0	 2.9	kΩ
$I_{OUT(LKG)}$	Output leakage current Balance off, open load detect disabled at V_{DS} = 4.0 V	 —	 —	 1.0	µA
$R_{DS(on)}$	Drain-to-source on resistance I_{OUT} = 300 mA, T_J = 105 °C I_{OUT} = 300 mA, T_J = 25 °C I_{OUT} = 300 mA, T_J = −40 °C	 — — —	 — 0.5 0.4	 0.80 — —	Ω
I_{LIM_CB}	Driver current limitation (shorted resistor)	310	—	950	mA
t_{CB_AUTOP}	CB_AUTOPAUSE timing	—	4.0	—	µs
t_{ON}	Cell balance driver turn on R_L = 15 Ω	 —	 350	 450	µs
t_{OFF}	Cell balance driver turn off R_L = 15 Ω	 —	 200	 —	µs
$t_{BAL\_DEGLICTH}$	Short/open detect filter time	19	20	42.1	µs
Internal temperature measurement					
IC_TEMP1_ERR	IC temperature measurement error	−3.0	—	3.0	K
IC_TEMP1_RES	IC temperature resolution	—	0.032	—	K/LSB
TSD_TH	Thermal shutdown	155	170	185	°C
TSD_HYS	Thermal shutdown hysteresis	5.0	10	12.2	°C
Default operational parameters					
$V_{CTOV(TH)}$	Cell overvoltage threshold (8 bits), typical value is default value after reset	0.0	4.2	5.0	V
$V_{CTOV(RES)}$	Cell overvoltage threshold resolution	—	19.53125	—	mV/LSB
$V_{CTUV(TH)}$	Cell undervoltage threshold (8 bits), typical value is default value after reset	0.0	2.5	5.0	V
$V_{CTUV(RES)}$	Cell undervoltage threshold resolution	—	19.53125	—	mV/LSB
$V_{GPIO\_OT(TH)}$	GPIOx configured as ANx input overtemperature threshold from POR	—	1.16	—	V
$V_{GPIO\_OT(RES)}$	Temperature voltage threshold resolution	—	4.8828125	—	mV/LSB
$V_{GPIO\_UT(TH)}$	GPIOx configured as ANx input undertemperature threshold from POR	—	3.82	—	V
$V_{GPIO\_UT(RES)}$	Temperature voltage threshold resolution	—	4.8828125	—	mV/LSB
General purpose input/output GPIOx					
V_{IH}	Input high-voltage (3.3 V compatible)	2.0	—	—	V
V_{IL}	Input low-voltage (3.3 V compatible)	—	—	1.0	V
V_{HYS}	Input hysteresis	—	100	—	mV
I_{IL}	Input leakage current Pins tristate, V_{IN} = V_{COM} or AGND	 −100	 —	 100	nA
I_{IDL}	Differential Input Leakage Current GPIO 5,6 GPIO 5,6 configured as digital inputs for current measurement	 −30	 —	 30	nA
V_{OH}	Output high-voltage I_{OH} = −0.5 mA	V_{COM} − 0.8	—	—	V
V_{OL}	Output low-voltage I_{OL} = +0.5 mA	—	—	0.8	V
V_{ADC}	Analog ADC input voltage range for ratiometric measurements	AGND	—	V_{COM}	V
$V_{OL(TH)}$	Analog input open pin detect threshold	0.1	0.15	0.23	V
R_{OPENPD}	Internal open detection pull-down resistor [14]	3.8	5.0	6.2	kΩ
t_{GPIO0_WU}	GPIO0 WU de-glitch filter	47	50	85	µs
t_{GPIO0_FLT}	GPIO0 daisy chain de-glitch filter both edges	19	20	48	µs
t_{GPIO2_SOC}	GPIO2 convert trigger de-glitch filter	1.9	2.0	2.1	µs
t_{GPIOx_DIN}	GPIOx configured as digital input de-glitch filter	2.5	—	5.6	µs
Reset input					
V_{IH_RST}	Input high-voltage (3.3 V compatible)	2.0	—	—	V
V_{IL_RST}	Input low-voltage (3.3 V compatible)	—	—	1.0	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{HYS}	Input hysteresis	—	0.6	—	V
$t_{RESETFLT}$	RESET de-glitch filter	—	100	—	µs
R_{RESET_PD}	Input logic pull down (RESET)	—	100	—	kΩ
SPI_COM_EN input					
V_{IH}	Input high-voltage (3.3 V compatible)	2.0	—	—	V
V_{IL}	Input low-voltage (3.3 V compatible)	—	—	1.0	V
V_{HYS}	Input hysteresis	—	450	—	mV
$R_{SPI\_COM\_EN\_PD}$	Input pull-down resistor (SPI_COM_EN)	—	100	—	kΩ
Bus switch for TPL communication					
R_{SW1} R_{SW2}	Bus switch RDS on resistance 0 V ≤ RDTX_IN+ ≤ 5.0 V 0 V ≤ RDTX_IN− ≤ 5.0 V	— —	— —	1.0 1.0	Ω
R_{SW}	Bus switch RDS on match = $\lvert R_{SW1} - R_{SW2} \rvert$	—	20	—	%
I_{SOL}	Bus switch open leakage RDTX_IN+ at 5.0 V to RDTX_OUT+ at 0 V RDTX_IN− at 5.0 V to RDTX_OUT− at 0 V RDTX_OUT+ at 5.0 V to RDTX_IN+ at 0 V RDTX_OUT− at 5.0 V to RDTX_IN− at 0 V	−10	—	10	µA
t_{SW1_ON}, t_{SW2_ON}	Bus switch switching time, turn on time	100	—	500	ns
t_{SW1_OFF}, t_{SW2_OFF}	Bus switch switching time, turn off time	100	—	1100	ns
RX_{TERM}	Bus termination resistor (open resistor when bus switch is closed)	—	150	—	Ω
Remark: If the bus switch is closed, then the termination resistor is open, else the termination resistor is connected. At the end of the daisy chain, the switch must be open, so that the transmission line is properly terminated.					
Digital interface					
V_{FAULT_HA}	FAULT output (high active, IOH = 1.0 mA)	4.0	4.9	6.0	V
I_{FAULT_CL}	FAULT output current limit	3.0	—	40	mA
R_{FAULT_PD}	FAULT output pull-down resistance	—	100	—	kΩ
V_{IH_COMM}	Voltage threshold to detect the input as high SI/RDTX_IN+, SCLK/RDTX_IN–, CSB, SDA, SCL (NOTE: needs to be 3.3 V compatible)	—	—	2.0	V
V_{IL_COMM}	Voltage threshold to detect the input as low SI/RDTX_IN+, SCLK/RDTX_IN–, CSB, SDA, SCL	0.8	—	—	V
V_{HYS}	Input hysteresis SI/RDTX_IN+, SCLK/RDTX_IN−, CSB, SDA, SCL	30	80	130	mV
I_{LOGIC_SS}	Sleep state input logic current CSB	−100	—	100	nA
R_{SCLK_PD}	Input logic pull-down resistance (SCLK/RDTX_IN–, SI/RDTX+)	—	20	—	kΩ
R_{I_PU}	Input logic pull-up resistance to V_{COM} (CSB, SDA, SCL)	—	100	—	kΩ
I_{SO_TRI}	Tristate SO input current 0 V to V_{COM}	−2.0	—	2.0	µA
V_{SO_HIGH}	SO high-state output voltage with $I_{SO(HIGH)}$ = −2.0 mA	V_{COM} − 0.4	—	—	V
V_{SO_LOW}	SO, SDA, SLK low-state output voltage with $I_{SO(HIGH)}$ = −2.0 mA	—	—	0.4	V
CSB_{WU_FLT}	CSB wake-up de-glitch filter, low to high transition	—	50	80	µs
System timing					
t_{CELL_CONV}	Time needed to acquire all 14 cell voltages and the current after an on demand conversion [15] 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	 56 76 117 197	 59 80 123 208	 62 84 129 218	µs
t_{SYNC}	V/I synchronization time [15] ADC1-A,B at 13 bit, ADC2 at 13 bit ADC1-A,B at 14 bit, ADC2 at 13 bit ADC1-A,B at 15 bit, ADC2 at 13 bit ADC1-A,B at 16 bit, ADC2 at 13 bit	 — — — —	 48.16 53.50 64.16 85.50	 — — — —	µs
t_{SYNC}	V/I synchronization time [15] ADC1-A,B at 13 bit, ADC2 at 14 bit ADC1-A,B at 14 bit, ADC2 at 14 bit ADC1-A,B at 15 bit, ADC2 at 14 bit ADC1-A,B at 16 bit, ADC2 at 14 bit	 — — — —	 52.14 57.48 68.14 89.48	 — — — —	µs

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SYNC}	V/I synchronization time [15]				
	ADC1-A,B at 13 bit, ADC2 at 15 bit	—	62.12	—	µs
	ADC1-A,B at 14 bit, ADC2 at 15 bit	—	65.46	—	
	ADC1-A,B at 15 bit, ADC2 at 15 bit	—	76.12	—	
	ADC1-A,B at 16 bit, ADC2 at 15 bit	—	97.46	—	
t_{SYNC}	V/I synchronization time [15]				
	ADC1-A,B at 13 bit, ADC2 at 16 bit	—	120.51	—	µs
	ADC1-A,B at 14 bit, ADC2 at 16 bit	—	117.84	—	
	ADC1-A,B at 15 bit, ADC2 at 16 bit	—	112.51	—	
	ADC1-A,B at 16 bit, ADC2 at 16 bit	—	113.39	—	
$t_{VPWR(READY)}$	Time after VPWR connection for the IC to be ready for initialization	—	—	5.0	ms
$t_{WAKE-UP}$	Sleep mode to normal mode device ready				
	Wake-up from fault	—	—	400	µs
	Wake-up from GPIO	—	—	400	
	Wake-up from network	—	—	400	
	Wake-up from CSB	—	—	400	
	Sleep mode to normal mode time after TPL bus wake-up	—	—	1.0	ms
t_{WAKE_DELAY}	Time between wake pulses	500	600	700	µs
t_{IDLE}	Idle timeout after POR	57	60	64	s
t_{WAKE_INIT}	Wake-up signaling timeout after POR	—	0.65	—	s
$t_{BALANCE}$	Cell balance timer range	0.5	—	511	min
t_{CYCLE}	Cyclic acquisition timer range	0.0	—	8.5	s
t_{FAULT}	Fault detection to activation of fault pin				
	Normal mode	—	—	56	µs
t_{DIAG}	Diagnostic mode timeout	0.047	1.0	8.5	s
t_{EOC}	SOC to data ready (includes post processing of data) [15]				
	13-bit resolution	140	148	156	µs
	14-bit resolution	190	201	211	
	15-bit resolution	291	307	323	
	16-bit resolution	494	520	546	
t_{SETTLE}	Time after SOC to begin converting with ADC1-A,B [15]	11.67	12.28	12.90	µs
t_{SYS_MEAS1}	Time needed to send an SOC command and read back 96 cell voltages, 48 temperatures, 1 current, and 1 coulomb counter and ADC1-A,B configured as follows:				
	13-bit resolution	—	3.73	—	ms
	14-bit resolution	—	3.78	—	
	15-bit resolution	—	3.89	—	
	16-bit resolution	—	4.10	—	
t_{SYS_MEAS2}	Time needed to send an SOC command and read back 96 cell voltages, 1 current, and 1 coulomb counter and ADC1-A,B configured as follows:				ms
	13-bit resolution	—	2.64	—	
	14-bit resolution	—	2.69	—	
	15-bit resolution	—	2.80	—	
	16-bit resolution	—	3.01	—	
t_{CLST_TPL}	Time needed to send an SOC command and read back 14 cell voltages, 7 temperatures, 1 current, and 1 coulomb counter with TPL communication working at 2.0 Mbps and ADC1-A,B configured as follows:				
	13-bit resolution	—	0.79	—	ms
	14-bit resolution	—	0.85	—	
	15-bit resolution	—	0.95	—	
	16-bit resolution	—	1.16	—	
t_{CLST_SPI}	Time needed to send an SOC command and read back 14 cell voltages, 7 temperatures, 1 current, and 1 coulomb counter with SPI communication working at 4.0 Mbps and ADC1-A,B configured as follows:				ms
	13-bit resolution	—	0.48	—	
	14-bit resolution	—	0.54	—	
	15-bit resolution	—	0.64	—	
	16-bit resolution	—	0.86	—	
$t_{I2C\_DOWNLOAD}$	Time to download EEPROM calibration after POR	—	—	1.0	ms
t_{I2C_ACCESS}	EEPROM access time, EEPROM write (depends on device selection)	—	5.0	—	ms
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time				
	$t_{WAVE\_DC\_BITx = 00}$	476	500	537	µs

Symbol	Parameter		Min.	Typ.	Max.	Unit
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx = 01}$		0.95	1.0	1.06	ms
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx = 10}$		9.53	10	10.53	ms
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx = 11}$		95.25	100	105.25	ms
$t_{WAVE\_DC\_ON}$	Daisy chain duty cycle on time		476	500	537	µs
t_{COM_LOSS}	Time out to reset the IC in the absence of communication		—	1024	—	ms
SPI interface						
F_{SCK}	CLK/RDTX_IN– frequency	[16]	—	—	4.0	MHz
t_{SCK_H}	SCLK/RDTX_IN– high time (A)	[16]	125	—	—	ns
t_{SCK_L}	SCLK/RDTX_IN– high time (B)	[16]	125	—	—	ns
t_{SCK}	SCLK/RDTX_IN− period (A+B)	[16]	250	—	—	ns
t_{FALL}	SCLK/RDTX_IN− falling time		—	—	15	ns
t_{RISE}	SCLK/RDTX_IN− rising time		—	—	15	ns
t_{SET}	SCLK/RDTX_IN− setup time (O)	[16]	20	—	—	ns
t_{HOLD}	SCLK/RDTX_IN– hold time (P)	[16]	20	—	—	ns
t_{SI_SETUP}	SI/RDTX_IN+ setup time (F)	[16]	40	—	—	ns
t_{SI_HOLD}	SI/RDTX_IN+ hold time (G)	[16]	40	—	—	ns
t_{SO_VALID}	SO data valid, rising edge of SCLK/RDTX_IN− to SO data valid (I)	[16]	—	—	40	ns
t_{SO_EN}	SO enable time (H)	[16]	—	—	40	ns
$t_{SO\_DISABLE}$	SO disable time (K)	[16]	—	—	40	ns
t_{CSB_LEAD}	CSB lead time (L)	[16]	100	—	—	ns
t_{CSB_LAG}	CSB lag time (M)	[16]	100	—	—	ns
t_{TD}	Sequential data transfer delay (N)	[16]	1.0	—	—	µs
TPL interface						
$V_{RDTX\ INTH}$	Differential receiver threshold		480	580	680	mV
$V_{RDTX\ INHYS}$	Differential receiver threshold hysteresis		70	100	130	mV
t_{RES}	Slave response after write command (echo)		1.7	2.35	3.2	µs

[1] Use of ADC1-A,B can be performed with a duty cycle of t_{EOC}/period (µs). For example, SYS_CFG1[CYCLIC_TIMER] = 010, corresponding to 100000 µs period, and ADC_CFG[ADC1_A_DEF] = ADC_CFG[ADC1_B_DEF] = 11, corresponding to 16 bits and therefore t_{EOC} = 520 µs, given a duty cycle of 0.0052 (or ROM). When an ADC is configured in continuous mode, the duty cycle is equal to 1, resulting in high-current consumption.

[2] To calculate the current consumption in sleep mode, the following formula has to be used: $I_{SLEEP\_MODE} = (1 – \tau_{NORMAL})$. $I_{VPWR(SS)} + \tau_{NORMAL}$. $[I_{VPWR} + I_{VPWR(ADC)}] + I_{VPWR(CBON)}$ (not zero only if SYS_CFG1[CB_DRVEN] = 1), where $\tau_{NORMAL} = (t_{VCOM} + t_{EOC})$/period (µs), where t_{EOC} depends on the selected number of bits for the ADCs (see ADC_CFG[ADC1_A_DEF, ADC1_B_DEF, ADC2_DEF] fields) and period (µs) depends on SYS_CFG1[CYCLIC_TIMER], as explained in note [1] . Evidently $I_{SLEEP\_MODE} = I_{VPWR(SS)}$ only if no conversion is requested in sleep mode (for example, SYS_CFG1[CYCLIC_TIMER] = 000) and if the cell balancing is OFF.

[3] If the battery stack has at least eight cells and if $–1.5\ V < V_{PWR} – V_{CT\_14} < –0.\ 7\ V$, each cell voltage has to be greater than 2.0 V to meet the accuracy spec. If the battery stack has seven cells and if $–1.5\ V < V_{PWR} – V_{CT\_14} < –0.\ 7\ V$, each cell voltage has to be greater than 2.3 V to meet the accuracy spec.

[4] 16.5.0 % to 95 % rise time

[5] The cell voltage error includes all internal errors, for example; ADC offset, gain error, INL and DNL. Inaccuracies from soldering or aging are not included. Current measurement is not active when measuring the cell voltage. Single shot measurements are affected by noise, which has zero mean and standard deviation given by VV_NOISE and is not included in the cell voltage error. In order to reduce it, SW implemented IIR or FIR low pass filters may be used; example, a moving average, whose length is N samples, has output standard deviation VOUTPUT_NOISE = VV_NOISE /sqrt(N). Performance can be granted only if ADC1-A,B are configured at 16-bits resolution; ADC_CFG[ADC1_A_DEF] = ADC_CFG[ADC1_B_DEF] =11.

[6] If the battery stack has at least eight cells, for all accuracy ranges, the accuracy for a given cell except cell #2, whose positive terminal is connected to CT2 can be guaranteed if all other cells are at least at 1.2 V. The achievement of the accuracy spec for cell #2 requires cell #1, whose positive terminal is connected to CT1, has a voltage of at least 1.5 V. If the battery stack has seven cells, for all accuracy ranges, the achievement of the accuracy spec for a given cell can be guaranteed if all other cells are at least at 1.8 V.

[7] Inaccuracies from soldering (MSL3 preconditioning) and aging (after 1000 h HTOL at T_J = 145 °C) are included.

[8] Offset error is considered at PGA inputs, with PGA gain being set to 256. Both PGA inputs are grounded (shorted together). The offset value, guaranteed by design, does not include the noise, which is considered to be averaged. The noise is characterized by V_{I_NOISE} and is also with PGA gain set to 256 and PGA inputs shorted together.

[9] Performance can be granted only if the ADC2 is configured at the best resolution, namely, ADC_CFG[ADC2_DEF] = 11.

[10] Setting the SYS_DIAG[ISENSE_OL_DIAG] bit to logic 1 causes the injection of the current I_{ISENSE_OL} in both ISENSE ± pins, so if the shunt is disconnected, in one or both of the input pins there is an increased voltage due to charging of external capacitors. Comparison to the threshold V_{ISENSE_OL} detects the open fault.

[11] Only one of the three threshold values shall be selected, dependent on the voltage range in which the cell is typically working, provided a 5 KΩ resistor is used for the input cell low pass filter. Using a dynamic selection of the threshold, depending on the measured voltage is not allowed.

[12] Diagnostic threshold when the PGA inputs are shorted together, the PGA gain is set at 256 and the ADC2 is configured at 16 bit.

[13] This threshold value corresponds to having a safety margin of 40 mV.

[14] During internal open detection, an internal pull-up current of 10 µA typical is generated in the pin.
[15] See Figure 9
[16] See Figure 5

8.5 Timing diagrams

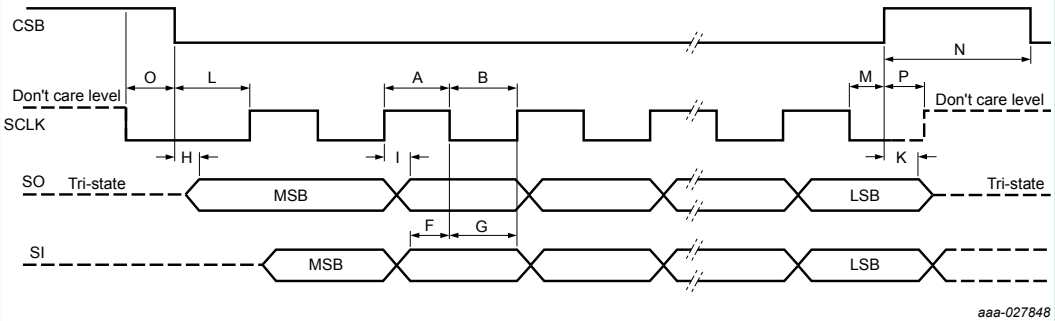


Figure 5. Low-voltage SPI interface timing

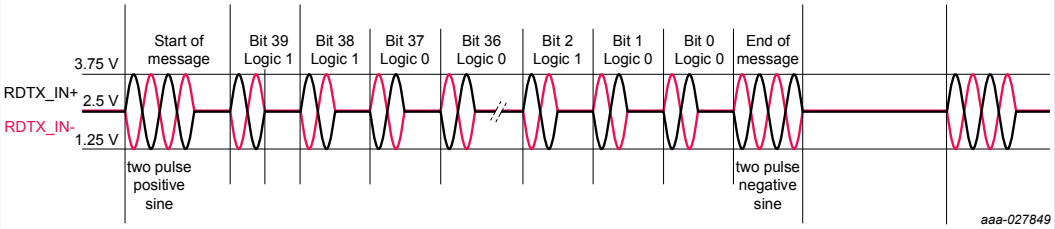


Figure 6. Transformer communication signaling

9 Functional description

9.1 Introduction

The 33771 contains all circuit blocks necessary to perform synchronous battery voltage/current measurement, coulomb counting, cell temperature measurement and integrated cell balancing. These features along with high speed communication make the 33771 ideal for automotive Lithium-ion battery monitoring. In addition to the battery management functions, the 33771 is designed to monitor many internal and external functions to validate the integrity of the measurements and the measurement system. The following section describes in detail the features, functions and modes of operation of the device. Table 10 summarizes the IC measurement capability depending on the operating mode. Following terms, phrasings and conventions are used in this document:

- User: this word denotes the battery pack controller, including at least one MCU, where the intelligence of the system is located. The pack controller uses one or more 33771 to sense the physical quantities of a battery.
- User parameter (or simply parameter): it is a datum memorized in the IC registers which is readable or writable by the user and is denoted by an identifier within square brackets preceded by a prefix, for example, REGISTER_NAME[FIELD_NAME], where REGISTER_NAME is the mnemonic for the intended register and FIELD_NAME is the mnemonic for the parameter itself, which is, in general, a portion of the 16-bit register data.

- Channel: it is a signal, which can be measured. There are external channels, for example, cell voltages and temperatures, and internal channels, for example, die temperature, and voltage diagnostic references.
- Conversion: this word denotes an analog to digital conversion performed by an ADC and is often meant as measurement of a given channel.
- Sequence: this term denotes a scan of channels which enter some multiplexers to be routed to the ADCs according to a certain sequence. During the scan, each ADC performs subsequent data conversions, where each conversion affects a predetermined channel. Sequences are necessary because the number of channels is much greater than the number of ADCs.
- Cyclic measurement: this means the bank of ADCs perform sequences autonomously, for example, with no intervention requested to the user. The user has to do a single programming of an internal timer by providing it with the period value. Then the timer provides the periodic trigger starting each measurement sequence. For example, the period may be 100 ms, while the sequence duration is order of magnitudes shorter. The main purpose of performing cyclic measurements is to carry out automatic comparisons of some measured channels against predefined tunable thresholds, so some fault bits can be set accordingly. Fault bits are readable by the user by accessing the proper fault registers through the ordinary communication channel; or the fault bits may be used to assert the FAULT pin, for the safety information be propagated to the user through the fault line of daisy chained devices.
- On demand measurement: this means the bank of ADCs perform a sequence when triggered by a SOC command, where SOC means start of conversion. Typically, the user periodically sends a SOC command followed by the reading of the measured values of the most important channels, namely all cell voltages, temperatures and current.

Table 10. Working mode versus measurements

Operating mode	On demand measurements	Voltage/temperature cyclic measurements	Current measurement	Coulomb counter	Reference
Normal mode	Available (measurements registers updated after reception of ADC_CFG[SOC] = 1 and the end of the conversion)	Available, if SYS_CFG1[CYCLIC_TIMER] ≠ 0	Available and running continuously if enabled by setting SYS_CFG1[I_MEAS_EN] = 1	Available and running continuously if enabled by setting SYS_CFG1[I_MEAS_EN] = 1 Exception: when the device transitions from sleep to normal mode, it is frozen until it is read and reset by the user	Section 9.3.1
Diagnostic mode	Available (measurements registers updated after reception of ADC_CFG[SOC] = 1 and the end of the conversion)	Not available	Available and running continuously if enabled by setting SYS_CFG1[I_MEAS_EN] = 1	Available and running continuously if enabled by setting SYS_CFG1[I_MEAS_EN] = 1	Section 9.3.3
Sleep mode	Not available	Available, if SYS_CFG1[CYCLIC_TIMER] ≠ 0	Available if enabled by setting SYS_CFG1[I_MEAS_EN] = 1, timing depends on SYS_CFG1[CYCLIC_TIMER] (it must be ≠ 0)	Available if enabled by setting SYS_CFG1[I_MEAS_EN] = 1, timing depends on SYS_CFG1[CYCLIC_TIMER] (it must be ≠ 0)	Section 9.3.2
other modes	Not available	Not available	Not available	Not available	

9.2 Power supplies and reset

9.2.1 VPWR overvoltage, low-voltage

The 33771 incorporates comparators to monitor VPWR pins for overvoltage, undervoltage, and low-voltage conditions. In the event the voltage on VPWR pin is above the overvoltage threshold VPWR(OV_Flag) for greater than the $t_{VPWR(Filter)}$ period, the overvoltage fault flag is set in FAULT1_STATUS[VPWR_OV_FLT].

When unmasked by FAULT_MASK1[MASK_12_F], the FAULT1_STATUS[VPWR_OV_FLT] bit sets the FAULT output pin high. An overvoltage condition on the VPWR pin does not cause the 33771 to perform a shutdown. The pack controller may clear the FAULT1_STATUS[VPWR_OV_FLT] bit when V_{PWR} returns to the normal operating range by writing logic 0 to the FAULT1_STATUS[VPWR_OV_FLT] bit.

A low-voltage condition on VPWR pin causes the FAULT1_STATUS[VPWR_LV_FLT] bit to be set. The FAULT1_STATUS[VPWR_LV_FLT] bit may be cleared when the normal operating range voltage resumes on the VPWR pin and logic 0 is written to the FAULT1_STATUS[VPWR_LV_FLT].

9.2.2 VCOM supply

The VCOM supply is a linear regulator used to supply power for communication, GPIOx, SPI interface, external temperature sensor reference, and optional external EEPROM.

The VCOM supply is monitored by the 33771 for undervoltage. Excessive load on the VCOM pin activates VCOM current limit causing an undervoltage fault condition to occur. During the event, the FAULT2_STATUS[VCOM_UV_FLT] fault bit is set and the regulator enters $t_{VCOM(retry)}$ shutdown/retry strategy.

Undervoltage shutdown of the VCOM supply directly affects communication, GPIO outputs and external temperature measurements. In addition to setting the individual fault bits for each ANx/GPIO, multiple faults may be set in the FAULTx_STATUS register.

Faults may be cleared by the pack controller when communication resumes. VCOM also has a comparator which monitors for overvoltage. In the event the voltage on VCOM becomes greater than VCOM(OV), the FAULT2_STATUS[VCOM_OV_FLT] fault flag is set.

9.2.3 VANA supply

The VANA supply is an internal 2.5 V supply used by the 33771 for analog control. No circuits other than the decoupling capacitor should be terminated to the VANA pin. The VANA supply is monitored by the 33771 for undervoltage. External load on the VANA pin activates the VANA current limit causing an undervoltage fault condition to occur. During the event, the FAULT2_STATUS[VANA_UV_FLT] fault bit is set and the regulator enters $t_{VANA(retry)}$ shutdown/retry strategy.

Undervoltage shutdown of the VANA supply directly affects the performance of the analog to digital converters generating fault condition. Additionally, VANA is monitored by the ADC converter for an overvoltage condition each time a conversion sequence is performed. In the event VANA exceeds the VANA(OV) threshold, the FAULT2_STATUS[VANA_OV_FLT] is set.

9.2.4 VPRE supply

The VPRE supply is an internal pre-regulator supply which sources power to low-voltage sections of the 33771. VPRE is the input supply to the VCOM and VANA regulators.

9.2.5 Power on reset POR

The 33771 has two sources of POR in the IC system. An undervoltage condition for greater than $t_{VPWR(Filter)}$ on the VPWR pin causes the 33771 to reset. Upon returning from undervoltage, the 33771 performs a power on reset (POR).

The second source of potential POR occurs during transient conditions when the internal digital logic supply voltage drops below the critical threshold where logic states cannot be guaranteed. In this case, the 33771 performs a power on reset.

Power on reset is indicated by the FAULT1_STATUS[POR] bit. In the event of a POR, all registers in the 33771 are set to their power on reset state and the FAULT pin becomes active.

9.2.6 Hardware and software reset

An active high on the RESET pin for greater than the $t_{RESETFLT}$ filter time causes the 33771 to reset. Software resets are performed when the 33771 receives a message written to the SYS_CFG1[SOFT_RST] bit. Hardware and software resets are indicated by the status of the FAULT1_STATUS[RESET_FLT] bit, and the FAULT pin becomes active. After a HW or SW reset, it is necessary to wait for the time interval $t_{VPWR(READY)}$ before being possible to reprogram the part.

9.3 Modes of operation

After initialization, the 33771 enters one of three basic modes (normal mode, diagnostic mode or sleep mode). In normal mode the device is in full operation performing the necessary safety functions as well as on demand conversions. When commanded to sleep mode, the device may continue monitoring safety functions with reduced current consumption. Diagnostic mode provides a method for diagnosing the integrity of many safety functions as well as internal or external faults which may have occurred. From power on reset (POR), the 33771 must be initialized with a device address before the device is allowed to enter normal mode.

In the event the device is powered up and not initialized, the 33771 enters the low-power idle mode after a t_{IDLE} timeout period. Detecting a wake-up pattern transfers the 33771 to the initialization state INIT where the address can be programmed. In Figure 7, an integer number enclosed in round brackets close to a transition arc indicates the priority of such a state transition in case the conditions are verified at the same time. The lower the number is, the higher is the priority, so if several conditions are true at the same time, the one with lowest priority number determines the state transition; a boolean condition is enclosed between square brackets. A list of actions after the state transition condition is preceded by the slash symbol. Symbol "t" represents the absolute time, symbol t_0 stays for a variable having the dimension of time.

The table in Figure 7 provides information about the mapping between all possible values of the SYS_CFG2[FLT_RST_CFG] field, which may be written and read by the user, and the corresponding values of the following internal bits, which are not user readable:

- CommResetEN: if it is equal to 1, the IC reset due to a communication timeout in normal mode is enabled, else it is disabled
- OscResetEN: if it is equal to 1, the IC reset due to the detection of a defective oscillator in sleep mode is enabled, else it is disabled
- OscMonitorEN: if it is equal to 1, the oscillator monitoring is enabled, else it is disabled

The value "others" readable in the column labeled as SYS_CFG2[FLT_RST_CFG] refers to values which are different from those listed above.

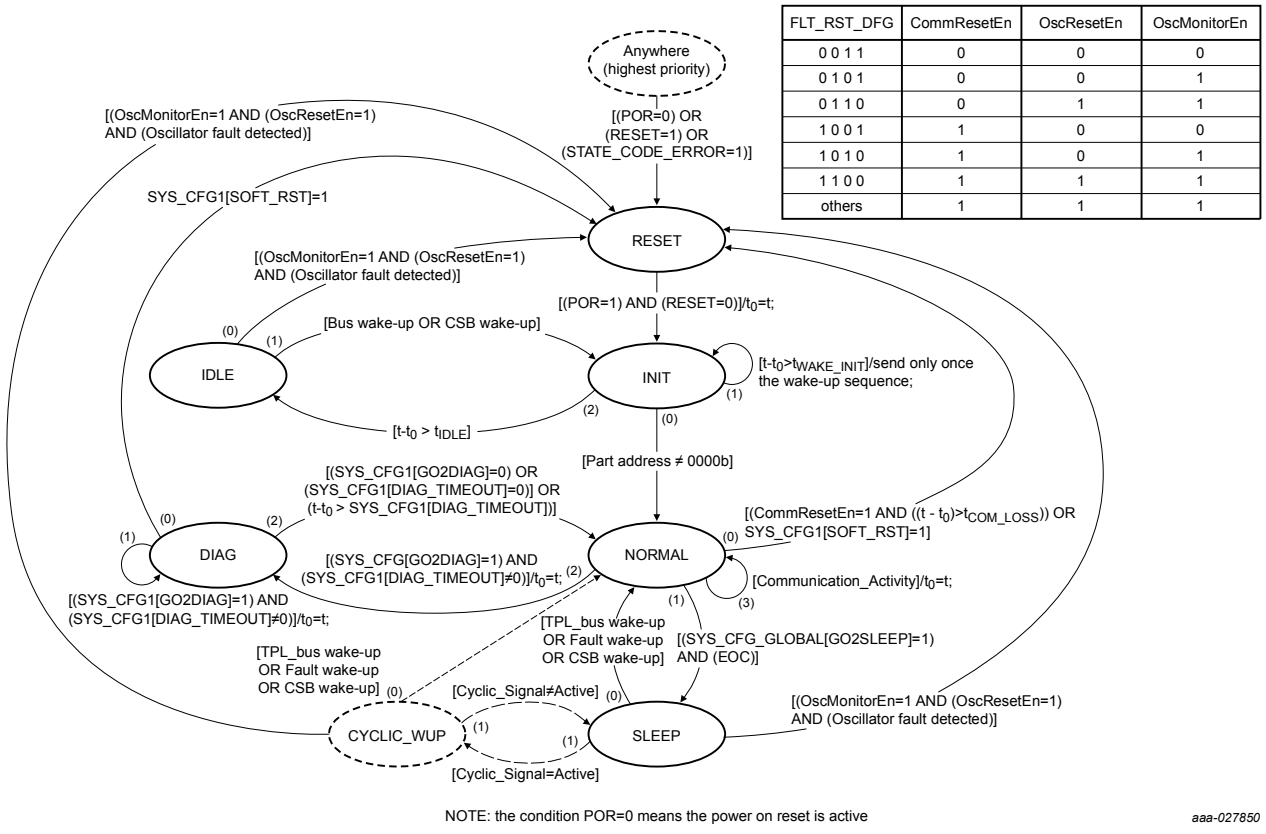


Figure 7. Operating mode state diagram

Table 11. Power supply mode operation

	Normal mode	Diagnostic mode	Sleep mode	Idle mode
Supplies active	VCOM = ON, VANA = ON	VCOM = ON, VANA = ON	VCOM = Duty cycle, VANA = Duty cycle	VCOM = 0, VANA = 0
Communication	SPI transformer	SPI transformer	No communication wake-up	No communication wake-up

9.3.1 Normal mode

In normal mode, commands sent over the bus are directly ported through the transformer or through the SPI to the 33771. On reception of a valid message, the 33771 executes the commanded operation. Device configuration registers control the operating characteristics of the 33771 and are all programmed while the device is in normal mode. Once programmed, the 33771 performs safety operations like overvoltage and undervoltage in the background without further instruction from the pack controller.

To accomplish the safety operations in normal mode, the 33771 performs a cyclic conversion sequence at the programmed timed interval. In the event the 33771 receives an on demand conversion request from the pack controller during a cyclic conversion, the device stops the cyclic conversion and immediately starts the on demand conversion cycle. Halting the cyclic conversion and performing the on demand conversion allows all 33771 devices in the system to achieve synchronized measurements. From normal mode, the 33771 may be commanded to sleep mode or diag mode. If instructed by

a proper value of the SYS_CFG2[FLT_RST_CFG] field, the part automatically resets whenever the communication is absent for longer than t_{COM_LOSS}.

9.3.2 Sleep mode

Sleep mode provides a method to significantly reduce battery current and the overall quiescent current of the battery management system. In sleep mode, the overvoltage, undervoltage, overtemperature, undertemperature, and overcurrent circuitry can remain cyclically active, as well as the monitoring of V_{PWR}.

Based on the CYCLIC_TIMER setting, the 33771 may continue performing cyclic conversions in sleep mode. This is the meaning of the dotted bubble labeled as CYCLIC_WUP in the state diagram shown in Figure 7. The permanence time in the CYCLIC_WUP transient state is really short; it is basically the time needed to turn on the VCOM power supply and to acquire 20 channels.

In the event a conversion value is greater than or less than the threshold value and the particular wake-up/fault is unmasked, the 33771 performs a bus wake-up and can activate the FAULT pin.

To instruct the 33771 to enter the sleep mode, the user sets the SYS_CFG_GLOBAL[GO2SLEEP] bit to logic 1. If the communication type is TPL, only a global write command can be used, while in case of pure SPI communication, a local write command is necessary. Upon receipt of a "go to sleep" command, if the IC is being performing a conversion sequence, then the state transition is delayed until an EOC occurs (end of conversion); else, the state transition occurs immediately.

Exit from sleep mode is possible if one of the following occurs:

- Upon detection of a bus wake-up sequence, in TPL mode only
- By transitioning the CSB pin from low state to high state (shortly referred to as CSB wake-up)
- Upon detection of at least one out of a certain number of fault conditions (see FAULT1_STATUS, FAULT2_STATUS and FAULT3_STATUS along with their associated wake-up mask registers WAKEUP_MASK1, WAKEUP_MASK2 and WAKEUP_MASK3)
- Depending on the content of SYS_CFG2[FLT_RST_CFG] field, it is possible to set the OscResetEn variable to 1.

9.3.3 Diagnostic mode

In diagnostic mode, the system controller has extended control of the 33771 in order to execute performance integrity checks of the device. It is critical to note that when the 33771 is in diagnostic mode, cyclic conversions are halted and OV/UV/OT/UT detection is not performed automatically. To perform OV/UV/OT/UT or any other protection feature which requires a conversion, an on demand conversion message must be sent by the pack controller.

To prevent the 33771 from remaining in diagnostic mode without automatic OV/UV/OT/UT detection, a protection DIAG_TIMEOUT timer has been implemented. In the event of the timeout, the 33771 reverts to normal mode.

To enter diagnostic mode, the user must set the SYS_CFG1[GO2DIAG] bit to logic 1. To exit diagnostic mode, the user must clear the GO2DIAG bit.

9.3.4 Idle mode

The 33771 enters IDLE mode from POR when the communication bus is not active for the t_{IDLE} time period. While the 33771 is in idle mode, no messages are recognized, only a valid wake-up sequence lets the device transition from idle mode to init mode. When the 33771 is configured as a SPI interface and enters idle mode, the device transitions from idle mode to init mode when a rising edge of CSB is received and remains at logic 1 for CSBWU_FLT filter time period.

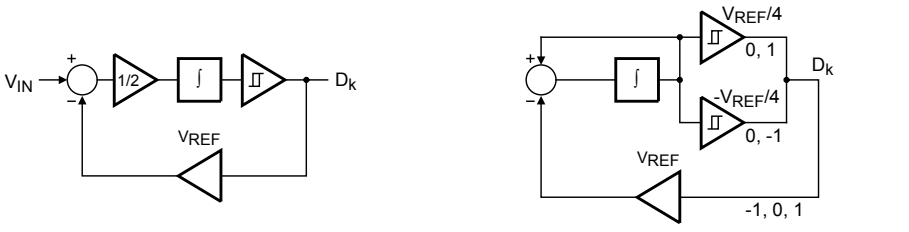
The CSB wake-up capability imply some system considerations when SPI communication is used. Assumed the CSB line is pulled up to the same power supply used by the MCU. When the MCU commands the 33771 to go sleep and then the MCU itself goes to sleep, both devices sleep until the time the MCU wakes up. However, when this happens, the 33771 wakes up, because the CSB line transitions from low state to high state. To avoid this behavior, the MCU has to take care to force the CSB line to the high state during the whole sleep time.

9.4 Analog to digital converters ADC1-A, ADC1-B, ADC2

At the heart of the 33771 are three hybrid ADCs, using a 6.0 MHz clock and having two modes of operation, called phases:

- Incremental phase: it is necessary to compute the most significant bits. During this first phase, the ADC operates as shown in Figure 8 (left part). It appears equal to a 1st order ΣΔ, but it has no memory, as the initial state is always 0.
- The second phase, referred to as cyclic phase, is needed to extract the least significant bits. During this phase, the converter is blind to the input (but not to the reference) and performs the conversion of the residual error.

This ADC, which is built around a switched capacitor integrator, is much faster than a ΣΔ, an essential feature when the input comes from a multiplexer and the channel switching has to be very fast. There is no decimation downstream the ADC.



The output of the integrator V_N at the end of the incremental phase is given by:

$$V_N = \frac{N \cdot V_{IN} - V_{REF} \cdot \sum_{k=1} D_k}{2}$$

The integrator is updated at each cycle. The current output of the integrator, V_k, is linked to the previous one, V_{k-1}, by the following relationship.

$$V_k = 2 \cdot V_{k-1} - D_{k-1} \cdot V_{REF}$$

aaa-027851

Figure 8. ADC converter: incremental phase (left) and cyclic phase (right)

The ADC architecture affords the user the flexibility to select the speed vs. accuracy. Conversion resolution setting for ADC1-A, ADC1-B and ADC2 are programmable from 13 to 16 bits (see Section 11.1.6 "ADC configuration register – ADC_CFG"). ADC1-A and ADC1-B settings must be equal to each other.

9.4.1 High precision voltage reference

To guarantee the accuracy of all ADC conversion data the 33771 integrates a high precision fully compensated voltage reference.

9.4.2 Measurement sequence

The 33771 performs on demand differential measurements of external inputs and internal measurements using three ADC converters for measurement, calibration, and diagnostics. Once the device is initialized, on demand conversions are initiated by writing to the ADC_CFG [SOC] convert register or a GPIO2 input trigger.

The ADC_CFG register contains the conversion parameters for ADC1-A, ADC1-B, and ADC2 converters and the start conversion bit for synchronization. Writing a logic 1 to the SOC bit initiates the conversion sequence. Conversions in progress may be interrupted by reinitiating a new conversion. Measurements for each ADC converters in the 33771 have a predefined measuring sequence. Voltage conversions coming from ADC1-A and ADC1-B are synchronized with free running current measurements performed by ADC2.

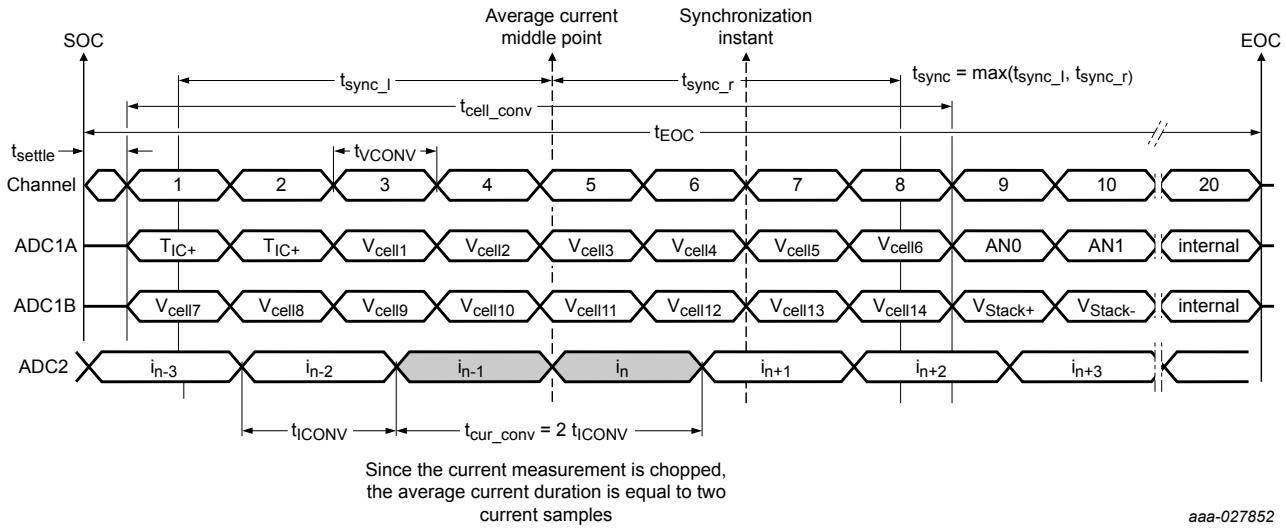


Figure 9. ADC conversion sequence in normal mode

Immediately after receipt of a conversion request, there is a dead time t_{SETTLE}, after which ADC1-A and ADC1-B converters start their conversion sequence. Voltage conversions of ADC1-A and ADC1-B run asynchronously with the current measurements performed by ADC2 as shown in Figure 9.

At time t_{CELL_CONV}, all voltage and current samples are frozen and then post-elaborated. Offset is measured and canceled, a multiplicative correction with a gain depending on the IC die temperature is performed. The completion of the whole sequence, whose length is equal to 20 time slots, occurs at time t_{EOC}. All results are stored into user registers and their associated data ready bits are set to Logic 1. Channels identified as "internal" are used for calibration purposes and are performed at each conversion sequence. Information on how the data is tagged and stored is provided in communication section of this document. On demand conversions are not only used for storing measurement results in user registers, but also for OV/UV/OT/UT comparisons.

The 33771 features a synchronized voltage and current measurements for each requested conversion. Synchronization point is after the 6th channel, that is, at this time

the IC takes a snapshot of the latest two chopped conversions of the current signal, the average of which is calculated to get rid of the current offset.

The meaning of the time t_{SYNC} is the maximum value of two time intervals, t_{SYNC_L} and t_{SYNC_R}, where:

- t_{SYNC_L} is the time interval between the middle point of the first voltage conversion and the instant corresponding to middle point of the latest valid average current value
- t_{SYNC_R} is the time interval between the previously mentioned instant and the middle point of the eighth converted channel

In addition to on demand conversion requests, the 33771 provides timing control for cyclic measurements, that is, conversions occurring with no need for the pack controller to repeatedly send SOC commands. Cyclic measurements are useful for automatic OV/UV/OT/UT check. The user may select the cycle period by programming register SYS_CFG1[CYCLIC_TIMER]. The effective duration of a cyclic sequence is given by the t_{EOC} parameter. A cyclic sequence does not affect the content of the measurement registers (namely, of registers MEAS_ xxxx), while it has effect on the content of CELL_OV_FLT, CELL_UV_FLT, AN_OT_UT_FLT and FAULTx_STATUS registers.

9.5 ADC1-A and ADC1-B functional verification

To functionally verify the integrity of ADC1-A and ADC1-B conversion data, the 33771 has been designed with an independent voltage reference measured by the converters during each on demand and cyclic conversion. Measurement values may be obtained by reading the MEAS_VBG_DIAG_ADC1A and MEAS_VBG_DIAG_ADC1B registers.

These must be compared with the expected value, V_{BGP}, which is the voltage reference used in ADC1-A,B functional verification. The modulus of the error shall not exceed $ADC1_{aFV}$ and $ADC1_{bFV}$.

Detection performance can be guaranteed only if ADC_CFG[ADC1_A_DEF] = ADC_CFG[ADC1_B_DEF] = 11. It is necessary that the system controller performs a moving average of N consecutive values of MEAS_VBG_DIAG_ADC1A and N consecutive values of MEAS_VBG_DIAG_ADC1B before deciding about the fault. N shall be equal or greater than 6.

Before starting the above procedure:

- Disable the ADC1_A and ADC1_B fault detection by setting FAULT_MASK2 ($28) register, MASK_11_F = MASK_10_F = 1.
- Disable the wake-up, due to ADC1_A and ADC1_B faults, by setting WAKEUP_MASK2 ($2B) register, MASK_11_F = MASK_10_F = 1.

9.6 Cell terminal voltage measurement

Cell terminal voltages are monitored differentially, level shifted and multiplexed to the ADC1-A and ADC1-B for conversion.

Unused cell terminal (CTx) inputs may be terminated as shown in Figure 12 or as described in Section 13.2.2 "Unused cells". Overvoltage and undervoltage of unused inputs should be disabled through the OV_UV_EN[CTx_OVUV_EN] bits to prevent the input from triggering fault events. Conversions performed on unused inputs result in nearly zero ADC values.

The differential measurement of each cell terminal input is designed to function in conjunction with external anti-aliasing filter (see Section 13.2 "33771 PCB components").

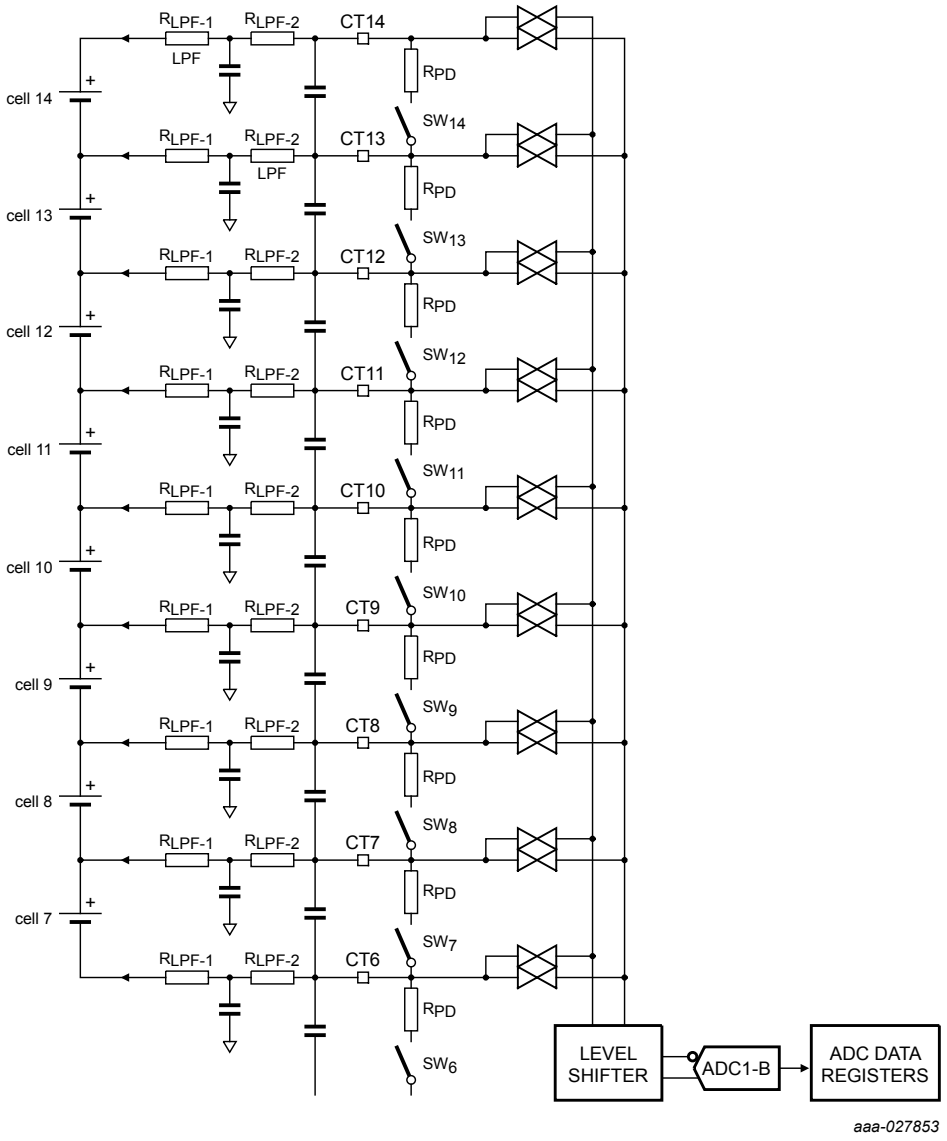


Figure 10. ADC1-B voltage measurement chain

Cell terminal CT7 through CT14 have the same type input structure as CTref through CT6 and are multiplexed to ADC1-A.

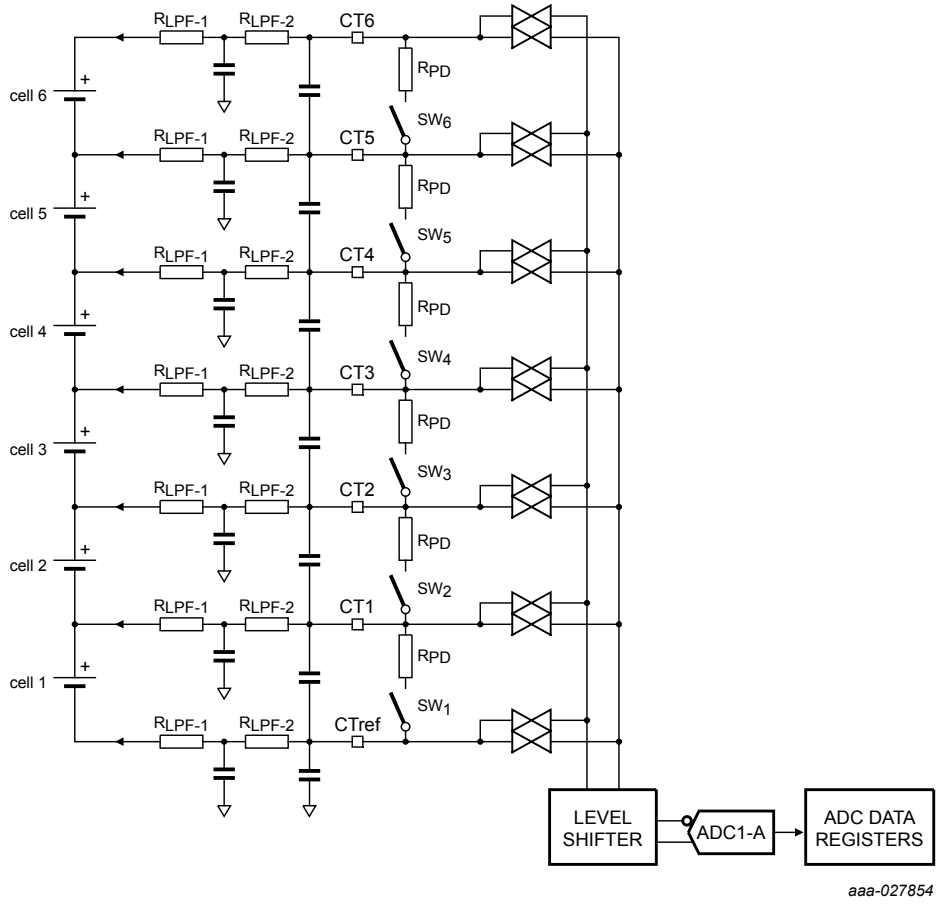


Figure 11. ADC1-A voltage measurement chain

9.7 Cell terminal overvoltage and undervoltage

Overvoltage and undervoltage monitoring is a transparent safety feature which operates in both normal mode and sleep mode. Cyclic and on demand conversions are digitally compared to the programmed overvoltage and undervoltage threshold values in registers TH_CTx. ADC conversions greater than the overvoltage threshold set the corresponding CELL_OV_FLT [CTx_OV_FLT] fault bits. ADC conversions less than the undervoltage threshold value set the corresponding CELL_UV_FLT [CTx_UV_FLT] fault bits.

The overvoltage and undervoltage monitoring feature allows the user to individually program cell overvoltage and undervoltage thresholds. The default overvoltage threshold from POR is TH_CTx[CTx_OV_TH], and may be re-programmed individually or collectively by writing to the TH_CTx [CTx_OV_TH] or TH_ALL_CT [ALL_CT_OV_TH] register fields. The default undervoltage threshold from POR is TH_CTx[CTx_UV_TH], and may be reprogrammed individually or collectively by writing to the TH_CTx [CTx_UV_TH] or TH_ALL_CT [ALL_CT_UV_TH] register fields.

Both overvoltage and undervoltage monitors have an associated fault register. ADC conversion values above the overvoltage threshold or below the undervoltage threshold set the appropriate fault bit in the CELL_OV and CELL_UV fault register. The fault bits in the CELL_OV register are ORed to the FAULT1_STATUS [CT_OV_FLT] bit. The fault bits in the CELL_UV register are ORed to the FAULT1_STATUS [CT_UV_FLT] bit.

9.8 Overvoltage and undervoltage functional verification

Purpose of overvoltage and undervoltage functional verification is to verify OV/UV detection through digital comparators against tunable thresholds function properly. This can be made by forcing an overvoltage or an undervoltage condition on cell terminal pins. Such an operation is performed in diagnostic mode by the 33771 in conjunction with the pack controller. Closing the switches SWx+1 and SWx-1 above and below the generic pair (CTx, CTx-1) of cell terminal pins while keeping open the switch SWx corresponding to this pair (see Figure 11) creates a simulated overvoltage condition between CTx and CTx-1 pins. Opening the switches SWx+1 and SWx-1 above and below the generic pair (CTx, CTx-1) of cell terminal pins while closing the switch SWx corresponding to this pair (see Figure 11) creates a simulated undervoltage condition between CTx and CTx-1 pins. The switches SWx cannot be commanded closed or open individually; it is only possible to command them in groups, as shown in Table 12. Closure of both even and odd switches must be avoided. Quitting the diagnostic mode implies the automatic opening of all switches. If the number of used cells is odd, the logic of opening and closing diagnostic switches is negated for SW6 to SW14.

Table 12. CT diagnostic switches operation

SYS_CFG2 [NUMB_ODD]	SYS_DIAG [CT_OL_ODD,CT_OL_EVEN]	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8...13	SW14
0	01	Open	Closed	Open	Closed	Open	Closed	Open	...	Closed
	10	Closed	Open	Closed	Open	Closed	Open	Closed	...	Open
1	01	Open	Closed	Open	Closed	Open	Open	Closed	...	Open
	10	Closed	Open	Closed	Open	Closed	Closed	Open	...	Closed

If the cluster has missing cells, one possibility to terminate the corresponding CT pin is shown in Figure 12. It is a general rule unused CTx have to be terminated to CT4. To perform the overvoltage and undervoltage functional verification, the master controller has to execute the following sequence.

CONFIGURATION instructions:

1. If the number of cells on the cluster is odd, then write the bit SYS_CFG2[NUMB_ODD] to logic 1, else write it to logic 0.

NORMAL USE instructions:

1. Write SYS_CFG1[GO2DIAG] bit to logic 1 to enter diagnostic mode.
2. Write OV_UV_EN[CTx_OVUV_EN] for x = 1..14 to enable OV/UV.
3. Set the OV and the UV thresholds to diagnostic values (see CTx_UV_TH and the CTx_UV_TH parameters in Table 9).
4. Write SYS_DIAG[CT_OV_UV] bit to logic 1 to enter OV and UV functional verification and write SYS_DIAG[CT_OL_ODD,CT_OL_EVEN] field to 01 configuration to command fault detect switches.
5. Wait for five times the diagnostic time constant $\tau_{diag,n}$ (see Equation (3), Equation (4), and Equation (5)).
6. Write the ADC_CFG[SOC] bit to logic 1 to initiate a conversion.
7. Wait for conversion time.
8. Read CELL_OV_FLT fault register to functionally verify OV faults on those cells whose diagnostic switch is open.
9. Read CELL_UV_FLT fault register to functionally verify UV faults on those cells whose diagnostic switch is closed.

10. Write SYS_DIAG[CT_OL_ODD,CT_OL_EVEN] field to the 10 configuration to command fault detection switches.
11. Wait for five times the diagnostic time constant $\tau_{diag,n}$ (see Equation (3), Equation (4), and Equation (5)).
12. Write the ADC_CFG[SOC] bit to logic 1 to initiate a conversion.
13. Wait for conversion time.
14. Read CELL_OV_FLT fault register to functionally verify OV faults on those cells whose diagnostic switch is open.
15. Read CELL_UV_FLT fault register to functionally verify UV faults on those cells whose diagnostic switch is closed.
16. Write to SYS_DIAG[CT_OL_ODD,CT_OL_EVEN] field to the 00 configuration and write SYS_DIAG[CT_OV_UV] bit to logic 0 to exit OV and UV functional verification.
17. Wait for ten times the measurement time constant τ (see Equation (1) and Equation (2)).
18. Restore normal functional values for the OV and UV thresholds.
19. Clear CELL_OV_FLT and CELL_UV_FLT fault registers, as well as FAULT1_STATUS[CT_OV_FLT, CT_UV_FLT] bits.
20. Write SYS_CFG1[GO2DIAG] bit to logic 0 to exit diagnostic mode.

Note: *Creating a simulated fault in diagnostic mode activates the FAULT output when enabled. To prevent activation of the FAULT output the MCU Controller must mask the simulated fault. This is a general rule.*

Note: *Diagnostic values and normal values of OV and UV thresholds may be very different. Diagnostic values serve to check the digital comparison is functional, while normal values are needed to detect OV and UV on the cell.*

Note: *Open cell terminal inputs directly affect the validity of overvoltage and undervoltage functional verification. Prior to testing for overvoltage and undervoltage functional verification, it is recommended the user first testing for an open cell terminal condition on each input.*

Note: *CT pins may experience an overvoltage which exceeds their maximum rating during this diagnostic test and, nevertheless, the IC is completely tolerant to this special situation.*

Note: *Activating the cell balance during this diagnostics may increase the diagnostic coverage of certain faults, for example, shorted pins. Therefore, this is a recommendable practice.*

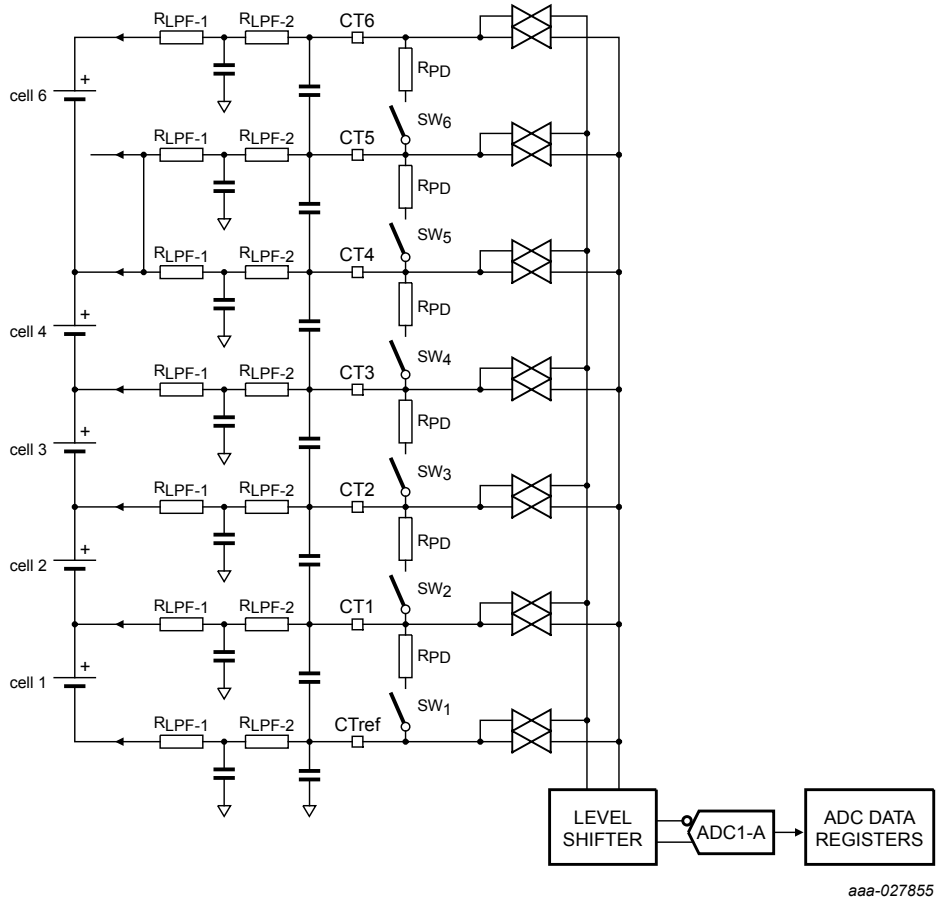


Figure 12. Voltage measurement chain with missing cells

9.9 CTx open detect and open detect functional verification

Cell terminal open detection is performed in diagnostic mode by the 33771 in conjunction with commands from the master controller. The detection can be achieved by taking ADC readings of cell terminal voltages before and after closing detection switches SWx. Data comparison is performed by the master controller. Table 13 describes the conversions data generated in open and normal conditions. If the number of cells is odd, the SYS_CFG2[NUMB_ODD] configuration bit must be set to logic 1, otherwise to logic 0.

Table 13. CT open detect and functional verification

SW_x command status	Normal condition during test execution	Open line condition during test execution	CTx connected and SWx failed shorted	CTx connected and SWx failed open
SWx commanded OFF	V ≥ min(Vcell) (voltage not lower than minimum cell voltage)	**No decision**	V< TH_CTx[CTx_UV_TH] **(shorted SWx detected)**	**No decision** (voltage condition like in 2nd column)
SWx commanded ON	V < TH_CTx[CTx_UV_TH]	V < VOL_DETECT **(open line detected)**	**No decision** (cell voltage condition like in 2nd column)	V ≥ min(Vcell) **(open SWx detected)**

The master controller can perform cell terminal detection using the following sequence.

CONFIGURATION instructions:

1. If the number of cells on the cluster is odd, then write the bit SYS_CFG2[NUMB_ODD] to logic 1, else write it to logic 0.

NORMAL USE instructions:

1. Write SYS_CFG1[GO2DIAG] bit to logic 1 to enter diagnostic mode.
2. Write SYS_DIAG[CT_OL_ODD,CT_OL_EVEN] field to 10 configuration to command fault detect switches.
3. Wait for five times the diagnostic time constant τ_{diag} (see Equation (6), Equation (7), Equation (8), Equation (9), Equation (10), and Equation (11)).
4. Write the ADC_CFG[SOC] bit to logic 1 to initiate a conversion.
5. Wait for conversion time.
6. Read conversion results.
7. Determine fault mode according to Table 13.
8. Write SYS_DIAG[CT_OL_ODD,CT_OL_EVEN] field to 01 configuration to command fault detect switches.
9. Wait for five times the diagnostic time constant τ_{diag} (see Equation (6), Equation (7), Equation (8), Equation (9), Equation (10), and Equation (11)).
10. Write the ADC_CFG[SOC] bit to logic 1 to initiate a conversion.
11. Wait for conversion time.
12. Read conversion results.
13. Determine fault mode according to Table 13.
14. Write SYS_DIAG[CT_OL_ODD,CT_OL_EVEN] field to 00 configuration to open fault detect switches.
15. Wait for ten times the measurement time constant τ (see Equation (1) and Equation (2)).
16. Clear CELL_OV_FLT and CELL_UV_FLT fault registers, as well as FAULT1_STATUS[CT_OV_FLT, CT_UV_FLT] bits.
17. Write SYS_CFG1[GO2DIAG] bit to logic 0 to exit diagnostic mode.

Note: *Checking for open terminals in diagnostic mode may activate the FAULT output for OV or UV when enabled. To prevent activation of the FAULT output, the MCU Controller must mask the simulated fault.*

Note: *Look at the notes in Section 9.7 "Cell terminal overvoltage and undervoltage" for the meaning of diagnostic settling time and cell terminal settling time.*

9.10 Cell voltage channel functional verification

Cells associated to pin pairs CTx – CTx-1, with x > 2, have level shifters which may introduce gain variations, so masking over/ undervoltage. Multiplexers used to route CTx pins to ADC1-A,B can also introduce gain variations. The purpose of cell voltage channel functional verification is to verify such gain variations are small compared to the unity. The diagnostics disconnects the cell terminal input circuitry and places a precision zener reference on the input to each differential amplifier attenuator to verify the integrity of the level shifting differential amplifier, attenuator, and multiplexer chain.

The conversion result is stored in the MEAS_CELLx register for the system controller to read. The values of the MEAS_CELLx registers may be compared by the pack controller to the zener reference MEAS_CELL2 register. Channel functional verification may be performed in diagnostic mode only using the following sequence:

1. Write SYS_CFG1[GO2DIAG] bit to logic 1 to enter diagnostic mode.

2. Write SYS_DIAG[DA_DIAG] bit to logic 1 to isolate CTx inputs and place reference at the amplifier input.
3. Write register ADC_CFG[SOC] to initiate a conversion.
4. Wait for conversion time.
5. The system controller reads MEAS_CELLx results and computes errors V_err_x = (MEAS_CELLx – MEAS_CELL2), for x = 3 to 14.
6. The system controller checks, for any x = 3 to 14, if inequalities min (V_{CVFV}) ≤ V_err_x ≤ max (V_{CVFV}) are true. If yes, the check is ok, otherwise an error is detected.
7. Clear cell OV faults in both the FAULT1_STATUS[CT_OV_FLT] bit and the CELL_OV_FLT register.
8. Exit diagnostic mode by writing SYS_CFG1[GO2DIAG] bit to logic 0.

Note: *Functional verification assumes a minimum cell voltage not lower than max(1.5, 12 / N_{CELL}) Volt, where N_{CELL} is the number of cells of the cluster. For example, N_{CELL} = 7 implies a minimum cell voltage of 1.715 V, while N_{CELL} = 9 implies the value of 1.5 V.*

Note: *Detection performance can be guaranteed only if ADC1-A, B are configured at 16 bit resolution, that is, ADC_CFG[ADC1_A_DEF] = ADC_CFG[ADC1_B_DEF] = 11.*

Note: *To reduce the effect of the noise, it is good practice to cycle through steps 3 and 4 a few times to get an average of the results before proceeding to step 5.*

Note: *Checking all channels from 3 to 14 is necessary only if all 14 cells are used; otherwise, unused cell voltage channels may be skipped.*

9.11 Cell terminal leakage diagnostics

The 33771 is capable of diagnosing all cell terminal pin leakage currents and some cell balancing leakage currents. Diagnostics is accomplished by using one cell balance terminal and one cell voltage terminal as an input to the ADC, so measuring the differential voltage across the external LPF resistor and the cell balance resistor, as shown in Figure 13. More precisely, what is measured is shown in Table 14. To verify the cell voltage terminal or the cell balance terminal are not sinking or sourcing current an inverted and non-inverted differential measurement is made across the above mentioned resistors. Leakage current producing a voltage effect in excess of V_{LEAK} can be detected.

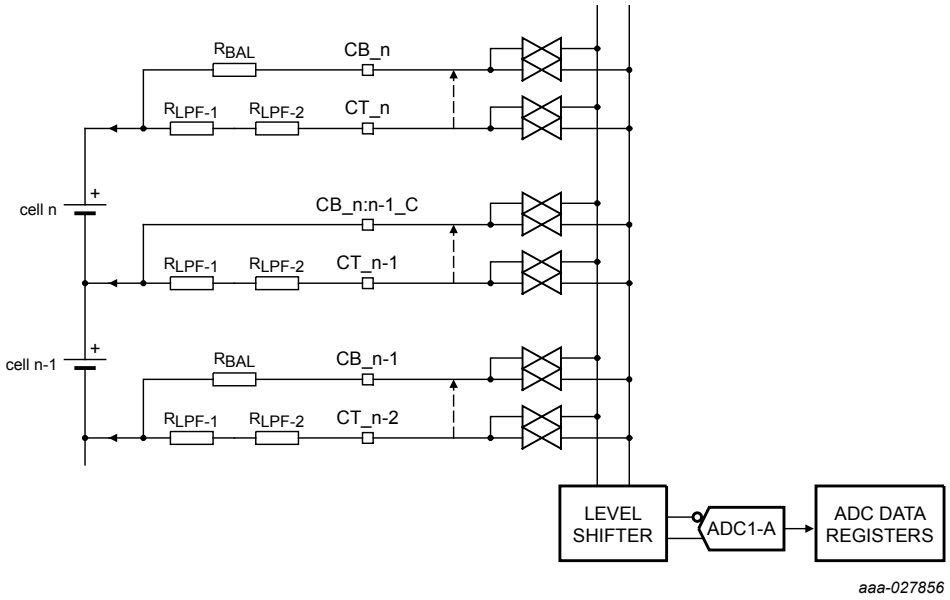


Figure 13. Cell terminal pin leakage detection

Table 14. Routing table and cell leakage measurement results

Result stored to	What is measured with SYS_DIAG[POLARITY] = 0	What is measured with SYS_DIAG[POLARITY] = 1
MEAS_STACK	Max(0, V(CT_14) – V(CB_14))	Max(0, V(CB_14) – V(CT_14))
MEAS_CELL14	Max(0, V(CB_14:13_C) – V(CT_13))	Max(0, V(CT_13) – V(CB_14:13_C))
MEAS_CELL13	Max(0, V(CB_13) – V(CT_12))	Max(0, V(CT_12) – V(CB_13))
MEAS_CELL12	Max(0, V(CB_12:11_C) – V(CT_11))	Max(0, V(CT_11) – V(CB_12:11_C))
MEAS_CELL11	Max(0, V(CB_11) – V(CT_10))	Max(0, V(CT_10) – V(CB_11))
MEAS_CELL10	Max(0, V(CB_10:9_C) – (CT_9))	Max(0, V(CT_9) – V(CB_10:9_C))
MEAS_CELL9	Max(0, V(CB_9) – V(CT_8))	Max(0, V(CT_8) – V(CB_9))
MEAS_CELL8	Max(0, V(CB_8:7_C) – (CT_7))	Max(0, V(CT_7) – V(CB_8:7_C))
MEAS_CELL7	Max(0, V(CB_7) – V(CT_6))	Max(0, V(CT_6) – V(CB_7))
MEAS_CELL6	Max(0, V(CB_6:5_C) – (CT_5))	Max(0, V(CT_5) – V(CB_6:5_C))
MEAS_CELL5	Max(0, V(CB_5) – V(CT_4))	Max(0, V(CT_4) – V(CB_5))
MEAS_CELL4	Max(0, V(CB_4:3_C) – V(CT_3))	Max(0, V(CT_3) – V(CB_4:3_C))
MEAS_CELL3	Max(0, V(CB_3) – V(CT_2))	Max(0, V(CT_2) – V(CB_3))
MEAS_CELL2	Max(0, V(CB_2:1_C) – V (CT_1))	Max(0, V(CT_1) – V(CB_2:1_C))
MEAS_CELL1	Max(0, V(CB_1) – V(CT_REF))	Max(0, V(CT_REF) – V(CB_1))

Cell terminal leakage detection is performed in diagnostic mode by the 33771 in conjunction with commands from the master controller. Leakage detection is achieved by taking an ADC reading of the cell terminals referenced to cell balance terminals. Comparison of the data is performed by the master controller. The procedure is described by the following:

1. Write SYS_CFG1[GO2DIAG] bit to a logic 1 to enter diagnostic mode.
2. Put the cell balance drivers in pause by setting the SYS_CFG1[CB_MANUAL_PAUSE] bit to logic 1.

3. Write SYS_DIAG[CT_LEAK_DIAG,POLARITY] = 10 to route cell terminal and balancing pins according to the logic of the routing table.
4. Write register ADC_CFG[SOC] to initiate a conversion.
5. Wait for conversion time.
6. Read all MEAS_CELLx and MEAS_STACK registers.
7. Compute leakage indices $IND0_x$ = MEAS_CELLx, for x = 1 to 14.
8. Compute leakage index $IND0_{15}$ = MEAS_STACK.
9. Write SYS_DIAG[CT_LEAK_DIAG,POLARITY] = 11 to route cell terminal and balancing pins according to the logic of the routing table.
10. Write register ADC_CFG[SOC] to initiate a conversion.
11. Wait for conversion time.
12. Read all MEAS_CELLx and MEAS_STACK registers.
13. Compute leakage indices $IND1_x$ = MEAS_CELLx, for x = 1 to 14.
14. Compute leakage index $IND1_{15}$ = MEAS_STACK.
15. Compute $Vleak_x(k) = IND0_x + IND1_x$, for x = 1 to 15.
16. Calculate $Vleak\_AV_x(k) = MA_{Nx}(Vleak_x(k))$, where $MA_{Nx}()$ is the moving average operator of length N.
17. Evaluate the decision criterion, for x = 1 to 15: If $Vleak\_AV_x(k) \geq V_{LEAK}$ then cell x is leaky, else cell x is not leaky.
18. Clear CELL_OV and CELL_UV fault register.
19. Clear SYS_DIAG[CT_LEAK_DIAG,POLARITY].
20. End the pause state of cell balance drivers by setting the SYS_CFG1[CB_MANUAL_PAUSE] bit to logic 0.
21. Exit diagnostic mode SYS_CFG1[GO2DIAG] bit to logic 0.

The time index (k) is increased each time the cell terminal leakage diagnostics is performed, so the decision is based on the history of N executions of this diagnostics. Of course, k is just a symbol to highlight this fact, and is not something needing to be implemented. MA_{Nx} internal state must be initialized to all zeros at the very beginning of the operation. The length N of the moving average depends on the system fault tolerant time, the FTTI, and on the diagnostic test interval, the DTI, of this specific diagnostics. As a rule of thumb, N = ROUND(FTTI/(2·DTI)). For instance, assuming FTTI = 1000 ms and DTI = 25 ms, the result is N = 20.

Note: *The MEAS_STACK register contains the cell terminal 14 leakage data. The number of measurements is 15: the one in CT_REF is stored in MEAS_CELL1, the one in CT_1 is stored in MEAS_CELL2,… the one in CT_13 is stored in MEAS_CELL14 and the one in CT_14 is stored in MEAS_STACK.*

Note: *The voltage measurement polarity contained in MEAS_STACK is opposite polarity the ones contained in MEAS_CELLx.*

Note: *Balancing is **prohibited** during this diagnostic.*

Note: *This diagnostics may also be helpful to detect some inadvertently activated or leaky CB drivers. However, not all CB leakages can be detected in this way. See Table 14.*

Note: *Before using the content of measurement registers, the user must check associated DATA_RDY bits attain the logic 1 value. If the check is not successful, the read operation must be repeated.*

9.12 VPWR stack voltage measurement

V_{PWR} stack voltage measurement is converted from the VPWR pin to the AGND pin. The voltage is attenuated using internal resistive divider. Stack measurement conversion is performed with every conversion sequence and is stored in the MEAS_STACK register. It is recommended to compare the sum of the cell voltages to the stack measurement as a congruence check.

9.13 Current measurement

Current measurement channel features 16-bit ADC with an automatic programmable gain amplifier (PGA) allowing the user to accurately measure current from −1500 A to 1500 A (the actual range is in terms of voltage and is given by min and max of V_{IND}) with a 6.0 mA resolution (in terms of voltage it is V_{2RES}) when using a single 100 µΩ shunt resistor. The current channel includes automatic offset calibration, redundant measurement path, and internal diagnostics.

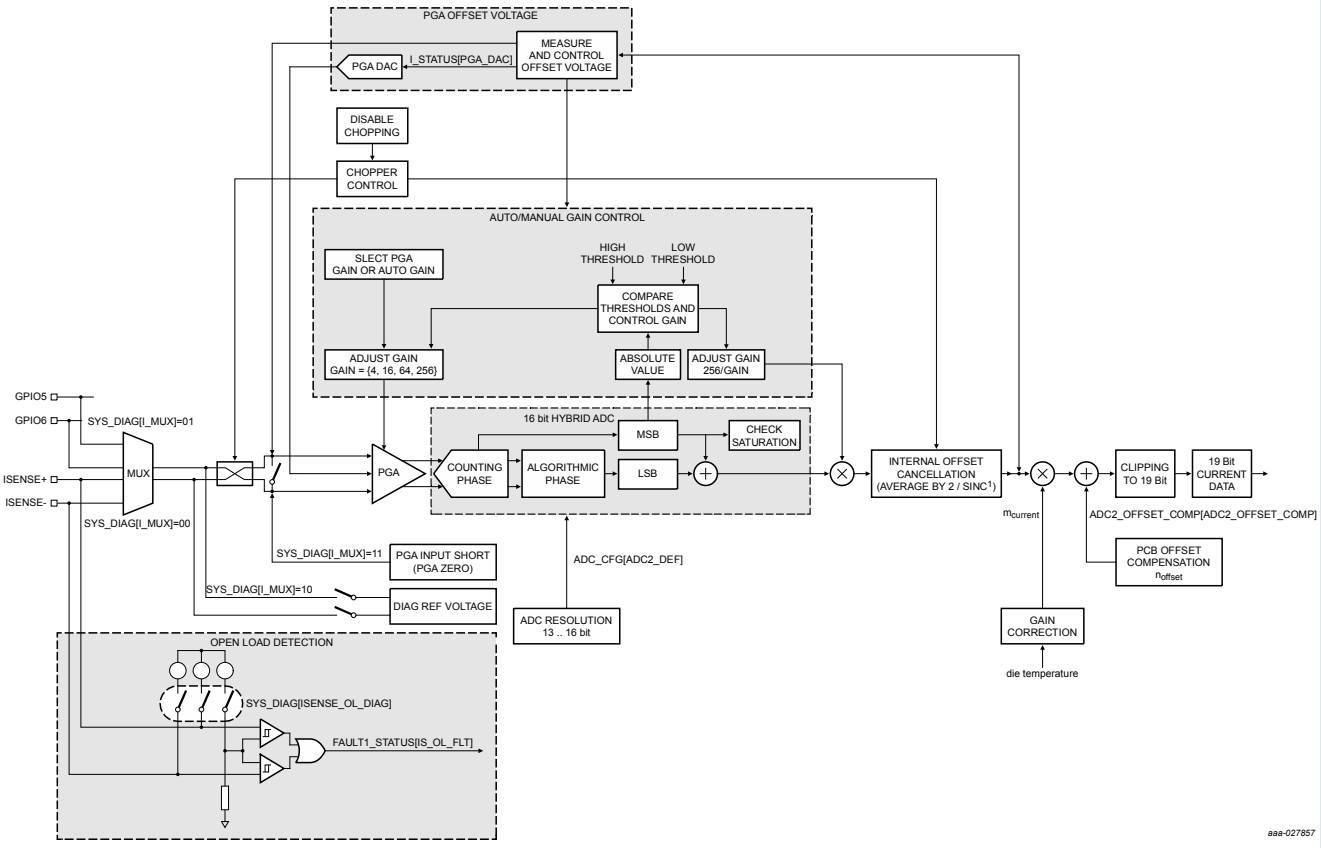


Figure 14. Current measurement channel

From initialization, the current measurement chain is disabled. The MCU controller must enable the measurement chain by setting the SYS_CFG1[I_MEAS_EN] bit to logic 1, to initiate continuous current conversions. Current measurement conversions for coulomb counting are performed continuously in normal and diagnostic modes, while in sleep mode they occur periodically and the period is given by SYS_CFG1[CYCLIC_TIMER].

An automatic auto-zero compensation for the PGA is performed each time the current measurement channel gets enabled, for example, this occurs in a one shot way. The time

to perform the procedure is given by the parameter t_{AZC_SETTLE}. This auto-zero sequence is as follows:

- The PGA gain is set to the value of 256 during the whole procedure
- The PGA inputs get shorted together. In such condition, in front of the PGA, there is only its own offset voltage, which gets amplified and goes to the ADC2 input. The PGA settling time is awaited.
- An ADC2 conversion is started and its end is awaited
- The conversion result is divided by the PGA gain
- A proper digital code for a DAC is generated
- The DAC output signal is subtracted in front of the PGA and the offset gets cancelled

Even though the auto-zero compensation fixes the PGA dynamic range, this action alone is not capable of removing all the offset from the current channel. For such reason, a chopper is used, which sends alternatively and repetitively, the ISENSE+/– differential inputs and the ISENSE–/+ differential inputs (reverse input pair) to the PGA differential inputs. Downstream, the ADC2, a digital post-processor computes the semi-difference between the current sample and the past sample. Therefore, the ADC post-processor receives the input stream (..., $+I_1$ + off, $–I_2$ + off, $+I_3$ + off, $–I_4$ + off, $+I_5$ + off, ...) and gives as output stream (..., $(I_1 + I_2) / 2$, $(I_2 + I_3) / 2$, $(I_3 + I_4) / 2$, $(I_4 + I_5) / 2$, ...).

The mechanism works because the offset remains uninverted, since it is located downstream from the chopper. So, it is the combination of mixer and digital post-processing which compensates the whole offset which may affect the channel.

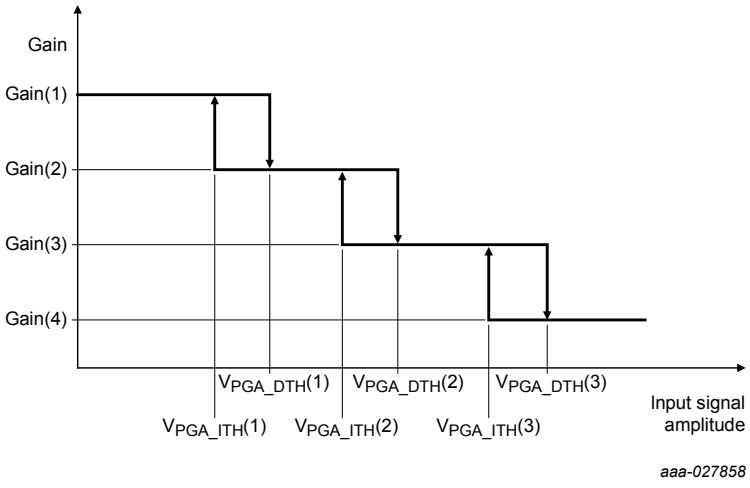


Figure 15. Current measurement channel (gain vs. input signal amplitude)

The PGA gain can be programmed at each conversion request by writing to the ADC_CFG[PGA2_GAIN] register field. The PGA can be set to a manual gain of 4, 16, 64, and 256 or programmed for automatic gain control. Automatic gain control allows the device to obtain the most appropriate gain setting for the amplifier input signal level. In automatic gain control mode, the conversion result is digitally compared with internally programmed thresholds. Gain is automatically adjusted to maintain the digital result within the threshold window. PGA auto-gain is implemented by applying a hysteresis to each threshold. Saturation of the ADC is reported by the flag MEAS_ISENSE2[ADC2_SAT]. A PGA setting change between two chopped measurements is reported by the flag MEAS_ISENSE2[PGA_GCHANGE] to indicate reduced accuracy for the resulting measurement value. An external low pass filter is required to prevent an over range event within the PGA. Such event may happen if the

time derivative of the current signal is so high that it causes the voltage drop across the ISENSE+/- terminals to exceed the maximum allowed slope value of ±4 V/s. The way this limit on the slope has to be understood is the following: if the battery current changes like a large ideal step, the output signal of the input filter must have a slope whose absolute value must not exceed the aforementioned value. So, this limit only applies to large signals, that is, it does not apply, for example, to a sinusoidal current signal having small amplitude but very large frequency, because a small signal normally does not require a change in the gain value. Large signal signifies that the signal magnitude is so high that the PGA gain is required to be switched to a value different from the currently used one.

ADC2, dedicated to the current measurement channel, performs continuous conversions in normal and diagnostic modes. Receiving an on demand conversion request, the most recent current measurement obtained before the last cell voltage gets converted is stored in MEAS_ISENSE1 and MEAS_ISENSE2 registers, so synchronizing the current with all voltages within the t_{SYNC} window.

The current measurement channel includes a sleep mode wake-up feature. In sleep mode, the PGA gain is constantly equal to 256 and each cyclic current measurement result is compared with the current wake-up threshold TH_ISENSE_OC register. Three out of four current values above the threshold trigger a system wake-up and activate the fault output when the wake-up enable bit is set.

9.14 Current measurement diagnostics

In diagnostic mode, the user may perform functions to verify the integrity of the current measurement chain, detect open ISENSE terminals and perform offset measurement. To verify the integrity of the current measurement chain, the 33771 allows the user to multiplex the differential PGA input terminals between several sources. By using the following procedure, differential measurements may be taken on ISENSE inputs, AN5 and AN6 inputs, the internal precision reference and the internally shorted amplifier inputs.

1. Disable the current measurement by setting SYS_CFG1[I_MEAS_EN] = 0.
2. Write SYS_CFG1[GO2DIAG] bit to logic 1 to enter diagnostic mode.
3. Read the coulomb counter register COULOMB_CNT to retain count information.
4. Configure the current measurement chain for the specific diagnostic source by writing to the SYS_DIAG[I_MUX] bits.
5. Enable the current measurement by setting SYS_CFG1[I_MEAS_EN] = 1.
6. Wait for the time to perform auto-zero procedure t_{AZC_SETTLE}.
7. Write ADC_CFG[CC_RST] = 1 and ADC_CFG[SOC] = 1 to reset the coulomb counter COULOMB_CNT and initiate a conversion.
8. Wait for the conversion time.
9. Read the conversion results in register MEAS_ISENSE1 and MEAS_ISENSE2 and compare data with the expected result. Alternatively, use the coulomb counter registers to perform this check.
10. Exit diagnostic mode SYS_CFG1[GO2DIAG] bit to logic 0.
11. Reset the coulomb counter COULOMB_CNT.

To verify if the current shunt is properly connected to the current channel low-pass filter, the user has to perform the following procedure:

1. Disable the current measurement by setting SYS_CFG1[I_MEAS_EN] to logic 0.
2. Read the coulomb counter COULOMB_CNT to retain count information.
3. Write SYS_CFG1[GO2DIAG] bit to logic 1 to enter diagnostic mode.

4. Configure the current measurement chain for the open detection check by setting the SYS_DIAG[ISENSE_OL_DIAG] to logic 1.
5. Wait for the diagnostic time t_{diag} (see Equation (14) in Section 13.2.4 "Current channel filter").
6. Read the flag FAULT1_STATUS[IS_OL_FLT].
7. Configure the current measurement chain for the open detection block by setting SYS_DIAG[I_SENSE_OL_DIAG] to logic 0.
8. Wait for ten times the current measurement time constant τ_I (see Equation (12) and Equation (13) in Section 13.2.4 "Current channel filter").
9. Enable the current measurement and exit diagnostic mode by setting SYS_CFG[I_MEAS_EN] to logic 1 and SYS_CFG1[GO2DIAG] to logic 0.
10. Reset the coulomb counter COULOMB_CNT.

Table 15. Current measurement fault diagnostics

DIAG type	Unfaulted condition	Faulted condition	Diagnostic description
ISENSE ± open detection	FAULT1_STATUS[IS_ OL_FLT] = 0 [1]	FAULT1_STATUS[IS_ OL_FLT] = 1	Diagnostic of open between shunt and PGA (condition ISENSE_OL_DIAG = 1)
Amplifier inputs grounded	|MEAS_ISENSE1,MEAS_ISENSE2| ≤ VOFF_DIAG	|MEAS_ISENSE1,MEAS_ISENSE2| > VOFF_DIAG	Diagnostic of measurement chain offset with PGA inputs grounded (condition SYS_DIAG[I_MUX] = 11)
VREF_DIAG reference (gain 4)	MEAS_ISENSE1,MEAS_ISENSE2 = VREF_DIAG	MEAS_ISENSE1,MEAS_ISENSE2 ≠ VREF_DIAG	Diagnostic of measurement chain with known reference and gain of 4 (condition SYS_DIAG[I_MUX] = 10)
GPIO5, GPIO6	Application dependent [2]	Application dependent	Diagnostic of external AAF open and short or leaking devices (condition SYS_DIAG[I_MUX] = 01)

[1] Setting the SYS_DIAG[ISENSE_OL_DIAG] bit to logic 1 causes the injection of the current I_{ISENSE_OL} in both ISENSE ± pins, so if the shunt is disconnected, in one or both of the input pins there is an increased voltage due to charging of external capacitors. Comparison to the threshold V_{ISENSE_OL} detects the open fault.

[2] GPIO5, GPIO6 diagnostics enable the user to monitor a differential voltage coming from an external circuit. They can be used for diagnostic purposes, for example, to measure the voltage drop across a resistor used in the external anti-aliasing filter connected to ISENSE ± or to monitor a backup copy of the voltage drop across the current shunt.

9.15 Coulomb counting

In normal and diagnostic mode, all conversions of ADC2 increment the internal coulomb counter, referred to as COULOMB_CNT, which represents the discrete integral of ADC2 samples, where the time index can only take positive integer values. COULOMB_CNT is copied to registers COULOMB_CNT1, COULOMB_CNT2. In addition to this, the 33771 provides the number of accumulated samples in register CC_NB_SAMPLES, which represents the elapsed time expressed in integer units. The coulomb counter registers COULOMB_CNT1, COULOMB_CNT2 and CC_NB_SAMPLES are reset by writing the ADC_CFG[CC_RST] reset bit.

In the event an overflow occurs in either COULOMB_CNT or CC_NB_SAMPLES, the CC_OVR_FLT bit is set and, when unmasked, the FAULT pin is activated. The coulomb count value is impacted by conversions performed during diagnosis of the current measurement chain.

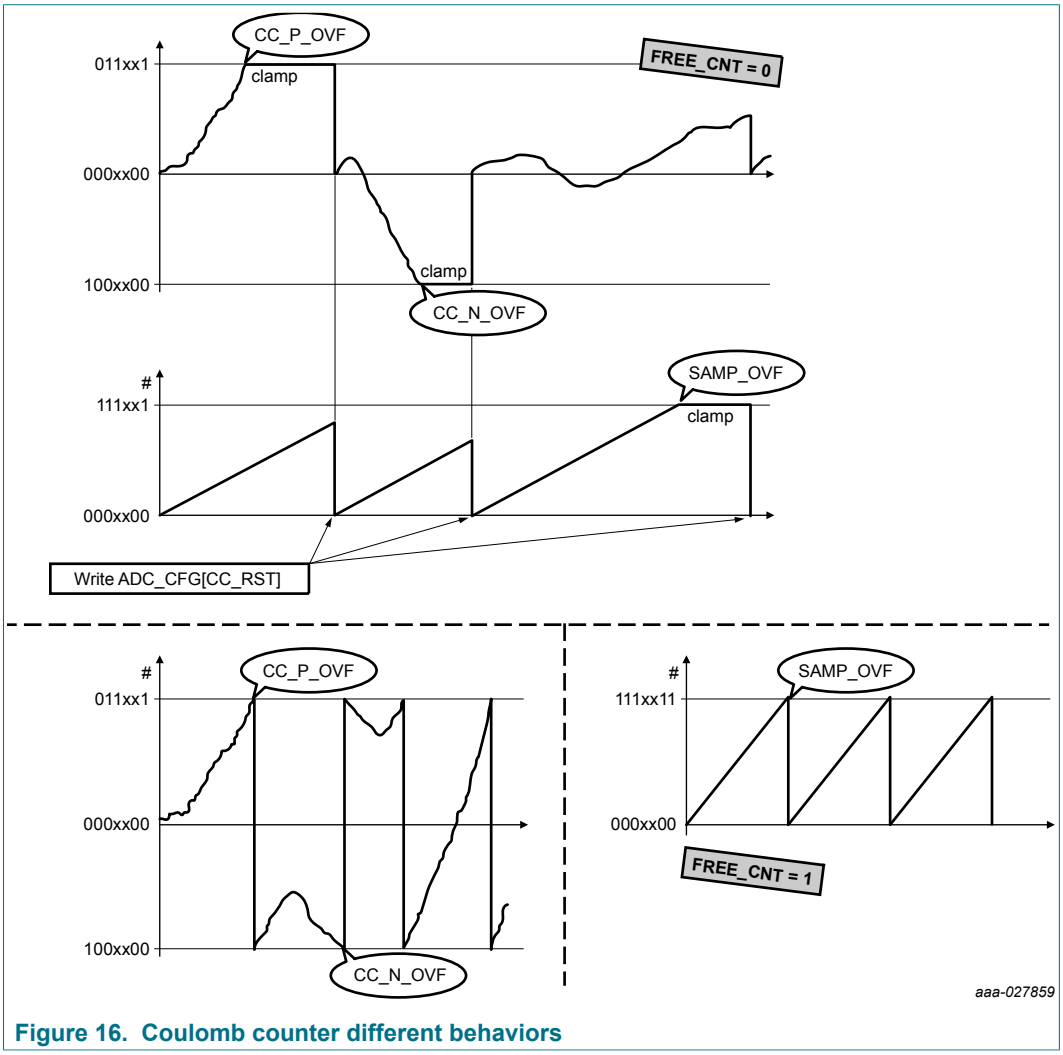


Figure 16. Coulomb counter different behaviors

The COULOMB_CNT is an integer whose associated resolution is V_{2RES}, therefore COULOMB_CNT·V_{2RES} gives µV. If the shunt resistance R_{SHUNT} is expressed in µΩ, then COULOMB_CNT·V_{2RES} / R_{SHUNT} gives µA.

The coulomb counting feature allows the pack controller to compute the average current. Value of R_{SHUNT} is only owned by the pack controller. By assuming two snapshots of the above mentioned registers are taken at two consecutive times T_{k-1} and T_k, the ratio $Iav_k = (ACC_k – ACC_{k-1}) / (N_k – N_{k-1})$ provides the average value of the current during the time interval $(T_k – T_{k-1})$, where ACC_k and ACC_{k-1} are the values of the quantity COULOMB_CNT·V_{2RES} / R_{SHUNT} respectively at times T_k and T_{k-1}, and N_k and N_{k-1} are the values of CC_NB_SAMPLES corresponding to the same two instants. To get an electric charge, the pack controller needs to multiply the ratio Iav_k by $(T_k – T_{k-1})$ to get an electric charge.

It is important to reset the whole coulomb counter status each time the type of input source is changed. In fact, the coulomb counter integrates not only the current signal, but also other possible diagnostic inputs (see Section 9.14 "Current measurement diagnostics").

Reading one of the three user registers COULOMB_CNT1, COULOMB_CNT2, and CC_NB_SAMPLES, triggers the 33771 to copy the content of the coulomb counter

internal registers into these three user registers. The content of the coulomb counter user registers is updated only when an address different from $2D, $2E, and $2F is read, and then one or more of the registers COULOMB_CNT1, COULOMB_CNT2, and CC_NB_SAMPLES are read again.

If the bit ADC2_OFFSET_COMP[CC_RST_CFG] is set to logic 1, reading any coulomb counter register (from @ $2D to @ $2F) also resets the coulomb counter.

The coulomb counter can behave in two different ways: clamping mode (by setting ADC2_OFFSET_COMP[FREE_CNT] = 0) and rollover mode (by setting ADC2_OFFSET_COMP[FREE_CNT] = 1): see Figure 16.

Flags ADC2_OFFSET_COMP[CC_P_OVF] and ADC2_OFFSET_COMP[CC_N_OVF] respectively signal an occurred overflow or an occurred underflow in the coulomb counter accumulator; they can be reset to zero by writing a logic 0 in those bits.

The flag ADC2_OFFSET_COMP[SAMP_OVF] signals an occurred overflow of the number of samples. It can be reset to zero by writing a Logic 0 in it. Any kind of occurring overflow is reflected in the content of the FAULT3_STATUS[CC_OVR_FLT] bit as well.

If ADC2 is enabled (SYS_CFG1[I_MEAS_EN] = 1) AND cyclic measurement is active (SYS_CFG1[CYCLIC_TIMER] ≠ 0), the coulomb counter is calculated also in sleep mode. If so, the ADC2 acquires four current samples in chopper mode, with the configured resolution (ADC_CFG[ADC2_DEF]) and a locked gain of 256 at the configured interval time of the cyclic timer (SYS_CFG1[CYCLIC_TIMR]). The resulting 2 dechopped values are averaged and the result is added to the accumulator whereby the sample counter is incremented by one.

If any fault condition occurs by these operations, depending on the fault and wake-up mask configuration, the device is awakened and the fault line is activated, including the case where the coulomb counter crosses the threshold TH_COULOMB_CNT, which is specific to sleep mode and produces the setting of both ADC2_OFFSET_COMP[CC_OVT] and FAULT3_STATUS[CC_OVR_FLT] bits.

When the device transitions from sleep mode to normal mode, the coulomb counter is frozen until it is read and reset by the user, and the acquisition speed is turned from the configured one (by the cyclic timer (SYS_CFG1[CYCLIC_TIMER]) to continuous.

TYPE A (free running mode with explicit reset):

CONFIGURATION instructions:

1. SYS_CFG1[IMEAS_EN] = 1; //Enable the current measurement
2. ADC2_OFFSET_COMP[FREE_CNT] = 1; // Select the free running mode
3. ADC2_OFFSET_COMP[CC_RST_CFG] = 0; // Do not reset to zero upon read:

RESET instructions:

1. write ADC_CFG[CC_RST] = 1; //Reset to zero:
2. COULOMB_CNT = COULOMB_CNT_old = CC_NB_SAMPLES_old = Time = Time_old = 0; // Variables initialization

NORMAL USE instructions:

1. Time = get_abs_time(); // get the absolute time
2. Read registers COULOMB_CNT1, COULOMB_CNT2 and CC_NB_SAMPLES;
3. COULOMB_CNT = (COULOMB_CNT1, COULOMB_CNT2); // concatenate MSB and LSB

4. I_AVG = (COULOMB_CNT - COULOMB_CNT_old)/(CC_NB_SAMPLES - CC_NB_SAMPLES_old); // this is average current
5. DELTA_Q = I_AVG * (Time – Time_old); // this delta charge may be accumulated in a different variable
6. COULOMB_CNT_old = COULOMB_CNT;
7. CC_NB_SAMPLES_old = CC_NB_SAMPLES;
8. Time_old = Time;
9. Read any register different from COULOMB_CNT1, COULOMB_CNT2 and CC_NB_SAMPLES
10. Jump to step 1

TYPE B (free running mode with implicit reset):

CONFIGURATION instructions:

1. SYS_CFG1[IMEAS_EN] = 1; // Enable the current measurement
2. ADC2_OFFSET_COMP[FREE_CNT] = 1; // Select the free running mode
3. ADC2_OFFSET_COMP[CC_RST_CFG] = 1; // Reset to zero upon read:

RESET instructions:

1. ADC_CFG[CC_RST] = 1; // Reset to zero
2. Time = Time_old = 0; // Variables initialization

NORMAL USE instructions:

1. Time = get_abs_time(); // get the absolute time
2. Read registers COULOMB_CNT1, COULOMB_CNT2 and CC_NB_SAMPLES;
3. COULOMB_CNT = (COULOMB_CNT1, COULOMB_CNT2); // concatenate MSB and LSB
4. I_AVG = COULOMB_CNT/CC_NB_SAMPLES; // this is average current
5. DELTA_Q = I_AVG *(Time-Time_old); // this delta charge may be accumulated in a different variable
6. Time_old = Time;
7. Read any register different from COULOMB_CNT1, COULOMB_CNT2 and CC_NB_SAMPLES
8. Jump to step 1

9.16 GPIOx port control and diagnostics

For user flexibility, the 33771 has seven GPIO to support overtemperature, undertemperature, temperature measurement, and general purpose digital I/O. All GPIOs may be individually configured as digital inputs or output ports, wake-up inputs, convert trigger inputs, ratiometric analog inputs with reference to VCOM, or analog inputs with absolute measurements. With the exception of the GPIO0, no external voltage has to be applied on GPIOx pins when the device is off or in sleep mode.

Table 16. GPIO port configurations

GPIO port	GPIO		Anx			ISENSE (diagnostic mode only)
	Standard GPIO	Wup and daisy chain	Convert trigger	Absolute	Ratiometric	
0	x	x		x	x	
1	x			x	x	
2	x		x	x	x	
3	x			x	x	
4	x			x	x	
5	x			x	x	x
6	x			x	x	x

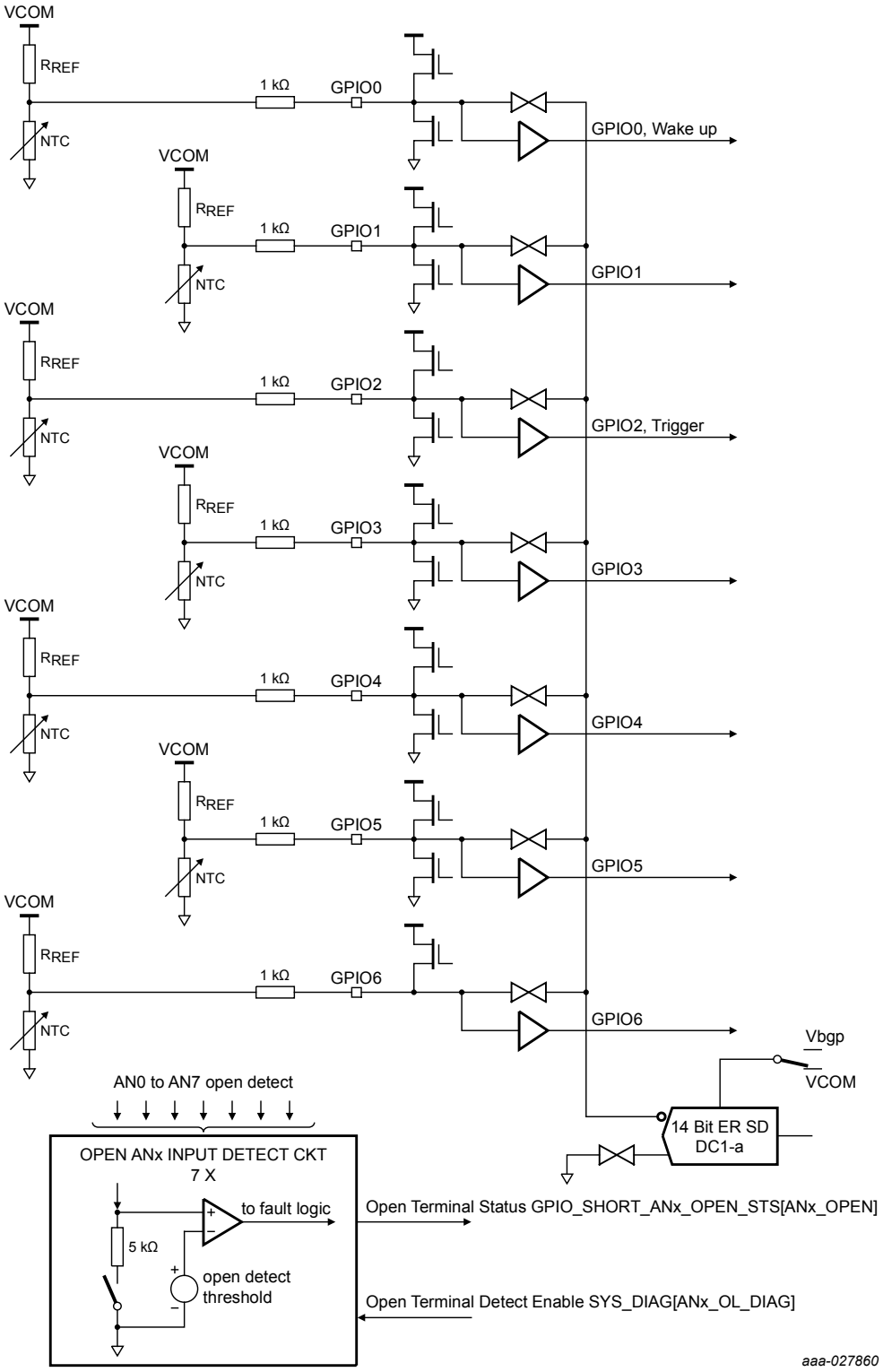


Figure 17. GPIO internal input structure

9.16.1 GPIOx used as digital I/O

Setting the GPIO_CFG1[GPIOx_CFG] bits to 10 or 11 configures the specific port as an input or output. Pins configured as outputs are driven high or low by writing to the GPIO_CFG2 register. Status of the ports, regardless of the digital configuration, is provided in the GPIO_STS register, which basically is a feedback of the actually commanded output.

Ports configured as GPIO outputs are diagnosed by the 33771. An output state GPIOx_ST[GPIOx_ST] which is opposite of the commanded state GPIOx_DR is considered to be shorted. Each short fault bit GPIOx_SH associated with each GPIOx is OR wired to the FAULT2_STATUS[GPIO_SHORT_FLT] bit. GPIO_SH bit when unmasked activates the FAULT pin.

9.16.2 GPIO0 used as wake-up input or fault pin activation input

Setting the GPIO_CFG1[GPIO0_CFG] bits to 10 is used to configure a GPIO0 port as an input. To program GPIO0 as wake-up input, the user must set the GPIO_CFG2[GPIO0_WU] bit to logic 1. In this case, the device performs a wake-up on the rising or falling edge.

By setting the GPIO_CFG2[GPIO0_FLT_ACT] to logic 1, the GPIO0 port may be used to activate the FAULT pin in normal, sleep, and diagnostic modes of operation. This feature allows the user to daisy chain the FAULT pin in high-voltage battery pack applications.

9.16.3 GPIO2 used as ADC trigger

The 33771 provides a convenient method to trigger an ADC conversion from an external digital source. To use GPIO2 as an ADC trigger, configure the port as a digital input through the setting GPIO_CFG1[GPIO2_CFG] = 10 and enable the trigger through the setting GPIO_CFG2[GPIO2_SOC] = 1. With the port configured, positive edge events on GPIO_CFG2[GPIO2_SOC] triggers a start of conversion sequence.

With a GPIO2 trigger, the converter operates as programmed in the ADC_CFG[SOC] bit. The tag associated with the GPIO2 trigger is taken from the programmed value in the ADC_CFG[TAG_ID] register field. The GPIO2 convert trigger feature is not available in sleep mode.

9.16.4 GPIOx used as analog

Setting the GPIO_CFG1[GPIOx_CFG] bits to 00 or 01 configures the specific port as an analog ratiometric input or single ended. GPIOs configured as analog inputs are usually used for temperature measurement. Using the digital result for temperature the 33771 may be programmed to detect overtemperature and undertemperature.

To detect overtemperature and undertemperature, the generated digital value is compared to an individually programmed threshold in the TH_ANx_OT and TH_ANx_UT registers. ADC1-A results on any temperature measurement input which exceed the threshold activates the FAULT1_STATUS[AN_OT_FLT,AN_UT_FLT] bit. The conversion results for the analog inputs are available in MEAS_ANx register for the pack controller to read.

9.16.5 GPIO5, GPIO6 used as ISENSE

To use GPIO5 and GPIO6 as inputs to the current sense PGA, the 33771 must be in diagnostic mode. As a redundant method of measuring current for functional verification, the user may connect input ports 5 and 6 as inputs to the positive and negative inputs of the PGA, that is, GPIO5 plays the role of ISENSE+ and GPIO6 plays the role of ISENSE–.

Customers using GPIO5 and GPIO6 as a redundant current measurement in diagnostic mode must command GPIO5 and GPIO6 to digital inputs by setting GPIO_CFG1[GPIO5_CFG] = 10 and GPIO_CFG1[GPIO6_CFG] = 10.

9.16.6 GPIOx OT/UT functional verification

Overtemperature and undertemperature functional verification is performed in diagnostic mode only. With OT/UT thresholds programmed, use the following sequence to functionally verify overtemperature:

1. Write SYS_CFG1[GO2DIAG] bit to logic 1 to enter diagnostic mode.
2. Optionally program GPIOx to be tested as analog through GPIO_CFG1[GPIOx_CFG] register.
3. Set GPIO_CFG2[GPIOx_DR] register to drive output for overtemperature or undertemperature.
4. Enable the GPIOx output buffer through the SYS_DIAG[ANx_TEMP_DIAG].
5. Request the 33771 to perform a conversion sequence by writing to ADC_CFG register.
6. Conversions below the TH_ANx_OT threshold trigger the ANx_OT fault bit. Conversions above the TH_ANx_UT threshold trigger the ANx_UT fault bit.
7. Exit diagnostic mode by setting SYS_CFG1[GO2DIAG] bit to logic 0.

Note: *In diagnostic mode, only GPIOx configured as analog inputs have buffers activated by the ANx_TEMP_DIAG bit.*

9.16.7 GPIOx open terminal diagnostics

To detect open terminals on the GPIO pins, a weak internal pull-down is commanded on and off. Voltages below the VOL(TH) threshold are considered open terminals.

To perform open terminal detection, perform the following sequence:

1. Enter diagnostic mode.
2. Program GPIOx to be tested as analog input through GPIO_CFG1[GPIOx_CFG] bits.
3. Activate GPIOx weak pull down through the SYS_DIAG[ANx_OL_DIAG].
4. Voltages below the VOL(TH) threshold set the GPIO_SHORT_ANx_OPEN_STS[ANx_OPEN] bit and the FAULT2_STATUS[AN_OPEN_FLT] fault bit.
5. Exit diagnostic mode.

Note: *In diagnostic mode, only GPIOx configured analog have a weak pull down activated by the ANx_OL_DIAG bit.*

9.17 Cell balance control

The 33771 features fully protected integrated cell balancing drivers with fault diagnostics. The cell balancing feature is active in normal, sleep and diagnostic modes. The 33771 contains registers to control and monitor cell balance drivers and cell balance fault status.

The SYS_CFG1 register contains the CB_DRVEN bit. The CB_DRVEN bit must be enabled for any of the drivers to be activated. All drivers are disabled when CB_DRVEN bit is logic 0. For cell balance drivers to be active, both the SYS_CFG1[CB_DRVEN] AND the CBx_CFG[CB_EN] bits must be set to logic 1.

The individual cell balance timer is set through the CBx_CFG[CB_TIMER]. Timing parameters can be found in the register map of this specification. Each time the cell balance CBx_CFG[CB_TIMER] bit is written by the MCU controller, the 33771 initiates the cell balance timer. It is important to explicitly mention, each time the CB_DRVEN bit is set to logic 0, then cell balancing timers get reset to 0 and all cell balancing MOSFETs are turned off. Even though the CB_DRVEN bit is set again to logic 1, all CBx_CFG registers must be rewritten in order to restart the cell balancing.

The SYS_CFG1 register contains the CB_AUTO_PAUSE bit which instructs the 33771 to temporarily disable the cell balance switch during ADC1-A and ADC1-B cyclic conversions. The SYS_CFG1 register contains the CB_MANUAL_PAUSE bit, which, if set to logic 1, instructs the 33771 to disable the cell balance switches during ADC1-A and ADC1-B on demand conversions. When the CB_MANUAL_PAUSE bit is set again to logic 0, the cell balance switches are restored according to the programming. However, the cell balance timers are not frozen during a manual pause.

9.18 Cell balance fault diagnostics

Cell balance short detection is a continuous process performed in all modes of operation (normal, sleep, diagnostic), when the output driver is enabled. Open load fault detection is only performed in diagnostic mode. To detect open load on the cell balance terminals, a R_{PD_CB} resistor is applied between the CB_X outputs and their common terminal. In diagnostic mode, CB_x voltages below the VOUT(FLT_TH) activate the CB_OPEN_FLT register bits.

The following sequence is used to determine open load condition on each CB_X inputs:

1. Write SYS_CFG1[GO2DIAG] bit to logic 1 to enter diagnostic mode.
2. If the number of cells on the cluster is odd, then write the bit SYS_CFG2[NUMB_ODD] to logic 1, else write it to logic 0.
3. Command the cell balance outputs OFF by setting SYS_CFG1[CB_MANUAL_PAUSE] to logic 1.
4. Command the SYS_DIAG[CB_OL_ODD,CB_OL_EVEN] field to the 10 configuration.
5. Wait for the time delay t_{delay}.
6. Read the CB_OPEN_FLT register to determine all CBx_OPEN_ FLT open load fault bits.
7. Command the SYS_DIAG[CB_OL_ODD,CB_OL_EVEN] field to the 01 configuration.
8. Wait for the time delay t_{delay}.
9. Read the CB_OPEN_FLT register to determine all CBx_OPEN_ FLT open load fault bits.
10. Restore the cell balance outputs by setting SYS_CFG1[CB_MANUAL_PAUSE] to logic 0.

11.Exit diagnostic mode by setting SYS_CFG1[GO2DIAG] bit to logic 0.

Note: *Exit from diagnostic mode automatically deactivates all cell balance open load detect switches.*

Note: *Even though it has not been explicitly stated in the procedure, it is recommended to cancel cell balancing faults after terminating the procedure.*

Note: t_{delay} *= 100 µs*

Cell balance short detection is diagnosed with the cell balance FET active. In the event of a shorted load, the CB_SHORT_FLT[CBx_SHORT_FLT] is set. When a shorted load is detected, the driver is immediately commanded off. To reactivate the output, the MCU controller must command the driver on again. The shorted load fault remains at logic 1 until cleared by writing logic 0 to the CB_SHORT_FLT register.

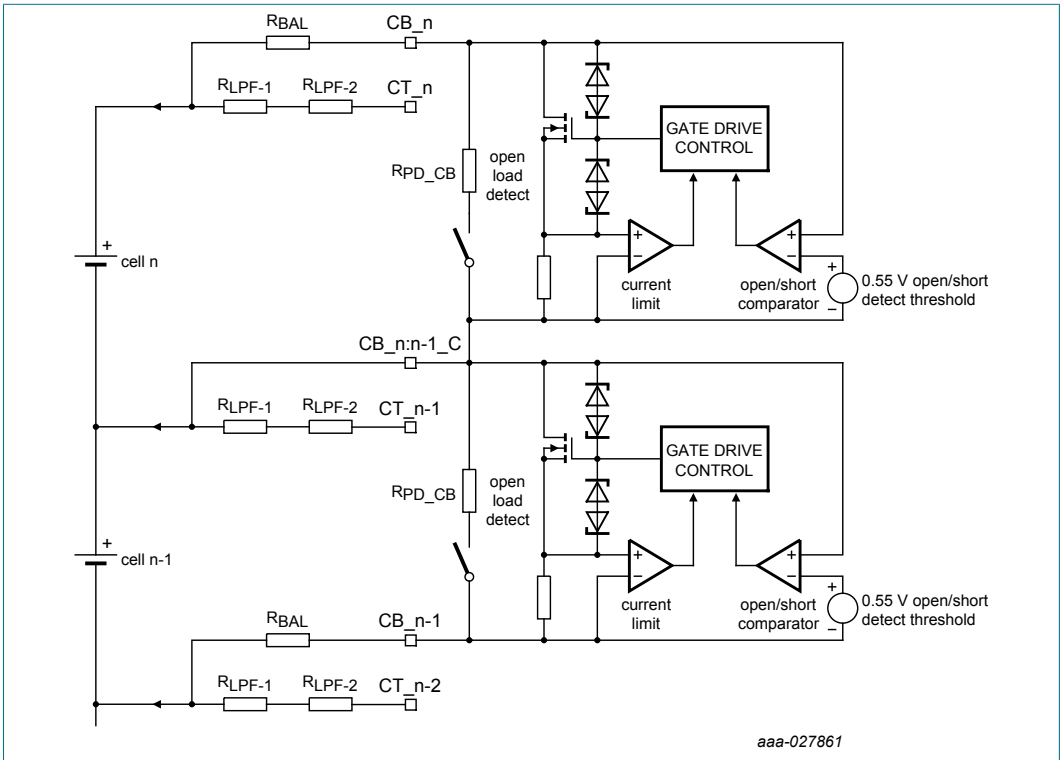


Figure 18. Cell balance driver internal block diagram

Cell balance diagnostic switches are managed at the same way as cell terminal diagnostic switches.

Table 17. CB diagnostic switches operation

SYS_CFG2 [NUMB_ODD]	SYS_DIAG [CT_OL_ODD,CT_OL_EVEN]	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8...13	SW14
0	01	open	closed	open	closed	open	closed	open	...	closed
	10	closed	open	closed	open	closed	open	closed	...	open
1	01	open	closed	open	closed	open	open	closed	...	open
	10	closed	open	closed	open	closed	closed	open	...	closed

9.19 Oscillator frequency monitor

The 33771 has been designed with a clock monitoring feature for the internal low frequency clock. After the 33771 has been initialized, the clock monitoring feature monitors each clock cycle for a low to high transition.

In the event the low frequency clock fails, the 33771 is programmed to activate the FAULT pin. The user may disable the clock monitoring feature to conserve current while the device is in sleep mode. To disable the oscillator monitor in sleep mode, the user has to set the SYS_CFG2 [FLT_RST_CFG] field correctly. To mask the oscillator monitor from activating the fault pin, set the FAULT_ MASK2[MASK_2_F] bit to 1.

Note: *Disabling the clock monitoring feature or masking the failure from the FAULT pin is not recommended.*

9.20 Internal IC temperature

Internal temperature measurement is completed automatically during each ADC conversion sequence. The MEAS_IC_TEMP register containing the IC temperature measurement may be read at any time by the pack controller. Resolution of MEAS_IC_TEMP is 32 mK/LSB.

9.21 Internal temperature fault

In addition to the digital temperature measurement register, the 33771 is equipped with a silicon overtemperature thermal shutdown (TSD). In the event the silicon thermal shutdown is activated in normal mode, the 33771 halts all monitoring operations and enters a low-power state with the FAULT pin activated. When the die temperature returns to normal, the 33771 resumes operation in normal mode.

In the event of an internal TSD:

1. Conversion sequence is aborted and the 33771 stops converting.
2. The FAULT2_STATUS[IC_TSD_FLT] bit is set.
3. VCOM and VANA are in shut down, communication gets blocked.
4. All cell balance switches are disabled and CB_DRVEN cleared.

When the die temperature returns to normal level, the 33771 resumes normal mode operation with cell balancing disabled.

Overtemperature TSD events are also detected while the 33771 is in sleep mode during cyclic measurements. TSD events detected during the sleep mode cyclic measurement force the 33771 to set the IC_TSD_FLT bit and activate the FAULT pin while remaining in sleep mode. When the 33771 returns to normal operating temperature it transfers to normal mode and initiates a wake-up sequence on the bus.

9.22 Storage of parameters in an optional EEPROM

NXP provides parts with optimal calibration values. Standard parameters are stored in a read only memory called fuses cell array. It is typically neither necessary nor advised to change the standard values. Nevertheless, sometimes this might be required. An example is adjusting the gain calibration of the current channel to take into account the behavior of the external shunt resistor, due to the temperature coefficient and individual resistance deviation from the nominal value. New gains may be determined in normal

mode and then stored in an external EEPROM. In such cases, EEPROM calibration parameters must be programmed at the manufacturer's assembly and final test.

If the 33771 is linked to an EEPROM, the latter device is automatically recognized, provided the address $00 of the EEPROM contains the proper one byte key value, namely $CB hex. To program the EEPROM with calibration parameters, the user's final test and assembly must write to the EEPROM_CTRL register. The user must simply send the write command with the EEPROM address and data to be written, and set the write bit to logic 0. The 33771 automatically writes the data to the given EEPROM address. To read data from the EEPROM, the user has to first send a write command with the EEPROM address and set the Write bit to logic 1, then send a read command to access the data.

Each time the part experiments a power up or reset event, an internal R/W memory, which is referred to as mirror memory, is first of all uploaded with the value of the fuses cell array. The content of such memory is propagated to the applicative part of the chip. All calibration values, before being used in the IC, are protected by an ECC (Hamming error-correction code). But if an EEPROM is recognized, the mirror registers bank, in which the content of the fuses memory was stored at the very beginning of the initialization process (transparent to the user), gets automatically reloaded with the content of the EEPROM.

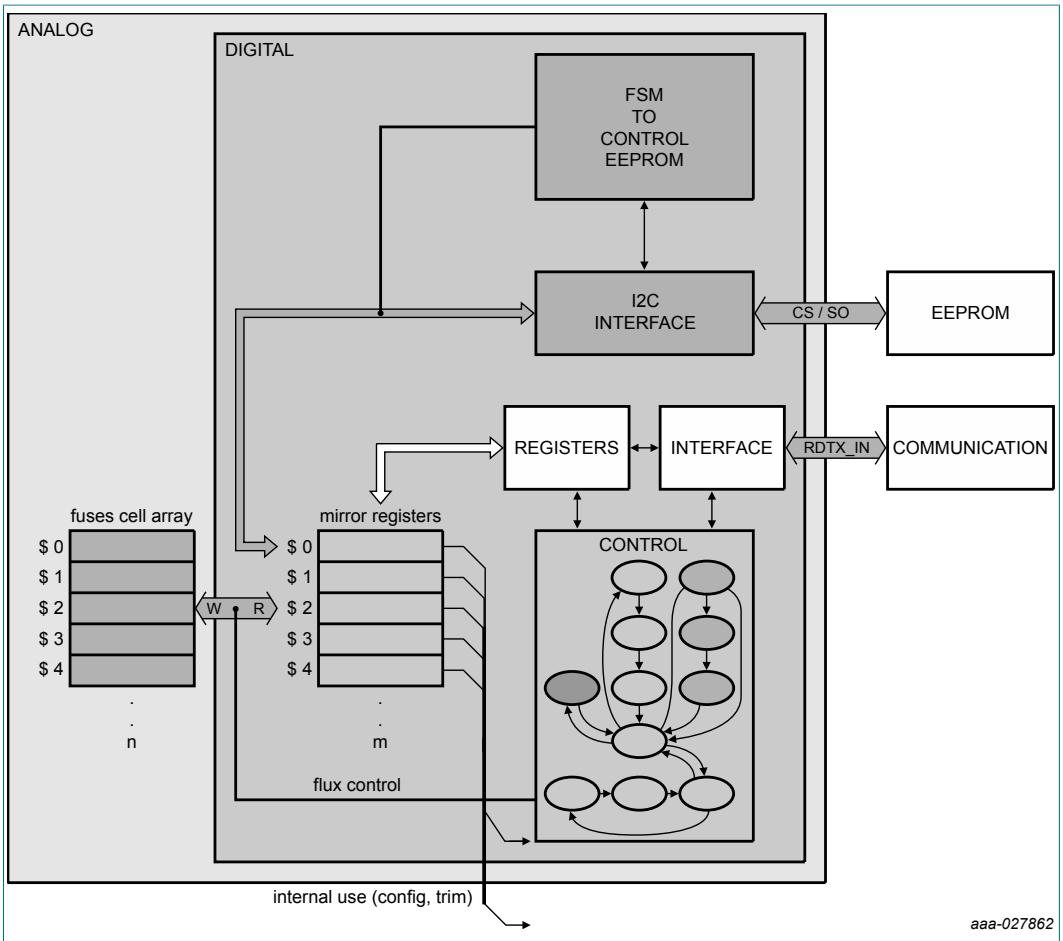


Figure 19. Memories

The space of EEPROM-addresses and the space of mirror-addresses correlate to each other. Mirror data are organized in 16 bit words, while the data of the EEPROM have

been thought as bytes. As at EEPROM-address $00 there is the key value, the first calibration byte of the EEPROM must have EEPROM-address $01 and corresponds to the most significant byte of the mirror word having mirror-address $00. The second calibration byte of the EEPROM must have EEPROM-address $02 and corresponds to the least significant byte of the mirror word still having mirror-address $00, and so on.

To understand the meaning of calibrations, it is necessary to explain how they are used. This can be seen in Table 19. The columns labeled as "Gain comp.?" and "by …" show if the input signals are gain compensated (yes/no) and by which gain. For instance, GCF_c1 stays for a gain which may be calculated by using GCF_room_c1, GCF_hot_c1 and GCF_cold_c1 variables specified in Table 94. In this table, attributes "cold" and "hot" refer to extreme temperatures, and attribute room refers to 25 °C. A gain may or may not depend on the temperature (column "Temp. comp.?" may attain the value yes or no). If a gain depends on the IC temperature, there are three scalar gains: for instance, gain_cold_a, acq_gain_a, gain_hot_a represent respectively the values at cold (typ. −40 °C) room (typ. +25 °C) and hot (typ. +125 °C) temperature of the die. They are used to calculate, by interpolation, the actual value of gain_a at any temperature. ADC2 works with GCF_ix (x= 4, 16, 64, 256), depending on the current gain used by the PGA. See Table 94. The value of a gain is centered on the unity, so it is of the form 1 + DG. Therefore DG is centered on zero and is represented in two's complement. In the IC, only the DG part of the gain needs to be stored. See Table 18.

Even if the most typical usage of the EEPROM is as storage of gains, nothing prevents the user to use it as a generic information storage. If this is the case, the first portion of the EEPROM has to be reserved to the copy of all gains, even if this is identical to the content of the fuse memory.

Table 18. Gain format

Gain = 1 + DG	Representation: 2's complement	Min.	Max.	Resolution
DG	**Number of bits**	**Percentage**	**Percentage**	**Percentage**
GFC_cx (cell voltage)	10	−6.2500 %	6.2378 %	0.01221 %
GCF_Vbgtj1-2 (diagnostic voltage reference)	8	−3.1250 %	3.1006 %	0.02441 %
GCF_i4-256 (current)	9	−25.0000 %	24.9023 %	0.09766 %
GCF_stack (Stack voltage)	7	−3.1250 %	3.0762 %	0.04883 %
GCF_ANx_ratio (ANx ratio)	5	−1.5625 %	1.4648 %	0.09766 %
GCF_IcTemp (IC temperature)	4	−3.1250 %	2.7344 %	0.39063 %

Table 19. Gain compensation

Measured channel	#	Offset comp.?	Gain comp.? By...		Temp. comp. ?	Result stored in…	…checked by…	… in the range of	
By ADC1-A									
ICTEMP1	1	Chopper	Yes	GCF_IcTemp	No	MEAS_IC_TEMP	N/A	N/A	N/A
ICTEMP1	2	Chopper	Yes	GCF_IcTemp	No	MEAS_IC_TEMP	N/A	N/A	N/A
CT1	3	Yes	Yes	GCF_c1	Yes	MEAS_CELL1	IC	CT1_UV_TH	CT1_OV_TH
CT2	4	Yes	Yes	GCF_c2	Yes	MEAS_CELL2	IC	CT2_UV_TH	CT1_OV_TH
CT3	5	Yes	Yes	GCF_c3	Yes	MEAS_CELL3	IC	CT3_UV_TH	CT1_OV_TH
CT4	6	Yes	Yes	GCF_c4	Yes	MEAS_CELL4	IC	CT4_UV_TH	CT1_OV_TH

Measured channel	#	Offset comp.?	Gain comp.? By...		Temp. comp. ?	Result stored in…	…checked by…	… in the range of	
CT5	7	Yes	Yes	GCF_c5	Yes	MEAS_CELL5	IC	CT5_UV_TH	CT1_OV_TH
CT6	8	Yes	Yes	GCF_c6	Yes	MEAS_CELL6	IC	CT6_UV_TH	CT1_OV_TH
AN0	9	Yes	Yes	GCF_ANx_ratio [1]	No [1]	MEAS_AN0	IC	AN0_UT_TH	AN0_OT_TH
AN1	10	Yes	Yes	GCF_ANx_ratio [1]	No [1]	MEAS_AN1	IC	AN1_UT_TH	AN1_OT_TH
AN2	11	Yes	Yes	GCF_ANx_ratio [1]	No [1]	MEAS_AN2	IC	AN2_UT_TH	AN2_OT_TH
AN3	12	Yes	Yes	GCF_ANx_ratio [1]	No [1]	MEAS_AN3	IC	AN3_UT_TH	AN3_OT_TH
AN4	13	Yes	Yes	GCF_ANx_ratio [1]	No [1]	MEAS_AN4	IC	AN4_UT_TH	AN4_OT_TH
AN5	14	Yes	Yes	GCF_ANx_ratio [1]	No [1]	MEAS_AN5	IC	AN5_UT_TH	AN5_OT_TH
AN6	15	Yes	Yes	GCF_ANx_ratio [1]	No [1]	MEAS_AN6	IC	AN6_UT_TH	AN6_OT_TH
V_{BG_TJ}	16	Yes	Yes	GCF_Vbgtj1	Yes	MEAS_VBG_DIAG_ADC1A	IC	thresholds vs. fuse_bg_ti	
Reserved	17	No	Yes	N/A	Yes	ADC1_A_RESULT	N/A	N/A	N/A
Reserved	18	No	Yes	N/A	Yes	ADC1_A_RESULT	N/A	N/A	N/A
Reserved	19	No	Yes	N/A	Yes	ADC1_A_RESULT	N/A	N/A	N/A
Reserved	20	No	Yes	N/A	Yes	ADC1_A_RESULT	N/A	N/A	N/A
By ADC1-B									
CT7	1	Yes	Yes	GCF_c7	Yes	MEAS_CELL7	IC	CT7_UV_TH	CT7_OV_TH
CT8	2	Yes	Yes	GCF_c8	Yes	MEAS_CELL8	IC	CT8_UV_TH	CT8_OV_TH
CT9	3	Yes	Yes	GCF_c9	Yes	MEAS_CELL9	IC	CT9_UV_TH	CT9_OV_TH
CT10	4	Yes	Yes	GCF_c10	Yes	MEAS_CELL10	IC	CT10_UV_TH	CT10_OV_TH
CT11	5	Yes	Yes	GCF_c11	Yes	MEAS_CELL11	IC	CT11_UV_TH	CT11_OV_TH
CT12	6	Yes	Yes	GCF_c12	Yes	MEAS_CELL12	IC	CT12_UV_TH	CT12_OV_TH
CT13	7	Yes	Yes	GCF_c13	Yes	MEAS_CELL13	IC	CT13_UV_TH	CT13_OV_TH
CT14	8	Yes	Yes	GCF_c14	Yes	MEAS_CELL14	IC	CT14_UV_TH	CT14_OV_TH
Stack	9	Chopper	Yes	GCF_stack	No	MEAS_STACK	N/A	N/A	N/A
Stack	10	Chopper	Yes	GCF_stack	No	MEAS_STACK	N/A	N/A	N/A
Reserved	11	No	Yes	N/A	Yes	ADC1_B_RESULT	N/A	N/A	N/A
VANA	12	Yes	Yes	GCF_c1	Yes	ADC1_B_RESULT	IC	N/A	VANA_OV_TH
V_{BG_TJ}	13	Yes	Yes	GCF_Vbgtj2	Yes	MEAS_VBG_DIAG_ADC1B	IC	thresholds vs. fuse_bg_ti	
Reserved	14	No	Yes	N/A	Yes	ADC1_B_RESULT	N/A	N/A	N/A
Reserved	15	No	Yes	N/A	Yes	ADC1_B_RESULT	N/A	N/A	N/A
Reserved	16	No	Yes	N/A	Yes	ADC1_B_RESULT	N/A	N/A	N/A
Reserved	17	No	Yes	N/A	Yes	ADC1_B_RESULT	N/A	N/A	N/A
By ADC2									
ISENSE	1	Yes	Yes	GCF_i4-256	Yes	MEAS_I	IC	N/A	TH_ISENSE_H
ISENSE	2	Yes	Yes	GCF_i4-256	Yes	MEAS_I	IC	N/A	TH_ISENSE_H

[1] It is assumed that all ANx have been programmed as ratiometric; in case a certain ANx is programmed as an absolute input, the gain GCF_ANx_ratio gets replaced by GFC_c1 and the 'No' value contained in the column labeled 'Temp. comp. ?' is replaced by a 'Yes'.

9.22.1 Gain correction of the current channel

The following is a detailed explanation of the gain correction of the current channel.

- Room temperature delta gains:
  GCF_ix (for x = 4, 16, 64, 256 representing all possible PGA gains) with resolution 0.09765625 %, spanning the range (-256…+255)·0.09765625 %
- Cold temperature delta gains:
  GCF_cold_ix (for x = 4, 16, 64, 256 representing all possible PGA gains) with resolution 0.09765625 %, spanning the range (-16…+15)·0.09765625 %
- Hot temperature delta gains:
  GCF_hot_ix (for x = 4, 16, 64, 256 representing all possible PGA gains) with resolution 0.09765625 %, spanning the range (-16…+15)·0.09765625 %

In contrast to i_gain_x, which is represented by a 9 bit word, GCF_hot_ix and GCF_cold_ix are represented by a reduced number of bits (5) and therefore their range is 16 times smaller than the one at room temperature, since the resolution is the same for all gains. Basically GCF_hot_ix and GCF_cold_ix can only additively correct the i_gain_x respectively in hot and cold conditions. This becomes clear by considering the gain temperature dependency, which is as follows:

If (temperature T is higher than T_room) Then // T is the IC temperature

gain_selected = GCF_hot_ix

Else

gain_selected = GCF_cold_ix

EndIf

DG = GCF_ix + (gain_selected * k(T)) // where k(T) is a stored function, such that: 0 ≤ k(T) ≤ 1, k(T_room) = 0 and k(T_cold) = k(T_hot) = 1

Gain = 1 + DG

If there is an EEPROM containing the equivalent of the fuse memory, some ECC bits are needed to protect them, as in the standard case of the fuse memory. The customized values and their own ECC values are completely independent on the NXP basic calibrations and their specific ECC stored in the fuses. Therefore, the user has to evaluate new ECC bits starting from its own calibration data and, finally, save both in the EEPROM.

There is a special calculation sheet the customer has to request NXP to get the correct values for DED_ENCODE_2 and DED_ENCODE_1 information, that is, ECC words used in the 33771 to detect a single error in the data and to correct it. In case of a double error, the problem can only be detected. However, in the normal usage, the SYS_CFG2[HAMM_ENCOD] bit has to be set at logic 0. For safety reasons, it is recommended the value of such bit is periodically checked to be at logic 0. If the bit is not at logic 0, then it must be written at logic 0 again.

9.23 Mirror memory access

The mirror memory can be changed by using the FUSE_MIRROR_DATA and FUSE_MIRROR_CNTL general registers. The former contains the value of the data to be written into the mirror or to be read from it, while the latter contains the data address FMR_ADDR (whose value is in the range 0 to 31 decimal), some control fields (FSTM and FST) and a read only information about a possibly occurred detection and correction of data values (SEC_ERR_FLT).

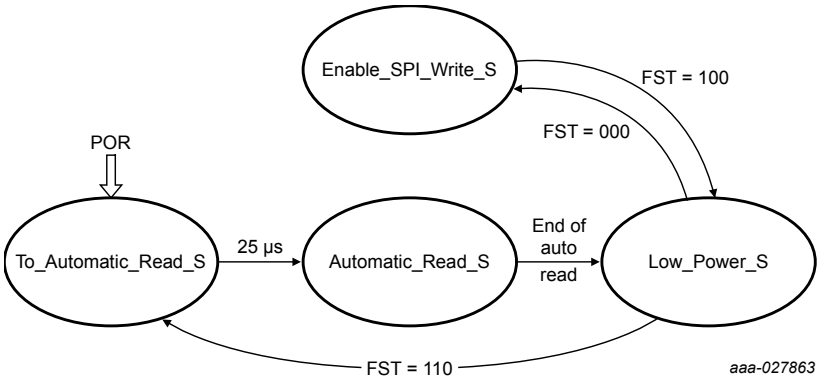


Figure 20. Mirror memory control

To manage the mirror memory the FSM of Figure 20 must be used.

Meaning of the states:

- To_Automatic_Read_S: transient state for slightly delaying the automatic read
- Automatic_Read_S: in this state the whole bank of fuses is automatically read
- Low_Power_S: low power state; it must be the initial and final state of a sequence of write operations
- Enable_SPI_Write_S: state allows writing into the mirror

Table 20. Sequence of read operations

Type of command	FSTM	FSM	FMR_ADDR	FUSE_MIRROR_DATA
FUSE_MIRROR_CNTL[FMR_ADDR] set	0	000	00000	X
FUSE_MIRROR_DATA	X	X	X	data read at addr $0
FUSE_MIRROR_CNTL[FMR_ADDR] set	0	000	00001	X
FUSE_MIRROR_DATA	X	X	X	data read at addr $1
FUSE_MIRROR_CNTL[FMR_ADDR] set	0	000	00010	X
FUSE_MIRROR_DATA read	X	X	X	data read at addr $2

The read sequence may be useful, for example when the user wants to read the traceability information (serial number) contained in some specific words of the mirror memory (see Table 41 and Table 94).

Table 21. Sequence of write operations

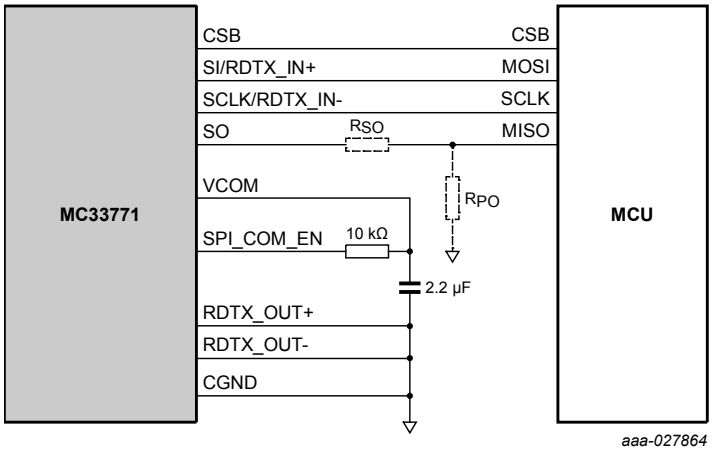
Type of command	FSTM	FSM	FMR_ADDR	FUSE_MIRROR_DATA
FUSE_MIRROR_CNTL to enable writing	1	000	00000	X
FUSE_MIRROR_CNTL[FMR_ADDR] at $0	1	000	00000	X
FUSE_MIRROR_DATA	X	X	X	Data to be written at addr $0
FUSE_MIRROR_CNTL[FMR_ADDR] at $1	1	000	00001	X
FUSE_MIRROR_DATA	X	X	X	Data to be written at addr $1
FUSE_MIRROR_CNTL[FMR_ADDR] at $2	1	000	00010	X
FUSE_MIRROR_DATA	X	X	X	Data to be written at addr $2
FUSE_MIRROR_CNTL to low power	1	100	X	X

10 Communication

The 33771 is designed to support serial peripheral interface (SPI) or transformer communication. SPI communication uses the standard CSB to select the 33771 and clocks data in and out using SCLK/RDTX_IN−, SI, and SO. Using SPI to communicate to the 33771, provides system isolation when used in conjunction with galvanic isolators. Serial communication is enabled using the SPI_COM_EN pin. To select SPI communication, the SPI_COM_EN pin must be terminated to the VCOM supply. Terminating the SPI_COM_EN pin to CGND pin selects transformer communication. Systems using only SPI communication to the 33771 may leave RDTX_OUT+ and RDTX_OUT– unterminated or may short them to ground.

Note: *The 33771 supports only one communication method at a time and is determined by the state of SPI_COM_EN pin. Changing the state of the SPI_COM_EN pin after POR and VCOM is in regulation is considered a communication fault, and sets the COM_LOSS_FLT bit. The 33771 remains in same configuration determined at POR.*

10.1 SPI communication



In the presence of 3.3 V SPI interface, resistors represented by a dotted line should have R_{SO} = 5.23 kΩ and R_{PO} = 10 kΩ. For a 5.0 V SPI interface, it must be R_{SO} = 0 kΩ (short) and R_{SO} = ∞ kΩ (open).

Figure 21. SPI interface termination

SPI input signal levels to the 33771 operate at 5.0 V logic levels but are 3.3 V compatible.

The SO output driver provides 5.0 V levels only and therefore must be attenuated to be compatible with a 3.3 V MCU.

The 33771 SPI interface is a standard SPI interface with a chip select (CSB), clock (SCLK/RDTX_IN–), master in slave out (MISO), and master out slave in (MOSI). The SI/SO shifting of the data follows a first-in-first-out protocol, with both input and output words transferring the most significant bit (MSB) first. All SPI communication to the 33771 is controlled by the microcontroller.

One 40-bit register of previously requested data is retrieved through serial out for each current serial in message sent by the MCU. For message integrity and communication robustness, each SPI transmit message consists of six fields containing 40 bits. The six transmit fields are defined as following:

1. Cyclical redundancy check (8 bits)
2. Command field (4 bits)
3. Cluster ID field (4 bits)
4. Memory address field (7 bits)
5. Master/slave field (1 bit)
6. Memory data field (16 bits)

Messages having less or more than 40 bits, incorrect CRC, or incorrect SCLK/RDTX_IN– phase are disregarded. Communication faults set the COM_ERR_FLT fault bit in the FAULT1_STATUS register and increments the COM_STATUS[COM_ERR_COUNT] register.

Note: *It is required that the SCLK/RDTX_IN– input is low before the falling edge of CSB (SCLK/RDTX_IN– phase).*

Table 22. SPI transmit format

Memory data	Master/slave	Memory address	Device address (cluster ID)	Command				CRC
Bit[39:24]	Bit[23]	Bit[22:16]	Bit[15:12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]	Bit[7:0]

Information is transferred to and from the 33771 through the read and write commands. On power-up (POR) or RESET (pin) or SYS_CFG1[SOFT_RST], the 33771 device only responds to the cluster ID of 0000. The user must change the cluster ID of the device by writing a new cluster ID into register INIT[CID]. Subsequent read/write command must use the new cluster ID to communicate to the device. Whatever the type of transmitted message, the master has to write a logic 0 in the master/slave bit. The 33771 ignores messages having the master/slave bit at logic 1.

Note: *In SPI communication, global write commands are not allowed and the 33771 responds with an all zero message with the correct CRC in the subsequent message frame.*

Note: *In SPI communication, the 33771 responds with all zero and the correct CRC to the very first 33771/ MCU message frame.*

The response structure is similar to the transmit structure and includes the 4-bit TAG ID provided by the MCU master after writing the ADC_CFG register. Reading registers which are linked to the measurements (addresses $2D to $4A) or to the diagnostic state (SYS_DIAG, FAULT1_STATUS, FAULT2_STATUS and FAULT3_STATUS) results in responses, which have in the TAG ID field of the frame, the same TAG ID value sent in the write command instructing the 33771 to perform data conversion. In all other cases, the command field of a response frame carries the 2-bit RC field (see Table 28 in contrast to Table 29).

1. Cyclic redundancy check CRC (8 bits)
2. Tag ID field (4 bits)
3. Physical Address (4 bits)
4. Memory address – corresponds to cell ID (7 bits)
5. Master/slave field (1 bit)
6. Data field (16 bits)

Table 23. SPI response format

Memory data	Master/slave	Memory address	Device address (cluster ID)	Command				CRC
Bit[39:24]	Bit[23]	Bit[22:16]	Bit[15:12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]	Bit[7:0]

To initiate communication, the MCU transitions CSB from high to low. The data from the MCU is sent with the most significant bit first. The SI data is latched by the device on the falling edge of SCLK/RDTX_IN–. Data on SO is changed on rising edge of SCLK/RDTX_IN– and read by MCU on falling edge of SCLK/RDTX_IN–. The SO response message is dependent on the previous state command.

Falling edge of CSB initiates the following:

1. Enables the SI Input
2. Enables the SO output driver

Rising edge of CSB initiates the following operation:

1. Disables the SO driver (high-impedance)
2. Activates the received 40 bit command word allowing the 33771 to act upon the new command

Note: *The 33771 responds to a NO_OPERATION command with an echo of the command in the subsequent response.*

Note: *After initialization, when writing to a register, the 33771 responds with an echo of the written data.*

Note: *The 33771 does not execute a write command if the master/slave bit is equal to logic 1.*

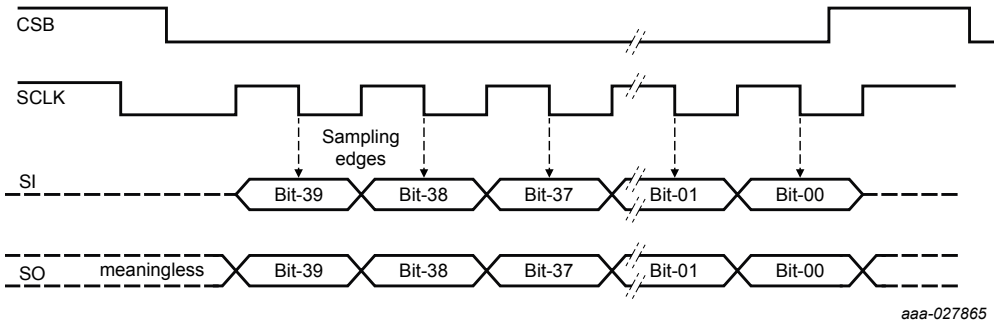


Figure 22. SPI transmission

10.2 TPL communication

High speed differential isolated communication is achieved through the use of pulse transformers. Terminating the SPI_COM_EN pin to the CGND pin selects transformer communication.

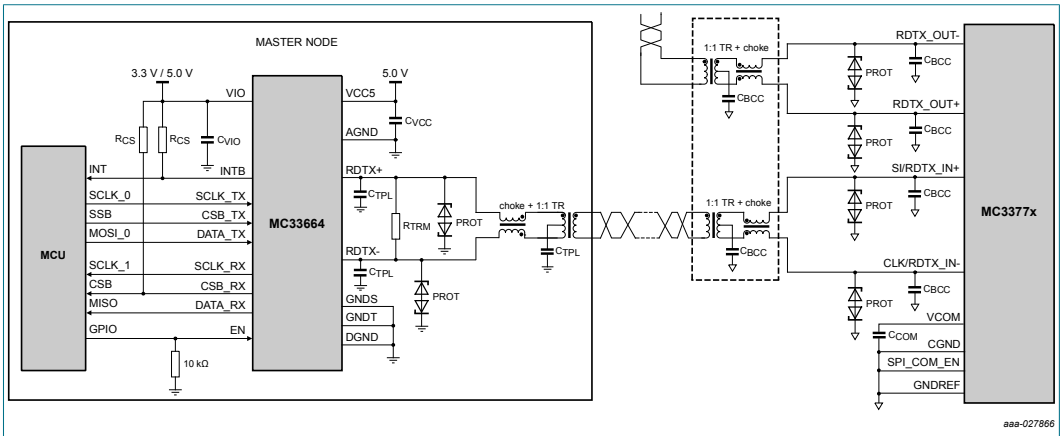


Figure 23. Transformer communication termination

For transformer communication, it is recommended the device be terminated as shown in Figure 23. Component values are given in Section 13.2 "33771 PCB components". Up to 15 nodes can be logically addressed, since CID = 0000 is reserved for network initialization. The actual maximum number of addressable nodes depends on physical implementation details, that is, wire lengths, number of used transformers, and so on. In transformer mode, the CSB pin may be used as a wake-up input. During sleep mode an edge transition of the CSB initiates the wake-up function. If this is not wanted, the CSB pin must be terminated or software masked to prevent undesired wake-up events.

Communication between the pack controller and the 33771 is half duplex communication with transformer isolation. Transformer physical layer in the pack controller creates a pulse phase modulated signal transmitted to the bus through the transformer. The 33771 physical layer is equipped with automatic termination resistor for impedance matching and network stability. Physical layer termination resistors are opened when the bus switches are closed. After initialization, the 33771 may be commanded to close the internal bus switches and allow the pack controller to communicate to the next 33771 in the system.

A start of frame and end of frame pulse is generated by the transformer driver and always occurs at the start and end of a communication message. The start of frame and end of frame pulse always contains two complete periods. Start of frame produces a double pulse with a logic 1 phase. End of frame produces a double pulse with logic 0 phase. Data pulses are single period pulse waves that indicate logic 1 or 0 based on the phase.

10.2.1 Command message bit order

Same as SPI interface

10.2.2 Response message bit order

Same as SPI interface

10.2.3 Transformer communication format

Command and response frames are exchanged primarily between a single master and a single slave. One exception to this is the use a global command which can be transmitted from one master to multiple slaves, but includes no slave response. The purpose of the

command and response transactions are to read and write to registers within the slave register map.

The command and response communication structure provides all context information required for unambiguous single-exchange transactions for extended memory applications requiring safety critical and efficient memory access.

The message structures have predefined fixed bit length frames and defined timing between transfers. Write commands to a single slave prompt a single echo response. To transfer data efficiently from the slave, multiple response packets may be requested by the read command. The 33771 defines a set of fields which constitute the command and response message structure.

Transformer message format is identical to the SPI format. Command message frames consist of six fields containing exactly 40 bits. The response structure is similar to the SPI format.

Note: *A slave device always responds to write command with an echo of the command. A read request responds with only the requested data. Global commands produce no response from slaves.*

After initialization, information is transferred to and from the 33771 through the read and write commands. On Power Up or POR, all bus switches are open and the first 33771 device in the chain responds to address 0000. The user must program the first device with a new address and command the bus switch to close by writing to the INIT[BUS_SW,CID] register. Programming the device with a new address and commanding the bus switches to close allows the pack controller to communicate and initialize the next device in the daisy chain. Subsequent read/write commands to the device must use the new address to communicate.

All write commands sent by the master must consist of a single frame. Each valid write command sent to the 33771 is acknowledged by the 33771 with a single frame response. The 33771 response contains an echo of the command and the written register data content.

Read commands sent by the master may generate a single response or multiple responses depending on the parameters sent in the read request. The packet size and memory start location is identified in the read command sent by the master.

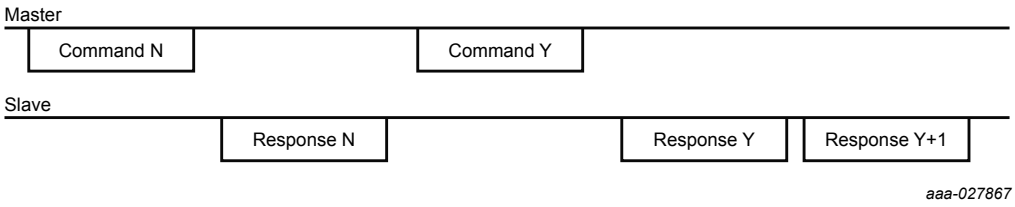


Figure 24. Bus traffic example

No response is generated by a slave 33771 when a global write command or corrupted message is received. Confirmation that a global write command is received by the slave must be done by reading the register in which it was written.

In cases where a bus error occurs (due to induced noise or a bus fault), both the master and slave detects bad data transfers. The 33771 slave reacts to communication faults by not sending a response, setting the FAULT1_STATUS[COM_ERR_FLT] and incrementing the COM_STATUS[COM_ERR_COUNT] register.

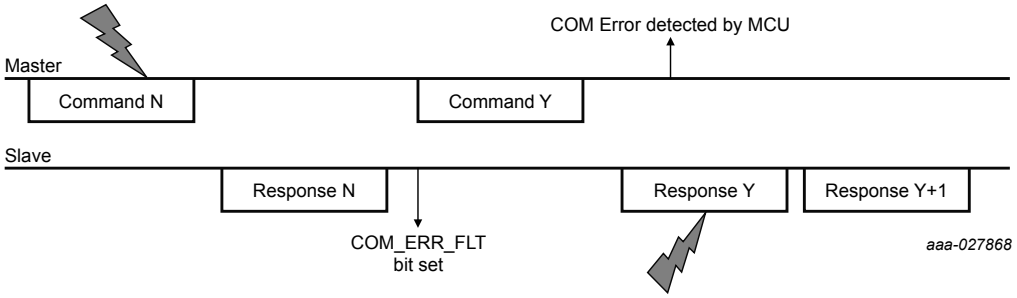


Figure 25. Bus traffic with receive error and recovery

All valid commands sent to an individual slave provide a response. In the event a slave does not respond to a message, the master must assume the message was corrupted or lost. To recover from the event, the master must retransmit the message. Corrupt messages transmitted by the slave are detected by the master through an incorrect CRC code. To recover, the master must request the data again.

10.2.4 Transformer communication timing

Command and response message frames are to be sent and received at 2.0 Mbps bit rate. The pulse transformer signal has a fixed frequency of 4.0 MHz. The echo response to a write command is provided within t_{RES} µs of the end of frame bit.

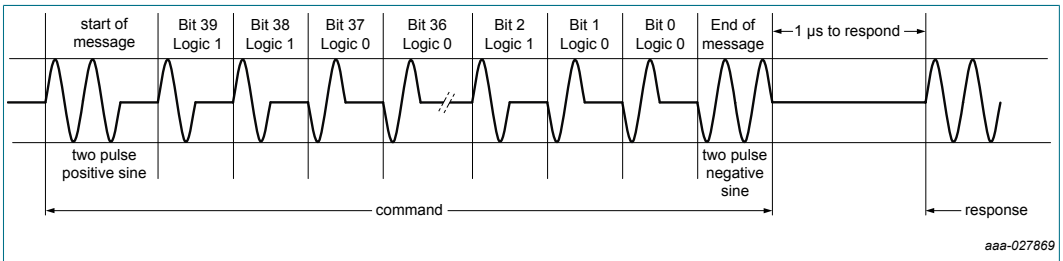


Figure 26. Transformer communication waveforms

Each send and receive message starts with a positive phase, double pulse start of message (SOM) bit followed by a 40 bit message and ending with a negative phase, double pulse end of message (EOM) bit.

10.2.5 Transformer communication wake-up

The 33771 contains bus wake-up capability. In the event the 33771 detects a wake-up condition, the device initiates a wake-up pulse sequence on the bus to alert the pack controller. After the pack controller exits sleep mode, it is recommended the pack controller interrogate each 33771 in the system to determine the source of the wake-up. To avoid contention during the wake-up, the 33771 deactivates the bus switch prior to transmitting the wake-up pulse sequence.

The wake-up pulse sequence consists of two transmit messages with no data transmitted. The messages are separated by a delay time (t_{WAKE_DELAY}). Each message contains a SOM and EOM pulse.

If the device experiences a reset and is not initialized within t_{WAKE_INIT} from the reset event, it sends a wake-up sequence on the bus, so the sleeping pack controller can get awakened and take control of the situation by reinitializing the network. See Section 12.2 "FAULT pin daisy chain operation".

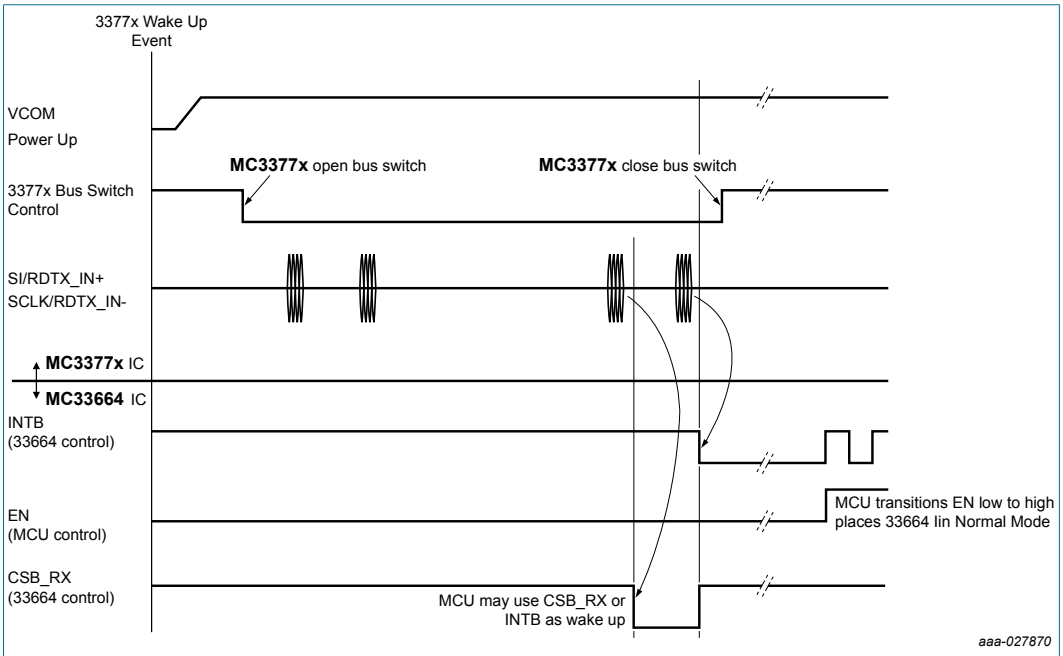


Figure 27. 33771 system wake-up

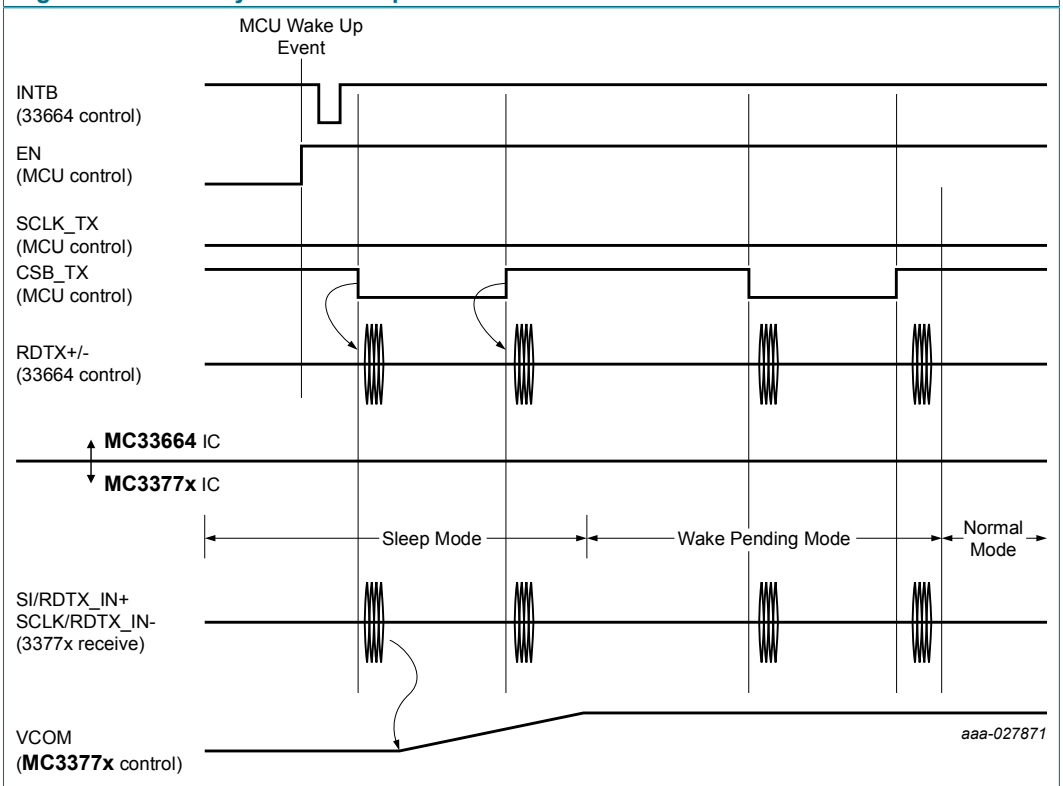


Figure 28. Pack controller system wake-up

10.3 CRC generation

The master and slaves calculate a CRC on the entire message using the processes detailed below.

The command and response CRC is fixed at 8 bits in length. The CRC is calculated using the polynomial $x^8 + x^5 + x^3 + x^2 + x + 1$ (identified by 0x2F) with a seed value of binary '11111111'.

An example CRC encoding HW implementation is shown in Figure 29.

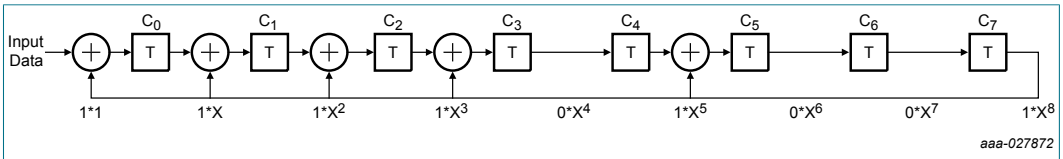


Figure 29. Command and response mode – example CRC encoder

The effect of CRC encoding procedure is shown in the following table. The seed value is appended into the most significant bits of the shift register.

Table 24. Data preparation for CRC encoding

Seed	Memory data	Master / Slave	Memory address	Cluster ID	Cmd / Tag ID
1111_1111	Bits[39:24] data	Bit[23] data	Bits[22:16] address	Bits[15:12]	Bits[11:8]

Seed…	…padded with the message to encode…	…padded with 8 zeros

1. Using a serial CRC calculation method, the transmitter rotates the seed and data into the least significant bits of the shift register.
2. During the serial CRC calculation, the seed and the data bits are XOR compared with the polynomial data bits. When the MSB is logic 1, the comparison result is loaded in the register, otherwise the data bits are simply shifted. It must be noted the 40 bit message to be processed must have the bits corresponding to the CRC byte all equal to zero (00000000).
3. Once the CRC is calculated, it replaces the CRC byte initially set to all zeros and is transmitted.

Following is the procedure for the CRC decoding:

1. The seed value is loaded into the most significant bits of the receive register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.
   - If the shift register contains all zeros, the CRC is correct.
   - If the shift register contains a value other than zero, the CRC is incorrect.

CRC calculation examples:

Table 25. Command CRC calculation examples

Data 16 bit (Hex)	Master/slave bit and memory address, 8 bit (Hex)	Physical address 4 bit (Hex)	Command 4 bit (Hex)	CRC 8 bit (Hex)
0x0101	0x08	0x1	0x0	0x22
0x0A0A	0x01	0xA	0x1	0xF6
0x01C4	0x0F	0x2	0x2	0x6A
0x7257	0x01	0x5	0x3	0x71

Table 26. Response CRC calculation examples

Data 16 bit (Hex)	Master/slave bit and memory address, 8 bit (Hex)	Physical address 4 bit (Hex)	Tag ID 4 bit (Hex)	CRC 8 bit (Hex)
0x1101	0x09	0x1	0x0	0xBD
0x2002	0x09	0x5	0x0	0x66
0x5103	0x09	0xA	0x5	0xFB
0xFF04	0x09	0x6	0x2	0xC0

10.4 Commands

10.4.1 Read command and response

Read command is intended to be used for SPI and transformer interface. The read command is local command used for retrieving data from the 33771 device. The data field contains the starting address of the data to be retrieved and the number of data registers to be returned. Requesting data from registers greater than address $FF forces the device to loop the register counter back to register $00.

Table 27. Read command table

Command name	Memory data		Master/slave	Memory address	Physical address (cluster ID)	Command		CRC
	Bit[39:24]		Bit[23]	Bit[22:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Read command	XXXX XXXX X	NRT- 01 to 7F	0	Memory address	CID	RC	01	Bit[7:0]

Table 28. Read response RC type format table

Response name	Memory data	Master/Slave	Memory address	Physical address (cluster ID)	Command		CRC
	Bit[39:24]	Bit[23]	Bit[22:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Read RC response	Memory data	1	Memory address	CID	RC	01	Bit[7:0]

Table 29. Read response TAG_ID type format table

Response name	Memory data	Master/slave	Memory address	Physical address (cluster ID)	Tag ID		CRC
	Bit[39:24]	Bit[23]	Bit[22:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Read TAG_ID response	Memory data	1	Memory address	CID	Tag ID		Bit[7:0]

Table 30. Legend for read command, read response RC type format, and read response TAG_ID type format tables

Read command		Read response	
Bit[7:0]	= 8 bit CRC	Bit[7:0]	= 8 bit CRC
Bit[11:8]	= Command field (RCI01)	Bit[11:8]	= Data tag ID or echo of command field (RCI01)
Bit[15:12]	= CID – device current address	Bit[15:12]	= CID – device current address
Bit[22:16]	= Start memory read address	Bit[22:16]	= Memory address
Bit[23]	= Master/slave = 0 (master)	Bit[23]	= Master/slave = 1 (slave)

Read command		Read response	
Bit[31:24]	= NRT, number of registers to transfer back. Max is FF, loop back on address $00	Bit[39:24]	= Data at memory address
Bit[39:32]	= X, don't care		

Note:

- *The read command is a local command*
- *Requesting a read of a reserved register provides a $0000 data response*
- *Registers are read only on devices which have not been initialized*
- *Requesting a number of NRT equal to 00 is the same as requesting 01*
- *If the pack controller sends a 2 bit rolling counter (labeled as RC) in Bits[11:10], it receives back the same RC value in the corresponding bits of the response frame*

10.4.2 Write local command

Unlike the read command which responds with data, the 33771 responds to the write command with a single frame echo of the command and updated register contents. Writing to read only registers generates an echo of the command and register contents, but it does not allow the register content to be updated.

Table 31. Write command table

Command name	Memory data	Master/slave	Memory address	Physical address (cluster ID)	Command		CRC
	Bit[39:24]	Bit[23]	Bit[22:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Write command	Memory data	0	Memory address	CID	RC	10	Bit[7:0]

Table 32. Write response table

Response name	Memory data	Master/slave	Memory address	Physical address (cluster ID)	Command		CRC
	Bit[39:24]	Bit[23]	Bit[22:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Write response	Memory data	1	Memory address	CID	RC	10	Bit[7:0]

Table 33. Legend for write command and write response tables

Write command		Write response	
Bit[7:0]	= 8 bit CRC	Bit[7:0]	= 8 bit CRC
Bit[11:8]	= Command field (RCI10)	Bit[11:8]	= Echo of command field
Bit[15:12]	= CID – cluster identification address	Bit[15:12]	= CID – cluster identification address
Bit[22:16]	= Memory address	Bit[22:16]	= Memory address where the data was written
Bit[23]	= Master/slave = 0 (master)	Bit[23]	= Master/slave = 1 (slave)
Bit[39:24]	= Data to be written to memory	Bit[39:24]	= Updated contents of the data register

Note: *Writing to reserved registers responds with an echo, but performs no operation and loads no data in the reserved register.*

10.4.3 Global write command

The global write command allows the transformer user to communicate to all devices on the bus at the same time. The global write command is useful to program all devices at

the same time with values for fault threshold or to synchronize conversions for all devices on the bus. When a slave receives a valid global write command the message is acted upon, but no response is generated.

Table 34. Global write command table

Command name	Memory data	Master/slave	Memory address	Physical address (cluster ID)	Command		CRC
	Bit[39:24]	Bit[23]	Bit[22:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Global write command	Memory data	0	Memory address	xxxx (global)	RC	11	Bit[7:0]

Table 35. Legend for global write command table

Write command	
Bit[7:0]	= 8 bit CRC
Bit[11:8]	= Command field (global write RCI11)
Bit[15:12]	= xxxx (global)
Bit[22:16]	= Memory address
Bit[23]	= Master/slave = 0 (master)
Bit[39:24]	= Data to be written to memory

10.4.4 No operation command

The no operation command allows the user to verify communication to a device on the bus without performing any operation. When a slave receives a valid no operation command, an echo of the command is the device response.

Table 36. No operation command table

Command name	Memory data	Master/slave	Memory address	Physical address (cluster ID)	Command		CRC
	Bit[39:24]	Bit[23]	Bit[22:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
No op command	Memory data	0	Memory address	CID	RC	00	Bit[7:0]

Table 37. No operation response table

Response name	Memory data	Master/slave	Memory address	Physical address (cluster ID)	Command		CRC
	Bit[39:24]	Bit[23]	Bit[22:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
No op response	Memory data	1	Memory address	CID	RC	00	Bit[7:0]

Table 38. Legend for no operation command and no operation response tables

No op command		No op response	
Bit[7:0]	= 8 bit CRC	Bit[7:0]	= 8 bit CRC
Bit[11:8]	= Command field (RCI00)	Bit[11:8]	= Echo of command field
Bit[15:12]	= CID – cluster identification address	Bit[15:12]	= CID – cluster identification address
Bit[22:16]	= Memory address	Bit[23:16]	= Memory address
Bit[23]	= Master/slave = 0 (master)	Bit[23]	= Master/slave = 1 (slave)
Bit[39:24]	= Don't care	Bit[39:24]	= Don't care

10.4.5 Command and response summary

Table 39. Command summary table

Command name	Memory data	Master/slave	Memory address	Device address (cluster ID)	Command		CRC
	Bit[39:24]		Bit[23:16]	Bit15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
No op command	Dummy data	0	Dummy address	CID	RC	00	8 Bits
Read command	Number of registers	0	Register address	CID	RC	01	8 Bits
Write command	Data	0	Register address	CID	RC	10	8 Bits
Global write command	Data	0	Register address	xxxx	RC	11	8 Bits

Cluster ID of 0000 only writes to register INIT. First message from MCU controller writing to cluster ID 0000 and with an address other than INIT generates no response.

After initialization, each time the device receives a frame having the master/slave bit equal to logic 1, this frame is not recognized, even though the address contained in the CID field is equal to the programmed one. In this condition, the device neither acts upon nor answers the command. This is a wanted behavior, whose purpose is to avoid the device acting upon or responding to a frame generated by another slave device of the network.

Table 40. Response summary table

Response name	Memory data	Master/slave	Memory address	Device address (cluster ID)	Command		CRC
	Bit[39:24]		Bit[23:16]	Bit15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
No op response	Dummy data	1	Dummy address	CID	RC	00	8 Bits
Read RC response	Memory data	1	Register address	CID	RC	01	8 Bits
Read TAG_ID response	Memory data	1	Register address	CID	TAG_ID		
Write response	Data	1	Register address	CID	RC	10	8 Bits

10.4.6 I^2C communication interface

As an optional feature, the 33771 has an integrated I^2C communication link to an external local EEPROM, which may be used to store calibration parameters defined by the user. If the EEPROM is not used, then the SCL and SDA pins must be left open. In such case, the FAULT1_STATUS[I2C_ERR_FLT] bit is automatically updated to logic 1. The automatic update happens even if an error bit is masked. If no EEPROM is mounted, the pack controller has to ignore the content of FAULT1_STATUS[I2C_ERR_FLT].

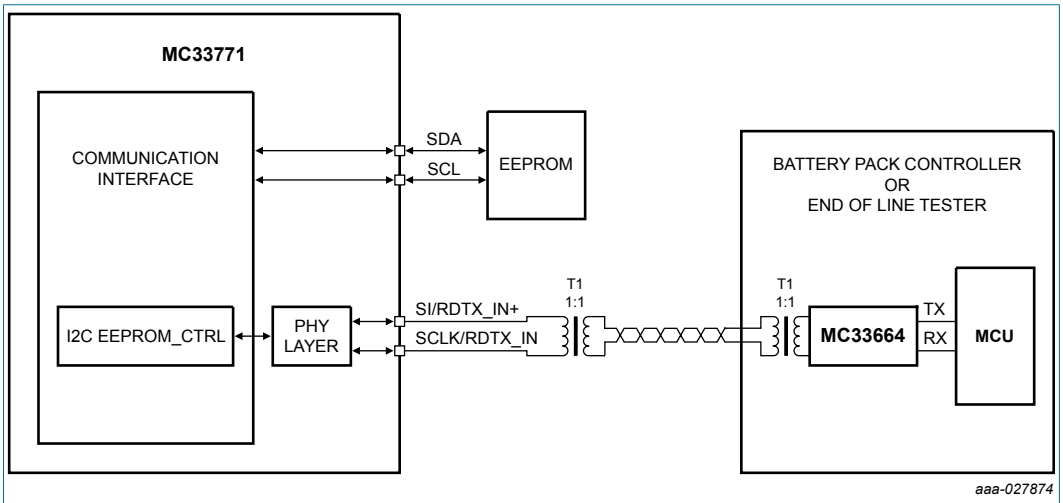


Figure 30. 33771 calibration registers

11 Registers

11.1 Register map

Important: *Trying to access registers marked as reserved produces responses having all zeros in the data field.*

In all register descriptions, POR means power on reset or hardware reset or software reset, or reset event based on SYS_CFG2[FLT_RST_CFG] register configuration, unless otherwise stated.

Table 41. Register table

Register		RC or TAG ID	Reference	Description	Notes
A[6:0]	Mnemonic	Format			
$00	Reserved	Table 28		Reserved	Not readable or writeable
$01	INIT	Table 28	Section 11.1.1	Device initialization	Global write is forbidden for CID
$02	SYS_CFG_GLOBAL	Table 28	Section 11.1.2	Global system configuration	GLOBAL access only and no ECHO in transformer mode. In SPI mode it can be written by a standard write command.
$03	SYS_CFG1	Table 28	Section 11.1.3	System configuration	
$04	SYS_CFG2	Table 28	Section 11.1.4	System configuration	
$05	SYS_DIAG	Table 29	Section 11.1.5	System diagnostic	Writable in DIAG mode only, automatically cleared when exiting DIAG mode
$06	ADC_CFG	Table 28	Section 11.1.6	ADC configuration	
$07	ADC2_OFFSET_COMP	Table 28	Section 11.1.7	ADC2 offset compensation	
$08	OV_UV_EN	Table 28	Section 11.1.8	CT measurement selection	
$09	CELL_OV_FLT	Table 28	Section 11.1.9	CT overvoltage fault	
$0A	CELL_UV_FLT	Table 28	Section 11.1.10	CT undervoltage fault	
$0B	Reserved	Table 28	Section 11.1.46	Reserved	
$0C	CB1_CFG	Table 28	Section 11.1.12	CB configuration for cell 1	
$0D	CB2_CFG	Table 28	Section 11.1.12	CB configuration for cell 2	
$0E	CB3_CFG	Table 28	Section 11.1.12	CB configuration for cell 3	
$0F	CB4_CFG	Table 28	Section 11.1.12	CB configuration for cell 4	
$10	CB5_CFG	Table 28	Section 11.1.12	CB configuration for cell 5	
$11	CB6_CFG	Table 28	Section 11.1.12	CB configuration for cell 6	
$12	CB7_CFG	Table 28	Section 11.1.12	CB configuration for cell 7	
$13	CB8_CFG	Table 28	Section 11.1.12	CB configuration for cell 8	
$14	CB9_CFG	Table 28	Section 11.1.12	CB configuration for cell 9	
$15	CB10_CFG	Table 28	Section 11.1.12	CB configuration for cell 10	
$16	CB11_CFG	Table 28	Section 11.1.12	CB configuration for cell 11	
$17	CB12_CFG	Table 28	Section 11.1.12	CB configuration for cell 12	
$18	CB13_CFG	Table 28	Section 11.1.12	CB configuration for cell 13	
$19	CB14_CFG	Table 28	Section 11.1.12	CB configuration for cell 14	

Register		RC or TAG ID	Reference	Description	Notes
A[6:0]	Mnemonic	Format			
$1A	CB_OPEN_FLT	Table 28	Section 11.1.13	Open CB fault	
$1B	CB_SHORT_FLT	Table 28	Section 11.1.14	Short CB fault	
$1C	CB_DRV_STS	Table 28	Section 11.1.15	CB driver status	
$1D	GPIO_CFG1	Table 28	Section 11.1.16	GPIO configuration	
$1E	GPIO_CFG2	Table 28	Section 11.1.17	GPIO configuration	
$1F	GPIO_STS	Table 28	Section 11.1.18	GPIO diagnostic	
$20	AN_OT_UT_FLT	Table 28	Section 11.1.19	AN over and undertemperature	
$21	GPIO_SHORT_ANx_OPEN_STS	Table 28	Section 11.1.20	Short GPIO/open AN diagnostic	
$22	I_STATUS	Table 28	Section 11.1.21	PGA DAC value	
$23	COM_STATUS	Table 28	Section 11.1.22	Number of CRC error counted	
$24	FAULT1_STATUS	Table 29	Section 11.1.23	Fault status	
$25	FAULT2_STATUS	Table 29	Section 11.1.24	Fault status	
$26	FAULT3_STATUS	Table 29	Section 11.1.25	Fault status	
$27	FAULT_MASK1	Table 28	Section 11.1.26	FAULT pin mask	
$28	FAULT_MASK2	Table 28	Section 11.1.27	FAULT pin mask	
$29	FAULT_MASK3	Table 28	Section 11.1.28	FAULT pin mask	
$2A	WAKEUP_MASK1	Table 28	Section 11.1.29	Wake-up events mask	
$2B	WAKEUP_MASK2	Table 28	Section 11.1.30	Wake-up events mask	
$2C	WAKEUP_MASK3	Table 28	Section 11.1.31	Wake-up events mask	
$2D	CC_NB_SAMPLES	Table 29	Section 11.1.32	Number of samples in coulomb counter	
$2E	COULOMB_CNT1	Table 29	Section 11.1.33	Coulomb counting accumulator	
$2F	COULOMB_CNT2	Table 29	Section 11.1.33		
$30	MEAS_ISENSE1	Table 29	Section 11.1.34	ISENSE measurement	
$31	MEAS_ISENSE2	Table 29	Section 11.1.34	ISENSE measurement	
$32	MEAS_STACK	Table 29	Section 11.1.35	Stack voltage measurement	
$33	MEAS_CELL14	Table 29	Section 11.1.35	Cell 14 voltage measurement	
$34	MEAS_CELL13	Table 29	Section 11.1.35	Cell 13 voltage measurement	
$35	MEAS_CELL12	Table 29	Section 11.1.35	Cell 12 voltage measurement	
$36	MEAS_CELL11	Table 29	Section 11.1.35	Cell 11 voltage measurement	
$37	MEAS_CELL10	Table 29	Section 11.1.35	Cell 10 voltage measurement	
$38	MEAS_CELL9	Table 29	Section 11.1.35	Cell 9 voltage measurement	
$39	MEAS_CELL8	Table 29	Section 11.1.35	Cell 8 voltage measurement	
$3A	MEAS_CELL7	Table 29	Section 11.1.35	Cell 7 voltage measurement	
$3B	MEAS_CELL6	Table 29	Section 11.1.35	Cell 6 voltage measurement	
$3C	MEAS_CELL5	Table 29	Section 11.1.35	Cell 5 voltage measurement	
$3D	MEAS_CELL4	Table 29	Section 11.1.35	Cell 4 voltage measurement	
$3E	MEAS_CELL3	Table 29	Section 11.1.35	Cell 3 voltage measurement	
$3F	MEAS_CELL2	Table 29	Section 11.1.35	Cell 2 voltage measurement	
$40	MEAS_CELL1	Table 29	Section 11.1.35	Cell 1 voltage measurement	
$41	MEAS_AN6	Table 29	Section 11.1.35	AN6 voltage measurement	
$42	MEAS_AN5	Table 29	Section 11.1.35	AN5 voltage measurement	
$43	MEAS_AN4	Table 29	Section 11.1.35	AN4 voltage measurement	
$44	MEAS_AN3	Table 29	Section 11.1.35	AN3 voltage measurement	

Register		RC or TAG ID	Reference	Description	Notes
A[6:0]	Mnemonic	Format			
$45	MEAS_AN2	Table 29	Section 11.1.35	AN2 voltage measurement	
$46	MEAS_AN1	Table 29	Section 11.1.35	AN1 voltage measurement	
$47	MEAS_AN0	Table 29	Section 11.1.35	AN0 voltage measurement	
$48	MEAS_IC_TEMP	Table 29	Section 11.1.35	IC temperature measurement	
$49	MEAS_ VBG_DIAG_ADC1A	Table 29	Section 11.1.35	ADCIA voltage reference measurement	
$4A	MEAS_ VBG_DIAG_ADC1B	Table 29	Section 11.1.35	ADCIA voltage reference measurement	
$4B	TH_ALL_CT	Table 28	Section 11.1.36	CTx over and undervoltage threshold	
$4C	TH_CT14	Table 28	Section 11.1.37	CT14 over and undervoltage threshold	
$4D	TH_CT13	Table 28	Section 11.1.37	CT13 over and undervoltage threshold	
$4E	TH_CT12	Table 28	Section 11.1.37	CT12 over and undervoltage threshold	
$4F	TH_CT11	Table 28	Section 11.1.37	CT11 over and undervoltage threshold	
$50	TH_CT10	Table 28	Section 11.1.37	CT10 over and undervoltage threshold	
$51	TH_CT9	Table 28	Section 11.1.37	CT9 over and undervoltage threshold	
$52	TH_CT8	Table 28	Section 11.1.37	CT8 over and undervoltage threshold	
$53	TH_CT7	Table 28	Section 11.1.37	CT7 over and undervoltage threshold	
$54	TH_CT6	Table 28	Section 11.1.37	CT6 over and undervoltage threshold	
$55	TH_CT5	Table 28	Section 11.1.37	CT5 over and undervoltage threshold	
$56	TH_CT4	Table 28	Section 11.1.37	CT4 over and undervoltage threshold	
$57	TH_CT3	Table 28	Section 11.1.37	CT3 over and undervoltage threshold	
$58	TH_CT2	Table 28	Section 11.1.37	CT2 over and undervoltage threshold	
$59	TH_CT1	Table 28	Section 11.1.37	CT1 over and undervoltage threshold	
$5A	TH_AN6_OT	Table 28	Section 11.1.38	AN6 overtemperature threshold	
$5B	TH_AN5_OT	Table 28	Section 11.1.38	AN5 overtemperature threshold	
$5C	TH_AN4_OT	Table 28	Section 11.1.38	AN4 overtemperature threshold	
$5D	TH_AN3_OT	Table 28	Section 11.1.38	AN3 overtemperature threshold	
$5E	TH_AN2_OT	Table 28	Section 11.1.38	AN2 overtemperature threshold	
$5F	TH_AN1_OT	Table 28	Section 11.1.38	AN1 overtemperature threshold	
$60	TH_AN0_OT	Table 28	Section 11.1.38	AN0 overtemperature threshold	
$61	TH_AN6_UT	Table 28	Section 11.1.38	AN6 undertemperature threshold	

Register		RC or TAG ID	Reference	Description	Notes
A[6:0]	Mnemonic	Format			
$62	TH_AN5_UT	Table 28	Section 11.1.38	AN5 undertemperature threshold	
$63	TH_AN4_UT	Table 28	Section 11.1.38	AN4 undertemperature threshold	
$64	TH_AN3_UT	Table 28	Section 11.1.38	AN3 undertemperature threshold	
$65	TH_AN2_UT	Table 28	Section 11.1.38	AN2 undertemperature threshold	
$66	TH_AN1_UT	Table 28	Section 11.1.38	AN1 undertemperature threshold	
$67	TH_AN0_UT	Table 28	Section 11.1.38	AN0 undertemperature threshold	
$68	TH_ISENSE_OC	Table 28	Section 11.1.39	ISENSE overcurrent threshold	
$69	TH_COULOMB_CNT_MSB	Table 28	Section 11.1.40	Coulomb counter threshold (MSB)	
$6A	TH_COULOMB_CNT_LSB	Table 28	Section 11.1.40	Coulomb counter threshold (LSB)	
$6B	SILICON_REV	Table 28	Section 11.1.41	Silicon revision	
$6C	EEPROM_CNTL	Table 28	Section 11.1.42	EEPROM transfer control	
$6D	DED_ENCODE1	Table 28	Section 11.1.43	ECC signature 1	
$6E	DED_ENCODE2	Table 28	Section 11.1.44	ECC signature 2	
$6F	FUSE_MIRROR_DATA	Table 28	Section 11.1.45	Fuse mirror data	
$70	FUSE_MIRROR_CNTL	Table 28	Section 11.1.45	Fuse mirror address	
$71	Reserved	Table 28	Section 11.1.46	NXP reserved	
...	Reserved	Table 28	Section 11.1.46	NXP reserved	
$7F	Reserved	Table 28	Section 11.1.46	NXP reserved	

Table 42. Mirror memory

Register		Description	Notes
A[4:0]			
$00	FUSE_MIRROR_BANK	Fuse bank 0	
$01	FUSE_MIRROR_BANK	Fuse bank 1	
$02	FUSE_MIRROR_BANK	Fuse bank 2	
$03	FUSE_MIRROR_BANK	Fuse bank 3	
$04	FUSE_MIRROR_BANK	Fuse bank 4	
$05	FUSE_MIRROR_BANK	Fuse bank 5	
$06	FUSE_MIRROR_BANK	Fuse bank 6	
$07	FUSE_MIRROR_BANK	Fuse bank 7	
$08	FUSE_MIRROR_BANK	Fuse bank 8	
$09	FUSE_MIRROR_BANK	Fuse bank 9	
$0A	FUSE_MIRROR_BANK	Fuse bank 10	
$0B	FUSE_MIRROR_BANK	Fuse bank 11	
$0C	FUSE_MIRROR_BANK	Fuse bank 12	
$0D	FUSE_MIRROR_BANK	Fuse bank 13	
$0E	FUSE_MIRROR_BANK	Fuse bank 14	
$0F	FUSE_MIRROR_BANK	Fuse bank 15	
$10	FUSE_MIRROR_BANK	Fuse bank 16	
$11	FUSE_MIRROR_BANK	Fuse bank 17	
$12	FUSE_MIRROR_BANK	Fuse bank 18	
$13	FUSE_MIRROR_BANK	Fuse bank 19	
$14	FUSE_MIRROR_BANK	Fuse bank 20	
$15	FUSE_MIRROR_BANK	Fuse bank 21	
$16	FUSE_MIRROR_BANK	Fuse bank 22	DED_ENCODE 1
$17	FUSE_MIRROR_BANK	Fuse bank 23	DED_ENCODE 2
$18	FUSE_MIRROR_BANK	Fuse bank 24	
$19	FUSE_MIRROR_BANK	Fuse bank 25	
$1A	FUSE_MIRROR_BANK	Fuse bank 26	
$1B	FUSE_MIRROR_BANK	Fuse bank 27	
$1C	FUSE_MIRROR_BANK	Fuse bank 28	
$1D	FUSE_MIRROR_BANK	Fuse bank 29	
$1E	FUSE_MIRROR_BANK	Fuse bank 30	
$1F	FUSE_MIRROR_BANK	Fuse bank 31	

11.1.1 Initialization register – INIT

Following power-up or soft POR, the 33771 is in a reset state with the bus terminated and the bus switch open. In the INIT mode, the pack controller may read the internal register of the 33771 using the address 0000. The 33771 must be initialized before it responds to write commands.

To initialize the device, a write command has to be sent with the value of 0000 in the device address field of the frame, that is, bit 15 to bit 12, while the new cluster ID, that is, the new address to be assigned to the node, must be written to the CID field of the INIT register. Only a device with current cluster ID of 0000 may be programmed to a new address. In this condition, the internal communication bus switch is open and the related termination resistance is connected to the bus. By programming the device with a new CID the device is considered initialized. After a device has been initialized, it only acts on subsequent global write (transformer mode) or acts on and responds to subsequent local write or read commands matching the device cluster ID. Once a device has been initialized, the CID bits in the register INIT may not be reprogrammed unless the device receives a hard or soft reset. The bus switch may be opened or closed at any time by writing to the field BUS_SW of the initialization register INIT. The bus switch may be closed when the device is programmed with CID different than 0000 (this may occur at the same time), while a bus closure command to a never initialized device is not actuated.

The bus is terminated when the bus switches are open. If the INIT[RTERM] flag is set to 0, the termination resistor is disconnected when the communication switch is closed, and is connected when the switch is open. If the INIT[RTERM] flag is set to 1, the termination resistor is connected to the bus regardless of the bus switch status. With the first device in the sequence programmed and the bus switch closed, commands may then be received by the next device in the daisy chain.

Table 43. INIT

INIT																
$01	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write											RTERM	BUS_SW	CID			
Read																
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RTERM	Description	Control of the internal termination resistor connection to the communication bus
	0	The bus termination resistor depends on the status of the communication switch
	1	The bus termination resistor is connected regardless of the bus switch status, unless the CID is equal to 0
	Reset condition	POR
BUS_ SW	Description	Bus switch control
	0	Disabled
	1	Enabled – bus switch closed, as long as CID is not 0000
	Reset condition	POR
CID	Description	Cluster Identifier. Can be overridden by any combination different from all zeros. Not accessible with global write.
	0 0 0 0	Default
	XXXX	CID
	Reset condition	POR

11.1.2 System configuration global register SYS_CFG_GLOBAL

In TPL mode, only a global command can be used to write to register $02, while a local write is disregarded. In contrast, if using the SPI mode, only a local write to register $02 can be executed.

Table 44. SYS_CFG_GLOBAL

SYS_CFG_GLOBAL																
$02	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																GO2SLEEP
Read																0
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GO2SLEEP		Description		Go to sleep command												
		0		Disabled												
		1 (active pulse)		Device goes to sleep mode after all conversions in progress are completed												
		Reset condition		POR												

11.1.3 System configuration register 1 – SYS_CFG1

The SYS_CFG1 register contains control bits and register settings which allow the user to adapt the 33771 to specific applications and system requirements. Of these control bits, it is important to note the SYS_CFG1[SOFT_RST] bit is used to reset register contents of the device.

Table 45. SYS_CFG1

SYS_CFG1																
$03	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	CYCLIC_TIMER			DIAG_TIMEOUT			I_MEAS_EN	CB_AUTO_PAUSE	CB_DRVEN	GO2DIAG	CB_MANUAL_PAUSE	SOFT_RST	FAULTWAVE	WAVE_DC_BITx		RESERVD_0
Read										DIAG_ST		0				
Rst	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1
CYCLIC_TIMER		Description		Timer to trigger cyclic measurements in normal mode or sleep mode												
		0 0 0		Cyclic measure is disabled, whatever the mode												
		0 0 1		Continuous measurements												
		0 1 0		0.1 s												
		0 1 1		0.2 s												
		1 0 0		1.0 s												
		1 0 1		2.0 s												
		1 1 0		4.0 s												
		1 1 1		8.0 s												
		Reset condition		POR												
DIAG_TIMOUT		Description		DIAG mode timeout. Length of time the device is allowed to be in diag mode before being forced to normal mode.												
		0 0 0		No timer, not allowed to enter diag mode												
		0 0 1		0.05 s												
		0 1 0		0.1 s												
		0 1 1		0.2 s												
		1 0 0		1.0 s												
		1 0 1		2.0 s												
		1 1 0		4.0 s												
		1 1 1		8.0 s												
		Reset condition		POR												

I_MEAS_EN	Description	Enable for current measurement chain
	0	Disabled
	1	Current measurement chain is enabled
	Reset condition	POR
CB_AUTO_PAUSE	Description	Disables cell balance for ADC1-A and ADC1-B during the conversion cycle
	0	Disabled
	1	CB switches are forced off each time a cyclic measurement is performed, no impact on CB counters
	Reset condition	POR
CB_DRVEN	Description	General enable or disable for all cell balance drivers.
	0	Disabled
	1	Enabled, each cell balance driver can be individually switched on and off by CB_xx_CFG register.
	Reset condition	POR
GO2DIAG	Description	Commands the device to diag mode. Rewriting the GO2DIAG bit restarts the DIAG_TIMEOUT.
	0	Exit diag mode
	1	Enter diag mode (starts timer)
	Reset condition	POR
CB_MANUAL_PAUSE	Description	Cell balancing manual pause
	0	Disabled CB switches can be normally commanded on/off by the dedicated logic functions
	1	CB switches are forced off, CB counters are not frozen
	Reset condition	POR
DIAG_ST	Description	Identifies when the device is in diag mode
	0	System is not in diag mode
	1	System is in diag mode
	Reset condition	POR
SOFT_RST	Description	Software reset
	0	Disabled
	1 (active pulse)	Active software reset
	Reset condition	POR (bit is not reset if reset was due to sotware reset)
FAULT_WAVE	Description	FAULT pin wave form control bit.
	0	FAULT pin has high or low level behavior. FAULT pin high, fault is present. FAULT pin low indicates no fault present.
	1	FAULT pin has heart beat wave when no fault is present. Pulse high time is fixed at 500 µs.
	Reset condition	POR
WAVE_DC_BITx	Description	Controls the off time of the heart beat pulse.
	0 0	500 µs
	0 1	1.0 ms
	1 0	10 ms
	1 1	100 ms
	Reset condition	POR

11.1.4 System configuration register 2 – SYS_CFG2

Table 46. SYS_CFG2

SYS_CFG2																
$04	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	RESERVD_0 [1]	RESERVD_1 [1]	RESERVD_2 [1]	x	x	x	FLT_RST_CFG				TIMEOUTCOMM		RESERVD_4 [1]	RESERVD_5 [1]	NUMBODD	HAMMENCOD
Read				PREVIOUS_STATE												
Rst	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0

PREVIOUS_STATE	Description	Information about the previous state of the device
	0 0 0	The device is coming from INIT state
	0 0 1	The device is coming from IDLE state
	0 1 0	The device is coming from NORMAL state
	0 1 1	The device is coming from DIAG state
	1 1 1	The device is coming from SLEEP state
	1 1 0	The device is coming from CYCLIC_WUP state
	Reset condition	POR
TIMOUT_COMM	Description	No communication timeout - flag in FAULT1_STATUS[COM_LOSS] if no communication during…
	0 0	32 ms
	0 1	64 ms
	1 0	128 ms
	1 1	256 ms
	Reset condition	POR
FLT_RST_CFG	Description	Fault reset configuration
	0 0 1 1	Disabled COM timeout (1024 ms) reset and OSC fault monitoring and reset
	0 1 0 1	Enabled OSC fault monitoring
	0 1 1 0	Enabled OSC fault monitoring and reset
	1 0 0 1	Enabled COM timeout (1024 ms) reset
	1 0 1 0	Enabled COM timeout (1024 ms) reset and OSC fault monitoring
	1 1 0 0	Enabled COM timeout (1024 ms) reset and OSC fault monitoring and reset
	others	Invalid, leads to enabled COM timeout (1024 ms) reset and OSC fault monitoring and reset (1100)
	Reset condition	POR (except after a reset caused by a communication timeout or caused by an oscillator fault)
NUMB ODD	Description	Odd number of cells in the cluster (useful for open load diagnosis)
	0	Even configuration
	1	Odd configuration
	Reset condition	POR
HAMM ENCOD	Description	Hamming encoders
	0	Decode - the DED Hamming decoders fulfill their job
	1	Encode - the DED hamming decoders generate the redundancy bits
	Reset condition	POR

[1] Do not change

11.1.5 System diagnostics register – SYS_DIAG

Table 47. SYS_DIAG

SYS_DIAG																
$05	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	FAULT_DIAG			I_MUX		ISENSE_OL_DIAG	ANx_OLDIAG	ANx_TEMP_DIAG	DA_DIAG	POLARITY	CT_LEAK_DIAG	CT_OV_UV	CT_OL_ODD	CT_OL_EVEN	CB_OL_ODD	CB_OL_EVEN
Read																
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FAULT_DIAG	Description	FAULT pin driver command
	0	No FAULT pin drive, FAULT pin is under command of the pack controller
	1	FAULT pin is forced to high level
	Reset condition	POR
I_MUX	Description	Allows user to select between various inputs to PGA to be converted by ADC2
	0 0	(ISENSE+, ISENSE−)
	0 1	(GPIO5, GPIO6)
	1 0	Calibrated internal reference (VREF_DIAG)
	1 1	PGA zero (PGA differential inputs terminated to ground)
	Reset condition	POR
ISENSE_OL_DIAG	Description	ISENSE open load diagnostic control bit. Enables or disables internal pull-up resistors on the ISENSE input pins.
	0	Disabled
	1	Enabled
	Reset condition	POR
ANx_OL_DIAG	Description	ANx open load diagnostic control bit. Used to activate the pull down on GPIO input pins.
	0	Diagnostic disabled
	1	Diagnostic enabled
	Reset condition	POR
ANx_TEMP_DIAG	Description	Control bit to activate the OT/UT diagnostic on GPIOx configured as ANx ratiometric or single ended ADC input
	0	Diagnostic inactive
	1	Diagnostic active
	Reset condition	POR
DA_DIAG	Description	Differential amplifier diagnostic. Diagnostic mode function only
	0	No check
	1	Check is enabled (floating Zener conversion, ground Zener measurement added, comparison)
	Reset condition	POR
POLARITY	Description	Control bit used in terminal leakage detection. Controls the polarity between the level shifter and the ADC1-A and ADC1-B converters
	0	Non-inverted
	1	Inverted
	Reset condition	POR
CT_LEAK_DIAG	Description	Control bit used in terminal leakage detection. Commands the MUX to route the CTx/CBx pin to ADC1-A,B converters. This bit must be exclusive vs. DA_DIAG.
	0	Normal operation, CTx are MUXed to converter
	1	Δ between CT and CB pins are routed to the analog front end, to be converted
	Reset condition	POR

CT_OV_UV	Description	OV and UV diagnostic is enabled. This bit must be set to logic 0 when performing CT open load diagnostic.
	0	OV and UV diagnostic disabled
	1	OV and UV diagnostic enabled
	Reset condition	POR
CT_OL_ODD	Description	Control bit used to control the odd numbered cell terminal open detect switches
	0	Odd switches are open
	1	Odd switches are closed (may be set only when CT_OL_EVEN is logic 0)
	Reset condition	POR
CT_OL_EVEN	Description	Control bit used to control the even numbered cell terminal open detect switches
	0	Even switches are open
	1	Even switches are closed (may be set only when CT_OL_ODD is logic 0)
	Reset condition	POR
CB_OL_ODD	Description	Control bit used to control the cell balance open load ODD detection switches.
	0	ODD cell balance open load detection switches are open
	1	ODD cell balance open load detection switches are closed
	Reset Condition	POR
CB_OL_EVEN	Description	Control bit used to control the cell balance open load EVEB detection switches
	0	EVEN cell balance open load detection switches are open
	1	EVEN cell balance open load detection switches are closed
	Reset condition	POR

11.1.6 ADC configuration register – ADC_CFG

The ADC_CFG is used to set the conversion parameters of the three ADC converters and command the 33771 to perform on demand conversions in both normal and diagnostic modes.

Table 48. ADC_CFG

ADC_CFG																
$06	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	TAG_ID				SOC	PGA_GAIN			CC_RST	DIS_CH_COMP	ADC1_A_DEF		ADC1_B_DEF		ADC2_DEF	
Read					EOC_N	PGA_GAIN_S			0							
Rst	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	1
TAG_ID		Description		The TAG_ID is provided by the system controller during each conversion request. Tag ID should be incremented for each conversion request sent by the system controller. When reading the data for the requested conversion the tag field contains the TAG_ID.												
		0 0 0 0		TAG_ID provided in conversion												
		...														
		1 1 1 1														
		Reset condition		POR												
SOC		Description		Control bit to command the 33771 to initiate a conversion sequence												
		0		Disabled. Writing SOC to 0 has no effect on an ongoing conversion sequence.												
		1 (active pulse)		Enabled. Initiate a conversion sequence.												
		Reset condition		POR												

EOC_N	Description	End of conversion flag
	0	Device has completed the commanded conversion
	1	Device is performing the commanded conversion
	Reset condition	POR
PGA_GAIN	Description	Define the gain of the ADC2 programmable gain amplifier
	0 0 0	4
	0 0 1	16
	0 1 0	64
	0 1 1	256
	1 x x	Automatic gain selection (internally adjusted)
	Reset condition	POR
PGA_GAIN_S	Description (bit 10)	Automatic gain mode status (information available only if SYS_CFG1[I_MEAS_EN] = 1)
	0	Fixed gain
	1	Automatic gain control
	Reset condition	POR
	Description (bit[9:8])	Report the current gain of the ADC2 programmable gain amplifier (automatically settled or not). (information available only if SYS_CFG1[I_MEAS_EN] = 1)
	0 0	4
	0 1	16
	1 0	64
	1 1	256
	Reset condition	POR
CC_RST	Description	Control bit used to reset the value of the coulomb counter to 0
	0	No action
	1 (active pulse)	Reset coulomb counter registers COULOMB_CNT1 and COULOMB_CNT2 and the CC_NB_SAMPLES registers
	Reset condition	POR
ADC1_A_DEF	Description	ADC1_A measurement resolution
	0 0	13 bit
	0 1	14 bit
	1 0	15 bit
	1 1	16 bit
	Reset condition	POR
ADC1_B_DEF	Description	ADC1_B measurement resolution
	0 0	13 bit
	0 1	14 bit
	1 0	15 bit
	1 1	16 bit
	Reset condition	POR
ADC2_DEF	Description	ADC2 measurement resolution
	0 0	13 bit
	0 1	14 bit
	1 0	15 bit
	1 1	16 bit
	Reset condition	POR

11.1.7 Current measurement chain offset compensation – ADC2_OFFSET_COMP

This register contains an 8 bit signed data (two's complement). The content of the offset compensation register is added directly to the data at the end of the channel measurement, independent on the PGA gain. Even though the current channel is fully offset compensated, the PCB HW introduces an extra offset which can be compensated by means of this data. This register provides several bits which are able to influence the behavior of the coulomb counter.

Table 49. ADC2_OFFSET_COMP

ADC2_OFFSET_COMP																
$07	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	CC_RST_CFG	FREE_CNT	0	0	0	0		ALLCBOFF ON SHORT	ADC2_OFFSET_COMP							
Read			CC_P_OVF	CC_N_OVF	SAMP_OVF	CC_OVT	RESERVED									
Rst	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CC_RST CFG	Description	Configuration of the action linked to the read of coulomb count results
	0	No linked action
	1	Reading any CC register (from @ $2D to @ $2F) also resets the coulomb counters
	Reset condition	POR
FREE_CNT	Description	Configuration of the free running coulomb counters
	0	No free-running, coulomb counters clamp on min/max values
	1	Free-running mode. No clamp but rollover
	Reset condition	POR
CC_P_OVF	Description	Overflow indicator on the COULOMB_CNT1,2[COULOMB_CNT]
	0	No overflow
	1	COULOMB_CNT1,2[COULOMB_CNT] went in overflow
	Reset condition	POR / clear on write 0
CC_N_OVF	Description	Underflow indicator on the COULOMB_CNT1,2[COULOMB_CNT]
	0	No underflow
	1	COULOMB_CNT1,2[COULOMB_CNT] went in underflow
	Reset condition	POR / clear on write 0
SAMP_OVF	Description	Overflow indicator on the CC_NB_SAMPLES
	0	No underflow
	1	CC_NB_SAMPLES went in overflow
	Reset condition	POR / clear on write 0
CC_OVT	Description	Overthreshold indicator on the COULOMB_CNT1,2[COULOMB_CNT]
	0	No over threshold
	1	COULOMB_CNT1,2[COULOMB_CNT] went in over threshold (TH_COULOMB_CNT)
	Reset condition	POR / clear on write 0
ALLCBOFF ON SHORT	Description	All CB's turn off in case of at least one short
	0	Only shorted CB's are turned off
	1	If at least one CB is shorted, all CB's are then turned off (CB_DRVEN is reset)
	Reset condition	POR

ADC2_OFFSET_COMP	Description	Offset value, signed (two's complement) with V_{2RES} resolution. It can be used to compensate for a PCB offset.
	00000000	
	Reset condition	POR

11.1.8 Cell select register – OV_UV_EN

The user has the option to select a common overvoltage and undervoltage threshold, or individual thresholds for each cell. To use a common threshold for all cell terminal inputs, the user must program register TH_ALL_CT and enable the common threshold bit. An individual threshold may be programmed for each cell terminal through register TH_CTx. Either threshold selection requires the CTx_OVUV_EN bit be set for the 33771 to monitor the cell terminal input for over and undervoltage.

Table 50. OV_UV_EN

OV_UV_EN																
$08	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write Read	COMMON_OV_TH	COMMON_UV_TH	CT14_OVUV_EN	CT13_OVUV_EN	CT12_OVUV_EN	CT11_OVUV_EN	CT10_OVUV_EN	CT9_OVUV_EN	CT8_OVUV_EN	CT7_OVUV_EN	CT6_OVUV_EN	CT5_OVUV_EN	CT4_OVUV_EN	CT3_OVUV_EN	CT2_OVUV_EN	CT1_OVUV_EN
Rst	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
COMMON_OV_TH		Description		All CTx measurement use the common overvoltage threshold register for comparison												
		0		Use individual threshold register												
		1		Use common threshold register												
		Reset condition		POR												
COMMON_UV_TH		Description		All CTx measurement use the common undervoltage threshold register for comparison												
		0		Use individual threshold register												
		1		Use common threshold register												
		Reset condition		POR												
CTx_OVUV_EN		Description		Enable or disable ADC data to be compared with thresholds for OV/UV. If disabled no OVUV fault is set.												
		0		OVUV disabled												
		1		OVUV is enabled												
		Reset condition		POR												

11.1.9 Cell terminal overvoltage fault register – CELL_OV_FLT

The CELL_OV_FLT register contains the overvoltage fault status of each cell. The CELL_OV_FLT register is updated with each cyclic conversion and each on demand conversion from the system controller. In normal mode, the CTx_OV_FLT bit may be cleared by writing logic 0 when overvoltage is no longer present at the cell terminal inputs.

Table 51. CELL_OV_FLT

CELL_OV_FLT																
$09	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read			CT14_OV_FLT	CT13_OV_FLT	CT12_OV_FLT	CT11_OV_FLT	CT10_OV_FLT	CT9_OV_FLT	CT8_OV_FLT	CT7_OV_FLT	CT6_OV_FLT	CT5_OV_FLT	CT4_OV_FLT	CT3_OV_FLT	CT2_OV_FLT	CT1_OV_FLT
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CTx_OV_FLT		Description		CTx_OV_FLT register contains the status of the overvoltage fault for each cell terminal. Register is updated with each internal and system controller on demand conversion cycle.												
		0		No Cell Terminal overvoltage												
		1		Cell Terminal overvoltage detected on terminal x												
		Reset condition		POR/clear on write 0												

11.1.10 Cell terminal undervoltage fault register – CELL_UV_FLT

The CELL_UV_FLT register contains the undervoltage fault status of each cell. The CELL_UV_FLT register is updated with each cyclic conversion and each on demand conversion from the system controller. In normal mode, the CTx_UV_FLT bit may be cleared by writing logic 0 when undervoltage is no longer present at the cell terminal inputs.

Table 52. CELL_UV_FLT

CELL_UV_FLT																
$0A	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read			CT14_UV_FLT	CT13_UV_FLT	CT12_UV_FLT	CT11_UV_FLT	CT10_UV_FLT	CT9_UV_FLT	CT8_UV_FLT	CT7_UV_FLT	CT6_UV_FLT	CT5_UV_FLT	CT4_UV_FLT	CT3_UV_FLT	CT2_UV_FLT	CT1_UV_FLT
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CTx_UV_FLT		Description		CTx_UV_FLT register contains the status of the overvoltage fault for each cell terminal. Register is updated with each internal and system controller requested conversion cycle.												
		0		No cell terminal undervoltage												
		1		Cell terminal undervoltage detected on terminal x												
		Reset condition		POR/clear on write 0												

11.1.11 Reserved

Table 53. Reserved

Reserved																
$0B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read																
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.1.12 Cell balance configuration register – CBx_CFG

The cell balance configuration register holds the operating parameters of the cell balance output drivers.

Table 54. CBX_CFG

CBx_CFG																
$0C to $19	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write							CB_EN	CB_TIMER								
Read							CB_STS									
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CBx_EN		Description		Cell balance enable												
		0		Cell balance driver disabled												
		1		Cell balance is enabled or re-launched if overwritten (restarts the timer count from zero and enables the driver)												
		Reset condition		POR												
CBx_STS		Description		Cell balance driver status												
		0		Cell balance driver is off												
		1		Cell balance driver is on												
		Reset condition		POR												
CBx_TIMER		Description		Cell balance timer in minutes												
		000000000		0.5 minutes												
		...														
		111111111		511 minutes												
		Reset condition		POR												

11.1.13 Cell balance open load fault detection register – CB_OPEN_FLT

Table 55. CB_OPEN_FLT

CB_OPEN_FLT																
$1A	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read			CB14_OPEN_FLT	CB13_OPEN_FLT	CB12_OPEN_FLT	CB11_OPEN_FLT	CB10_OPEN_FLT	CB9_OPEN_FLT	CB8_OPEN_FLT	CB7_OPEN_FLT	CB6_OPEN_FLT	CB5_OPEN_FLT	CB4_OPEN_FLT	CB3_OPEN_FLT	CB2_OPEN_FLT	CB1_OPEN_FLT
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CBx_OPEN_FLT		Description		Cell balancing open load detection – (info) Logic OR of CBx_OPEN_FLT is provided in the FAULT2_STATUS[CB_OPEN_FLT]												
		0		No open load cell balance fault detected												
		1		Off state open load detected												
		Reset condition		POR/Clear on write 0												

11.1.14 Cell balance shorted load fault detection register – CB_SHORT_FLT

The cell balance short detection register holds the cell balance shorted load status.

Table 56. CB_SHORT_FLT

CB_SHORT_FLT																
$1B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read			CB14_SHORT_FLT	CB13_SHORT_FLT	CB12_SHORT_FLT	CB11_SHORT_FLT	CB10_SHORT_FLT	CB9_SHORT_FLT	CB8_SHORT_FLT	CB7_SHORT_FLT	CB6_SHORT_FLT	CB5_SHORT_FLT	CB4_SHORT_FLT	CB3_SHORT_FLT	CB2_SHORT_FLT	CB1_SHORT_FLT
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CBx_SHORT_FLT	Description	Cell balancing shorted load fault detection – (info) CBx_SHORT_FLT Ored is provided in the FAULT2[CB_SHORT_FLT]
	0	No shorted load fault detected
	1	Shorted load fault detected
	Reset condition	POR/clear on write 0

11.1.15 Cell balance driver on/off status register – CB_DRV_STS

Table 57. CB_DRV_STS

CB_DRV_STS																
$1C	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write			x	x	x	x	x	x	x	x	x	x	x	x	x	x
Read			CB14_STS	CB13_STS	CB12_STS	CB11_STS	CB10_STS	CB9_STS	CB8_STS	CB7_STS	CB6_STS	CB5_STS	CB4_STS	CB3_STS	CB2_STS	CB1_STS
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CBx_STS		Description		Contains the state of the cell balance driver												
		0		Driver CBx is off												
		1		Driver CBx is on												
		Reset condition		POR												

11.1.16 GPIO configuration register 1 – GPIO_CFG1

The GPIO_CFG1 register programs the individual GPIO port as a ratiometric, single ended, input or output port.

Table 58. GPIO_CFG1

GPIO_CFG1																
$1D	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write			GPIO6_CFG		GPIO5_CFG		GPIO4_CFG		GPIO3_CFG		GPIO2_CFG		GPIO1_CFG		GPIO0_CFG	
Read																
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIOx_CFG		Description		Register controls the configuration of the GPIO port												
		0 0		GPIOx configured as analog input for ratiometric measurement												
		0 1		GPIOx configured as analog input for absolute measurement												
		1 0		GPIOx configured as digital input												
		1 1		GPIOx configured as digital output												
		Reset condition		POR												

11.1.17 GPIO configuration register 2 – GPIO_CFG2

Table 59. GPIO_CFG2

GPIO_CFG2																
$1E	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write							GPIO2_SOC	GPIO0_WU	GPIO0_FLT_ACT	GPIO6_DR	GPIO5_DR	GPIO4_DR	GPIO3_DR	GPIO2_DR	GPIO1_DR	GPIO0_DR
Read																
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO2_SOC	Description	GPIO2 used as ADC1_A/ADC1_B start-of-conversion. Requires GPIO2_CFG = 10.
	0	GPIO2 port ADC trigger is disabled
	1	GPIO2 port ADC trigger is enabled. A rising edge on GPIO2 triggers an ADC1-A and ADC1-B conversion – only when in normal mode
	Reset condition	POR
GPIO0_WU	Description	GPIO0 wake-up capability. Valid only when GPIO0_CFG = 10.
	0	No wake-up capability
	1	Wake-up on any edge, transitioning the system from sleep to normal
	Reset condition	POR
GPIO0_FLT_ACT	Description	GPIO0 activate fault output pin. Valid only when GPIO0_CFG = 10.
	0	Does not activate FAULT pin when GPIO0 is configured as an input and is logic 1
	1	Activates the FAULT pin when GPIO is configured as an input and is logic 1
	Reset condition	POR
GPIOx_DR	Description	GPIOx pin drive. Valid only when GPIOx_CFG = 11 (normal mode), functional in diagnostic mode for OT/UT diagnostics.
	0	Drive GPIOx to low level
	1	Drive GPIOx to high level
	Reset condition	POR

11.1.18 GPIO status register – GPIO_STS

Table 60. GPIO_STS

GPIO_STS																
$1F	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write		0	0	0	0	0	0	0		x	x	x	x	x	x	x
Read		GPIO6_H	GPIO5_H	GPIO4_H	GPIO3_H	GPIO2_H	GPIO1_H	GPIO0_H		GPIO6_ST	GPIO5_ST	GPIO4_ST	GPIO3_ST	GPIO2_ST	GPIO1_ST	GPIO0_ST
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIOx_H		Description		The GPIOx_H bits detects and latches the low to high transition occurring on the GPIOx input												
		0		No high state detected												
		1		A high state has been detected												
		Reset condition		POR/clear on write 0												
GPIOx_ST		Description		Real time GPIOx status												
		0		Report GPIOx at low level												
		1		Report GPIOx at high level												
		Reset condition		POR												

11.1.19 Overtemperature/undertemperature fault register – AN_OT_UT_FLT

Table 61. AN_OT_UT_FLT

AN_OT_UT_FLT																
$20	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Read		AN6_OT	AN5_OT	AN4_OT	AN3_OT	AN2_OT	AN1_OT	AN0_OT		AN6_UT	AN5_UT	AN4_UT	AN3_UT	AN2_UT	AN1_UT	AN0_UT
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Anx_OT	Description	Overtemperature detection for AN n°x – Anx_OT ored is provided in FAULT1_STATUS[AN_OT_FLT]
	0	No overtemperature fault detected
	1	Overtemperature fault detected on Anx
	Reset condition	POR/clear on write 0 (Anx_OT is set again on next cyclic conversion or on demand conversion if overtemperature persists)
Anx_UT	Description	Undertemperature detection for AN n°x – Anx_UT ored is provided in FAULT1_STATUS[AN_UT_FLT]
	0	No undertemperature fault detected
	1	Undertemperature fault detected on Anx
	Reset condition	POR/clear on write 0 (Anx_UT is set again on next cyclic conversion or on demand conversion if undertemperature persists)

11.1.20 GPIO open short register – GPIO_SHORT_ANx_OPEN_STS

Table 62. GPIO_SHORT_ANx_OPEN_STS

GPIO_SHORT_ANx_OPEN_STS																
$21	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Read		GPIO6_SH	GPIO5_SH	GPIO4_SH	GPIO3_SH	GPIO2_SH	GPIO1_SH	GPIO0_SH		AN6_OPEN	AN5_OPEN	AN4_OPEN	AN3_OPEN	AN2_OPEN	AN1_OPEN	AN0_OPEN
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOx_SH	Description	GPIOx short detection GPIOx_SH ored is provided in FAULT2_STATUS[GPIO_SHORT_FLT]
	0	No short detected
	1	Short detected, pad sense is different from pad command
	Reset condition	POR/clear on write 0
ANx_OPEN	Description	Analog inputs open load detection. ANx_OPEN ored is provided in FAULT2_STATUS[AN_OPEN_FLT]
	0	No open load detected
	1	Open load detected on Anx
	Reset condition	POR/Clear On Write 0 (ANx_OPEN is set again with open load detect switch closed and open load persists)

11.1.21 Current measurement status register – I_STATUS

Table 63. I_STATUS

I_STATUS																
$22	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	PGA_DAC															
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PGA_DAC	Description	DAC value used with PGA gain = 256, available after PGA auto zeroing (signed, two's complement, resolution 2.44 µV/LSB). The PGA offset is available at ADC output, so the DAC code is divided by four every time the gain is divided by four, then it is applied at the PGA input.
	0 0 0 0 0 0 0 0	
	1 1 1 1 1 1 1 1	
	Reset condition	POR

11.1.22 Communication status register – COM_STATUS

Table 64. COM_STATUS

COM_STATUS																
$23	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	x															
Read	COM_ERR _COUNT															
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
COM_ERR_COUNT		Description		Number of communication errors detected												
		0 0 0 0 0 0 0 0		0 communication errors have been detected												
		...														
		1 1 1 1 1 1 1 1		255 communication errors have been detected. Overflow of counter sets FAULT1_STATUS[COMM_ERR_OVR_FLT]. Count remains at 255 until cleared by controller.												
		Reset condition		POR/clear on write 0												

11.1.23 Fault status register 1 – FAULT1_STATUS

Table 65. FAULT1_STATUS

FAULT1_STATUS																
$24	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x
Read	POR	RESET_FLT	COM_ERR_OVR_FLT	VPWR_OV_FLT	VPWR_LV_FLT	COM_LOSS_FLT	COM_ERR_FLT	CSB_WUP_FLT	GPIO0_WUP_FLT	I2C_ERR_FLT	IS_OL_FLT	IS_OC_FLT	AN_OT_FLT	AN_UT_FLT	CT_OV_FLT	CT_UV_FLT
Rst	1	0*	0	0	0*	0*	0*	0	0	0	0	0	0	0	0	0
Depending on the voltage conditions occurring on some pins at the IC initialization, the initial value of bits marked by a * may be flipped.																
POR		Description		Power on reset indication (POR)												
		0		No POR												
		1		Device has PORed												
		Reset condition		POR/clear on write 0												
RESET_FLT		Description		RESET Indication (non-maskable)												
		0		No reset												
		1		Device has been reset through the RESET pin or by a write command setting the SYS_CFG1[SOFT_RST] or by a communication loss or an oscillator monitoring fault												
		Reset condition		POR/clear on write 0												
COM_ERR_OVR_FLT		Description		Overflow indicator on the COM_STATUS[COM_ERR_COUNT]												
		0		No error												
		1		COM_STATUS[COM_ERR_COUNT] went in overflow												
		Reset condition		POR/clear on write 0												
VPWR_OV_VLT		Description		VPWR overvoltage notification												
		0		No overvoltage (VPWR < VPWR(OV_FLAG)) detected												
		1		Overvoltage detected (VPWR > VPWR(OV_FLAG), timing filtered)												
		Reset condition		POR/clear on write 0												
VPWR_LV_FLT		Description		VPWR low-voltage notification												
		0		No low-voltage (VPWR > VPWR(LV_FLAG)) detected												
		1		Low-voltage detected (VPWR < VPWR(LV_FLAG), timing filtered)												
		Reset condition		POR/clear on write 0												

COM_LOSS_FLT	Description	In normal mode, each slave device must receive a local message within the programmed period or COM_LOSS_FLT flag is set
	0	No error
	1	Communication loss detected after a reset due to a communication loss
	Reset condition	POR/clear on write 0 (bit is not cleared if reset was caused by a communication loss)
COM_ERR_FLT	Description	Communication error detected
	0	No error
	1	An error has been detected during a communication
	Reset condition	POR/clear on write 0
CSB_WUP_FLT	Description	CBS wake-up notification
	0	No wake-up
	1	CSB wake-up detected
	Reset condition	POR/clear on write 0
GPIO0_WUP_FLT	Description	GPIO0_ wake-up notification
	0	No wake-up
	1	GPIO0 wake-up detected
	Reset condition	POR/clear on write 0
I2C_ERR_FLT	Description	I^2C communication error during the transfer from EEPROM to the IC
	0	No Error
	1	Error detected
	Reset condition	POR/clear on write 0
IS_OL_FLT	Description	ISENSE pins open load detected
	0	No open load detected
	1	Open load detected in one or both ISENSE pins
	Reset Condition	POR/ clear on write 0
IS_OC_FLT	Description	ISENSE overcurrent detected (sleep mode only)
	0	No overcurrent detected
	1	Overcurrent detected from ISENSE inputs
	Reset condition	POR/Clear On write 0
AN_OT_FLT	Description	Analog input overtemperature detection
	0	No overtemperature detected
	1	Overtemperature detected in one or more of the Anx analog inputs
	Reset condition	POR/Clear On Write 0 all AN_OT_UT[Anx_OT] bits
AN_UT_FLT	Description	Analog inputs undertemperature detection
	0	No undertemperature detected
	1	Undertemperature detected in at least one of the seven analog inputs
	Reset condition	POR/Clear On Write 0 all AN_OT_UT[ANx_UT] bits
CT_OV_FLT	Description	Cell terminal overvoltage detection
	0	No overvoltage detected
	1	Overvoltage detected in one or more of the 14 cell terminals
	Reset condition	POR/clear on write 0 all CELL_OV[CTx_OV] bits
CT_UV_FLT	Description	Cell terminal undervoltage detection
	0	No undervoltage detected
	1	Undervoltage detection in at least one of the 14 cell terminals
	Reset condition	POR/clear on write 0 all CELL_UV[CTx_UV] bits

11.1.24 Fault status register 2 – FAULT2_STATUS

Table 66. FAULT2_STATUS

FAULT2_STATUS																
$25	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	0	0	0	0	0	0	0	0	x	x	x	x	x	0	0	0
Read	VCOM_OV_FLT	VCOM_UV_FLT	VANA_OV_FLT	VANA_UV_FLT	ADC1_B_FLT	ADC1_A_FLT	GND_LOSS_FLT	IC_TSD_FLT	IDLE_MODE_FLT	AN_OPEN_FLT	GPIO_SHORT_FLT	CB_SHORT_FLT	CB_OPEN_FLT	OSC_ERR_FLT	DED_ERR_FLT	FUSE_ERR_FLT
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCOM_OV_FLT	Description	VCOM overvoltage notification
	0	No overvoltage detected
	1	Overvoltage has been detected on VCOM supply
	Reset condition	POR/clear on write 0
VCOM_UV_FLT	Description	VCOM undervoltage notification
	0	No undervoltage detected
	1	Undervoltage has been detected on VCOM supply
	Reset Condition	POR/clear on write 0
VANA_OV_FLT	Description	VANA overvoltage notification
	0	No overvoltage detected
	1	Overvoltage has been detected on the VANA supply
	Reset condition	POR/clear on write 0
VANA_UV_FLT	Description	VANA undervoltage notification
	0	No undervoltage detected
	1	Undervoltage has been detected on the VANA supply
	Reset condition	POR/clear on write 0
ADC1_B_FLT	Description	ADC1_B fault notification
	0	No fault detected
	1	ADC1_B fault (over or undervoltage has been detected on MEAS_VBG_DIAG_ADC1B)
	Reset condition	POR/clear on write 0
ADC1_A_FLT	Description	ADC1_A fault notification
	0	No fault detected
	1	ADC1_A fault (over or undervoltage has been detected on MEAS_VBG_DIAG_ADC1A)
	Reset condition	POR/clear on write 0
GND_LOSS_FLT	Description	Loss of ground has been detected on DGND or AGND
	0	No error
	1	Loss of ground detected
	Reset condition	POR/clear on write 0
IC_TSD_FLT	Description	IC thermal limitation notification
	0	No thermal limitation detected
	1	Thermal limitation detected
	Reset condition	POR/clear on write 0
IDLE_MODE_FLT	Description	IDLE mode notification
	0	No notification
	1	The system has transitioned through idle mode
	Reset condition	POR/clear on write 0

AN_OPEN_FLT	Description	Analog inputs open load detection
	0	No open load detected
	1	Open load detected in one of the seven analog inputs
	Reset condition	POR/clear on write 0 all GPIO_SHORT_ANx_OPEN_STS[ANx_OPEN] bits
GPIO_SHORT_FLT	Description	GPIO short detection
	0	No short detected
	1	Short detected in one or more of the seven GPIOs, pad sense is different from pad command
	Reset condition	POR/clear on write 0 all GPIO_SHORT_ANx_OPEN_STS (GPIOx_SH) bits
CB_SHORT_FLT	Description	Cell balance short-circuit detection
	0	No short-circuit detected
	1	On state short-circuit detected in one or more of the 14 cell balancing switches
	Reset condition	POR/clear on write 0 all CB_SHORT_FLT[CBx_SHORT] bits
CB_OPEN_FLT	Description	Cell balancing open load detection
	0	No cell balance open load detected
	1	Off state open load detected in one or more of the 14 cell balancing switches
	Reset condition	POR/clear on write 0 all CB_OPEN_FLT[CBx_OPEN] bits
OSC_ERR_FLT	Description	Low-power oscillator error
	0	No error
	1	The low-power oscillator frequency is out of range after a reset due to an oscillator monitoring fault
	Reset condition	POR/clear on write 0 (bit is not cleared if reset was caused by an oscillator monitoring fault)
DED_ERR_FLT	Description	ECC error, double error detection
	0	No error
	1	A double error has been detected (and only one corrected) in the fuses
	Reset condition	POR/clear on write 0
FUSE_ERR_FLT	Description	Error in the loading of fuses
	0	No error
	1	The lock bit was not set after loading, meaning transfer of the fuse values is aborted
	Reset condition	POR/clear on write 0

11.1.25 Fault status register 3 – FAULT3_STATUS

Table 67. FAULT3_STATUS

FAULT3_STATUS																
$26	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read	CC_OVR_FLT	DIAG_TO_FLT	EOT_CB14	EOT_CB13	EOT_CB12	EOT_CB11	EOT_CB10	EOT_CB9	EOT_CB8	EOT_CB7	EOT_CB6	EOT_CB5	EOT_CB4	EOT_CB3	EOT_CB2	EOT_CB1
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CC_OVR_FLT	Description	Overflow indicator on the COULOMB_CNT1,2[COULOMB_CNT] or CC_NB_SAMPLES
	0	No error
	1	COULOMB_CNT1,2[COULOMB_CNT] or CC_NB_SAMPLES went in overflow
	Reset condition	POR /Clear On Write 0 CC_P_OVF,CC_N_OVF, SAMP_OVF and CC_OVT
DIAG_TO_FLT	Description	Timeout of diagnostic state
	0	No timeout
	1	The system has exited itself from diagnostic state after timeout
	Reset condition	POR/clear on write 0
EOT_CBx	Description	End of time cell balancing notification – indicates when a cell balance timer has expired and driver has been shutoff
	0	Cell balance timer has not timed out
	1	Cell balance timer has timed out
	Reset condition	POR/clear on write 0

11.1.26 Fault mask register 1 – FAULT_MASK1

The FAULT_MASK1 register allows the user to selectively mask fault bits associated to the FAULT1_STATUS register. Masking a certain fault bit has the effect of preventing this bit from activating the FAULT output pin.

Table 68. FAULT_MASK1

FAULT_MASK1																
$27	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write				MASK_12_F	MASK_11_F	MASK_10_F	MASK_9_F	MASK_8_F	MASK_7_F	MASK_6_F	MASK_5_F	MASK_4_F	MASK_3_F	MASK_2_F	MASK_1_F	MASK_0_F
Read																
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MASK_x_F	Description	Prevent the corresponding flags in FAULT1_STATUS to activate the FAULT pin
	0	The flag in position (x) activates the FAULT pin
	1	No activation
	Reset condition	POR

11.1.27 Fault mask register 2 – FAULT_MASK2

The FAULT_MASK2 register allows the user to selectively mask fault bits associated to the FAULT2_STATUS register. Masking a certain fault bit has the effect of preventing this bit from activating the FAULT output pin.

Table 69. FAULT_MASK2

FAULT_MASK2																
$28	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write Read	MASK_15_F	MASK_14_F	MASK_13_F	MASK_12_F	MASK_11_F	MASK_10_F	MASK_9_F			MASK_6_F	MASK_5_F	MASK_4_F	MASK_3_F	MASK_2_F	MASK_1_F	MASK_0_F
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MASK_x_F		Description		Prevent the corresponding flags in FAULT2_STATUS to activate the FAULT pin												
		0		The flag in position (x) activates the FAULT pin												
		1		No activation												
		Reset condition		POR												

11.1.28 Fault mask register 3 – FAULT_MASK3

The FAULT_MASK3 register allows the user to selectively mask fault bits associated to the FAULT3_STATUS register. Masking a certain fault bit has the effect of preventing this bit from activating the FAULT output pin.

Table 70. FAULT_MASK3

FAULT_MASK3																
$29	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write Read	MASK_15_F	MASK_14_F	MASK_13_F	MASK_12_F	MASK_11_F	MASK_10_F	MASK_9_F	MASK_8_F	MASK_7_F	MASK_6_F	MASK_5_F	MASK_4_F	MASK_3_F	MASK_2_F	MASK_1_F	MASK_0_F
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MASK_x_F		Description		Prevent the corresponding flags in FAULT3_STATUS to activate the FAULT pin												
		0		The flag in position (x) activates the FAULT pin												
		1		No activation												
		Reset condition		POR												

11.1.29 Wake-up mask register 1 – WAKEUP_MASK1

The WAKEUP_MASK1 register allows to disable wake-up events related to several FAULT1_STATUS fault bits. If a certain bit contained in the latter register is not masked by the corresponding bit of the former register, the IC transitions from sleep mode to normal mode.

Table 71. WAKEUP_MASK1

WAKEUP_MASK1																
$2A	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write Read				MASK_12_F	MASK_11_FK			MASK_8_F	MASK_7_F			MASK_4_F	MASK_3_F	MASK_2_F	MASK_1_F	MASK_0_F
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MASK_x_F		Description		Prevent the corresponding flags in FAULT1_STATUS to wake-up the device												
		0		The flag in position (x) wakes the device up, when active												
		1		No wake-up is possible by this source												
		Reset condition		POR												

11.1.30 Wake-up mask register 2 – WAKEUP_MASK2

The WAKEUP_MASK2 register disables wake-up events related to several FAULT2_STATUS fault bits. If a certain bit contained in the latter register is not masked by the corresponding bit of the former register, the IC transitions from sleep mode to normal mode.

Table 72. WAKEUP_MASK2

WAKEUP_MASK2																
$2B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write Read	MASK_15_F	MASK_14_F	MASK_13_F	MASK_12_F	MASK_11_F	MASK_10_F	MASK_9_F	MASK_8_F			MASK_5_F	MASK_4_F		Mask_2_F	MASK_1_F	
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MASK_x_F		Description		Prevent the corresponding flags in FAULT2_STATUS to wake-up the device												
		0		The flag in position (x) wakes the device, when active												
		1		No wake-up is possible by this source												
		Reset condition		POR												

11.1.31 Wake-up mask register 3 – WAKEUP_MASK3

The WAKEUP_MASK3 register allows to disable wake-up events related to several FAULT3_STATUS fault bits. If a certain bit contained in the latter register is not masked by the corresponding bit of the former register, the IC transitions from sleep mode to normal mode.

Table 73. WAKEUP_MASK3

WAKEUP_MASK3																
$2C	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write Read	MASK_15_F		MASK_13_F	MASK_12_F	MASK_11_FK	MASK_10_F	MASK_9_F	MASK_8_F	MASK_7_F	MASK_6_F	MASK_5_F	MASK_4_F	MASK_3_F	MASK_2_F	MASK_1_F	MASK_0_F
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MASK_x_F		Description		Prevent the corresponding flags in FAULT3_STATUS to wake-up the device												
		0		The flag in position (x) wakes the device, when active												
		1		No wake-up is possible by this source												
		Reset condition		POR												

11.1.32 Coulomb count number of samples register – CC_NB_SAMPLES

The CC_NB_SAMPLES register contains the 16 bit value, which represents the number of samples accumulated in the coulomb counter at the moment of copying its value to the COULOMB_CNT registers.

Table 74. CC_NB_SAMPLES

CC_NB_SAMPLES																
$2D	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	CC_NB_SAMPLES															
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CC_NB_SAMPLES	Description	Number of samples accumulated for the coulomb count value
	Reset condition	POR / ADC_CFG[CC_RST]

11.1.33 Coulomb count register – COULOMB_CNT

The COULOMB_CNT register contains the current 32 bit value of the accumulated current samples. Data representation is signed two's complement, with V_{2RES} resolution. Division of ΔCOULOMB_CNT by ΔCC_NB_SAMPLES provides the average current, where the operator Δ denotes the variation over two different readings of a state. Subsequent multiplication by the corresponding elapsed time Δt provides the charge flowed out/in of the battery.

Table 75. COULOMB_CNT1

COULOMB_CNT1																
$2E	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	COULOMB_CNT_MSB															
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
COULOMB_CNT_MSB		Description		Coulomb counting accumulator												
		Reset condition		POR/ADC_CFG[CC_RST]												

Table 76. COULOMB_CNT2

COULOMB_CNT2																
$2F	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	COULOMB_CNT_LSB															
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
COULOMB_CNT_LSB		Description		Coulomb counting accumulator												
		Reset condition		POR / ADC_CFG[CC_RST]												

11.1.34 Current measurement registers – MEAS_ISENSE1 and MEAS_ISENSE2

The MEAS_ISENSEx registers contain the signed two's complement value of the battery current measured on demand.

Table 77. MEAS_ISENSE1

MEAS_ISENSE1																
$30	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	DATA_RDY	MEAS_I _MSB														
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DATA_RDY	Description	This bit is set when the conversion is complete and the register is updated. The Data_Rdy bit is cleared when a request to convert is received either through the SOC or GPIO2 convert trigger.
	0	A new sequence of conversions is currently running
	1	A data is available in MEAS_ISENSE1
	Reset condition	POR
MEAS_I_MSB	Description	ISENSE value, compensated in gain and temp, signed
	Reset condition	POR

Table 78. MEAS_ISENSE2

MEAS_ISENSE2																
$31	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	0															
Read	DATA_RDY						PGA_GAIN		ADC2_SAT	PGA_GCHANGE			MEAS_I _LSB			
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DATA_RDY		Description		This bit is set when the conversion is complete and the register is updated. The Data_Rdy bit is cleared when a request to convert is received either through the SOC or GPIO2 convert trigger.												
		0		A new sequence of conversions is currently running												
		1		A data is available in MEAS_ISENSE2												
		Reset condition		POR												
PGA_GAIN		Description		Report the current gain of the ADC2 programmable gain amplifier (automatically settled or not)												
		0 0		4												
		0 1		16												
		1 0		64												
		1 1		256												
		Reset condition		POR												
ADC2_SAT		Description		ADC2 saturation information												
		0		No saturation reported												
		1		ADC2 has saturated during the ISENSE on demand conversion												
		Reset condition		POR/clear on write 0												
PGA_GCHANGE		Description		PGA gain change information during ISENSE on demand conversion												
		0		No gain change during ISENSE on demand measurement; result is accurate												
		1		The PGA gain has changed between the two chopped measurements												
		Reset condition		POR/clear on write 0												
MEAS_I _LSB		Description		ISENSE value, compensated in gain and temp, signed												
		Reset condition		POR												

11.1.35 Measurement registers – MEAS_xxxx

The MEAS_xxxx registers contain the measured values as a result of on demand conversions. Note that the cyclic conversions leave no trace in these registers, as they are only used to update the OV/UV/OT/UT flags and other status information.

Table 79. MEAS_xxxx

MEAS_xxxx																
$32 to $4A	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	DATA_RDY	MEAS_xxxx														
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DATA_RDY		Description		This bit is set when the conversion is complete and the register is updated. The Data_Rdy bit is cleared when a request to convert is received either through the SOC or GPIO2 convert trigger.												
		0		A new sequence of conversions is currently running												
		1		A data is available in MEAS_xxxx												
		Reset condition		POR												
MEAS_xxxx		Description		Value is unsigned, resolution is $V_{CT\_ANx\_RES}$ independently on the selected resolution of ADC_CFG												
		Reset condition		POR												

11.1.36 Overvoltage undervoltage threshold register – TH_ALL_CT

Resolution for OV threshold and UV threshold are, respectively, $V_{CTOV(TH)}$ and $V_{CTUV(TH)}$.

Table 80. TH_ALL_CT

TH_ALL_CT																
$4B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	ALL_CT_OV_TH								ALL_CT_UV_TH							
Read																
Rst	1	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0
ALL_CT_OV_TH		Description		Overvoltage threshold setting for all cell terminals. Enabled through register OV_UV_EN												
		11010111		Default overvoltage threshold set to 4.2 V												
		Reset condition		POR												
ALL_CT_UV_TH		Description		Undervoltage threshold setting for all cell terminals. Enabled through register OV_UV_EN												
		10000000		Default undervoltage threshold set to 2.5 V												
		Reset condition		POR												

11.1.37 Overvoltage undervoltage threshold register – TH_CTx

Table 81. TH_CTX

TH_CTx																
$4C to $59	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	CTx_OV_TH								CTx_UV_TH							
Read																
Rst	1	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0

CTx_OV_TH	Description	Overvoltage threshold setting for individual cell terminals. OV_UV_EN[COMMON_OV_TH] bit must be logic 0 and OV_UV_EN[CTx_OVUV_EN] bit must be logic 1 to use TH_CTx register as threshold.
	11010111	Default overvoltage threshold set to 4.2 V
	Reset condition	POR
CTx_UV_TH	Description	Undervoltage threshold setting for individual cell terminals. OV_UV_EN[COMMON_UV_TH] bit must be logic 0 and OV_UV_EN[CTx_OVUV_EN] bit must be logic 1 to use TH_CTx register as threshold.
	10000000	Default undervoltage threshold set to 2.5 V
	Reset condition	POR

11.1.38 Overtemperature, undertemperature threshold registers – TH_Anx_OT, TH_Anx_UT

Registers TH_Anx_OT and TH_Anx_UT contain the individually programmed overtemperature and undertemperature value for each analog input.

Table 82. TH_ANX_OT

TH_Anx_OT																
$5A to $60	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write							ANx_OT_TH									
Read																
Rst	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	1
Anx_OT_TH		Description		Overtemperature threshold setting for analog input x												
		0011101101		Overtemperature default set to 1.16 V												
		Reset condition		POR												

Table 83. TH_ANX_UT

TH_Anx_UT																
$61 to $67	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write							ANx_UT_TH									
Read																
Rst	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	0
Anx_UT_TH		Description		Undertemperature threshold setting for analog input x												
		1100001110		Undertemperature default set to 3.82 V												
		Reset condition		POR												

11.1.39 Overcurrent threshold register – TH_ISENSE_OC

Registers TH_ISENSE_OC contains the programmed overcurrent threshold in sleep mode.

Table 84. TH_ISENSE_OC

TH_ISENSE_OC																
$68	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write					TH _ISENSE_OC											
Read																
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TH_ISENSE_OC		Description		Sleep mode ISENSE overcurrent threshold, unsigned. Resolution is 1.2 µV/LSB.												
		Reset condition		POR												

11.1.40 Over coulomb counter threshold registers – TH_COULOMB_CNT

The coulomb counter threshold in sleep mode is given by the following two registers.

Table 85. TH_COULOMB_CNT_MSB

TH_COULOMB_CNT_MSB																
$69	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	TH_COULOMB_CNT_MSB															
Read																
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TH_COULOMB_CNT_MSB		Description		Over coulomb counting accumulator threshold (MSB)												
		Reset condition		POR												

Table 86. TH_COULOMB_CNT_LSB

TH_COULOMB_CNT_LSB																
$6A	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	TH_COULOMB_CNT_LSB															
Read																
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TH_COULOMB_CNT_LSB		Description		Over coulomb counting accumulator threshold (LSB). Resolution is V_{2RES}.												
		Reset condition		POR												

11.1.41 Silicon revision register – SILICON_REV

Table 87. SILICON_REV

SILICON_REV																
$6B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read											FREV			MREV		
Rst	0	0	0	0	0	0	0	0	0	0	F	F	F	M	M	M
FREV		Description		Full mask revision												
		001		Pass 1.x												
		010		Pass 2.x												
		…														
		Reset condition		POR												
MREV		Description		Metal mask revision												
		000		Pass y.0												
		001		Pass y.1												
		…														
		Reset condition		POR												

11.1.42 EEPROM communication register EEPROM_CTRL

Table 88. EEPROM_CTRL

EEPROM_CTRL																
$6C	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	R/W	EEPROM_ADD							DATA_TO_WRITE							
Read	BUSY	ERROR	EE_PRESENT						READ_DATA							
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W		Description		Read/write bit, directs the 33771 to read or write from EEPROM												
		0		Write												
		1		Read												
		Reset condition		POR												
EEPROM_ADD		Description		EEPROM address to read or write												
		Reset condition		POR												
DATA_TO_WRITE		Description		Data to be written into the EEPROM												
		Reset condition		POR												
BUSY		Description		Busy bit												
		0		Indicates the IC has completed the EEPROM read or write operation												
		1		Indicates the IC is in the process of performing the EEPROM read or write operation.												
		Reset condition		POR												

ERROR	Description	EEPROM communication error bit.
	0	No error occurred during the communication to EEPROM
	1	An error occurred during the communication to EEPROM
	Reset condition	POR
EE_PRESENT	Description	EEPROM detection
	0	No EEPROM detected
	1	EEPROM has been detected and present
	Reset condition	POR
READ_DATA	Description	Data read in the EEPROM at address given by EEPROM_ADD
	Reset condition	POR

11.1.43 ECC signature 1 register

Table 89. DED_ENCODE1

DED_ENCODE1																
$6D	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	X															
Read	DED_HAMMING_COUT1_31_16															
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DED_HAMMING_COUNT1_31_16		Description		Reports the 16 MSBits to encode in the fuse matrix (ECC) – customer side												
		Reset condition		POR												

11.1.44 ECC signature 2 register

Table 90. DED_ENCODE2

DED_ENCODE2																
$6E	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	X															
Read	DED_HAMMING_COUT_1_15_0															
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DED_HAMMING_COUT_1_7_0		Description		Report the 16 LSBits to encode in the fuse matrix (ECC) - customer side												
		Reset condition		POR												

11.1.45 FUSE mirror and data control

Table 91. FUSE_MIRROR_DATA

FUSE_MIRROR_DATA																
$6F	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	FMR_DATA															
Read																
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FMR_DATA		Description		Fuse mirror data to read or write												
		Reset condition		POR												

Table 92. FUSE_MIRROR_CNTL

FUSE_MIRROR_CNTL																
$70	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write				FMR_ADDR									FSTM	FST		
Read	SEC_ERR_FLT												0	FST_ST		
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SEC_ERR_FLT		Description		ECC error, single error correction												
		0		No error												
		1		A single error has been detected and corrected. The IC is usable, must not be considered defective.												
		Reset condition		POR/clear on write 0												
FMR_ADDR		Description		Fuse mirror register address												
		Reset condition		POR												
FSTM		Description		Fuse state write mask. This bit controls the write access to the FST[2:0] bits.												
		0														
		1														
		Reset condition		POR												
FST		Description		Fuse state control. write to this register controls the switching of the fuse state machine. Read in this register enables tracing the current state.												
		0 0 0														
		1														
		Reset condition		POR												
FST_ST		Description		Fuse state control. Read in this register enables to trace the current state												
		0 0 0														
		1														
		Reset condition		POR												

11.1.46 Reserved

Table 93. RESERVED

Reserved																
$71 to $FF	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	Reserved															
Rst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.1.47 Fuse bank

Table 94. FUSE_BANK

Bank address	Data															
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	GCF_cold_c13						GCF_room_c13									
1	GCF_cold_c11						GCF_room_c11									
2	GCF_cold_c9						GCF_room_c9									
3	GCF_cold_c7						GCF_room_c7									
4	GCF_cold_c5						GCF_room_c5									
5	GCF_cold_c3						GCF_room_c3									
6	cold_c2vs1						GCF_room_c1									
7	GCF_hot_c13						GCF_hot_i256					GCF_cold_i256				
8	GCF_hot_c11						GCF_hot_i64					GCF_cold_i256				
9	GCF_hot_c9						GCF_hot_i16					GCF_cold_i16				
10	GCF_hot_c7						GCF_hot_i4					GCF_cold_i4				
11	GCF_hot_c5						GCF_ANx_ratio					room_c14vs13		hot_c14vs13		
12	GCF_hot_c3						hot_c2vs1					room_c12vs11		hot_c12vs11		
13		c2_offset		cold_c14vs13		cold_c12vs11		cold_c10vs9		cold_c6vs5		room_c10vs9		hot_c10vs9		
14	GCF_hot_c1							cold_c8vs7		cold_c4vs3		room_c8vs7		hot_c8vs7		
15	GCF_stack							room_c2vs1				room_c6vs5		hot_c6vs5		
16	GCF_cold_c1							GCF_IcTemp				room_c4vs3		hot_c4vs3		
17	cold_Vbgtj2vs1							GCF_i256								
18	cold_Vbgtj1vs1							GCF_i64								
19	hot_Vbgtj2vs1							GCF_i16								
20	hot_Vbgtj1vs1							GCF_i4								
21	room_Vbgtj2vs1									room_Vbgtj1vs1						
22	DED_ENCODE 1															
23	DED_ENCODE 2															
24	Traceability															
25	Traceability															
26	Reserved											Traceability				
27	Reserved															
28	Reserved															
29	Reserved															
30	Reserved															
31	Reserved															

12 Safety

12.1 Safety features table

A comprehensive list of safety features has been implemented in the MC33771. It can be used to achieve the required system automotive safety integrity level, for example, ASIL C with a single 33771 per cluster. Use of two 33771 per cluster allows easy achievement of ASIL D.

Table 95. User safety feature summary

Safety feature	Normal mode	Sleep mode	Sleep mode (during cyclic wake-up)	Diagnostic mode	Fault detected	Method and action
VPWR OV/UV	X		X	X	VPWR overvoltage and undervoltage	VPWR_OV_FLT or VPWR_UV_FLT flag activated, FAULT pin activated, bus wake-up
Cell OV/UV detection	X		X	With on demand conversion	Cell overvoltage and undervoltage	CT_OV_FLT or CT_UV_FLT error flag activated, FAULT pin activated, bus wake-up
OT/UT detection	X		X	With on conversion	External over/undertemperature	AN_OV_FLT or AN_UV_FLT error flag activated, FAULT pin activated, bus wake-up
FAULT pin heart beat	X	X	X	X	FAULT pin in stuck at 0 or 1	FAULT pin toggles if no fault; FAULT pin stuck at logic 1 if fault is present
CTx OV/UV functional verification				MCU control	Fault on digital comparators used for OV/UV detection	If no fault, then CTx_OV_FLT or CTx_OV_FLT activated; else missing activation. FAULT pin activated.
CTx open detection				MCU control	Open path from a cell to a CT pin	MCU checks cell voltages after diagnostic switch positioning. A value close to 0 V means open line.
CTx open detection functional verification				MCU control	Broken switch of CTx open detection safety mechanism	MCU checks cell voltages against expected results to detect a latent fault
CTx leakage test				MCU control	MCU verifies the input structures on the CTx pins have not degraded by measuring the input leakage	If the MCU detects leakages exceeding the OV/U safety margin
Cell voltage channel functional verification				MCU control	Lack of integrity of level-shifters embedded in the analog front end	MCU checks voltages of diagnostic Zener diodes against voltage of the reference Zener diode
ADC1-A, ADC1-B functional verification (precision reference to ADC)	X			With on demand conversion	ADC out of compliance due to voltage reference deviation or other error	MEAS_VBG_DIAG_ADC1A and MEAS_VBG_DIAG_ADC1B are compared with $ADC1a_{FV}$ and $ADC1b_{FV}$. See Section 9.5 "ADC1-A and ADC1-B functional verification".
Oscillator clock monitoring	X	X	X	X	Low frequency clock failure	OSC_ERR_FLT flag activated, FAULT pin activated

Safety feature	Normal mode	Sleep mode	Sleep mode (during cyclic wake-up)	Diagnostic mode	Fault detected	Method and action
Cell balance shorted load protection/ detection	X	X	X	X	Overcurrent condition on CB switches	CB_SHORT_FLT error flag activated, FAULT pin activated, bus wake-up
Cell balance open detection				MCU Control	Open cell balance circuit	CB_OPEN_FLT error flag activated. FAULT pin activated.
End of time CB notification (EOT_CBx)	X	X	X	X	Expiration of a cell balance timer	EOT_CBx flag activated. FAULT pin activated, bus wake-up
ISENSE ± precision reference				MCU Control	Current measurement out of compliance due to PGA or ADC2 or digital processing failure	Conversion of a known reference at the input of the PGA. MCU checks for an expected value.
ISENSE ± open detect				MCU control	Open circuit on ISENSE± input pins	Pin current injection. IS_OL_FLT error flag. FAULT pin activated.
ISENSE ± overcurrent fault			X		Overcurrent condition during sleep mode	I_OC_FLT error flag. FAULT pin activated, bus wake-up
Coulomb counter overflow	X		X	X	Overflow on the coulomb count registers	CC_OVR_ FLT error flag. FAULT pin activated
VCOM short/ UV protection detection	X		X	X	Undervoltage on the VCOM power supply	FAULT pin activated
VANA short/ UV protection detection	X		X	X	Undervoltage on the VANA power supply	VANA_UV_FLT flag, FAULT pin activated, bus wake-up
VANA short/ OV protection detection	X		X	X	Overvoltage on the VANA power supply	VANA_OV_FLT error flag. FAULT pin activated, bus wake-up
GPIO short detection protection	X		X	MCU control	GPIO opposite of the commanded state	GPIO_SH_FLT error flag. FAULT pin activated, bus wake-up
GPIO open detection	X			MCU control	Disconnected analog input	AN_OPEN_FLT error flag. FAULT pin activated.
Onboard temperature protection mode	X		X	X	Overtemperature of the silicon	FAULT pin activated: bus wake-up and IC_TSD_FLT error flag activated when normal temperature resumes
Exit diagnostic mode safety timer				X	Unauthorized permanence in diagnostic mode	Trace left in the PREVIOUS_STATE upon timer expiration
Idle mode fault (init to idle)					Indicator the device has entered idle mode without being programmed	FAULT pin activated for time period
Loss of ground detection has a fault bit and can generate a wake-up. No activation of output.	X	X	X	X	Loss of ground on DGND and AGND pins	FAULT pin activated, bus wake-up

Safety feature	Normal mode	Sleep mode	Sleep mode (during cyclic wake-up)	Diagnostic mode	Fault detected	Method and action
TAG ID for conversion data	X			X	Wrong sequencing of the requested conversions	MCU detects incorrect TAG ID in the message
Register address identification in message frame	X			X	Faulty decoder of data register addressing	MCU detects an incorrect physical address
Eight bit CRC with non-zero seed	X			X	Corrupted communication frame	MCU/33771 detect incorrect CRC
Unique identifiable start-of message and end-of-message	X			X	Wrong message delimitation	MCU/33771 detect incorrect message frame
Communication confirmation architecture	X			X	R/W register bits stuck at 0/1	MCU checks received data content after a write command
Communication loss fault	X			X	Stopped or slow communication from the MCU to the IC	COM_LOSS_FLT flag. FAULT pin activate
Communication error register overflow	X			X	Incorrect number of bits of the frame, incorrect clock phase	COM_ERR_FLT fault flag. FAULT pin activated
I^2C error fault (init mode)	X			X	Error when trying to load EEPROM data into memory mirror	I2C_ERR_FLT error flag. FAULT pin activated
ECC check	X	X	X	X	Corrupted calibration data. A double error has been detected (and only one corrected)	DED_ERR_FLT error flag. FAULT pin activated

VANA undervoltage, causing the activation of the FAULT2_STATUS[VANA_UV_FLT] error flag, automatically masks the detection of following faults:

FAULT1_STATUS[VPWR_OV_FLT]
FAULT1_STATUS[AN_UT_FLT]
FAULT1_STATUS[CT_OV_FLT]
FAULT2_STATUS[VANA_OV_FLT]
FAULT2_STATUS[ADC1_A_FLT]
FAULT2_STATUS[ADC1_B_FLT]

12.2 FAULT pin daisy chain operation

The FAULT pin may be programmed to provide the battery management system with a safety pulse heart beat. Two behaviors are possible. One is based on logic levels: low level indicates normal condition, high level reveals a faulty condition. The other possibility is based on the heart beat feature, which provides a higher integrity level.

Both modes can be activated in normal mode, sleep mode, and diagnostic mode. This heart beat signal is made into a current source and daisy chained to the next lower 33771 GPIO0 port. Subsequent 33771 devices are programmed to pass the heart beat through to the next device in the system. In this configuration, any fault detected by each 33771 in the system activates the FAULT line.

To configure the 33771 for daisy chain fault output, set the GPIO0 port as an input.

1. Set GPIO0 as an input GPIO0_CFG = 10.
2. Disable wake-up on GPIO0 with GPIO0_WU = 0.
3. Set GPIO0 to propagate signal to FAULT pin with GPIO0_FLT_ACT = 1.

To use the 33771 heart beat feature, the user must write a 1 in the SYS_CFG1[FAULT_WAVE] bit. The signaling square wave has constant on time, whereas the desired off time may be selected by writing a proper value in the SYS_CFG1[WAVE_DC_BITx] configuration field.

The usage of the fault pin is essential if the IC uses SPI communication and has to provide some monitoring functionality in sleep mode. In this condition the fault line is the only means to alert the system controller about an occurred fault, while in TPL mode, even if the IC is sleeping, it has the chance to send a wake-up signal through the bus. The fault line usage is optional in normal and diagnostic modes, as well as in sleep mode and TPL configuration; it is necessary in case of sleep mode with monitoring and SPI mode.

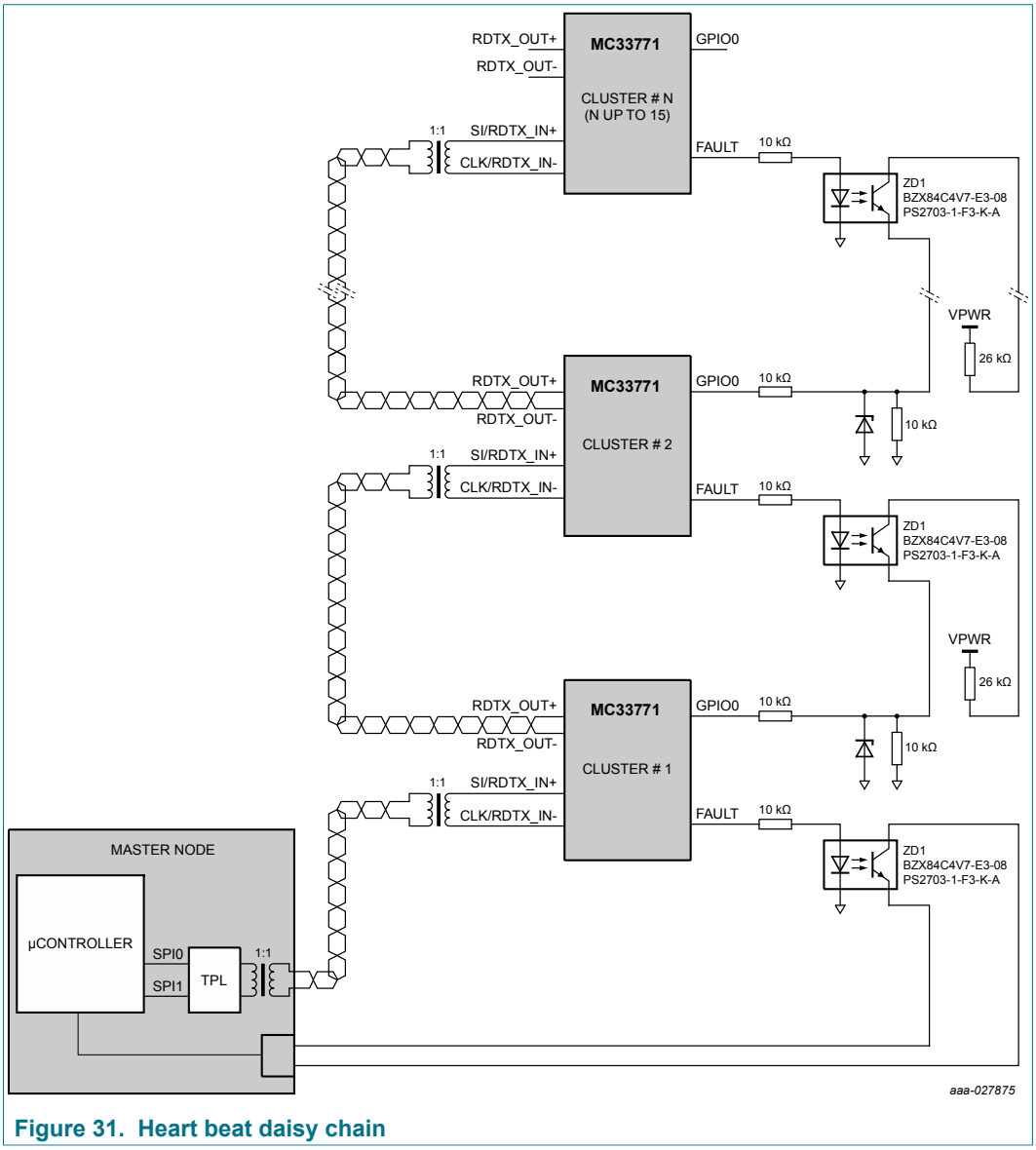


Figure 31. Heart beat daisy chain

13 Typical applications

13.1 Introduction

NXP Semiconductors has developed a battery cell controller IC supporting both centralized and distributed battery management architectures. Centralized battery monitoring systems contain a controller module sensing individual differential cell voltages through a wiring harness. Distributed systems locate monitoring devices close to the lithium-ion batteries and use a communication interface to transfer data to the main controller MCU.

13.1.1 Centralized battery management system

A centralized system is comprised of a single transformer driver and isolation transformers between each battery cell controller IC.

The communication system is a half duplex 2.0 MHz daisy chain master/slave network. The MC33664 transformer physical layer creates a phase encoded signal based on the bit pattern it receives from the MCU SPI transmit port. During initialization each 33771 device is assigned a specific address. With the system initialized, messages sent from the MCU are received by each 33771 in the daisy chain. Only the 33771 with the correct address acts upon and responds to the message. The phase encoded response generated by the 33771 are received by the MC33664 transceiver and converted to a SPI message for the MCU.

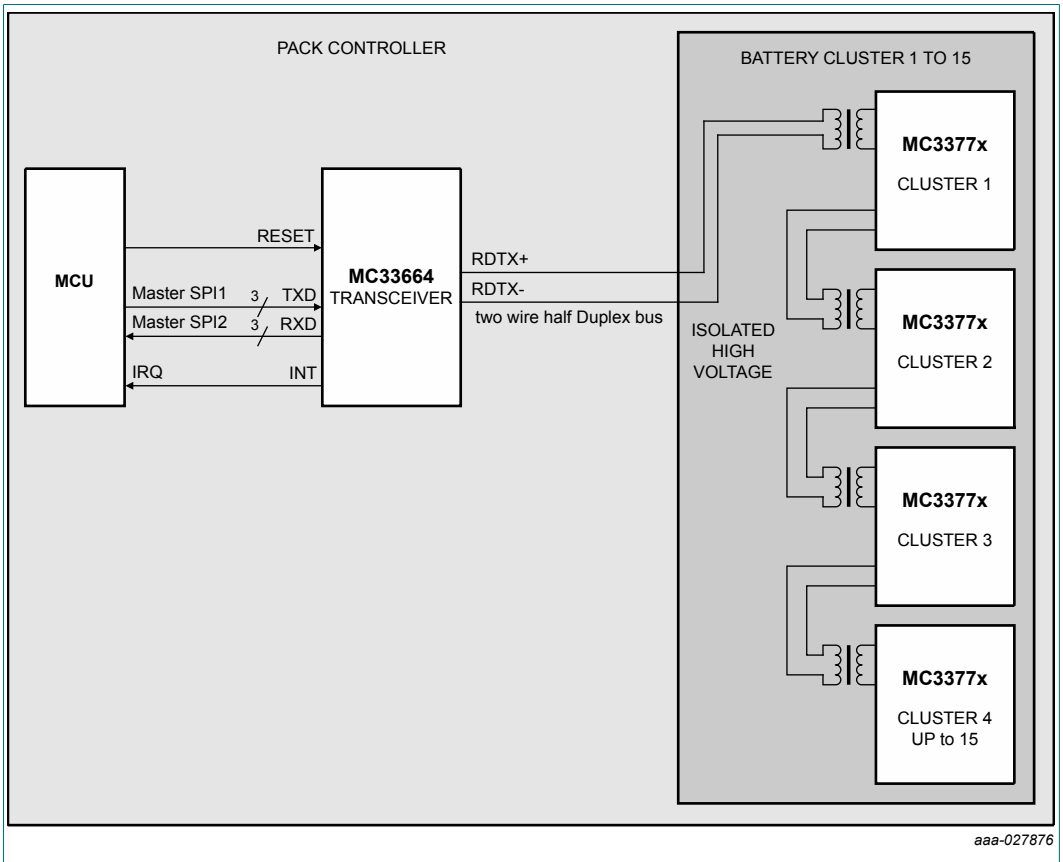


Figure 32. Centralized battery monitoring system

After initialization, the MCU may communicate globally to all slave devices by using a global command. No response is generated when a global command is received by each slave device in the chain.

13.1.2 Distributed battery management system

The distributed battery management solution is identical to the centralized system with an additional transformer in the pack controller.

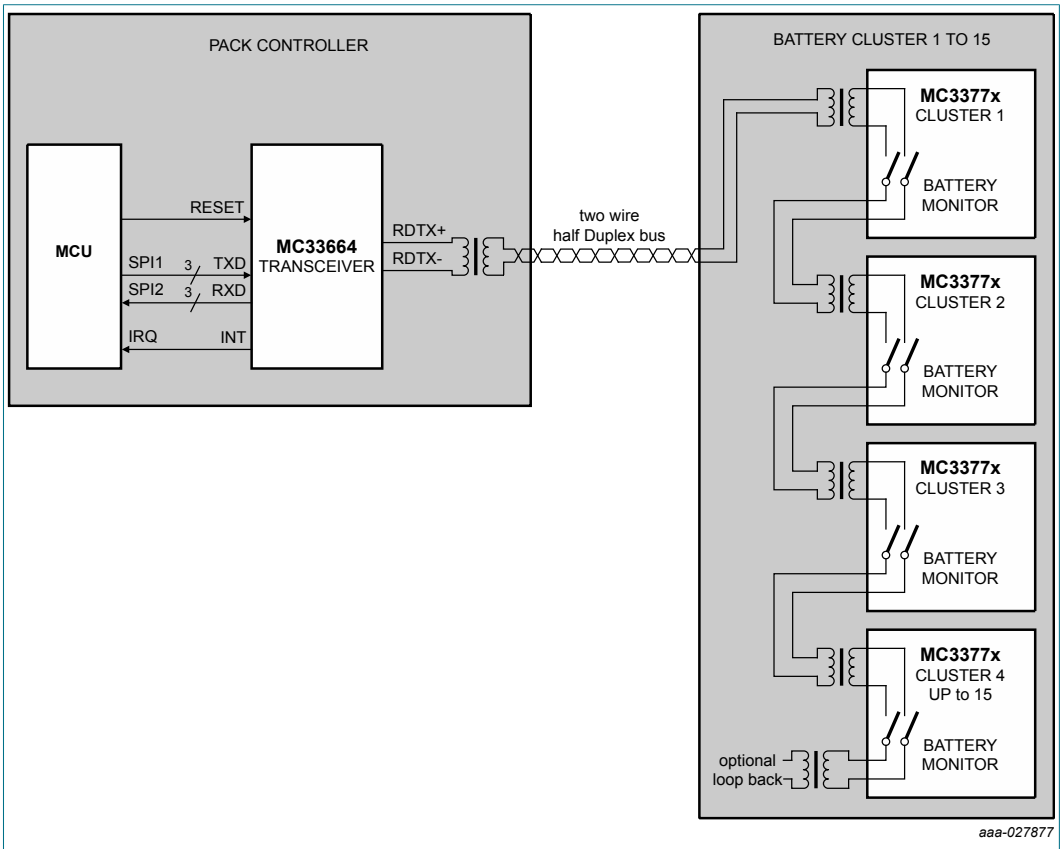


Figure 33. Distributed battery monitoring system

There are significant advantages to using transformers for isolation and communication. The most obvious benefit to the pulse transformers is the high degree of voltage isolation. Transformers specified in this document are automotive qualified and rated at 3750 Vrms. Using pulse transformers allow the NXP battery management system to achieve communication rates of 2.0 Mbps with very low radiated emissions. Transformers by virtue of magnetic coupling, force the secondary signals to be true differential, reducing radiated emissions while providing isolation.

An added benefit to the transformer daisy chain network is ability to loop the network back to the pack controller. This feature allows the user to verify communication to each node in the daisy chain.

13.2 33771 PCB components

This section provides application information.

13.2.1 Cell terminal filters

Figure 34 and Figure 38 show the recommended second order low-pass filters for cell voltages.

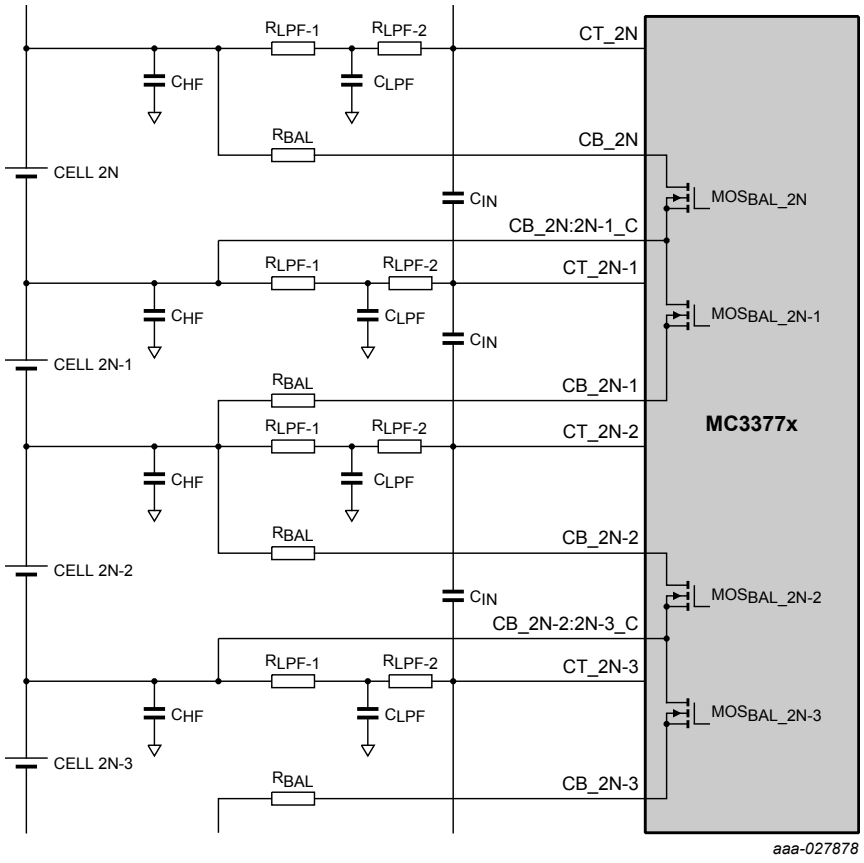


Figure 34. Second order cell terminal filters and cell balancing resistors (internal cell balancing MOSFETs are shown for clarity)

Table 96. CT filter components

ID	Value	Units	Comments
C_{HF}	0.047	µF	Value used and tested at NXP Semiconductors to withstand ESD gun and hot plug
R_{LPF-1}	3	kΩ	Value used and tested to withstand hot plug at NXP. Low-pass filter resistor R_{LPF-1} together with C_{LPF} determine the filter cut-off frequency. This value must not be changed. Component tolerance depends on the wanted accuracy for the bandwidth. See Equation (1) and Equation (2) .
C_{LPF}	0.47	µF	This capacitance value together with R_{LPF-1} provides 112 Hz cut-off frequency. This is the value which may be changed to achieve a different filter bandwidth. Component tolerance depends on the wanted accuracy for the bandwidth. See Equation (1) and Equation (2).
R_{LPF-2}	2	kΩ	Value used and tested to withstand hot plug at NXP. This value must not be changed. No special requirement for the tolerance of this component.
C_{IN}	0.047	µF	Value used and tested to withstand hot plug at NXP. This value must not be changed. No special requirement for the tolerance of this component.
R_{BAL}	X	Ω	Any value is possible, as long as the cell balance current does not exceed 300 mA

The arrangement shown in Figure 34, the filter cut-off frequency in Hz, depending on the measurement time constant τ, is given by the following formula.

$$f_{cut} = 1 / (2\pi\tau) \quad (1)$$

$$\tau = R_{LPF-1}C_{LPF} \quad (2)$$

For the OV/UV functional verification and the arrangement shown in Figure 34, the diagnostic time constant can be calculated as follows:

$$\tau_{diag,n} = \frac{1}{k\,[1-\sqrt{1-c\,/\,k^2}]} \tag{3}$$

$$k = \frac{C_{LPF}R_{LPF-1}(R_{PD}+2R_{LPF-2})+2C_{IN}R_{PD}(R_{LPF-1}+R_{LPF-2})}{4C_{LPF}C_{IN}R_{LPF-1}R_{LPF-2}R_{PD}} \tag{4}$$

$$c = \frac{R_{PD}+2(R_{LPF-1}+R_{LPF-2})}{2C_{LPF}C_{IN}R_{LPF-1}R_{LPF-2}R_{PD}} \tag{5}$$

For the CT_x open line detection and the arrangement in Figure 34 an approximated value for the diagnostic time constant τ_{diag} is given by:

$$\tau_{diag} = \tau_1+\tau_2+\tau_3+\tau_4+\tau_5 \tag{6}$$

$$\tau_1 = (R_{PD}+2R_{LPF-2})\frac{C_{LPF}}{2} \tag{7}$$

$$\tau_2 = ((2R_{LPF-1}) \parallel (2R_{LPF-2}+R_{PD}))\frac{C_{LPF}}{2} \tag{8}$$

$$\tau_3 = \big(R_{PD} \parallel (2R_{LPF-1}+2R_{LPF-2})\big)C_{IN} \tag{9}$$

$$\tau_4 = \big(R_{PD}+R_{LPF-1}+R_{LPF-2}+(R_{LPF-1}+R_{LPF-2}+R_{PD}) \parallel (R_{LPF-1}+R_{LPF-2})\big)C_{IN} \tag{10}$$

$$\tau_5 = R_{PD}C_{IN} \tag{11}$$

The above equations must be taken into account when considering the Section 9.8 "Overvoltage and undervoltage functional verification" and Section 9.9 "CTx open detect and open detect functional verification".

R_{PD} value is given in Table 9.

The symbol || stands for the parallel operator, x||y = xy / (x+y), which is associative and has higher priority than sum and multiplication operators.

13.2.2 Unused cells

If the cluster has less than the maximum number of cells, the usage of cell terminal pins CTx and cell balancing pins CBx has to satisfy some constraints. Each external LPF block is masked as shown in Figure 35, to simplify diagrams representation. As a convention, cell numbering is exactly the same as the associated CTx. For example, cell 12 is the one whose positive terminal is connected to CT12, even though it is the 5th cell in a seven cell system, see Figure 36. A minimum of seven cells must be used. At least

cell 1 through cell 4 and cell 12 through cell 14 must be used. Unused cells must start with CT5.

As a general rule, unused CTx have to be terminated to the positive terminal of cell 4. As shown, several external components may be removed. Cell balancing resistors (R_{BAL}) of unused cells are to be mounted and terminated at the positive terminal of cell 4. Resistors for hot plug protection R_{LPF-2} must also be mounted.

Different number of missing cells would lead to an application diagram analogous to Figure 36 . In general, if the cluster has N missing cells, it is possible to save N−2 times C_{HF}, N times R_{LPF-1}, N times C_{LPF} and N times C_{IN} mentioned in Table 96.

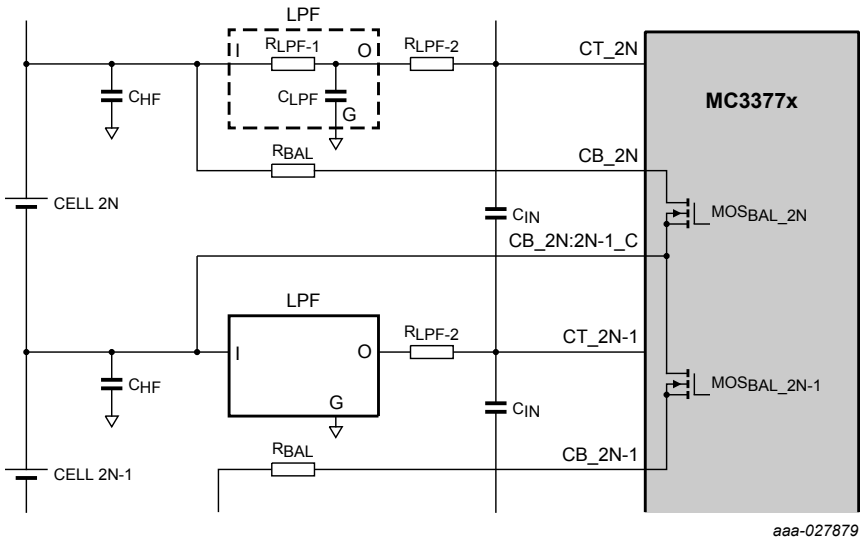


Figure 35. LPF block masking

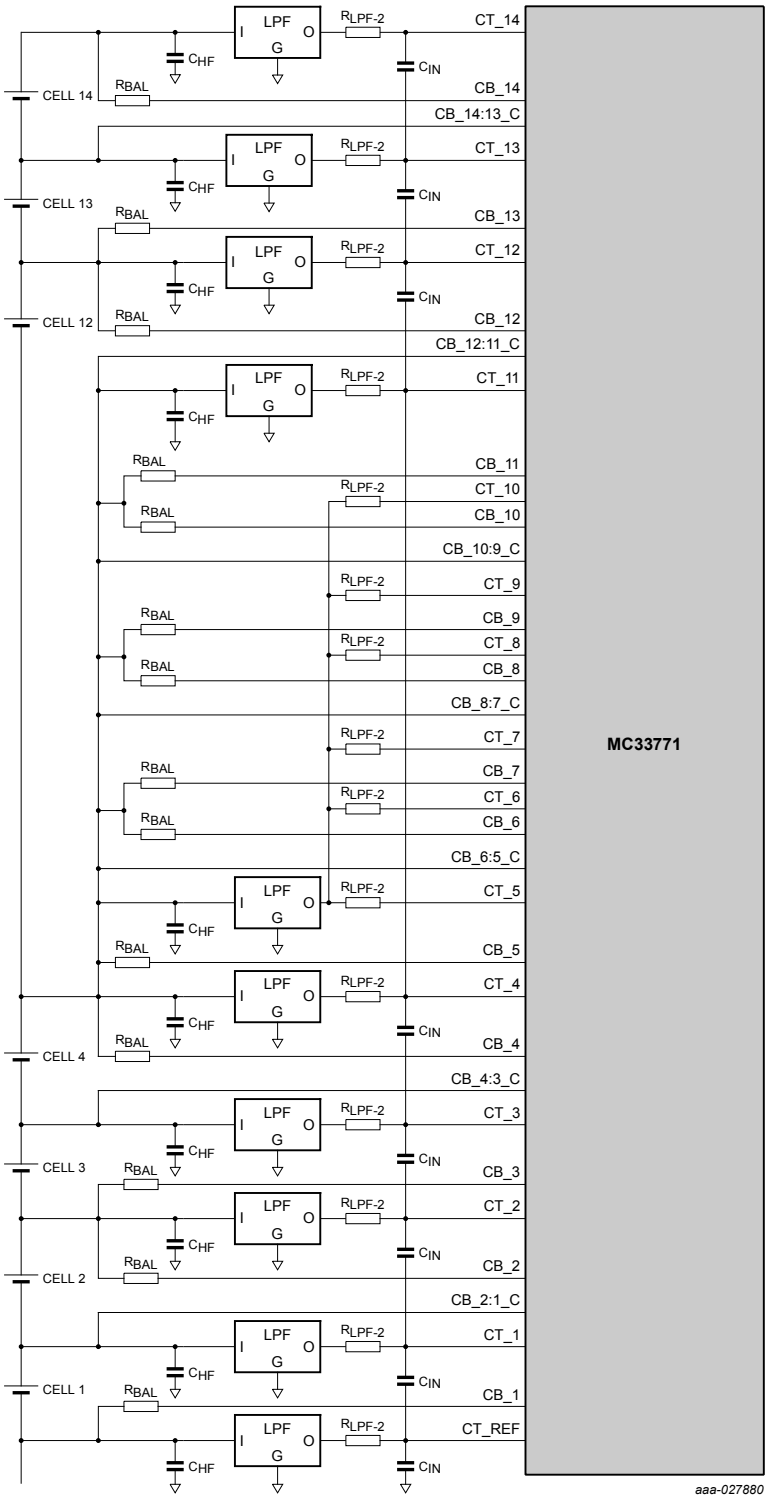


Figure 36. The seven cell configuration

13.2.3 Hot plug protection

The VPWR line, shown in Figure 37, must be protected by a serial resistor in order to limit the inrush current and a parallel capacitor to filter fast voltage variation. Higher value of R_{VPWR} provides better protection. The drawback of higher R_{VPWR} is higher voltage drop. As the stack voltage is measured across VPWR1, 2 pins and ground, stack measurement is affected by such voltage drop. Furthermore, voltage drops higher than V_{VPWR_CT} have a negative impact on cell measurement accuracy.

In order to withstand hot plug, it is mandatory to use Zener diodes as shown in Figure 37 close to the VPWR line. In general all components, whose values are given in Table 97, are mandatory to protect the IC when connection is made to the battery pack. Changing the value of any external components listed in Table 97 may result in serious IC damage during the connection to the battery pack. Capability of the device to sustain random connection to live voltage for pins VPWRx, CT_x, CB_x, CTREF, GND, ISENSE+ and ISENSE– has been extensively evaluated. Nevertheless, the total number of random combinations related to those pins cannot be entirely tested. Therefore, despite all engineering efforts performed by NXP, it is the responsibility of the system provider to ensure safe connection to the battery pack.

Furthermore, it is the responsibility of the system provider to manage the risk of short circuits on any external components connected to the IC, included external low-pass filters. Indeed a short-circuit on the pins connected to the battery can lead to high current flowing through the IC, causing a thermal event on the PCB. The system provider must employ common practices, such as fuse protection on the VPWR line, series of capacitors on the CT pins, appropriate power rating for external resistors, or any other appropriate measure capable to mitigate hazards.

Zener diodes D1 to D4 are required to protect internal ESD structures between VPWR and CB_x pins, when VPWR is connected before cells. The energy to charge the C_{HF} capacitors on CB_x pins exceeds the capability of the internal ESD devices for VPWR max operating range. Zener diodes D1 to D4 are placed on CB_14, CB_12, CB_10:9_C and CB_8:7_C pins according to the internal ESD protection network. The joint presence of these zener diodes and the set of internal cell balancing transistors, which are highly robust due to their large size, guarantee hot plug protection of the following pins: CB_14:13_C, CB_13, CB_12:11_C, CB_11, CB_10, CB_9, CB_8, and CB_7. All other CB_x pins do not need external zener diodes, since internal ESD clamping voltage is higher than VPWR max operating value. Clamping voltages of Zener diodes D1 to D4 are defined to be higher than the maximum rating between VPWR and CB_x, and lower than the clamping voltage of the internal ESD devices between these pins.

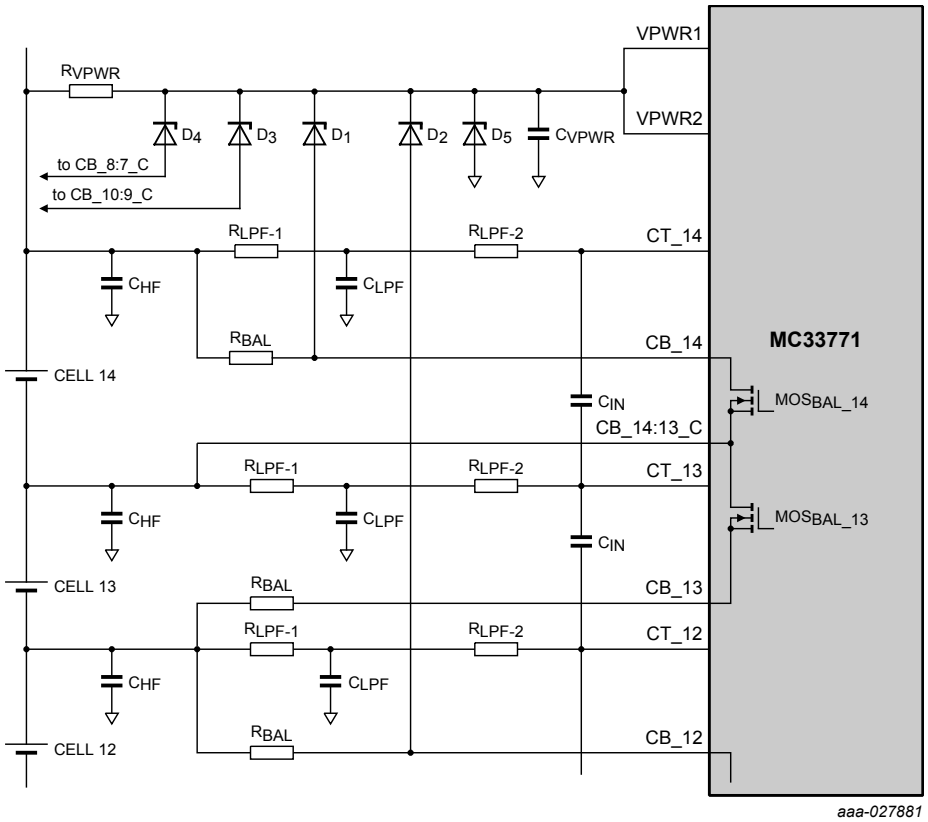


Figure 37. Top cell terminal filters and balancing resistors, VPWR1, 2 components to withstand hot plug

Table 97. Components to avoid hot plug issues

ID	Value	Units	Comments
D_5	75	V	To protect the IC against transient overvoltage, use the specified Zener voltage. For example, use BZX384-B75.
D_4	43	V	D4 is rated 43 V because max. rating between VPWR and CB_8:7_C is 35 V and internal ESD clamping voltage between VPWR and CB14 is 50 V, with a small snap back at 40 V. For example, use BZX384-B43.
D_3	27	V	D3 is rated in the range 26.5 V to 29.5 V, because max. rating between VPWR and CB_10:9_C is 25 V and internal ESD clamping voltage between VPWR and CB_14 is 50 V, with a small snap back at 40 V. For example, use BZX384-B27.
D_2	20	V	D2 is rated 20 V, because max. rating between VPWR and CB_12 is 10 V and internal ESD clamping voltage between VPWR and CB_14 is 50 V, with a small snap back at 40 V. For example, use BZX384-B20.
D_1	2 x 8.2	V	D1 is rated 16.2 V, because max. rating between VPWR and CB_14 is 10 V and internal ESD clamping voltage between VPWR and CB_14 is 50 V, with a small snap back at 40. Implementation may be done by using two diodes in series, each of which having half Zener voltage. For example, use two BZX384-B8V2.
R_{VPWR}	10	Ω	Reducing resistance value may jeopardize hot plug capability. Power rating is 0.1 W.
C_{VPWR}	0.22	µF	To withstand hot plug, this value must not be changed

13.2.4 Current channel filter

The current channel may be filtered as shown in Figure 38. Example component values are given in Table 98.

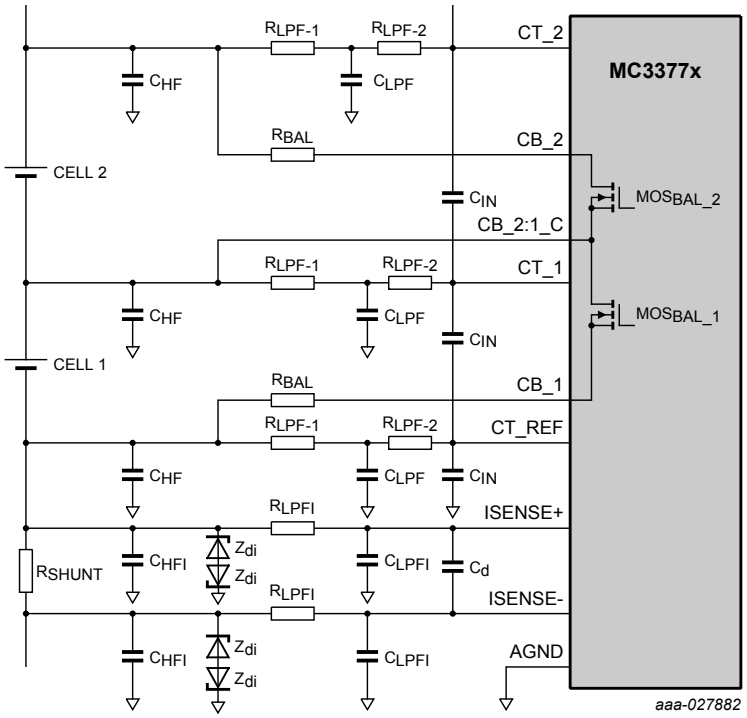


Figure 38. Bottom cell terminal filters, cell balancing components and current channel filter

Table 98. ISENSE filter components

ID	Value	Units	Comments
C_{HFI}	47	nF	This component serves to withstand ESD gun and its value must not be changed
R_{LPFI}	127	Ω	Warning: do not exceed 200 Ω. Use 5 % tolerance. Used value is to get both f_{CUTI} = 91.8 Hz and f_{ICM} = 26.67 kHz. See Equation (12), Equation (13), Equation (15), and Equation (16).
C_d	6.8	µF	This example value has been chosen to get f_{CUTI} = 91.8 Hz and t_{DIAG} ≤ 31.7 ms. See Equation (12), Equation (13), and Equation (14). Use 5 % tolerance.
C_{LPFI}	47	nF	Value is chosen in order to get: 91.8 Hz, t_{DIAG} ≤ 31.7 ms and f_{ICM} = 26.67 kHz. See Equation (12), Equation (13), Equation (14), Equation (15) and Equation (16). Use 5 % tolerance.
ZDI	2.0	V	To protect during hot plug in case one of the ISENSE± pin is connected before GND of the device. Recommended MMSZ4679T1G.

The signal cutoff frequency (in Hz) arrangement shown in Figure 38 of the current channel external filter depends on the measurement time constant τ_I given by the following formula. Ideally the current channel should have the same bandwidth as cell voltage channels.

$$f_{cutI} = 1 / (2\pi\tau_I) \quad (12)$$

$$\tau_I = R_{LPFI}(C_{LPFI} + 2C_d) \quad (13)$$

The diagnostic time to detect an open from the shunt to the current filter arrangement shown in Figure 38, is given by:

$$t_{diag} = (C_{LPFI} + C_d)\frac{V_{ISENSE-OL} + |R_{shunt}I_{max}|}{I_{SENSE-OL}} \quad (14)$$

The current channel external filter arrangement shown in Figure 38 of the common mode cutoff frequency in Hz, depends on the measurement time constant τ_{Icm}, given by the following formula, whose numeric result should be selected one decade above the signal cutoff frequency.

$$f_{Icm} = 1 / (2\pi\tau_{Icm}) \quad (15)$$

$$\tau_{Icm} = R_{LPFI}C_{LPFI} \quad (16)$$

Above equations must be taken into account when considering the procedure described in Section 9.14 "Current measurement diagnostics" to detect an open connection between ISENSE± and the input filter. Values for V_{ISENSE_OL} and I_{ISENSE_OL} are given in Table 9, values for the shunt resistance R_{SHUNT} and the maximum current I_{MAX} through it are application specific, while example values for the filter capacitors and resistors can be found in Table 97.

13.2.5 Temperature channels

Figure 39 shows usage of GPIOx as analog inputs (ANx) for temperature measurements. If not used, each GPIOx may be shorted to GND.

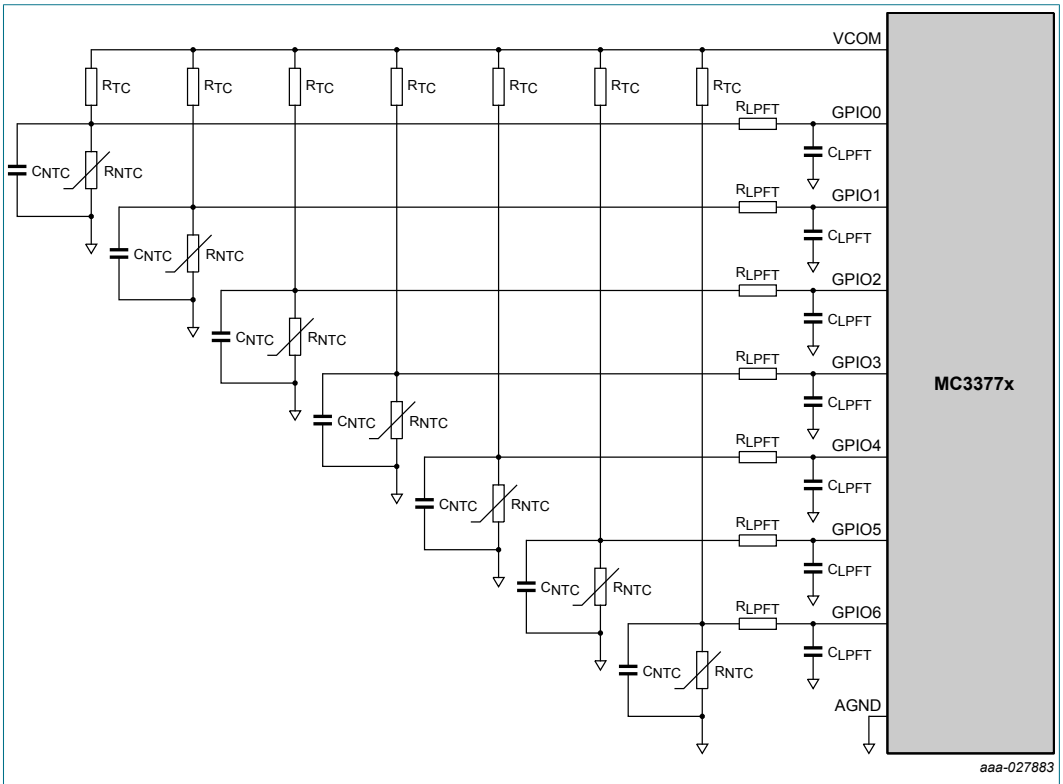


Figure 39. GPIOx used as ANx

Table 99. ANx filter components

ID	Value	Units	Comments
R_{TC}	10	kΩ	Component with 1 % tolerance, for accurate temperature measurement. Proposed value, together with all other proposed values, gives approximately f_{CUTT} = 10 kHz. See Equation (17), Equation (18), Equation (19), and Equation (20).
R_{NTC}	10	kΩ	Nominal resistance value is given at 25 °C, tolerance must be 5 % or better
C_{NTC}	2200	pF	This component is for ESD protection
R_{LPFT}	10	kΩ	Influences the channel bandwidth. See Equation (17), Equation (18), Equation (19), and Equation (20).
C_{LPFT}	1000	pF	5 % tolerance or better. Influences the channel bandwidth. See Equation (17), Equation (18), Equation (19), and Equation (20).

The signal cutoff frequency (in Hz) for the arrangement shown in Figure 39 of GPIOx used as radiometric analog inputs, depends on the measurement time constant τ_T, given by the following formula. Ideally the current channel should have the same bandwidth as cell voltage channels.

$$f_{cutT} = 1 / (2\pi\tau_T) \quad (17)$$

where,

$$\tau_T = \max(\tau_1, \tau_2) \quad (18)$$

$$\tau_1 = (R_{LPFT} + (R_{TC}R_{NTC})/(R_{TC} + R_{NTC}))C_{LPFT} \quad (19)$$

$$\tau_2 = C_{NTC}(R_{TC}R_{NTC}) / (R_{TC} + R_{NTC}) \quad (20)$$

In case the NTC resistor is located outside of the board and can be submitted to large EMC and ESD Gun constraints, the recommended filter for temperature is 2nd order as shown in Figure 40.

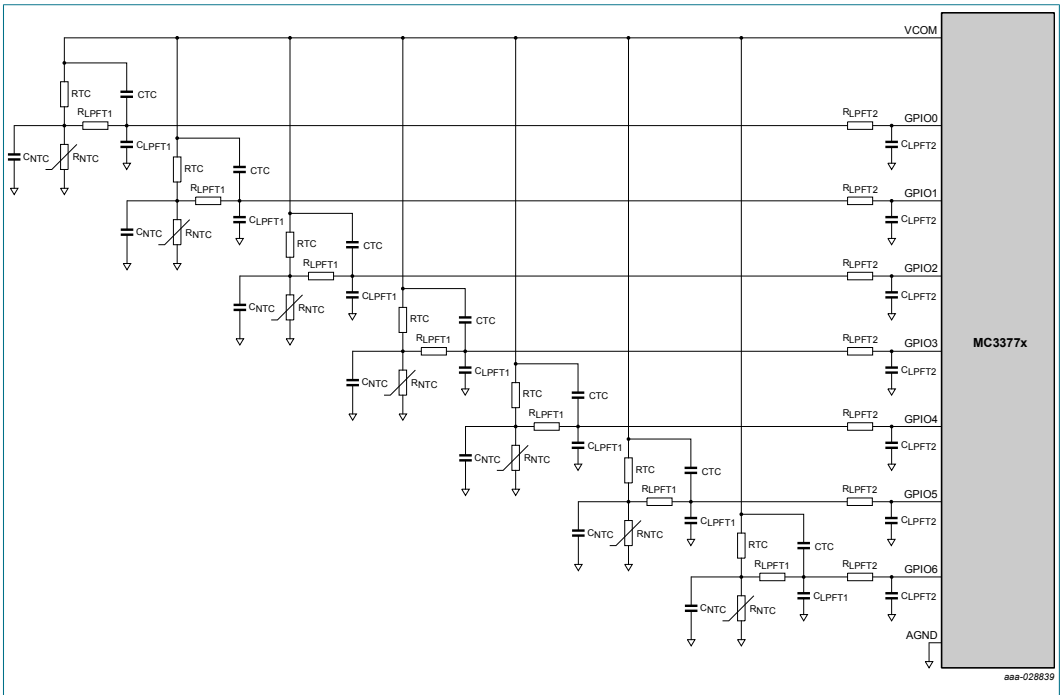


Figure 40. GPIOx used as ANX (with 2nd order filter)

Table 100. ANx second order filter components

ID	Value	Units	Comments
R_{TC}	10	kΩ	Component with 1 % tolerance, for accurate temperature measurement
C_{TC}	1.2	nF	
R_{NTC}	10	kΩ	Nominal resistance value is given at 25 °C, tolerance must be 5 % or better
C_{NTC}	1	nF	This component is for ESD protection
C_{LPFT1}	1.2	nF	5 % tolerance or better
R_{LPFT1}	3.3	kΩ	
C_{LPFT2}	1.2	nF	5 % tolerance or better
R_{LPFT2}	3.3	kΩ	

13.2.6 TPL bus components

It is convenient to split Figure 23 in two separate pictures, Figure 41 and Figure 42. It is worthwhile highlighting that using two transformers, one for each communication side (Figure 41), provides a higher degree of protection for the 33771, both in terms of common mode communication noise and isolation against shorts of the twisted pair at some potential. Components of Table 101 and Table 102 are strictly correlated and make sense only if considered together.

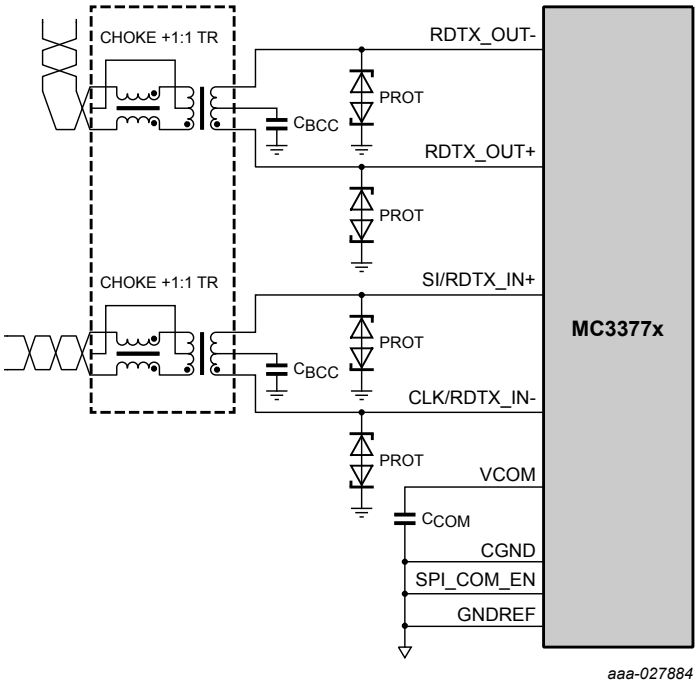


Figure 41. Slave node of a TPL bus

Table 101. Slave node TPL bus components

ID	Value	Units	Comments
C_{BCC}	100	pF	Ceramic capacitor
PROT	8	V	ESD protection. Use PESD5V0F1BL or equivalent. The indicated voltage is the nominal breakdown voltage.
CHOKE+ 1:1 TR	PULSE HM210xNL	NA	PULSE HM2102NL (dual transformer in a package) or PULSE HM2103NL (single transformer in a package)

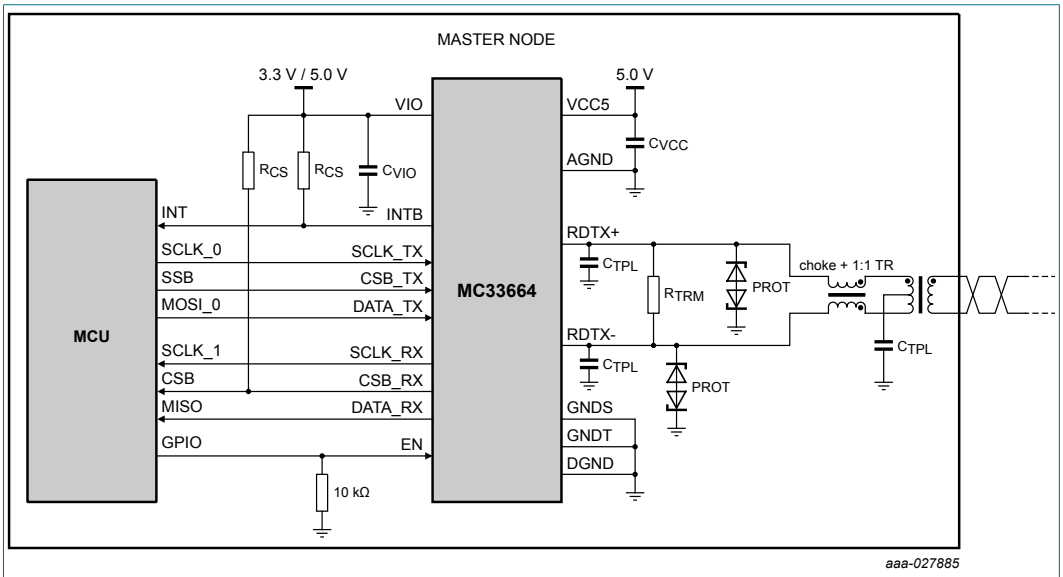


Figure 42. Master node of a TPL bus

Table 102. MC33664 TPL bus components

ID	Value	Units	Comments
C_{TPL}	100	pF	Ceramic capacitor
R_{TRM}	150	Ω	Termination resistor
PROT	8	V	ESD protection. Use PESD5V0F1BL or equivalent. The indicated voltage is the nominal breakdown voltage.
CHOKE+ 1:1 TR	PULSE HM210xNL	NA	PULSE HM2103NL (single transformer package)

13.2.7 Alternative cell balance resistors arrangement

To detect a possible leakage through a CB switch or a possible inadvertently activated CB switch, the following arrangement of balance resistors is recommended. Putting a small portion of the whole cell balancing resistance on the common CB_2X:2X-1_C pins provides a detectable voltage drop in case of leakage. As an example, assume the battery cells must work in the range 2.5 V to 4.2 V and the desired balancing current has to stay in the range 25 mA to 53 mA. Then, a total balancing resistance of 100 Ω is needed.

Assume R_{BAL} = 80 Ω, R_{BAL_C} = 20 Ω, and V_{LEAK} = 20 mV. When balancing one of the two cells served by the same pair of balancing MOSFET, the balancing resistance seen by this single cell is $R_{SINGLE} = R_{BAL} + R_{BAL\_C}$ = 100 Ω. When balancing both cells served by the same pair of balancing MOSFET at the same time, the balancing resistance seen by each cell is $R_{PAIR} = R_{BAL}$ = 80 Ω. So, the price to be paid for the detectability of CB leakages is a difference in the CB equivalent resistance. Assuming, for example, the leakage detection threshold to be just under the same assumptions stated above, the detection capabilities are as follows:

- Leakage current on odd cells $I_{BAL,leak(ODD)} = V_{LEAK} / R_{BAL\_C}$ = 20 mV / 20 Ω = 1.0 mA
- Leakage current on even cells $I_{BAL,leak(EVEN)} = V_{LEAK} / R_{BAL}$ = 20 mV / 80 Ω = 250 µA

On the contrary, assume it is desired to detect a predetermined balance leakage current $I_{BAL,LEAK}$. Then, the value of R_{BAL_C} is given by $R_{BAL\_C} = V_{LEAK} / I_{BAL,LEAK}$. For instance,

the wish value $I_{BAL,LEAK}$ = 10 mA gives R_{BAL_C} = 20 mV / 10 mA = 2.0 Ω only. Assuming same cell voltage range and cell balance current range discussed above results in R_{BAL} = 80 Ω. In this case, mutually close balance resistance values are achieved: R_{SINGLE} = R_{BAL} + R_{BAL_C} = 82 Ω and R_{PAIR} = R_{BAL} = 80 Ω. Using the smallest possible resistance on CB common pins, in addition to giving the advantage of a simpler balancing strategy at application level, is also beneficial in order to avoid CB driving problems when the cell voltage becomes too low. Using a ratio R_{BAL_C}/ R_{BAL} not greater than 1/5 is recommended.

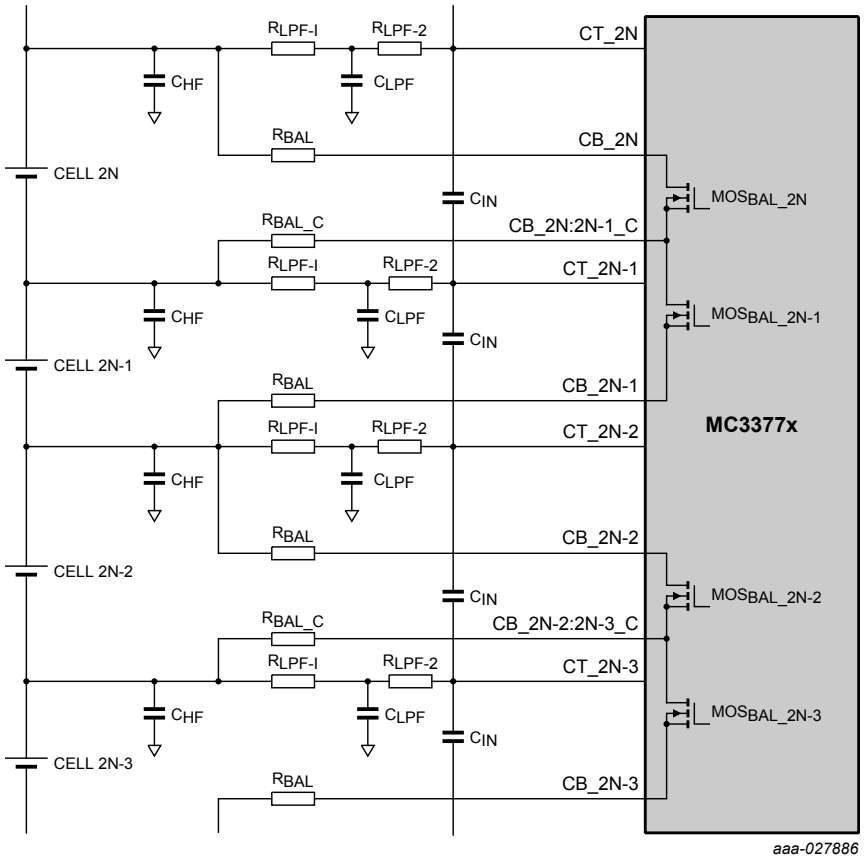


Figure 43. Cell balance arrangement for CB leakage detection

14 Packaging

14.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 103. Package Outline

Package	Suffix	Package outline drawing number
64-pin LQFP-EP	AE	98ASA10763D

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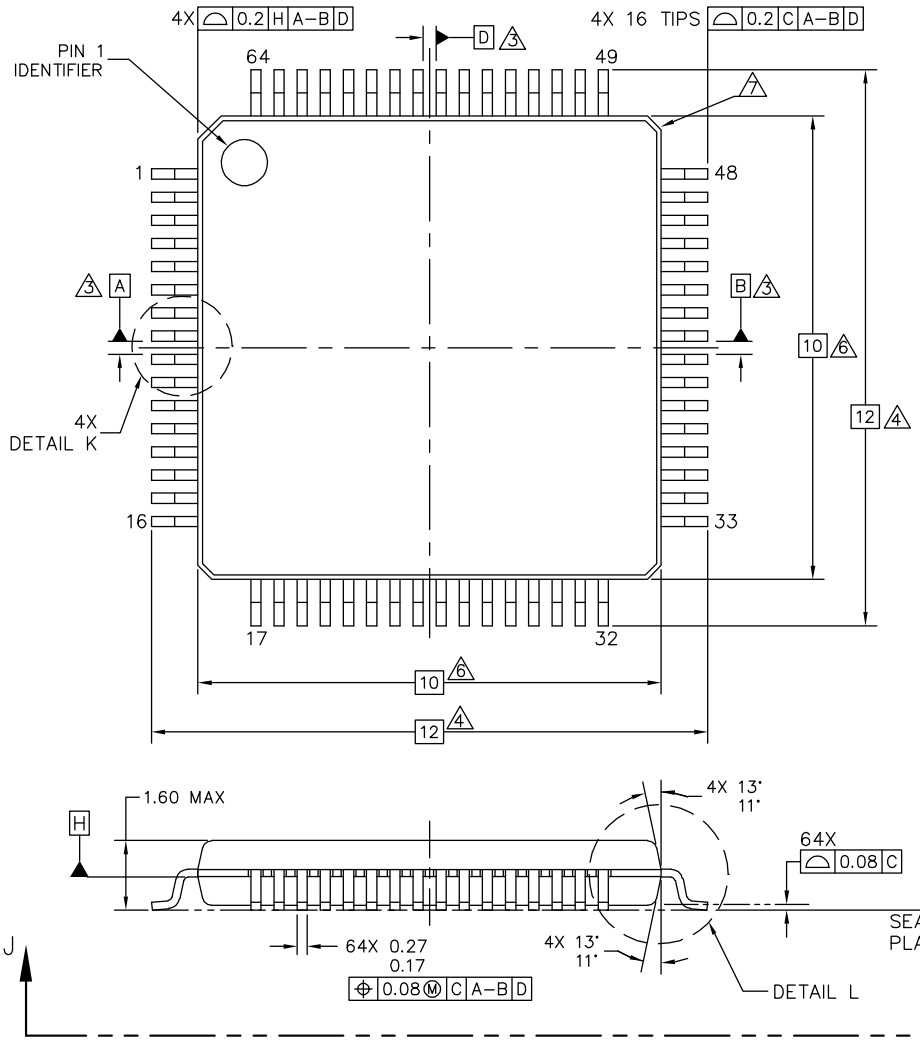
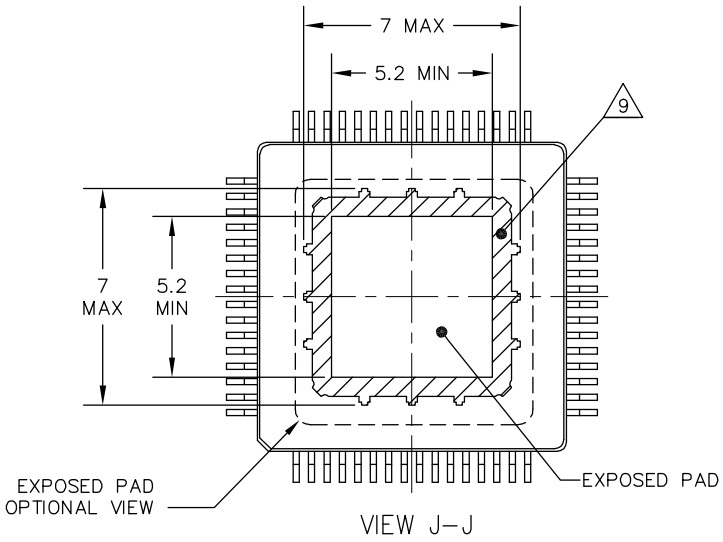
		PAGE: 1899
	DO NOT SCALE THIS DRAWING	REV: B

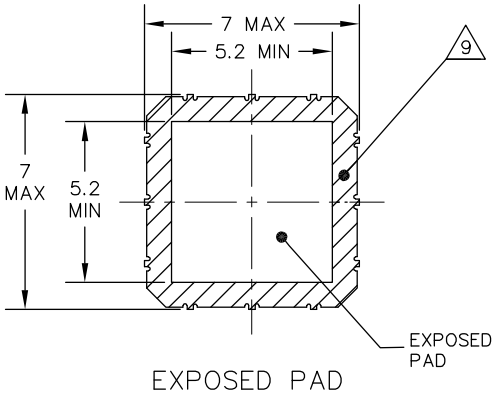


TITLE:	LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	CASE NUMBER:	1899-03
		STANDARD:	JEDEC MS-026 BCD
		SHEET:	1 OF 5

	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA10763D
		PAGE: 1899
	DO NOT SCALE THIS DRAWING	REV: B



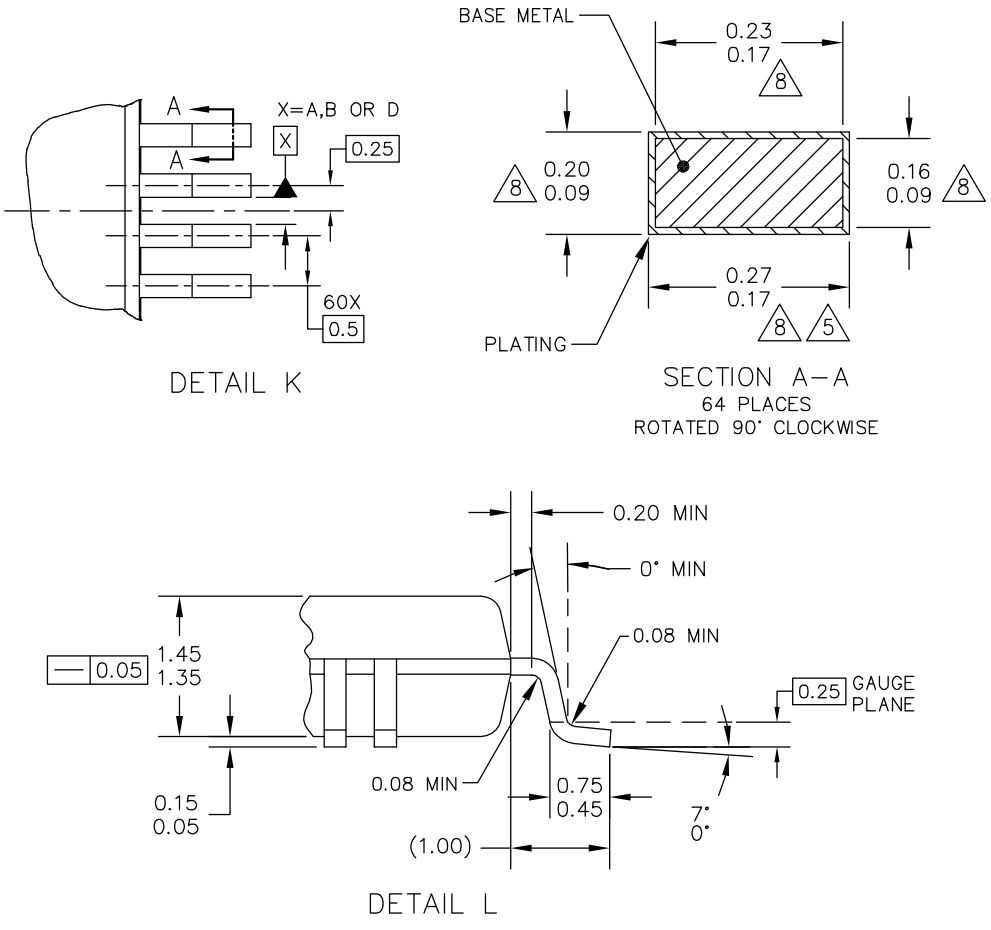
VIEW J–J



EXPOSED PAD
OPTIONAL VIEW

TITLE:	LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	CASE NUMBER: 1899-03
		STANDARD: JEDEC MS-026 BCD
		SHEET: 2

	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA10763D
		PAGE: 1899
	DO NOT SCALE THIS DRAWING	REV: B



TITLE:	LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	CASE NUMBER:	1899-03
		STANDARD:	JEDEC MS-026 BCD
		SHEET:	3

	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA10763D
		PAGE: 1899
	DO NOT SCALE THIS DRAWING	REV: B

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.
9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	CASE NUMBER: 1899-03
	STANDARD: JEDEC MS-026 BCD
	SHEET: 4

15 Revision history

Table 104. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MC33771B v.3.0	2017 Dec	Product preview	—	2.0
Modifications	• Added "Qualified in compliance with AECQ-100 Grade 0" to features • Updated the max. value for VPWR to CT14 in Table 7 (value changed from 10 to 10.5) • Updated min. and max. values for V_{CVFV} in Table 9 • Updated values for CTx_UV_TH and CTx_OV_TH in Table 9 • Added values for t_{RES} in Table 9 • Added the max. value for I_{VCOM} in Table 9 • Updated R_{PD} min. value from 750 to 850 in Table 9 • Updated the max. value for CSB_{WU_FLT} in Table 9 (value changed from 65 to 80) • Updated the max. value for $V_{OL(TH)}$ in Table 9 (value changed from 0.2 to 0.23) • Changed 98A number from 98ASA00544D to 98ASA10763D and updated package drawings in Section 14.1 • Updated Table 13			
MC33771B v.2.0	2017 August	—	—	1.0
Modifications	• Updated Section 5 "Ordering information" • Updated max. value for $I_{VPWR(SS)}$ SPI mode (105 °C) in Table 9 (replaced 90 by 100) • Updated V_{ERR} accuracy data in Table 9 • Updated Figure 7, Figure 17, Figure 23, Figure 41, and Figure 42 • Updated Table 34, Table 19 Table 47, and Table 95 • Updated Section 9.3 "Modes of operation", Section 9.18 "Cell balance fault diagnostics", Section 9.22 " Storage of parameters in an optional EEPROM"Section 9.2.1 "VPWR overvoltage, low-voltage", Section 9.5 "ADC1-A and ADC1-B functional verification", Section 9.8 "Overvoltage and undervoltage functional verification", Section 9.9 "CTx open detect and open detect functional verification", Section 9.11 "Cell terminal leakage diagnostics", Section 9.13 "Current measurement", Section 9.14, Section 9.16.1 "GPIOx used as digital I/O", Section 9.16.5 "GPIO5, GPIO6 used as ISENSE", Section 9.19 "Oscillator frequency monitor", Section 10.2 "TPL communication", Section 13.2.3 "Hot plug protection", and Section 13.2.6 "TPL bus components"			
MC33771B v.1.0	2017 April	Product preview	—	—

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17 Legal information

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Document number: