



# **IPC-7525B**

## **2011 - October**

### **Stencil Design Guidelines**

Supersedes IPC-7525A  
February 2007

*A standard developed by IPC*

*Association Connecting Electronics Industries*



---

**The Principles of Standardization**

In May 1995 the IPC's Technical Activities Executive Committee (TAEC) adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

**Standards Should:**

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

**Standards Should Not:**

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

**Notice**

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

**IPC Position Statement on Specification Revision Change**

It is the position of IPC's Technical Activities Executive Committee that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC publication is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision. Adopted October 6, 1998

**Why is there a charge for this document?**

Your purchase of this document contributes to the ongoing development of new and updated industry standards and publications. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards and publications development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low to allow as many companies as possible to participate. Therefore, the standards and publications revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards and publications, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit [www.ipc.org](http://www.ipc.org) or call 847/597-2872.

Thank you for your continued support.



**IPC-7525B**

# **Stencil Design Guidelines**

Developed by the Stencil Design Task Group (5-21e) of the Assembly and Joining Processes Committee (5-20) of IPC

***Supersedes:***

IPC-7525A - February 2007

IPC-7525 - May 2000

Users of this publication are encouraged to participate in the development of future revisions.

**Contact:**

IPC  
3000 Lakeside Drive, Suite 309S  
Bannockburn, Illinois  
60015-1249  
Tel 847 615.7100  
Fax 847 615.7105

This Page Intentionally Left Blank

## Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the Stencil Design Task Group (5-21e) of the Assembly and Joining Processes Committee (5-20) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

<b>Assembly and Joining Processes Committee</b>	<b>Stencil Design Task Group</b>	<b>Technical Liaisons of the IPC Board of Directors</b>
Chair Leo Lambert EPTAC Corporation	Co-Chairs William E. Coleman, Ph.D Photo Stencil Inc.  George Oxx Jabil Circuit, Inc. (HQ)	Dongkai Shangguan Flextronics International  Shane Whiteside TTM Technologies
<b>Stencil Design Task Group</b>		
Russell Nowland, Alcatel-Lucent Christopher Sattler, AQS - All Quality & Services, Inc. Ricky Bennett, Assembly Process Technologies Jay Hinerman, BAE Systems CNI Div. Ron Tripp, Cookson Electronics Jeff Schake, DEK International Craig Brown, DEK USA Inc. Richard Lieske, DEK USA Inc. Glenn Dody, Dody Consulting Robert Dervaes, FCT Assembly Michael Yuen, Foxconn CMMSG-NVPD Deepak Pai, General Dynamics Info. Sys., Inc	Joseph Brown, Hewlett-Packard Co- ProCurve Networking Jan Kilen, HP Etch AB Rongxiang Yang, Huawei Technologies Co., Ltd. Chris Anglin, Indium Corporation of America Tim Jensen, Indium Corporation of America William Kunkle, MET Associates Inc. Holly Wise, MicroScreen, LLC Robert Cass, Northrop Grumman Amherst Systems William May, NSWC Crane Narinder Kumar, Pelco by Schneider Electronics	Todd Woods, Photo Stencil Inc. Dale Kratz, Plexus Corporation Timothy Pitsch, Plexus Corporation Robert Rowland, RadiSys Corporation Guillermo Velazquez, Rain Bird Corporation David Nelson, Raytheon Company Jeff Shubrooks, Raytheon Company Mark Quealy, Schneider Automation Inc. Steve Sangillo, Swemco Daan Terstegge, Thales Nederland B.v. Huizen Richard Lathrop Ahne Oosterhof

This Page Intentionally Left Blank

# Table of Contents

<b>1 PURPOSE</b>	1	<b>3.2 Aperture Design</b>	4
1.1 Terms and Definitions	1	3.2.1 Aperture Size	4
1.1.1 *Aperture	1	3.2.2 Aperture Size versus Board Land Size for Tin Lead Solder Paste	8
1.1.2 *Area Ratio	1	3.2.3 Aperture Size versus Board Land Size for Lead Free Solder Paste	9
1.1.3 *Aspect Ratio	1	3.2.4 Glue Aperture Chip Component	10
1.1.4 Border	1	3.2.5 Glue Apertures for Combination of Chip Components and Leaded Devices	10
1.1.5 Enclosed Print Head	1	3.2.6 Relief Etch with Glue Stencils	11
1.1.6 Etch Factor	1	3.3 Mixed Technology Surface-Mount/Through-Hole (Intrusive Soldering)	11
1.1.7 Relief Etch	1	3.3.1 Solder Paste Volume	11
1.1.8 Fiducials	1	3.4 Mixed Technology Surface-Mount/Flip Chip	13
1.1.9 Fine-Pitch BGA	1	3.4.1 Two-Print Stencil for Surface-Mount/Flip Chip	13
1.1.10 Fine-Pitch Technology (FPT)	1	3.5 Step Stencil Design	13
1.1.11 Foil	1	3.5.1 Step-Down Stencil	14
1.1.12 Frame	1	3.5.2 Step-Up Stencil	14
1.1.13 Intrusive Soldering	1	3.5.3 Step Stencil for Enclosed Print Heads	14
1.1.14 *Land	1	3.5.4 Relief-Etch Stencil	14
1.1.15 Modification	1	3.6 Fiducials	14
1.1.16 *Overprinting	2	3.6.1 Global Fiducials	14
1.1.17 *Pad	2	3.6.2 Local Fiducials	14
1.1.18 Squeegee	2	3.7 Rework and Repair Stencils	14
1.1.19 Squeegee Direction	2	3.7.1 Mini Stencils	14
1.1.20 Standard BGA	2	3.7.2 Repair Tool for Printing Paste Directly on the Component	15
1.1.21 *Stencil	2	<b>4 STENCIL FABRICATION</b>	15
1.1.22 Step Stencil	2	4.1 Foils	15
1.1.23 *Surface-Mounting Technology (SMT)	2	4.2 Frames	15
1.1.24 *Through-Hole Technology (THT)	2	4.3 Stencil Border	15
1.1.25 Transfer Efficiency	2	4.4 Stencil Fabrication Technologies	15
1.1.26 Ultra-Fine Pitch Technology	2	4.4.1 Chemical Etch	15
<b>2 APPLICABLE DOCUMENTS</b>	2	4.4.2 Laser-Cut Stencils	16
2.1 IPC	2	4.4.3 Electroform	16
<b>3 STENCIL DESIGN</b>	3	4.4.4 Hybrid	16
3.1 Stencil Data	3	4.4.5 Trapezoidal Apertures	16
3.1.1 Data Format	3	4.4.6 Additional Options	16
3.1.2 Gerber® Format	3	<b>5 STENCIL MOUNTING</b>	16
3.1.3 Aperture List	3	5.1 Location of Image on Metal	16
3.1.4 Solder Paste Layer	3	5.2 Centering	16
3.1.5 Data Transfer	3	5.3 Additional Design Guidelines	16
3.1.6 Panelized Stencils	3		
3.1.7 Step-and-Repeat	3		
3.1.8 Image Orientation/Rotation	3		
3.1.9 Image Location	4		
3.1.10 Identification	4		

<b>6</b>	<b>STENCIL ORDERING</b>	16
<b>7</b>	<b>STENCIL USER'S INSPECTION/VERIFICATION</b>	17
<b>8</b>	<b>STENCIL CLEANING</b>	17
<b>9</b>	<b>END OF LIFE</b>	17
<b>APPENDIX A:</b>	<b>EXAMPLE ORDER FORM</b>	19

### Figures

Figure 3-1	4 mil Thick Stencil Tin Lead and Lead Free	6
Figure 3-2	5 mil Thick Stencil Tin Lead and Lead Free	6
Figure 3-3	6 mil Thick Stencil Tin Lead and Lead Free	7
Figure 3-4	8 mil Thick Stencil Tin Lead and Lead Free	7
Figure 3-5	Cross-Sectional View of A Stencil	8
Figure 3-6	Home Plate Aperture Design	8
Figure 3-7	Bow Tie Aperture Design	9
Figure 3-8	Oblong Aperture Design	9
Figure 3-9	Aperture Design for Cylindrical Components and Chip Components (All Corners Rounded)	9
Figure 3-10	Window Pane Design for Ground Plane	9
Figure 3-11	Glue Stencil Aperture Design	10
Figure 3-12	Chip Component and SOIC Present on Board	10

Figure 3-13	Print Only Mode 15 mil Thick Stencil	10
Figure 3-14	Glue Stencil With Glue Reservoir	10
Figure 3-15	Through-Hole Solder Paste Volume	11
Figure 3-16	Overprint Without Step	12
Figure 3-17	Overprint With Step (Squeegee Side)	12
Figure 3-18	Overprint With Step (Contact/Board Side)	12
Figure 3-19	Two-Print Through-Hole Stencil	13
Figure 3-20	Two-Print Stencil for Mixed Technology	13
Figure 3-21	Print With Step	13
Figure 3-22	Step Down	14
Figure 3-23	Step Up	14
Figure 3-24	BTC	15
Figure 3-25	BGA	15
Figure 4-1	Trapezoidal Apertures	16

### Tables

Table 3-1	Stencil Use Clauses	4
Table 3-2	General Aperture Design Guideline Examples for Selective Surface-Mount Devices (Tin Lead Solder Paste)	5
Table 3-3	Process Window for Intrusive Soldering - Maximum Limits Desirable	11



---

# Stencil Design Guidelines

---

## 1 PURPOSE

This document provides a guide for the design and fabrication of stencils for solder paste and surface-mount adhesive. It is intended as a guideline only. Much of the content is based on the experience of stencil designers, fabricators, and users. Printing performance depends on many different variables and therefore no single set of design rules can be established.

**1.1 Terms and Definitions** All terms and definitions used throughout this handbook are in accordance with IPC-T-50. Definitions noted with an asterisk (\*) are quoted from IPC-T-50. Other specific terms and definitions, essential for the discussion of the subject, are provided below.

**1.1.1 \*Aperture** An opening in the stencil foil.

**1.1.2 \*Area Ratio** The ratio of the area of aperture opening to the area of aperture walls.

**1.1.3 \*Aspect Ratio** The ratio of the width of the aperture to the thickness of the stencil foil.

**1.1.4 Border** Peripheral tensioned mesh, either polyester or stainless steel, which keeps the stencil foil flat and taut. The border connects the foil to the frame.

**1.1.5 Enclosed Print Head** A stencil printer head that holds, in a single replaceable component, the squeegee blades and a pressurized chamber filled with solder paste.

**1.1.6 Etch Factor** Etched Depth/Lateral; Etch in a chemical etching process.

**1.1.7 Relief Etch** Also known as Etch Relief and Under Etch. Adding an under etch of the foil to create a pocket for raised features, labels, or a multi-print function.

**1.1.8 Fiducials** Reference marks on the stencil foil (and other board layers) for aligning the board and the stencil when using a vision system in a printer.

**1.1.9 Fine-Pitch BGA** Ball grid array (BGA) with less than 1 mm [39 mil] pitch. Also known as chip scale package (CSP) when the package size is no more than 1.2X the area of the original die size.

**1.1.10 Fine-Pitch Technology (FPT)** A surface-mount assembly technology with component terminations on centers less than or equal to 0.625 mm [24.61 mil].

**1.1.11 Foil** The sheet used to create the stencil.

**1.1.12 Frame** A frame may be made of tubular or cast aluminum to which a tensioned mesh (border) is permanently bonded using an adhesive.

**1.1.13 Intrusive Soldering** A process in which the solder paste for the through-hole components is applied using the stencil. The through-hole components are inserted and reflow-soldered together with the surface-mount components. Also known as Paste-In-Hole, Pin-In-Hole, or Pin-In-Paste Soldering.

**1.1.14 \*Land** A portion of a conductive pattern usually used for the connection and/or attachment of components.

**1.1.15 Modification** The process of changing an aperture in size or shape.