




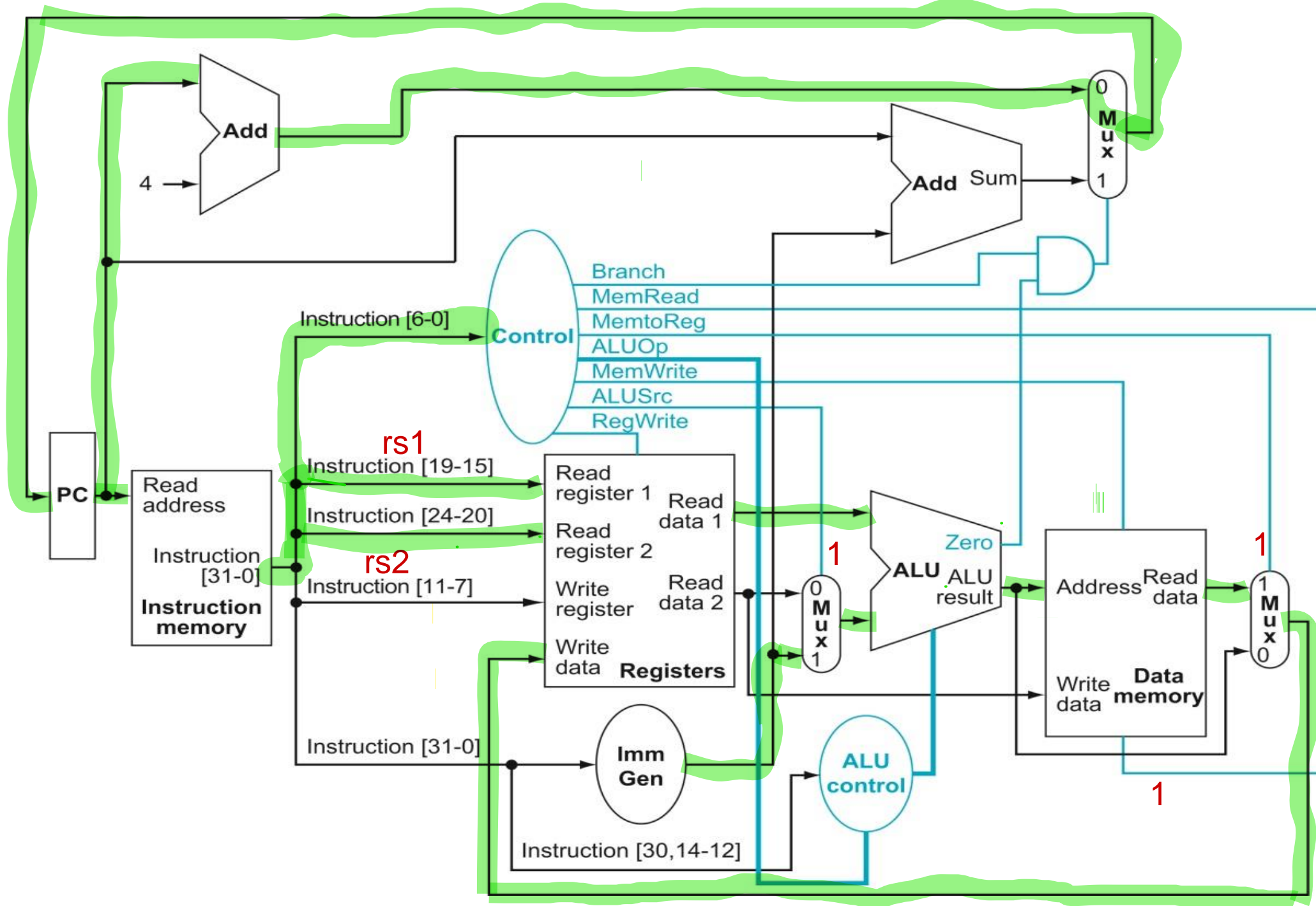


Homework 6 - Directions

1. For this homework you will be highlighting the datapath through the single cycle RISC-V design for 3 instructions. Note that I did Question 0 to show you what I want for the `jr` datapath. Notice how the data path itself is highlighted, the control signals are specified, and a brief writeup is provided showing the key steps that happen from fetching the `jr` instruction, all the way through the data path, until ultimately the PC is updated
2. You will be doing the same for the `sw` instruction, the `jal` instruction, and the `lui` instruction. Please consult the datasheet it will help you to setup the register file.
3. For each instruction you are allowed to cut wires, add any new wires, add new connections to existing wires, and to add additional components that we have used in Logisim – aka, multiplexors, adders, shifters, demux, etc. See the example I provided for `jr` as an example. Don't forget about the control signals, how should they be set? Does your instruction need new control signal(s)?
4. You can mark up and annotate each datapath any way that you want – on the computer, by hand, take pictures, etc. But your changes must be clear and easy to follow to receive full credit. On my sample I used:

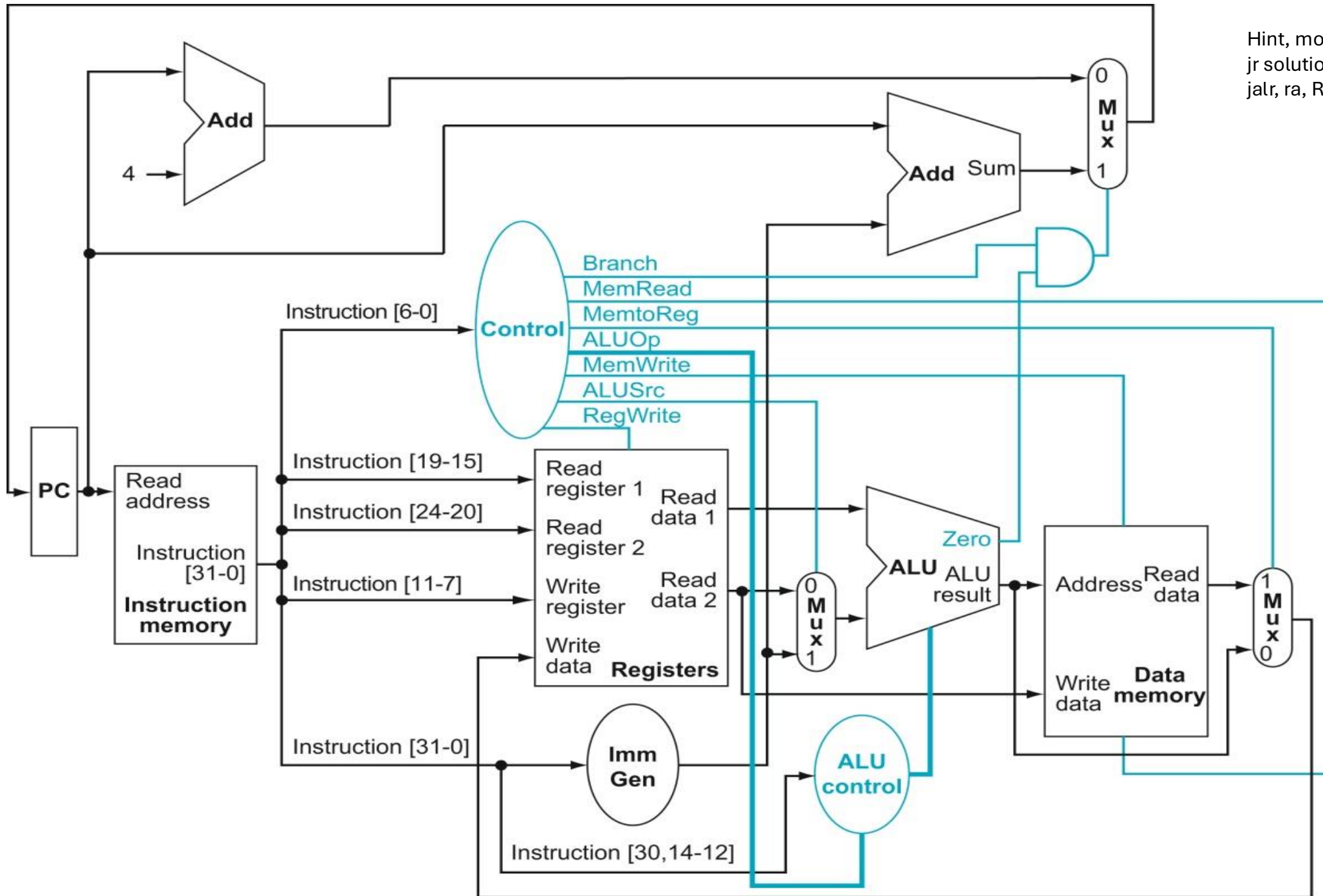
-  For the data path changes
-  For new control signals
-  For new components
-  For new wires
-  For annotations that support my description

Q1:
Store Word (sw)
Datapath



Q2:
Jump Link
jal
Datapath

Hint, modify
jr solution jal =
jalr, ra, Rs, imm



Q3:
Load Upper Immediate
lui Datapath

