CV – Shashikant Bhagalia

Personal Details

Name	Shashikant Bhagalia (Mr)	Profession	Electronic Engineer
Address	104 Eastcote Road, Pinner, Middlesex HA5 1EN	Email:	sbhagalia@virginmedia.com
Telephone	078910 88625	Age	51
Nationality	British	Clearance	Previous SC clearance
Driving Licence	Full Clean Licence	Marital Status	Married

Skills Summary

Hardware and FPGA Design

ASIC and FPGA design using VHDL. Digital and Analog Circuit Design.
Altera, Xilinx, Actel FPGA design, simulation, synthesis, test.
Microcontroller and Microprocessor based design.

Applications — Defence, Aerospace. Digital Telecoms: Cellular & Wireless Base Station, CPE. Cordless Products. OFDMA, CDMA, GSM/PCN, DECT Base Station and Subscriber Equipment. Dealing Room Systems: Data comms, Video Switching/Distribution.

Development Tools — Altera Quartus, Xilinx Vivado ISE/Chipscope, Actel Libero, HDL Designer. Mentor Graphics/Cadence, Orcad, Modelsim, System Generator.

Software Experience — Assembler, BASIC, some C, Pascal. Linux, Unix and DOS environment.

Education and Qualifications

1981-1985 **Brunel University**, Uxbridge, Middlesex, UB3 3PH
Electrical & Electronic Engineering, BSc 2.2 Hons

Course Structure: Four year thin sandwich including industrial work experience.
Subjects Studied: Communications, Digital Systems, Management, AI, Electronics, Software Languages, Maths, Physics, Control, Instrumentation.

1976-1981 **Islington Green School**, Prebend Street, London N1
A-Levels: Chemistry (A), Mathematics (B), Physics (A)
GCE O Levels 7 including English and Maths

Interests

Enjoy playing chess, sports (badminton, squash) and keeping fit (yoga, weight training).
Voluntary work with elderly and homeless.

Dec 2014–Present **BAE Systems,** Marconi Way, Rochester, ME1 2XX

Contract FPGA/VHDL Design Engineer

Lite HUD, video application, using Xilinx Vivado.

Dec 2012-Nov 2014 **UTC Aerospace Systems,** Motor Drive Systems Centre, Technology House, Maylands Avenue, Hemel Hempstead, Hertfordshire HP2 7DF

Contract FPGA/VHDL Design Engineer

Aircraft motor control firmware design to DO-254.
FPGA specification, VHDL code design, simulation and synthesis.
Requirements managed in DOORS. Dimensions code control tools.

2009-2012 **Ultra Electronics Ltd**, CIS, 419 Bridport Road, Greenford, Middlesex UB6 8UA.

Principal Digital Engineer. Responsible for FPGA design and hardware development. SC clearance.

- *End Crypto Unit:* Hardware development with Atmel Microcontroller; Xilinx and Actel FPGA: specification, VHDL design, simulation, synthesis, verification, test.
- *Watchkeeper UAV*: Xilinx and Actel FGPA design. SEF verification.

Dec 92-Dec 2008 **Airspan Communications Ltd** (formerly DSC)
Cambridge House, Oxford Road, Uxbridge, Middlesex UB8 1UN.
Now relocated to Capital Point, 33 Bath Road, Slough, Berkshire, SL1 3UF

Principal Engineer.

Development of fixed and mobile wireless systems. Initially working on proprietary CDMA system and then on an OFDMA WiMAX system. Patents for the CDMA system. Boards manufactured in large volumes and deployed in over 100 countries.

DCRT/QRDT Multiple Channel Radio Transceivers for WiMAX. Xilinx FPGA design:

- Digital transmit and receive filtering with DSP functions working up to 307.2MHz.
- 16bit DACs and 14bit ADC; PLLs for phase synchronisation of system clocks
- Control of Radio circuit with timers for TDMA operation
- Picochip; Optical interface using OBSAI standard, SERDES circuitry and SFP modules for up to 3Gbps operation; GPS module for clock recovery to lock Base Stations
- Mezzanine card to support CTC (Convolutional Turbo deCoder) IP
- Xilinx IP for DPD (Digital Pre-Distortion) to improve PA power efficiency

CDMA Design and development of Trinity farm for the AS4020 product using Altera FPGA:

- 16 Trinity2 ASICs on a card, CDMA summer and 8Mbps TDM switch for router; PCM/ADPCM timeslot/nibble switch; state machine to transfer TDM data to Trinity using shared memory interface; develop scripts to exercise CDMA functionality of Trinity farm for different modulations (e.g. QAM64) and chip rates.

Trinity2 ASIC Specify, Design, Develop, Simulate and Verify at block and chip level:

- Convolutional FEC Viterbi Decoder; Enhanced design to support code rates 5/8 and 3/4

May 90 – Nov 92 **BNR Europe Ltd** (formerly STC), Wireless Development, London Road, Harlow, Essex

Senior Design Engineer. Team developing a PCN handset, GSM base station and DECT wireless PBX.

DECT Designed modules for transmit, receive and layer one timer functions using Altera FPGA.

PCN/GSM PCN/GSM handset demonstrator partitioning and interface definition.

Altera HDL for design, simulation and prototyping baseband functions of PCN/GSM base station.

1985 - 1990 **Data Logic Ltd**, Queens House, Greenhill Way, Harrow, Middlesex HA1 1YR.

Dealing Room Systems Design of Intel microprocessor/microcontroller based comms interfaces & Multibus I cards. PC-AT keyboard emulation and VGA video conversion to analog for switching and dealer room distribution to dealer desks. Analog baseband design up to 50MHz bandwidth. Considerable assembler and some high level programming. Support manufacturing/test.

Referees:

1. Mr Uttam Parmar,
   88 Abercorn Crescent, South Harrow, Middlesex HA2 OPU
   Tel: 07951 561996

2. Mr David Kay,
   92 Dukes Avenue, London N10 2QA
   Tel: 07879 330529