Trinadh Pala

Date Of Birth: 24th June 1966
E-mail: trinadh_pala@yahoo.co.uk
Phone: +447999235176
uk.linkedin.com/in/trinadhpala

Address : 184, West High Wycombe,
High Wycombe, HP12 3AP, UK
Skype id - palatrinadh
VISA Status: BritishCitizen, UK

Availability: From 6th Nov 2019

Education:

1. M.Tech(Digital Electronics) , Cochin University., Cochin. 1989, First Class
   [Specialization: Electronic Instrumentation, DSP, Machine learning, speech processing, Audio and video coding, pattern recognition, Image processing, Computer Science]
2. B.E. (Electronics) , R.E.C. Nagpur, 1987, First Class
   [Specialization: Electrical & Communication systems, Control systems, Signal processing, Digital systems, Electrical Motors, Computing Science, Engineering Mathematics, Electromagnetic Theory]
3. M.Tech Project Training for 6 Months at LRDE, DRDO, Bangalore.
   [Project: 8085 based SDLC Mobile communication Controller]

Previous Jobs Summary:

1. ONCAM , Chiswick Park, London, UK
   Designation: Contract Software Engineer
   Duration: 23rd April 2019 to 17th May 2019

2. Cubic Transportation Systems, Salfords, Surrey, UK
   Designation : Contract Software Engineer
   Duration : since 24th July 2017 to 7th Sept 2018

3. **Onelan Ltd**,
   Henley-on-Thames,UK
   Designation: Sr. Software Engineer,
   Duration: Since 21st March 2016 to 28th Sept 2016

4. **Curtiss Wright Defense Solutions**,
   High Wycombe, UK
   Designation: Sr. Software Engineer.
   Duration: Since 15th Dec 2014- 27th July 2015

5. **Ericsson Television Ltd**, Southampton, UK
   Designation : IT consultant (worked as contractor)

Duration : March 2009 to 15th August 2014

6. **Wipro Technologies,** Bangalore, India.
   Designation: Technical Manager, Wireline IP,
   Duration : 19th Feb 2001 to 31st Dec 2008

7. **ISRO Satellite Center**, Bangalore, India
   Designation: Engineer/ Scientist SE,
   Duration : 23rd September 1991 to 31st January 2001.

   - **European Space Agency,** Netherlands, From 24th July 1995 to 8th Dec 1996 (ISRO-ESTEC Collaboration program, worked at **ESA)**

8. **DCM Data Products**, New Delhi, India
   R&D Engineer,
   Duration: August 1989 to September 1991.

Certifications:

1. IEEE wireless communication certification exam conducted in October 2008.
2. www.coursera.org: FPLP Digital Signal Processing Certificate 2013
3. www.coursera.org: Machine Learning, Stanford University certificate 2013, used matlab
4. www.coursera.org: Control of mobile robots, Georgia Institute of Technologies, 2014
5. www.coursera.org: Image and video processing: From Mars to Hollywood with a stop at the hospital, 22nd March 2015.

Key Skills

- Qt , GUI, QML, Qt quick,C, C++, Golang, STL, Linux
- Windows VC++, GUI, Python, CLion, Visual Studio
- Linux RTOS, ASM86
- Wind River, vxWorks, VxBus, gdb debugger.
- Source code management tools svn,cvs.
- Gstreamer
- DTV Middleware stacks ,
- JPEG compression, Huffman, Arithmetic coding.
- Baseband Modulation & Communication protocols
- Image processing, coding,
- Digital Signal processing
- DVB-S/C/T Broadcasting Encoders/Decoders
- Automated Test & Verification Tools Development
- AVC H.264/MPEG2 Video coding, ABR
- Consumer Electronics Devices Systems architecting
- Libero Microsemi SoC toolset
- Xilinx ISE
- NI TestStand
- Semiconductor IP development
- VHDL, Verilog, RTL, Simulations, Synthesis, DFT

- PLD, FPGA , ASIC design/development/verification
- RS232, IEEE1394,USB, 802.11 wifi, I2C,SPI communication standards
- ASI, PCI,ISA,AHB Interfaces
- TCP/IP, Ethernet,SBP2, IP over 1394, SNMP/MIB
- Encryption Standards 5C-DTCP, AES,DES
- Actel/Xilinx FPGA, ARM, Micro-controllers Atmel, Intel processors 8085,8086,80286

Objective: I am looking for work in the following areas

1. c/c++ software development in engineering applications. Qt GUI, Desktop, Embedded Software development vxworks, linux.
2. DVB Digital TV, Digital Signage, Video and audio coding, Image processing, Signal processing, machine learning, home networking, Telecommunication systems
3. Electronics and communications systems development and test verification.
4. FPGA, SOC development and test verification work. VHDL, Verilog RTL and Test verification for DSP algorithms/image processing/image coding algorithms.

Professional Experience:

ONCAM

Firmware development

- Linux GPIO driver development for ONCAM grand eye camera for controlling LED, IRCutFilter, Ambient Light Sensor, Golang based program development.

Cubic Transportation Systems: 24th July 2017 to 7th Sept 2018

BUS Reader Software development

- Bus Reader System Reset Monitor C++ based program development testing
- Bug investigation and fixing for the Bus Reader
- Test validation of Wireless Mobile Antenna board software.
- Data compression module development and testing using zlib library.
- Firmware development and testing for TR3 recorder on the fly remote uploading of new OS to existing platforms.
- NAND Flash device usage in embedded platform, software layers mapping and bad block management.

TR4 secure board A7 and M4 IMX based software development.

- Added GMI Debug and Profile data messages for Communication between Host and the Secure Board
- TLV data formatting of the payload and Testing.
- Configuration version data reading from json files and testing.

- GMI interface commands secure coding in c++ CLion IDE and gtest frame work test cases development.

ONELAN Ltd: 21st March 2016 to 28th Sept 2016

- Optimization of C++ based Movie player gstreamer media pipeline
  - for supporting live h264/mpeg transport streams with low latency,
  - Worked on static and dynamic gstreamer pipeline modeling, TS stream synchronization and latency adjustments, HDMI camera interfacing. H264/MPEG encoders interfacing and testing.
- Upgrading the NTB systems to DVB-T2 support
  - H377 cable TV tuner integration using Kernel lab tv driver APIs into NTB tv player.
  - python to c extensions using ctypes to bridge the Tv controller python scripts to kernelab's tuner driver C APIs.
  - Integrating the TV tuner data streams using Linux named pipes.
  - DVB-T2 tuning , programs displays, and video/audio playback of selected channel.
- Bug fixing and verification
  - Opengl and linux imlib based image player and Text player based on vector graphics cairo library bug fixes.
  - Gstreamer based media player dynamic player bug fixes
  - X11 Windows extensions and compositing window manager bug fixes
- Work involved understanding c/c++/python based NTB linux based codebase.

Curtiss Wright: 15th Dec 2014 to 27th July 2015

Designation: Sr. Software Engineer

- **VxWorks VxBus PCIe driver development** for fusionXF SDK supporting multiple PCIe root complex controllers on VPX3-131 SBC, with NXP P4080 QorIQ processor , to support VPX3-530 ADC/DAC Cards.
- **PCIe diagnostic software development.** PCIe config space access and AER report generation software development.
- **Porting and Testing of FusionXF SDK** to 32bit version to work on 64 linux RTOS , unit testing of the FusionXF SDK. Running Embedded systems test suits on ARM/PowerPC SBC boards.
- **Design and development of of SmartFusion2 FPGA** for controlling peripherals on I2C bus in VPX3-530 ADC/DAC board using MicroSemi cSOC. Worked on System block level development for Microsemi cSOC interfacing MSS and I2C bus controller component and FPGA fabric using Libero soc design suite. Did design entry, simulations, synthesis, programming and testing on the board. Developed I2C drivers also using SoftConsole.
- **NI TestStand, Test sequences development** and automated testing of VPX3-530 ADC/DAC boards.

Ericsson T.V Solutions : 4th March 2009 to 15th August 2014
Designation : Broadcast Engineer / IT consultant – on contract

- Development of Qt C/C++ based real-time ubuntu linux based Test automation software for DVB broadcast products.
- Developed real-time Test automation software DVB broadcast products using Qt GUI C/C++ for testing h.264/mpeg2 encoders , SCTE35,SCTE104 splicing and Dolby Digital audio frames. Used Qt widgets, Qwt libraries for displaying Audio waveforms, video streams.
- Developed following GUI based Application Software using Qt C/C++ development platform using C++11 constructs and STL containers and Qt threads.
  - **TS Analyzer:** displaying VBI,VideoUserdata, vanc,vbi, video, audio waveforms using Gstreamer.
  - **HD-SD SDI broadcast raw video analyzer**: Display of Video, VBI, VANC data, SCTE104 messages, Time-codes, CEA-608 data, frame capture.
  - **GPIO interface and scte35 analyzer:** supports GPI based splice triggering and automated testing comparing with TS stream splice information. Used Linux comedi drivers. Implemented using Qt c/c++ , comedi drivers, GUI.
  - **video switcher**: Automated triggering of SDI video using Device controlling using IP UDP port. Used Socket programming, SNMP/MIB trap message parsing. Implemented .Qt GUI interface for this application.
- Audio/Video streams over IP networks analysis and testing.
- Worked on MPEG2, H.264 AVC Encoders, DVB/ATSC transport stream multiplexers and DVB-S Satellite modulators, DolbyE audio, mpeg2 Test verification.
- Used AV equipments like Teletex, Closed Captions, video data simulators like Omnigen, Norpack, Tcube, Doremi during verification and validation.
- Performed MPEG2, H264 TS analysis, Audio video lipsync delay measurements, tested baseband modulation like QPSK.

Experience at Wipro Technologies (From 19th Feb 2001 to 31st Dec 2008)
Designation: Specialist VLSI/Technical Manager Wireline IP,
Semiconductor IP division

Handling of 1394, USB, Ethernet, Encryption Hardware IP cores and associated software stacks for Home networking applications. Worked on Digital TV, Settop box , camcorders, Hard-disk controller IPs.

- **Project/Program management :**
  - Experienced in preparing Technical proposals based on client requirements for VLSI & Embedded systems
  - Experienced in Project / Program management, metric collection, process improvements. Customer interaction and presale support for the home networking IPs. Managed Wireline semiconductor IP team in Wipro. Executed several projects as per the CMMI Level 5 guidelines.

- Worked on preparing Technical proposals for several clients across the world in wire-line semiconductor IP area, hardware customizations, software stacks porting and customization.

Home Networking & Digital TV Software projects:

- **DVD recorder product definition**, development and testing for Medical applications. Defining the software stacks and porting.
- Product architecting of **Low cost SetTopBox**. Selection of chipsets, software stacks. Development of boards, porting software and testing.
- 1394 Based AV(Audio/Video) server software development project for multiple channels, Samsung, South korea Involved adding multiple channel support. Developed using Linux C/C++. Used RTP/UDP streaming.
- **Automotive platform 5C-DTCP software** porting and performance tuning for ADIT. Implemented using linux C/C++. Used gdb for debugging.
- Worked on 1394.1 bridge, 1394 PAL and IP secure development. ARM Linux based software development using C.
- Porting of HANA software stacks Samsung, South Korea: 1394 Connection management protocol, device discovery protocol stacks porting and ip over 1394 software porting to linux RTOS. Software in C and used RTP/UDP streaming, used gdb for debugging. Used webserver http, cgi scripts.
- **D**evelopment of DTV software stacks such as ATSC Tuner subunit, EIA775 OSD consumer/producer, CEA2027, CEA931. Software in Linux C/C++.
- Porting of the 1394 drivers and software stack written in C to ARM, Linux platform.
- **Design of IIDC Camera based 1394 network** for in car entertainment. Customized 1394 configuration registers to support IIDC camera. Work involved software/hardware development. Software in C.
- **AVHDD 5C DTCP software**, written in C/C++, testing on Mediatek Taiwan DVD evaluation platform.
- 802.11abg/n presale support and consulting on Wipro Wireless LAN MAC. Software defined radio definition, and OFDM and other modulations schemes support.

VLSI Hardware IP development projects:

As VLSI specialist in Home networking semi conductor IP division, carried several IP development activities for 1394, Ethernet, USB, Encryption IP cores, RTL , Test bench design , Synthesis, codecoverage, customization and bug fixing activities.

- **1394 AVLINK IP RTL** and Test bench customizations to support multiple AV mpeg2 streams.
- Wireless **internet Radio Wifi module** interface FPGA RTL module development for Philips.

- **SBP2 Accelerator IP RTL** development and testing project, SONY, Japan. Integration of the accelerator, and testing SBP2 stack.
- **Multi-port 1394 AVLINK IP** (RTL & Testbench) development for Zoran, USA incorporating PVCI/BVCI RTL logic interface to the AVLINK IP. Modifications to the AVLINK driver software.
- Functional definition of the Base-band modules and baseband filters for Bluetooth
- **Digital TV Evaluation board development** for Wipro to test 1394b AVLINK IP. And porting of the software stacks. Worked on customizing the AVLINIP interface RTL.
- Integration of Fast **Ethernet and Gigabit Ethernet IPs** to create TriMAC IP. The project involved RTL/Test bench development, synthesis.
- **SATA Device IP development**, DTCP over IP development. The work involved verilog RTL , and verification in standalone test bench.
- **AES, DES** hardware RTL logic IP development.
- USB hardware IP customizations to support power management for a mobile camera application. Work involved RTL level changes.
- AVLINK IP interfacing with SDRAM on AV port. DFT/Scan insertion. Done in verilog RTL.
- **IEC61883-6 Audio support**, OSD DMA support in 1394 AVLINK IP for the Digital TV Chipset.
- Lint, Synthesis, DFT and code coverage on all IP cores in several projects.
- Creation of Cardbus IP core and I2C bus IP core customizations.
- **1394 OHCI Fast PCI** interface customization.
- Worked with fables semiconductor customers, automotive customers in South Korea, Taiwan, USA, Japan.

Experience at ESTEC, Netherlands. (24th July 1995 to 8th Dec 1996)
Designation : Trainee Engineer (RF Division –Mobile Communications)

- **A 32 bit processor Core** Behavioral and RTL level implementation in VHDL.
- Developed VHDL models for behavioral and RTL level implementation of the 7, 9,16 , point FFT processor and 112 & 1008 **FFT processors** based on good-thomas algorithm.
- Developed VHDL models for behavioral and RTL level implementation of the FIR Filters MAC architecture using distributive arithmetic
- Developmed VHDL models for behaviroral and RTL level implementation of **OFDM Demodulator** using Decimators and poly-phase filters. I did Matlab modeling of the FIR filters and results comparison.

Experience at ISRO Satellite Centre , Bangalore (23rd Sept 1991 to 31st Jan 2001).
Designation: Engineer/ Scientist SE, Digital Systems Group.

- **ADPCM Data compression system development and testing.**
- **Actel FPGA based ADCPM compression system development.**
- **JPEG Compression System modules development and testing. :**

- **Base band Data Formatter:** Implemented Differential Encoding and QPSK modulation in parallel architecture, which was fitted in Actel FPGA.
- Implemented RS channel encoder FPGA (FEC protection).
- Developed Satellite Health parameter simulator using ATMEL AVR 8 bit micro-controller and Compass `c' compiler for the software development.
- **ASIC based JPEG compression system:** Project manager for this CartoSAT II Satellite Base-band payload. Integration of the Satellite CCD Payload interface board and Formatter module with JPEG compression Module. Software using Borland C.
- **PC Based Test Systems:** I developed PC based Test System for Payload Video data simulation and Acquisition. VC++, C, Schematics orcard, FPGA in Viewlogic

- **Image Compression/processing Software development:**

  * **Study and Simulation (in `C' language) of Data Compression Algorithms** and their Evaluation for their suitability to Satellite real time payload applications.

  * Software development for ADPCM compression/decompression
  * DCT-Fixed Scalar Quantization algorithm.
  * JPEG Compression/decompression with bit rate control.
  * Wavelet-VQ software development.
  * Adaptive VQ scheme implementation in software.
  * Simulation of Channel error effects on ADPCM/JPEG compression schemes.
  * Sub-band coding, pyramid coding of images and multi-resolution analysis.
  * Developed X11 windows programming application for image processing and display of multi-spectral images using GL libraries.
  * Developed matlab based image display and wavelet transform signal processing of remote sensing applications. Developed Image quality comparisons software using matlab.

  ***X11 windows programming**: Developed x11 windows applications using motif graphics library and IBM graphics library. These programs use widgets like dialog boxes, list boxes, message boxes , pull down menus, even driven programming. Implemented edge extractors like 1st and 2nd order edges, LAPLACIAN, SOBLEL operators, false coloring, image quality comparison. This application software is for large size multi-spectral image display, processing and to display the wavelet transformed images. This application has been used for many compression systems evaluation.

Experience at DCM Data Products (Aug 1989 to Sep 1991)
Designation: Associate Design Engineer (PC R&D group)

a) I/O processor Board: Designed a 80286 based i/o processor Card for multi i/o terminal interfacing. Responsible for the development of diagnostics software in C. Monitor program in ASM86 for an 80286 based processor i/o board.
b) **Railway Signaling System:** Designed 8086 based processor card and LED panel control boards. Used PALs, PLDs in the design. ASM86 assemply language programming for the processor.

DRDO M.Tech Project Work:
DRDO – Defense Research and Development Organization
* Designed and developed of a Preprocessor Card for SDLC Data link layer Implementation. Developed the software for SDLC Controller based mobile communication system and implementation of go-back N ARQ scheme. Software in Assembly language. Software in C, for Neural networks training and classification, pattern recognition. Speech signal modeling.

Papers

1. A paper titled " An Adaptive DPCM (2D-ADPCM) scheme for Satellite Payload Data compression " has been published in the Conference proceedings of ICCS98, NIIT, New Delhi.
2. A paper on Loss less coding for Satellite image Data compression., Journal of Spacecraft Technology, Vol 6 No. 5 , July 1996.
3. Published a paper on `Effect of Transmission Channel errors on ADPCM and JPEG compression' in Journal of Spacecraft Technology, ISRO, vol.9. No.1 Jan 99.
4. A paper on `High bit rate data Formatter using Parallel Architecture' published in International Conference on Communications, Control and Signal processing CCSP-2000, organized by IEEE Bangalore Section.
5. A paper on 5C-DTCP Encryption/Decryption at 1394 Developer conference in Japan.
6. IEEE 1394 : Firewire in the Home, web based www.hometoys.com magazine Dec 2002.
7. A paper on Software defined radio (SDR) in Wipro Talon show, Dec 2007

Summary of EDA tools used in Projects

Synopsys VHDL Simulator, Synthesizer and verification, static timing tool, Formality, Design compiler. Nc Verilog simulator, signal scan, ut. Actel FPGA development system, Viewlogic Schematic and Actel Designer Series. Actel Desktop for VHDL support. Xilinx Foundation series. Orcad , Cadstar, Cronology timing designer, vcs logic simulator, CATC 1394 BUS analyzer, Lab test equipments like Logic analyzers, CROs, StreamXpert, DTV test & Verification tools, Project Management tools like Microsoft Project, cvs version control, UML, Microsoft visio, Test Director, gtest for c++ Unit testing,

Interests:

Fine Arts, Oil Painting, Drawing, reading books, doing online courses, traveling