PRIYANK KRISHNANI

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EMPLOYMENT EXPERIENCE

Aug, 2018 – FPGA Design Engineer (Contractor), Ultra Electronics PMES, Rugeley, UK

Model based verification within MATLAB environment for integral common modules used across numerous FPGAs for power converter designs. Developing test specification and testbench framework to be used across the project. Quick turn-around on numerous verification testbenches, performing co-simulation between MATLAB and ModelSim for FPGA models such as filters, ADCs, Memory Controllers.

Jan, 2017 – Aug, 2018 FPGA Design Engineer, Airbus Cyber Security, Newport, UK

Working with FPGA designs for IP (Internet Protocol) encryptors. Working in Altera and Microsemi environments for designs involved in Ethernet networking and encryption designs using different PRIME algorithms. Exposure to IKE (Internet Key Exchange) protocol of IPSec (IP Security) protocol suite for SA (Security Association) setup used within inline encryption designs. Self-checking test benches, Tcl scripting, experience with SmartFusion2 and Soft Console IDE. Involved with FPGA, Hardware Design Reviews, and CDRs.

Nov, 2015 – Jan, 2017 FPGA Design Engineer, ViaSat, Wareham, UK

Experience in hardware disk encryption design based products environment. Exposure to AES-256 cipher encryption and disk service management system. Experience in designing and debugging in Xilinx Vivado design suite and working with Xilinx IP and proprietary coding styles to synthesize appropriate logic blocks, Simplifying legacy HDL code with personal focus to satisfy and improve firmware requirements and promote ideas within team to develop and follow firmware processes.

VHDL test bench design for verification of high-speed data transfers interface driven using SATA protocol, design and verification for CDC (Clock Domain Crossing) design elements.

Aug, 2013 – Nov, 2015 Electronics Engineer, Lockheed Martin, Ampthill, UK

LRU (Line Replaceable Unit) FPGA lead, MilCAN protocol design on FPGA. Experience with Microsemi and Altera FPGAs. Presented in front of project's end customer at two Critical Design Reviews.

Safety related FPGA Verification responsibility. VHDL simulation models for FPGA with DO-254 level B certification. Prepared safety FPGA verification test plan, Property Specification Language verification training acquired, useful formal verification through assertions based verification.

Implemented Design For Test Debug interface used to debug FPGAs, it allows interrogating/controlling LRU FPGAs. **Awarded LMUK Technical Excellence Award, 2015 for DFT Debug interface.**

CAPL scripting experience with Vector CANoe system useful to debug/test teams to exhaustively test a design, experience with Tcl scripting.

Altium schematic and PCB design training acquired, PCB design for a microcontroller based design board containing RS-232, RS-485, MilCAN and Ethernet interfaces and layout for a switch panel board. Embedded C coding experience over PIC microcontroller.

EDUCATION

2013-2012 Imperial College London

MSc. in Analogue and Digital Integrated Circuit Design

Modules: Analogue Integrated Circuit and Systems, Full custom Integrated Circuit Design, VHDL & Logic Synthesis, Analogue Signal Processing, Digital Signal Processing, Real Time Digital Signal Processing, High Performance Analogue Electronics, RF Electronics.

Group projects: Design of Vector Display Processor (Draw unit, RAM, FSM) in VHDL, Input- sequence of line drawing commands from host processor, Output – read/write interface to video RAM. Speech Enhancement Project using Texas Instrument's 6713 DSP processor – Code composed in C using Spectral Subtraction algorithm.

Individual project: Design of Audio Processor Chip (Schematic and Layout) in CMOS 0.18µm technology provided by MOSIS. Clock, FIR filter, 7bit current mode DAC, op-amp buffer. Chip area -1 mm^2, Power Consumption – 40.5 mW, Dynamic Range – 20dB.Cadence Lab – Design, Analysis and Layouts of analogue building blocks – Current Mirrors, Operational Amplifiers. Thesis**: Verified Numerical Hardware**, translate results of a technique which is developed to show the rounding errors occurring in floating point number computation**;** this technique can be applied for efficient FPGA/ASIC implementation to maximise parallelism, minimize area or power consumption.

2012-2009 Queen Mary University, London

BEng. Electronic Engineering (First (Honours) obtained, Average grade – 79%)

Modules: Integrated Circuit Design, Digital Signal Processing, Multimedia Systems, Internet Protocols, Telecom Systems, Product Development, Enterprise Management, Communication System Electronics, Microprocessor Systems Design, Digital Systems Design, Microwave and Optical Transmission, Signal and Systems Theory, Electronic Devices and Applications, Engineering Mathematics, Electric and Magnetic Fields, Circuit Design and Applications, Digital Circuit Design, Programming Fundamentals, Professional Applications, Telecommunications and Internet Fundamentals, Introduction to Electronic Systems.

Projects: Human Reaction Time machine (group) **-** Measure response time to various patterns of light stimuli and transfer result to computer. Managed team of 7 people, improved leadership skills, **awarded second prize,** Temperature sensing and other basic programming experience over PIC microcontroller - Studied PIC microcontroller architecture -Interrupts, PWM, Infrared Sensor. Antenna Positioner using PIC via RS-232 interface- Controlling angle of turntable through computer by an applet designed in LABVIEW through RS-232 connection. Designed the PIC code in C, all interface connections**.** Designed and built an interface module with parallel port connectors attaching to the module controlling the motor of turntable. Image Feature detection software designed in Matlab.

2007-2009 HSC (Higher Secondary School Certificate)(A level equivalent), St. Xavier's School, Surat, India
Physics - 83%, Mathematics - 92%, Chemistry - 84%, Computer Education - 92%, English - 71%.

Work Experience

Course representative for MSc in Analogue and Integrated Design, Imperial College
Act as a link between fellow course colleagues and department, to address any problems/complaints faced by students and report them to course organiser and discuss actions to improve the course.

PASS (Peer Assisted Study Support) Student Organiser, Queen Mary University, London.
Organise the mentoring sessions for given by second year students to first year students, aliasing and supervising weekly sessions. **Best PASS mentor award** for 2010-2011.

Internship at ZTE, organised by Beijing University of Post Telecommunications.
A team of 5 students from Queen Mary, University were selected for a fully sponsored internship in Beijing. I lead the group through the 3-week period, wherein we attended technical lectures and labs given by industry leaders from ZTE, fifth largest telecom equipment maker in world.